Digitally Controlled VGA LF to 700MHz

Preliminary Technical Data AD8370

FEATURES

Differential Input and Output
- **200Ω Differential Input**
- **100Ω Differential Output**

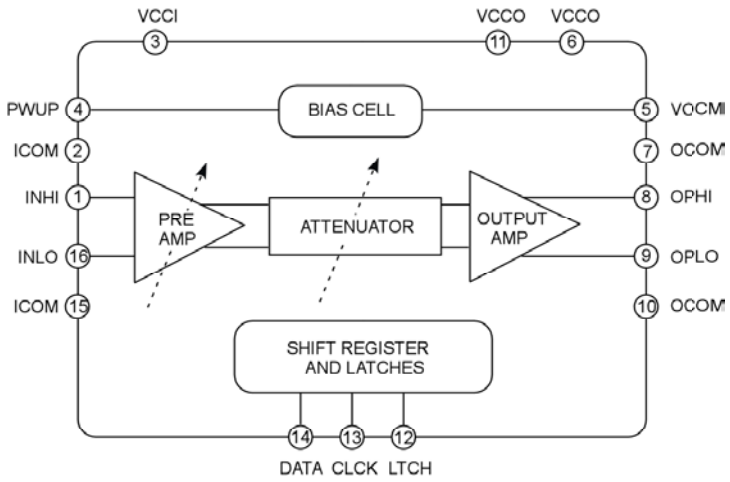
7dB Noise Figure @ Maximum Gain
Two Tone IP3 of 31dBm @ 70MHz
-3dB Bandwidth of 700MHz
40dB Precision Gain Range
Serial 7-bit Interface
Pin Programmable Low and High Gain
- **Low Range -11 to 17dB**
- **High Range 6 to 34dB**

Wide Input Dynamic Range
Operation Down to a 3 V Supply
Power Down Feature

APPLICATIONS

Differential ADC Driver
IF Sampling Receivers
Cellular/PCS Base Stations
RF/IF Gain Stages
SAW Filter Interfacing
Single-Ended to Differential Conversion

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8370 is a low cost, digitally controlled, variable gain amplifier that provides both high IP3 and low noise figure. The excellent distortion performance and wide bandwidth makes the AD8370 a suitable gain control device for modern receiver designs.

For wide input dynamic range applications the AD8370 provides two input ranges; high-gain and low-gain mode. A vernier 7-bit attenuator provides 28dB of attenuation range with better than 2 dB resolution, and up to 22dB of range with better than 1dB resolution. The input gain selection allows for an additional 17dB of range and provides for excellent output distortion levels with relatively high input levels.

The AD8370 may be powered on or off by applying the appropriate logic level to the PWUP pin. When powered down the AD8370 consumes less than 5mA and offers excellent input to output isolation.

Fabricated in ADI's high speed XFCB process, the high bandwidth of the AD8370 provides high frequency and low distortion. The quiescent current of the AD8370 is 78mA typically. The AD8370 amplifier comes in a compact 16 pin TSSOP package and will operate over the temperature range of -40°C to +85°C.

REV. PrC 3/12/03

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AD8370-SPECIFICATIONS

(V_S=5V, T=25°C, R_S=200Ω, R_L = 100Ω at max gain unless otherwise noted)

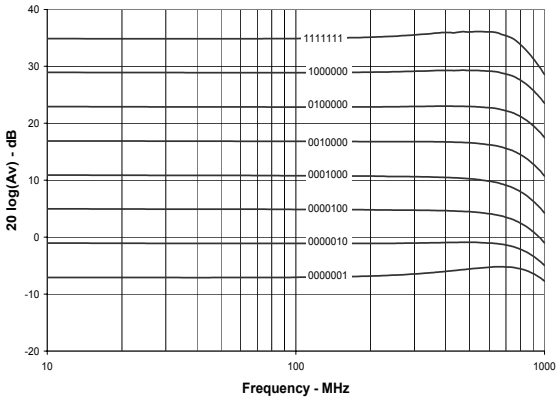
Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
- 3 dB Bandwidth	Vout<1 Vp-p		700		MHz
Bandwidth for 0.1 dB Flatness	Vout<1 Vp-p		TBD		MHz
INPUT STAGE					
Maximum Input	Low Gain (1dB Compression)		1.13		Vrms
Maximum Input	High Gain (1dB Compression)		500		mVrms
Input Resistance	Differential, f=10MHz		200		Ω
Input Capacitance	Differential, f=10MHz		TBD		pF
Common Mode Input Range			3.2		Vp-p
CMRR	Differential, f=10MHz		60		dB
GAIN CONTROL INTERFACE (GAIN)					
High Gain	Gain Code = 127		34.1		dB
High Gain	Gain Code = 5		6.0		dB
Low Gain	Gain Code = 127		17.1		dB
Low Gain	Gain Code = 5		-11.0		dB
Step Response	For 6 dB Gain Step		10	TBD	ns
OUTPUT STAGE					
Output Voltage Swing	$R_L \geq 1k\Omega$ (1dB Compression)		8.4		Vp-p
Output Resistance	Differential, f=10MHz		100		Ω
Output Capacitance	Differential, f=10MHz		TBD		pF
NOISE/HARMONIC PERFORMANCE 10MHz					
Noise Figure			7.2		dB
2nd Harmonic	Vout = 1Vp-p, R_L = 100Ω		-75		dBc
3rd Harmonic	Vout = 1Vp-p, R_L = 100Ω		-71		dBc
Two-Tone IMD	1Vp-p Composite		-72		dBc
Output 1dB Compression Point			15.8		dBm
70MHz					
Noise Figure			7.4		dB
2nd Harmonic	Vout = 1Vp-p, R_L = 100Ω		-68		dBc
3rd Harmonic	Vout = 1Vp-p, R_L = 100Ω		-61		dBc
Two-Tone IMD	1Vp-p Composite		-72		dBc
Output 1dB Compression Point			15.8		dBm
140MHz					
Noise Figure			7.6		dB
2nd Harmonic	Vout = 1Vp-p, R_L = 100Ω		-64		dBc
3rd Harmonic	Vout = 1Vp-p, R_L = 100Ω		-52		dBc
Two-Tone IMD	1Vp-p Composite		-69		dBc
Output 1dB Compression Point			14.8		dBm

AD8370-SPECIFICATIONS (V_S=5V, T=25°C, R_S=200Ω, R_L = 100Ω at max gain unless otherwise noted)

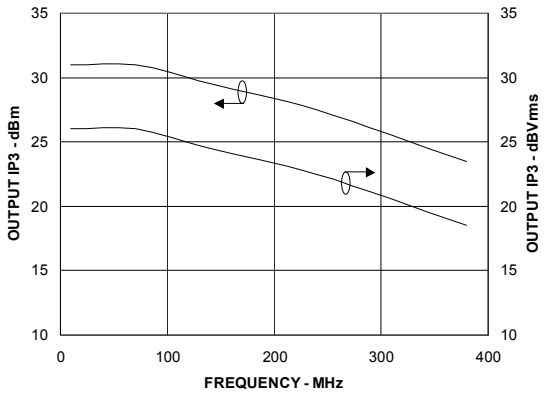
Parameter	Conditions	Min	Typ	Max	Units
NOISE/HARMONIC PERFORMANCE					
190MHz					
Noise Figure			7.6		dB
2nd Harmonic	Vout = 1Vp-p, R_L = 100Ω		-62		dBc
3rd Harmonic	Vout = 1Vp-p, R_L = 100Ω		-47		dBc
Two-Tone IMD	1Vp-p Composite		-67		dBc
Output 1dB Compression Point			13.6		dBm
240MHz					
Noise Figure			7.7		dB
2nd Harmonic	Vout = 1Vp-p, R_L = 100Ω		TBD		dBc
3rd Harmonic	Vout = 1Vp-p, R_L = 100Ω		TBD		dBc
Two-Tone IMD	1Vp-p Composite		-65		dBc
Output 1dB Compression Point			13.5		dBm
380MHz					
Noise Figure			7.8		dB
2nd Harmonic	Vout = 1Vp-p, R_L = 100Ω		TBD		dBc
3rd Harmonic	Vout = 1Vp-p, R_L = 100Ω		TBD		dBc
Two-Tone IMD	1Vp-p Composite		-56		dBc
Output 1dB Compression Point			11.2		dBm
POWER INTERFACE					
Supply Voltage		2.7		5.5	V
Quiescent Current	PWUP high		78		mA
vs. Temperature	-40°C ≤ T_A ≤ 85°C	TBD		TBD	mA
Total Supply Current	PWUP high, Vout = 1Vp-p, R_L= 100 Ω (includes load current)		80		mA
Power Down Current	PWUP low		4		mA
vs. Temperature	-40°C ≤ T_A ≤ 85°C	TBD		TBD	mA
POWER DOWN INTERFACE					
Power Up Threshold			1.2		V
PWUP Input Bias Current	PWUP = 0 V		135		nA

Notes

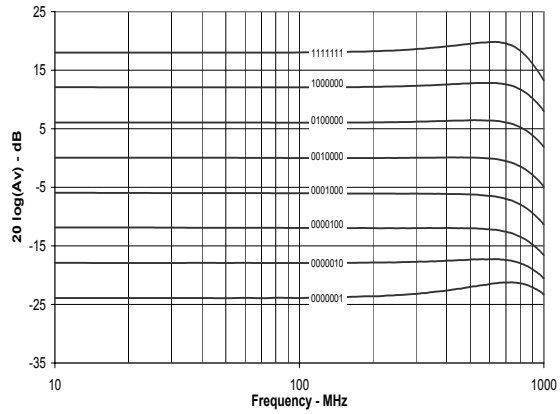
Typical Performance Characteristics (V_S = 5V, R_S=200Ω, R_L=100Ω, T=25°C, unless otherwise noted)



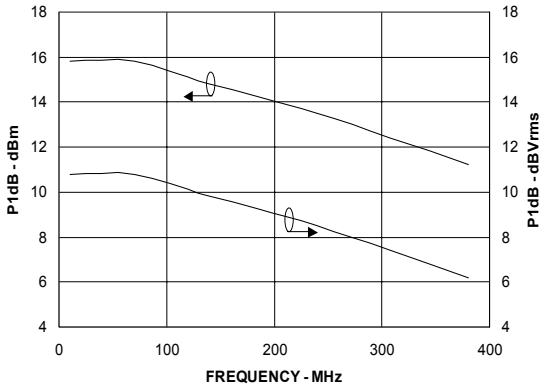
TPC 1. High-Gain Mode AC Response



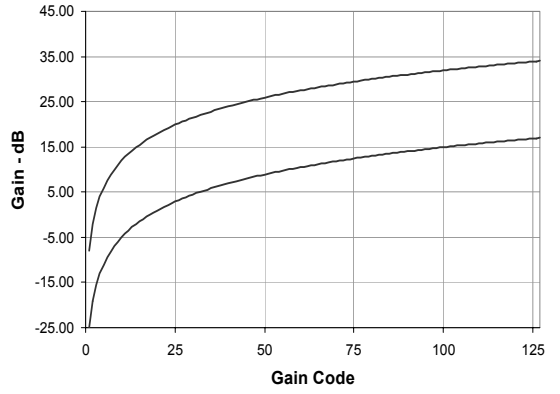
TPC 4. Output Third Order Intercept versus Frequency at Maximum Gain



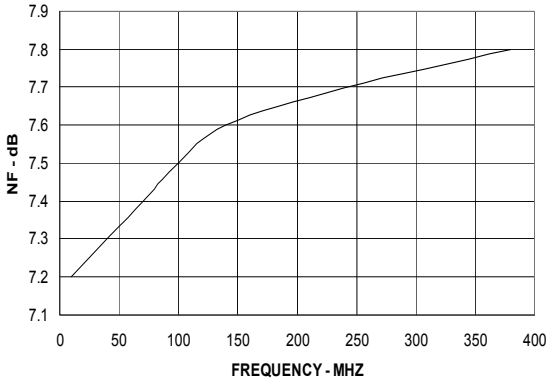
TPC 2. Low-Gain Mode AC Response



TPC 5. Output Compression Point versus Frequency at Maximum Gain



TPC 3. Gain versus Gain Code



TPC 6. Noise Figure versus Frequency at Maximum Gain

Basic Connections
Figure 1 shows the minimum connections required for basic operation of the AD8370. Supply voltages between 2.7 and 5.5V are allowed. The supply to the VCCO and VCCI pins should be decoupled with at least one low inductance surface-mount ceramic capacitor of 0.1 μF placed as close as possible to the device. More effective decoupling is provided by placing a 100-pF capacitor in parallel and including a ferrite bead in series with the supply.

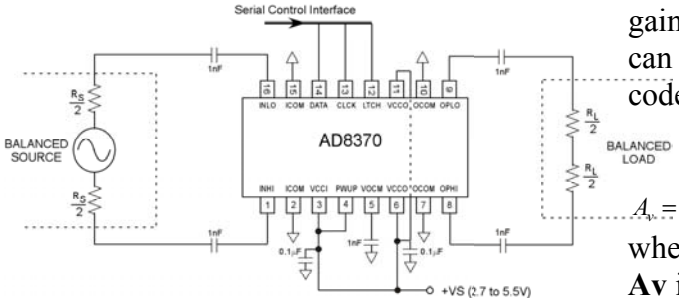


Figure 1. Basic Connections

The AD8370 is designed to be used in differential signal chains. Differential signaling allows for improved even-order harmonic cancellation and better common-mode immunity than can be achieved using a single-ended design. In order to fully exploit these benefits, it is necessary to drive and load the device in a balanced manner. This requires some care in order to ensure that the common-mode impedance values presented to each set of inputs or outputs is balanced. Driving the device using an unbalanced source can degrade the common-mode rejection ratio. Loading the device with an unbalanced load can cause degradation to even-order harmonic distortion and premature output compression. In general, optimum designs will be fully balanced, though the AD8370 can still provide impressive performance when used in an unbalanced environment.

The AD8370 is designed to be a fine gain adjustment variable gain amplifier. The gain control transfer function is linear in voltage gain. On a decibel scale, this results in the exponential transfer functions indicated in TPC 3. At the low end of the gain transfer function, the slope is steep, providing a rather coarse control function. At the higher end of the gain control range the dB step size is decreased allowing for precise gain adjustment. The linear voltage gain can be expressed with respect to the gain code as:

$$A_V = GainCode \cdot Vernier \cdot (1 + (PreGain - 1) \cdot MSB)$$

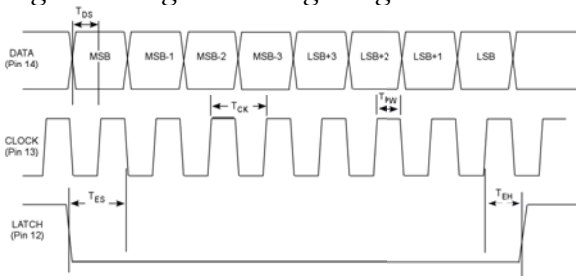
where
Av is the linear voltage gain.
Gain Code is the digital gain control word minus the MSB.
Vernier =0.055744 V/V
PreGain =7.079458 V/V
MSB is the most significant bit of the 8-bit gain control word.

For example, a gain control word of 10101101 (173 decimal) would result in a linear voltage gain of 17.76V/V, calculated as:
45×0.055744×(1+(7.079458-1)×1)

Digital Interface
The digital control port uses standard TTL interfacing. The 8-bit control word is read in a serial fashion when the LTCH pin is held low. The levels presented to the DATA pin are read on each rising edge of the CLCK signal. Figure 2 illustrates the timing diagram for the control interface. Typical

minimum values for various timing parameters are presented in table I.

Figure 2. Digital Timing Diagram



Parameter	Typ	Units
Clock Pulse Width (T_{PW})	10	ns
Clock Period (T_{CK})	20	ns
Setup Time Data vs. Clock (T_{DS})	2	ns
Setup Time Data Enable vs. Clock (T_{ES})	2	ns
Hold Time Data Enable vs. Clock (T_{EH})	2	ns

Table I. Serial Programming Timing Parameters

Single-Ended to Differential Conversion

The AD8370 is primarily designed for differential signal interfacing. The device can be used for single-ended to differential conversion simply by terminating the unused input to ground using a simple capacitor as depicted in Figure 3. Even though the differential balance is upset when using a single-ended drive, the distortion performance and gain accuracy will be adequate for most applications.

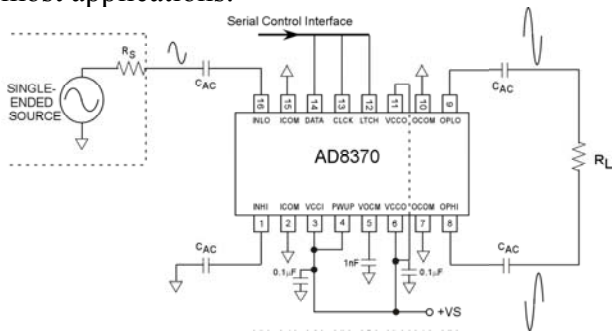


Figure 3. Single-Ended to Differential Conversion

Evaluation Board

The evaluation board allows for quick testing of the AD8370 using standard 50-Ω test equipment. The schematic is shown in Figure 5. Transformers T1 and T2 are used to transform 50-Ω source and load impedances to the desired input and output reference levels.

Evaluation Board Software

The evaluation board comes with the AD8370 control software that allows for serial gain control from most computers. The evaluation board is connected via a cable to the parallel port of the computer. By simply adjusting the slider bar in the control software, the gain code is automatically updated to the AD8370.

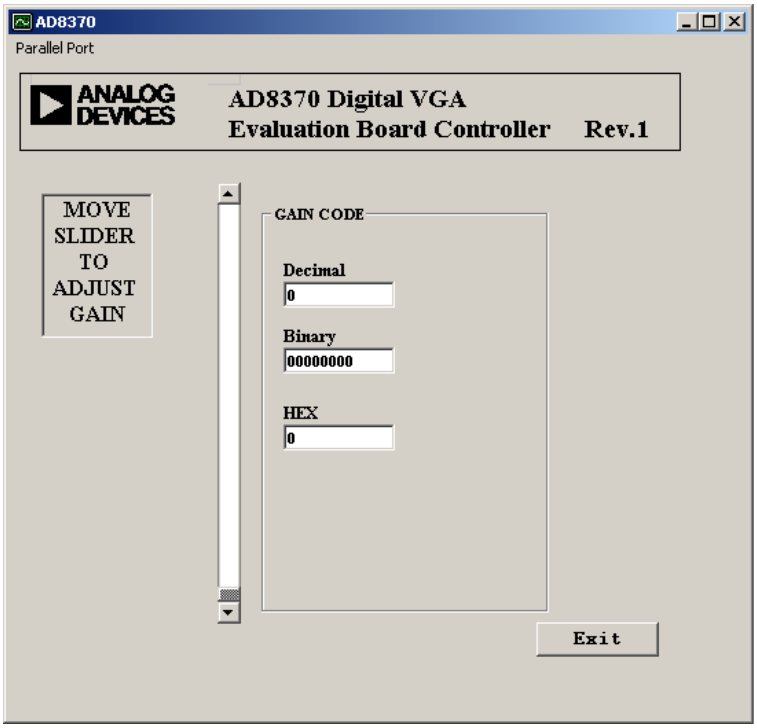


Figure 4. Evaluation Software

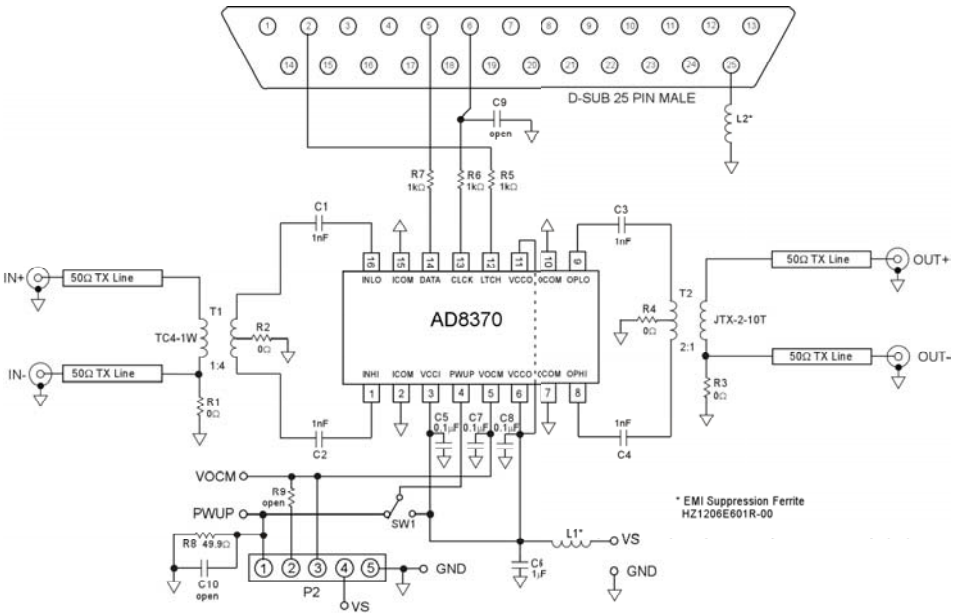
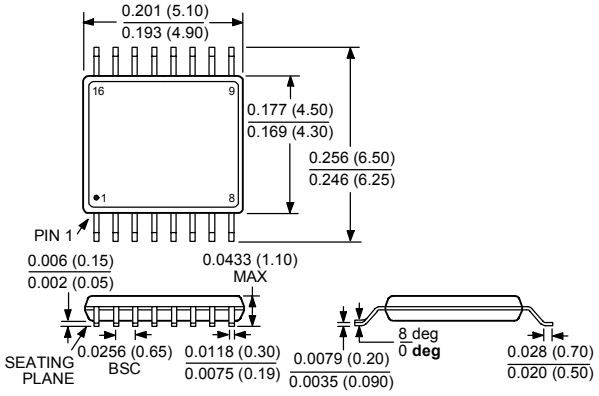


Figure 5. AD8370 Evaluation Board Schematic

AD8370 Evaluation Board Configuration Options

Component	Function	Default Condition
VS, GND, VOCM	**Power Interface Vector Pins:** Apply supply voltage between VS and GND. The VOCM pin allows for external monitoring of the common-mode input and output bias levels.	Not Applicable
SW1, R8, C10, PWUP	**Device Enable:** Set to position B to power-up the device. When in position A, the PWUP pin is connected to the PWUP vector-pin. The PWUP pin allows for external power cycling of the device. R8 and C10 are provided to allow for proper cable termination.	SW1 = installed R8=49.9Ω (Size 0805) C10=open (Size 0805)
P1, R5, R6, R7, C9	**Serial Control Interface:** The evaluation board can be controlled using most PCs. Windows based control software is shipped with the evaluation kit. A 25 pin D-sub connector cable is required to connect the PC to the evaluation board. It may be necessary to use a capacitor on the clock line depending on the quality of the PC - port signas. A 1nF capacitor for C9 is usually sufficient at reducing clock-overshoot.	P1 = installed R5, R6, R7=1kΩ (Size 0603) C9= open (Size 0603)
J1, J2, J6, J7	**Input and Output Signal Connectors:** These SMA connectors provide a convenient way to interface the evaluation board with 50-Ω test equipment. Typically the device will be evaluated using a single-ended source and load. The source should connect to J1 (IN+), and the load should connect to J6 (OUT+).	Not Applicable
C1, C2, C3, C4	**AC Coupling Capacitors:** Provides AC coupling of the input and output signals.	C1, C2, C3, C4 = 1nF (Size 0603)
T1, T2	**Impedance Transformers:** T1 provides a 50Ω to 200Ω impedance transformation. T2 provides a 100Ω to 50Ω impedance transformation.	T1=TC4-1W T2 = JTX-2-10T (*MiniCircuits*)
R1, R2, R3, R4	**Single Ended or Differential:** R2 and R4 are used to ground the center tap of the secondary windings on transformers T1 and T2. R1 and R3 should be used to ground J2 and J7 when used in single ended applications.	R1, R2, 3, R4 = 0Ω (Size 0603)
C5, C6, C7, C8 L1, L2	**Power Supply Decoupling:** Nominal supply decoupling consists of a ferrite bead series inductor followed by a 1µF capacitor to ground followed by a 0.1µF capacitor to ground positioned as close to the device as possible. C7 provides additional decoupling of the input common mode voltage. L2 provides high-frequency isolation between the analog and digital ground.	C6 = 1µF (Size 0805) C5, C7, C8 = 0.1µF (Size 0603) L1, L2=HZ1206E601R-00 (Size 1206, *Steward*)

OUTLINE DIMENSIONS
16 Lead TSSOP
(RU-16)



Dimensions shown in inches and (mm)