Zero-Drift, Single-Supply, Rail-to-Rail Input/Output Operational Amplifiers

AD8571/AD8572/AD8574

FEATURES
Low Offset Voltage: 1 μV
Input Offset Drift: 0.005 μV/°C
Rail-to-Rail Input and Output Swing
5 V/2.7 V Single-Supply Operation
High Gain, CMRR, PSRR: 130 dB
Ultralow Input Bias Current: 20 pA
Low Supply Current: 750 μA/Op Amp
Overload Recovery Time: 50 μs
No External Capacitors Required

APPLICATIONS
Temperature Sensors
Pressure Sensors
Precision Current Sensing
Strain Gage Amplifiers
Medical Instrumentation
Thermocouple Amplifiers

GENERAL DESCRIPTION

This new family of amplifiers has ultralow offset, drift and bias current. The AD8571, AD8572 and AD8574 are single, dual and quad amplifiers featuring rail-to-rail input and output swings. All are guaranteed to operate from 2.7 V to 5 V single supply.

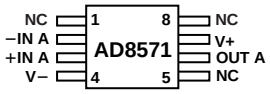
The AD857x family provides the benefits previously found only in expensive autozeroing or chopper-stabilized amplifiers. Using Analog Devices' new topology these new zero-drift amplifiers combine low cost with high accuracy. (No external capacitors are required.) In addition, using a patented spread-spectrum autozero technique, the AD857x family virtually eliminates the intermodulation effects from interaction of the chopping function with the signal frequency in ac applications.

With an offset voltage of only 1 μV and drift of 0.005 μV/°C, the AD8571 is perfectly suited for applications where error sources cannot be tolerated. Position, and pressure sensors, medical equipment, and strain gage amplifiers benefit greatly from nearly zero drift over their operating temperature range. Many more systems require the rail-to-rail input and output swings provided by the AD857x family.

The AD857x family is specified for the extended industrial/automotive (–40°C to +125°C) temperature range. The AD8571 single is available in 8-lead MSOP and narrow 8-lead SOIC packages. The AD8572 dual amplifier is available in 8-lead narrow SO and 8-lead TSSOP surface mount packages. The AD8574 quad is available in narrow 14-lead SOIC and 14-lead TSSOP packages.

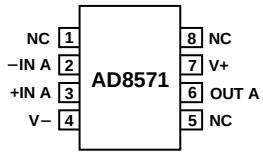
PIN CONFIGURATIONS

8-Lead MSOP (RM Suffix)



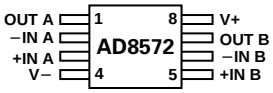
NC = NO CONNECT

8-Lead SOIC (R Suffix)

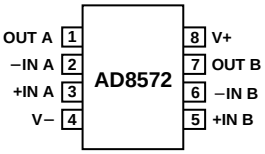


NC = NO CONNECT

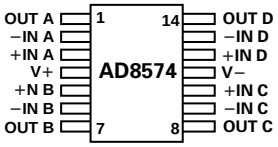
8-Lead TSSOP (RU Suffix)



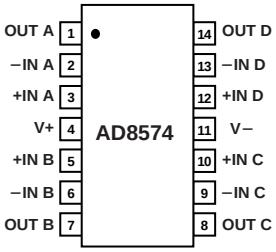
8-Lead SOIC (R Suffix)



14-Lead TSSOP (RU Suffix)



14-Lead SOIC (R Suffix)



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AD8571/AD8572/AD8574—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = 5 V, V_{CM} = 2.5 V, V_O = 2.5 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	5	μV
		–40°C ≤ T_A ≤ +125°C			10	μV
Input Bias Current	I_B			10	50	pA
		–40°C ≤ T_A ≤ +125°C		1.0	1.5	nA
Input Offset Current	I_{OS}			20	70	pA
		–40°C ≤ T_A ≤ +125°C		150	200	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	120	140		dB
		–40°C ≤ T_A ≤ +125°C	115	130		dB
Large Signal Voltage Gain[1]	A_{VO}	R_L = 10 kΩ , V_O = 0.3 V to 4.7 V	125	145		dB
		–40°C ≤ T_A ≤ +125°C	120	135		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C ≤ T_A ≤ +125°C		0.005	0.04	μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	4.99	4.998		V
		–40°C to +125°C	4.99	4.997		V
		R_L = 10 kΩ to GND	4.95	4.98		V
		–40°C to +125°C	4.95	4.975		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		1	10	mV
		–40°C to +125°C		2	10	mV
		R_L = 10 kΩ to V+		10	30	mV
		–40°C to +125°C		15	30	mV
Short Circuit Limit	I_{SC}		±25	±50		mA
		–40°C to +125°C		±40		mA
Output Current	I_O			±30		mA
		–40°C to +125°C		±15		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	120	130		dB
		–40°C ≤ T_A ≤ +125°C	115	130		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		850	975	μA
		–40°C ≤ T_A ≤ +125°C		1,000	1,075	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.4		V/μs
Overload Recovery Time				0.05	0.3	ms
Gain Bandwidth Product	GBP			1.5		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p–p	0 Hz to 10 Hz		1.3		μV p–p
	e_n p–p	0 Hz to 1 Hz		0.41		μV p–p
Voltage Noise Density	e_n	f = 1 kHz		51		nV/$\sqrt{\text{Hz}}$
Current Noise Density	i_n	f = 10 Hz		2		fA/$\sqrt{\text{Hz}}$

NOTE

[1]Gain testing is highly dependent upon test bandwidth.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = 2.7 V, V_{CM} = 1.35 V, V_O = 1.35 V, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	5	µV
		–40°C ≤ T_A ≤ +125°C			10	µV
Input Bias Current	I_B			10	50	pA
		–40°C ≤ T_A ≤ +125°C		1.0	1.5	nA
Input Offset Current	I_{OS}			10	50	pA
		–40°C ≤ T_A ≤ +125°C		150	200	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	115	130		dB
		–40°C ≤ T_A ≤ +125°C	110	130		dB
Large Signal Voltage Gain[1]	A_{VO}	R_L = 10 kΩ , V_O = 0.3 V to 2.4 V	110	140		dB
		–40°C ≤ T_A ≤ +125°C	105	130		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C ≤ T_A ≤ +125°C		0.005	0.04	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	2.685	2.697		V
		–40°C to +125°C	2.685	2.696		V
		R_L = 10 kΩ to GND	2.67	2.68		V
		–40°C to +125°C	2.67	2.675		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		1	10	mV
		–40°C to +125°C		2	10	mV
		R_L = 10 kΩ to V+		10	20	mV
		–40°C to +125°C		15	20	mV
Short Circuit Limit	I_{SC}		±10	±15		mA
		–40°C to +125°C		±10		mA
Output Current	I_O			±10		mA
		–40°C to +125°C		±5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	120	130		dB
		–40°C ≤ T_A ≤ +125°C	115	130		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		750	900	µA
		–40°C ≤ T_A ≤ +125°C		950	1,000	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.5		V/µs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			1		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p–p	0 Hz to 10 Hz		2.0		µV p–p
Voltage Noise Density	e_n	f = 1 kHz		94		nV/√Hz
Current Noise Density	i_n	f = 10 Hz		2		fA/√Hz

NOTE

[1]Gain testing is highly dependent upon test bandwidth.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 6 V
Input Voltage . . . . . GND to V_S + 0.3 V
Differential Input Voltage[2] . . . . . ±5.0 V
ESD (Human Body Model) . . . . . 2,000 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
RM, RU and R Packages . . . . . –65°C to +150°C
Operating Temperature Range
AD8571A/AD8572A/AD8574A . . . . . –40°C to +125°C
Junction Temperature Range
RM, RU and R Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Differential input voltage is limited to ±5.0 V or the supply voltage, whichever is less.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead MSOP (RM)	190	44	°C/W
8-Lead TSSOP (RU)	240	43	°C/W
8-Lead SOIC (R)	158	43	°C/W
14-Lead TSSOP (RU)	180	36	°C/W
14-Lead SOIC (R)	120	36	°C/W

NOTE
[1]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP packages, θ_{JA} is specified for device soldered in circuit board for SOIC and TSSOP packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Brand[1]
AD8571ARM[2]	–40°C to +125°C	8-Lead MSOP	RM-8	AJA
AD8571AR	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8572ARU[3]	–40°C to +125°C	8-Lead TSSOP	RU-8	
AD8572AR	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8574ARU[3]	–40°C to +125°C	14-Lead TSSOP	RU-14	
AD8574AR	–40°C to +125°C	14-Lead SOIC	SO-14	

NOTES
[1]Due to package size limitations, these characters represent the part number.
[2]Available in reels only. 1,000 or 2,500 pieces per reel.
[3]Available in reels only. 2,500 pieces per reel.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8571/AD8572/AD8574 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

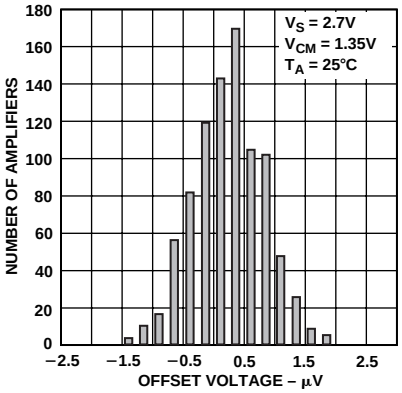


Figure 1. Input Offset Voltage Distribution at 2.7 V

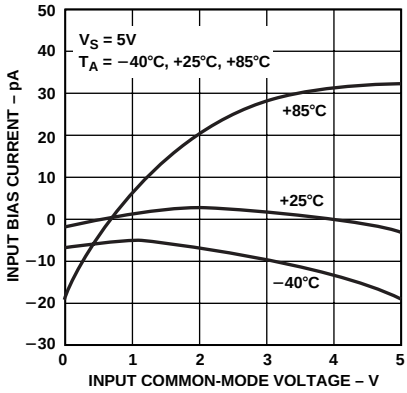


Figure 2. Input Bias Current vs. Common-Mode Voltage

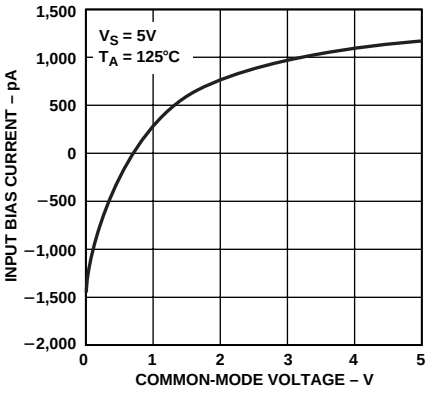


Figure 3. Input Bias Current vs. Common-Mode Voltage

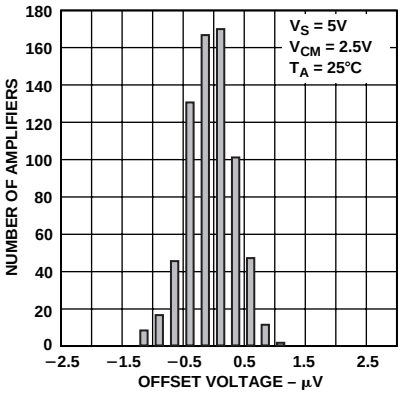


Figure 4. Input Offset Voltage Distribution at 5 V

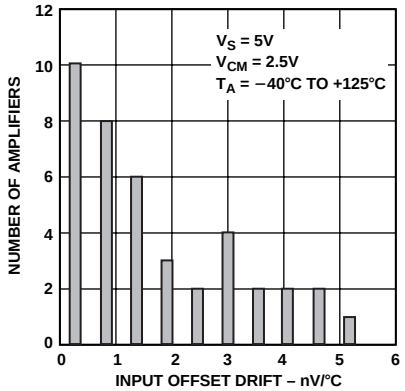


Figure 5. Input Offset Voltage Drift Distribution at 5 V

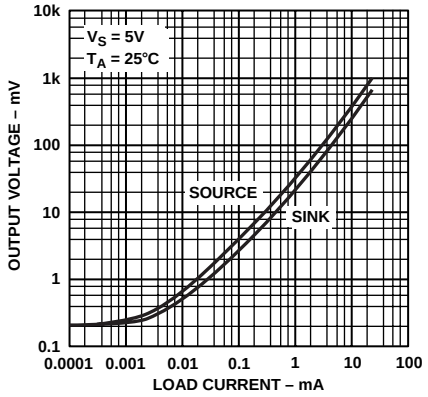


Figure 6. Output Voltage to Supply Rail vs. Output Current at 5 V

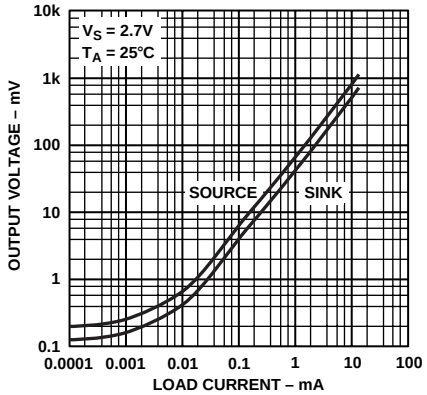


Figure 7. Output Voltage to Supply Rail vs. Output Current at 2.7 V

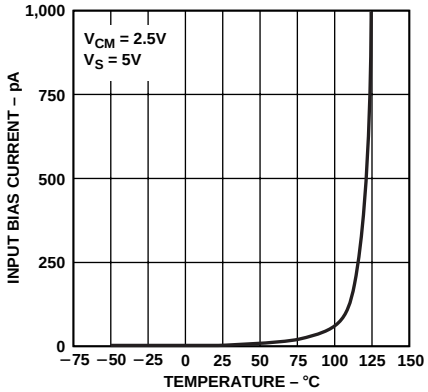


Figure 8. Bias Current vs. Temperature

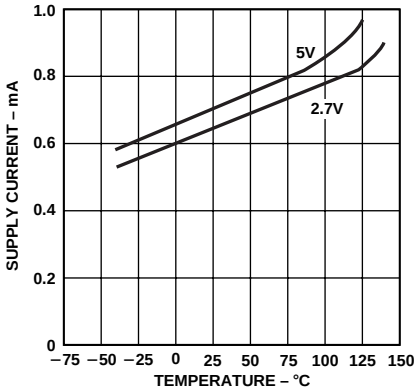


Figure 9. Supply Current vs. Temperature

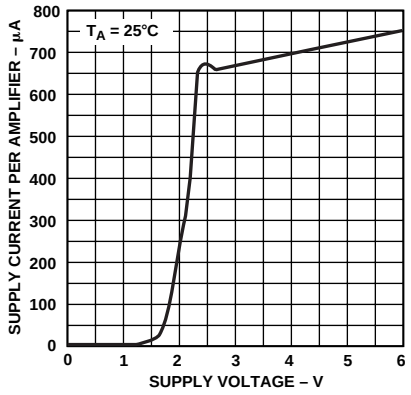


Figure 10. Supply Current vs. Supply Voltage

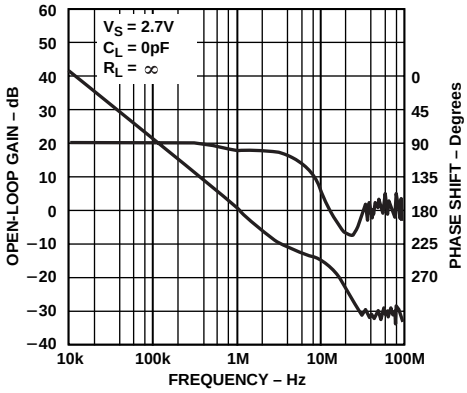


Figure 11. Open-Loop Gain and Phase Shift vs. Frequency at 2.7 V

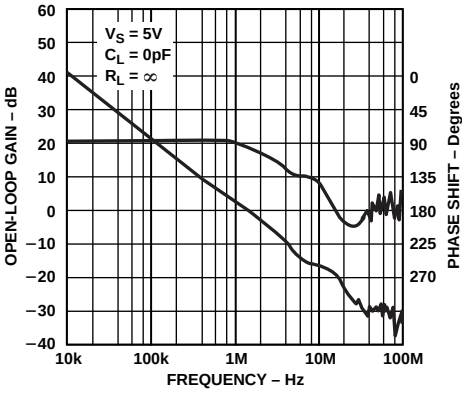


Figure 12. Open-Loop Gain and Phase Shift vs. Frequency at 5 V

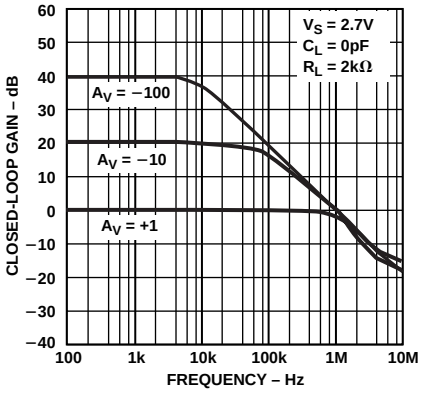


Figure 13. Closed Loop Gain vs. Frequency at 2.7 V

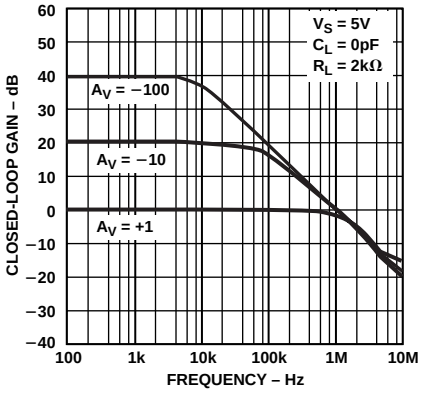


Figure 14. Closed Loop Gain vs. Frequency at 5 V

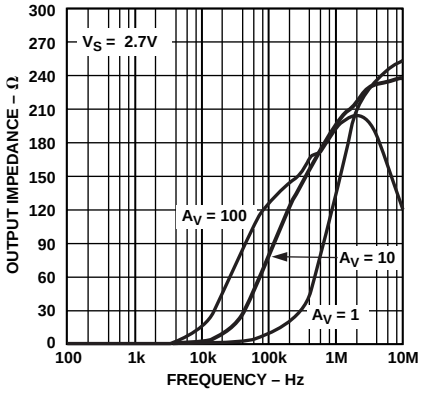


Figure 15. Output Impedance vs. Frequency at 2.7 V

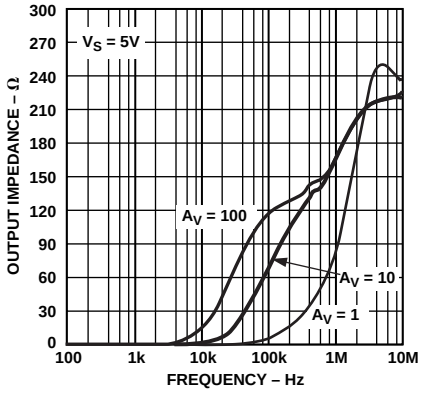


Figure 16. Output Impedance vs. Frequency at 5 V

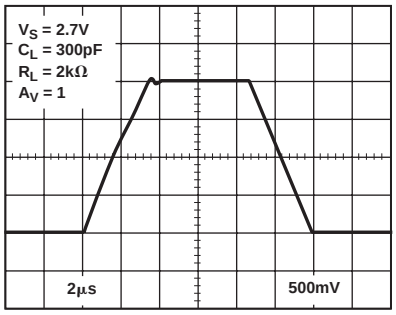


Figure 17. Large Signal Transient Response at 2.7 V

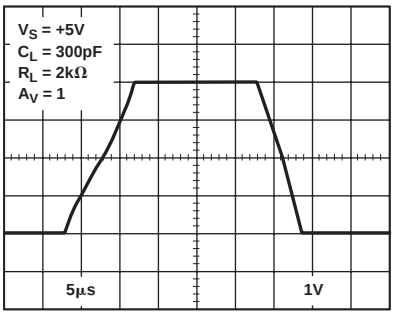


Figure 18. Large Signal Transient Response at 5 V

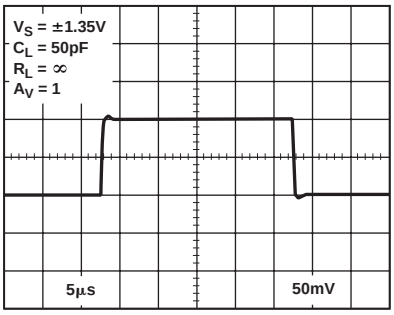


Figure 19. Small Signal Transient Response at 2.7 V

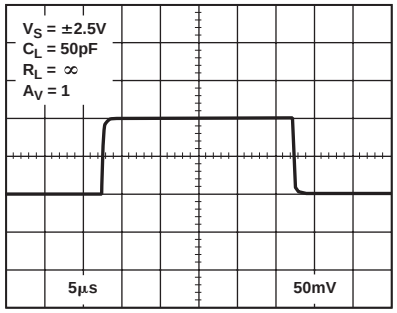


Figure 20. Small Signal Transient Response at 5 V

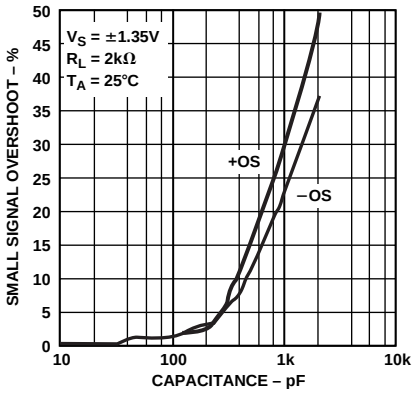


Figure 21. Small Signal Overshoot vs. Load Capacitance at 2.7 V

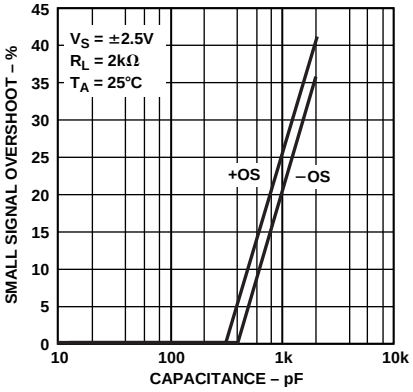


Figure 22. Small Signal Overshoot vs. Load Capacitance at 5 V

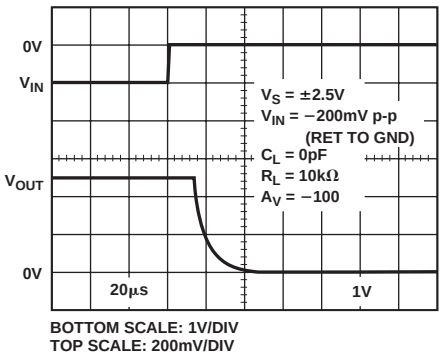


Figure 23. Positive Overvoltage Recovery

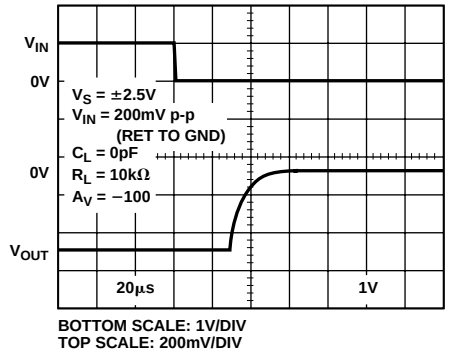


Figure 24. Negative Overvoltage Recovery

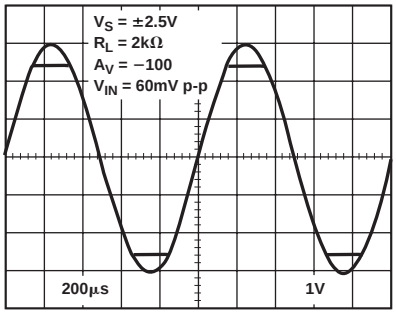


Figure 25. No Phase Reversal

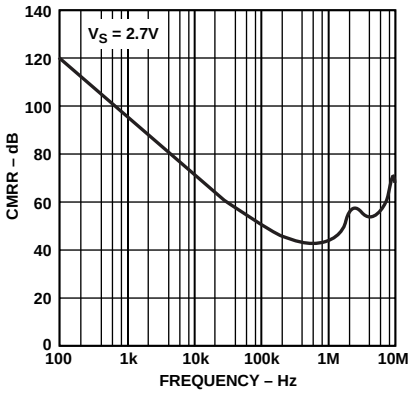


Figure 26. CMRR vs. Frequency at 2.7 V

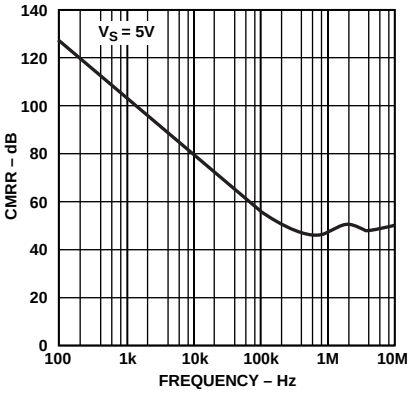


Figure 27. CMRR vs. Frequency at 5 V

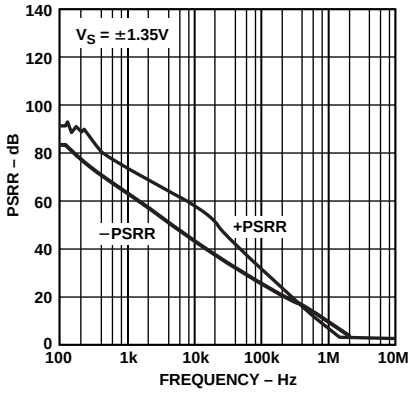


Figure 28. PSRR vs. Frequency at ±1.35 V

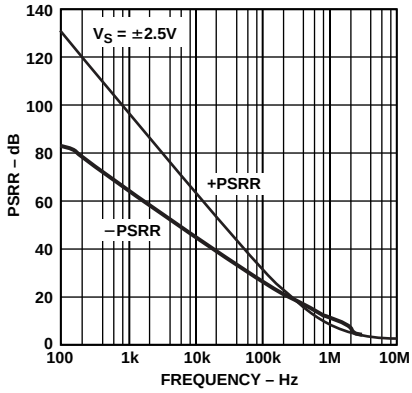


Figure 29. PSRR vs. Frequency at ±2.5 V

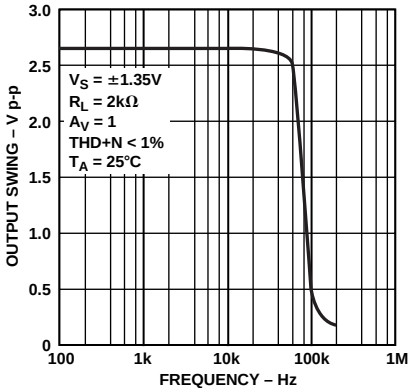


Figure 30. Maximum Output Swing vs. Frequency at 2.7 V

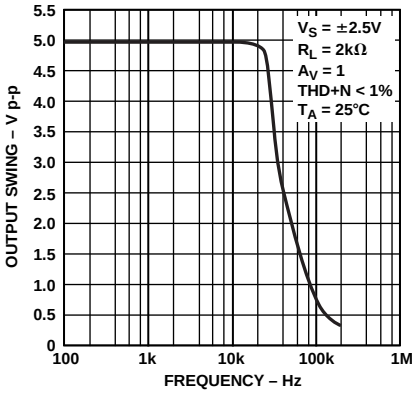


Figure 31. Maximum Output Swing vs. Frequency at 5 V

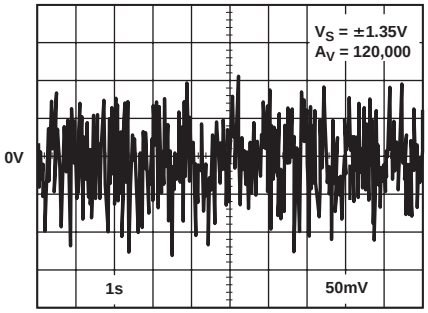


Figure 32. 0.1 Hz to 10 Hz Noise at 2.7 V

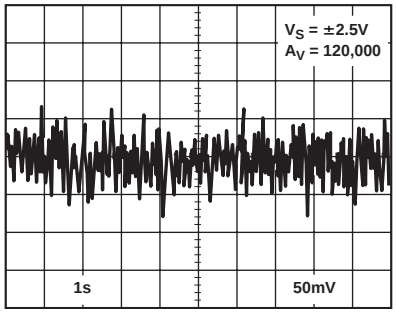


Figure 33. 0.1 Hz to 10 Hz Noise at 5 V

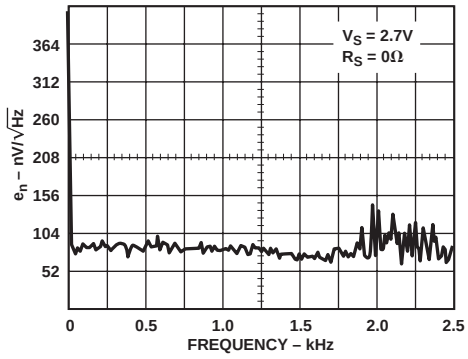


Figure 34. Voltage Noise Density at 2.7 V from 0 Hz to 2.5 kHz

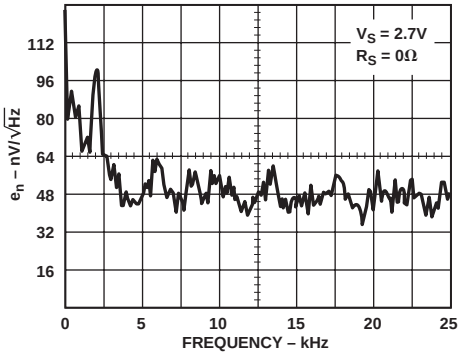


Figure 35. Voltage Noise Density at 2.7 V from 0 Hz to 25 kHz

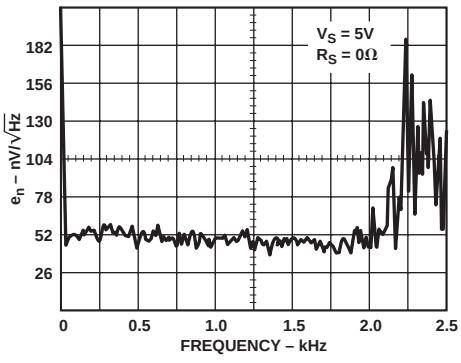


Figure 36. Voltage Noise Density at 5 V from 0 Hz to 2.5 kHz

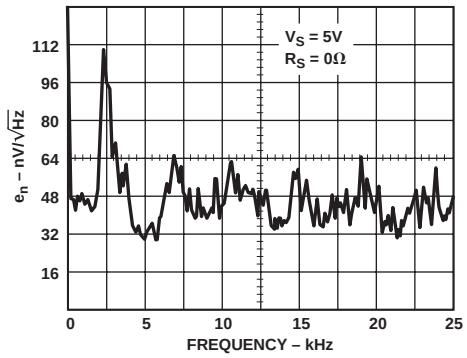


Figure 37. Voltage Noise Density at 5 V from 0 Hz to 25 kHz

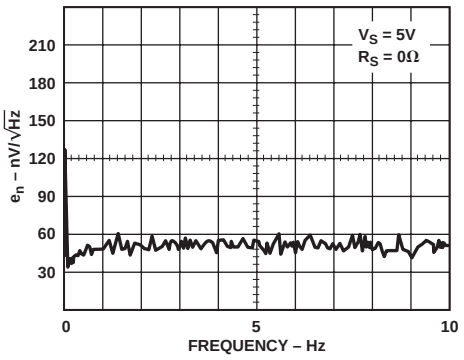


Figure 38. Voltage Noise Density at 5 V from 0 Hz to 10 Hz

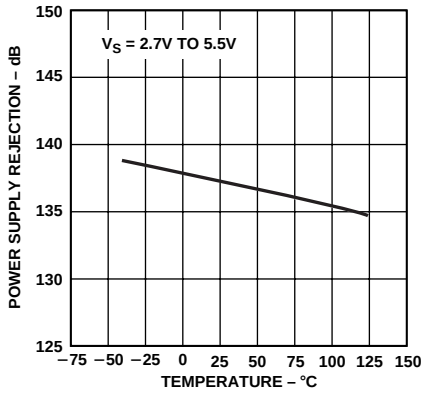


Figure 39. Power-Supply Rejection vs. Temperature

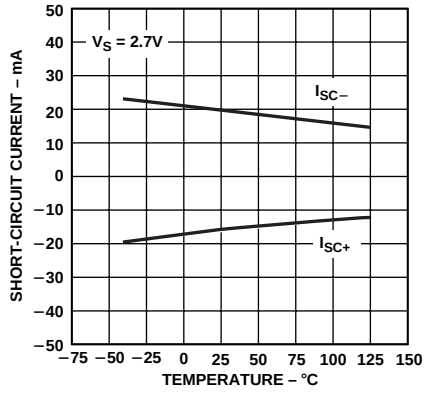


Figure 40. Output Short-Circuit Current vs. Temperature

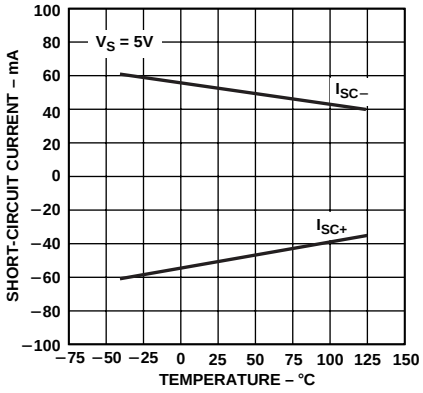


Figure 41. Output Short-Circuit Current vs. Temperature

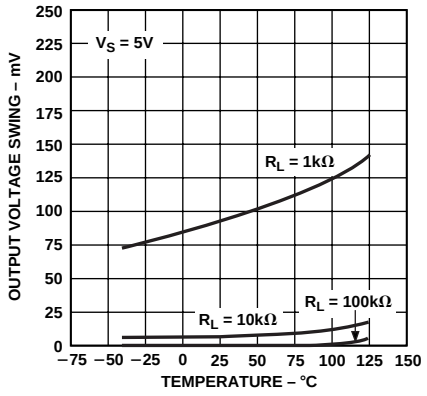


Figure 42. Output Voltage to Supply Rail vs. Temperature

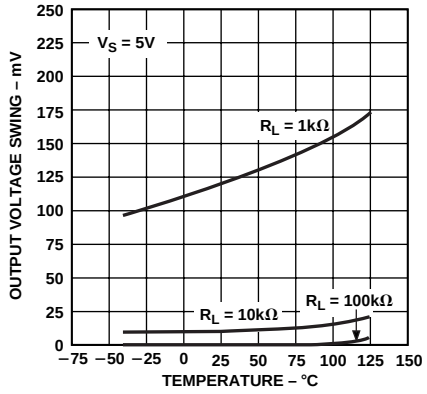


Figure 43. Output Voltage to Supply Rail vs. Temperature

FUNCTIONAL DESCRIPTION

The AD857x family are CMOS amplifiers that achieve their high degree of precision through random frequency autozero stabilization. The autocorrection topology allows the AD857x to maintain its low offset voltage over a wide temperature range, and the randomized autozero clock eliminates any intermodulation distortion (IMD) errors at the amplifier's output.

The AD857x can be run from a single supply voltage as low as 2.7 V. The extremely low offset voltage of 1 μV and no IMD products allows the amplifier to be easily configured for high gains without risk of excessive output voltage errors. This makes the AD857x an ideal amplifier for applications requiring both dc precision and low distortion for ac signals. The extremely small temperature drift of 5 nV/°C ensures a minimum of offset voltage error over its entire temperature range of –40°C to +125°C. These combined features make the AD857x an excellent choice for a variety of sensitive measurement and automotive applications.

Amplifier Architecture

Each AD857x op amp consists of two amplifiers, a main amplifier and a secondary amplifier, used to correct the offset voltage of the main amplifier. Both consist of a rail-to-rail input stage, allowing the input common-mode voltage range to reach both supply rails. The input stage consists of an NMOS differential pair operating concurrently with a parallel PMOS differential pair. The outputs from the differential input stages are combined in another gain stage whose output is used to drive a rail-to-rail output stage.

The wide voltage swing of the amplifier is achieved by using two output transistors in a common-source configuration. The output voltage range is limited by the drain-to-source resistance of these transistors. As the amplifier is required to source or sink more output current, the voltage drop across these transistors increases due to their rds. Simply put, the output voltage will not swing as close to the rail under heavy output current conditions as it will with light output current. This is a characteristic of all rail-to-rail output amplifiers. Figures 6 and 7 show how close the output voltage can get to the rails with a given output current. The output of the AD857x is short circuit protected to approximately 50 mA of current.

The AD857x amplifiers have exceptional gain, yielding greater than 120 dB of open-loop gain with a load of 2 kΩ. Because the output transistors are configured in a common-source configuration, the gain of the output stage, and thus the open-loop gain of the amplifier, is dependent on the load resistance. Open-loop gain will decrease with smaller load resistances. This is another characteristic of rail-to-rail output amplifiers.

Basic Autozero Amplifier Theory

Autocorrection amplifiers are not a new technology. Various IC implementations have been available for over 15 years and some improvements have been made over time. The AD857x design offers a number of significant performance improvements over older versions while attaining a very substantial reduction in device cost. This section offers a simplified explanation of how the AD857x is able to offer extremely low offset voltages and high open-loop gains.

As noted in the previous section on amplifier architecture, each AD857x op amp contains two internal amplifiers. One is used as the primary amplifier, the other as an autocorrection, or nulling, amplifier. Each amplifier has an associated input offset voltage that can be modeled as a dc voltage source in series with the noninverting input. In Figures 44 and 45 these are labeled as V_{OSX}, where x denotes the amplifier associated with the offset; A for the nulling amplifier, B for the primary amplifier. The open-loop gain for the +IN and –IN inputs of each amplifier is given as A_X. Both amplifiers also have a third voltage input with an associated open-loop gain of B_X.

There are two modes of operation determined by the action of two sets of switches in the amplifier: An autozero phase and an amplification phase.

Autozero Phase

In this phase, all ϕA switches are closed and all ϕB switches are opened. Here, the nulling amplifier is taken out of the gain loop by shorting its two inputs together. Of course, there is a degree of offset voltage, shown as V_{OSA}, inherent in the nulling amplifier, which maintains a potential difference between the +IN and –IN inputs. The nulling amplifier feedback loop is closed through ϕA_2 and V_{OSA} appears at the output of the nulling amp and on C_{M1}, an internal capacitor in the AD857x. Mathematically, we can express this in the time domain as:

$$V_{OA}[t] = A_A V_{OSA}[t] - B_A V_{OA}[t] \quad (1)$$

which can be expressed as,

$$V_{OA}[t] = \frac{A_A V_{OSA}[t]}{1 + B_A} \quad (2)$$

This shows us that the offset voltage of the nulling amplifier times a gain factor appears at the output of the nulling amplifier and thus on the C_{M1} capacitor.

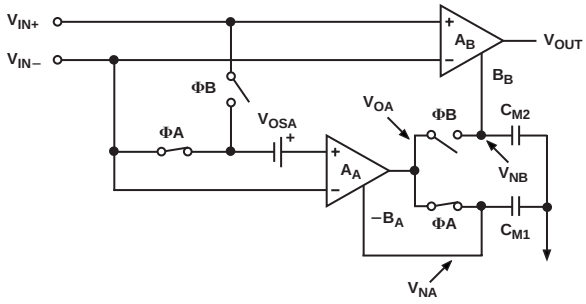


Figure 44. Autozero Phase of the AD857x

Amplification Phase

When the ϕB switches close and the ϕA switches open for the amplification phase, this offset voltage remains on C_{M1} and essentially corrects any error from the nulling amplifier. The voltage across C_{M1} is designated as V_{NA}. Let us also designate V_{IN} as the potential difference between the two inputs to the primary amplifier, or $V_{IN} = (V_{IN+} - V_{IN-})$. Now the output of the nulling amplifier can be expressed as:

$$V_{OA}[t] = A_A\left(V_{IN}[t] - V_{OSA}[t]\right) - B_A V_{NA}[t] \quad (3)$$

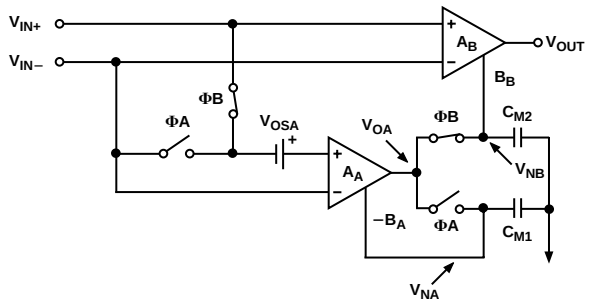


Figure 45. Output Phase of the Amplifier

Because ϕA is now open and there is no place for C_{M1} to discharge, the voltage V_{NA} at the present time t is equal to the voltage at the output of the nulling amp V_{OA} at the time when ϕA was closed. If we call the period of the autocorrection switching frequency T_S, then the amplifier switches between phases every $0.5 \times T_S$. Therefore, in the amplification phase:

$$V_{NA}[t] = V_{NA}\left[t - \frac{1}{2}T_S\right] \quad (4)$$

And substituting Equation 4 and Equation 2 into Equation 3 yields:

$$V_{OA}[t] = A_A V_{IN}[t] + A_A V_{OSA}[t] - \frac{A_A B_A V_{OSA}\left[t - \frac{1}{2}T_S\right]}{1 + B_A} \quad (5)$$

For the sake of simplification, let us assume that the autocorrection frequency is much faster than any potential change in V_{OSA} or V_{OSB}. This is a good assumption since changes in offset voltage are a function of temperature variation or long-term wear time, both of which are much slower than the auto-zero clock frequency of the AD857x. This effectively makes V_{OS} time invariant and we can rearrange Equation 5 and rewrite it as:

$$V_{OA}[t] = A_A V_{IN}[t] + \frac{A_A(1 + B_A)\ V_{OSA} - A_A B_A V_{OSA}}{1 + B_A} \quad (6)$$

or,

$$V_{OA}[t] = A_A\left(V_{IN}[t] + \frac{V_{OSA}}{1 + B_A}\right) \quad (7)$$

We can already get a feel for the autozeroing in action. Note the V_{OS} term is reduced by a $1 + B_A$ factor. This shows how the nulling amplifier has greatly reduced its own offset voltage error even before correcting the primary amplifier. Now the primary amplifier output voltage is the voltage at the output of the AD857x amplifier. It is equal to:

$$V_{OUT}[t] = A_B\left(V_{IN}[t] + V_{OSB}\right) + B_B V_{NB} \quad (8)$$

In the amplification phase, $V_{OA} = V_{NB}$, so this can be rewritten as:

$$V_{OUT}[t] = A_B V_{IN}[t] + A_B V_{OSB} + B_B\left[A_A\left(V_{IN}[t] + \frac{V_{OSA}}{1 + B_A}\right)\right] \quad (9)$$

Combining terms,

$$V_{OUT}[t] = V_{IN}[t]\left(A_B + A_A B_B\right) + \frac{A_A B_B V_{OSA}}{1 + B_A} + A_B V_{OSB} \quad (10)$$

The AD857x architecture is optimized in such a way that $A_A = A_B$ and $B_A = B_B$ and $B_A >> 1$. Also, the gain product to $A_A B_B$ is much greater than A_B. These allow Equation 10 to be simplified to:

$$V_{OUT}[t] \approx V_{IN}[t] A_A B_A + A_A\left(V_{OSA} + V_{OSB}\right) \quad (11)$$

Most obvious is the gain product of both the primary and nulling amplifiers. This $A_A B_A$ term is what gives the AD857x its extremely high open-loop gain. To understand how V_{OSA} and V_{OSB} relate to the overall effective input offset voltage of the complete amplifier, we should set up the generic amplifier equation of:

$$V_{OUT} = k \times \left(V_{IN} + V_{OS,\ EFF}\right) \quad (12)$$

Where k is the open-loop gain of an amplifier and $V_{OS,\ EFF}$ is its effective offset voltage. Putting Equation 12 into the form of Equation 11 gives us:

$$V_{OUT}[t] \approx V_{IN}[t] A_A B_A + V_{OS,\ EFF} A_A B_A \quad (13)$$

And from here, it is easy to see that:

$$V_{OS,\ EFF} \approx \frac{V_{OSA} + V_{OSB}}{B_A} \quad (14)$$

Thus, the offset voltages of both the primary and nulling amplifiers are reduced by the gain factor B_A. This takes a typical input offset voltage from several millivolts down to an effective input offset voltage of submicrovolts. This autocorrection scheme is what makes the AD857x family of amplifiers among the most precise amplifiers in the world.

High Gain, CMRR, PSRR

Common-mode and power supply rejection are indications of the amount of offset voltage an amplifier has as a result of a change in its input common-mode or power supply voltages. As shown in the previous section, the autocorrection architecture of the AD857x allows it to quite effectively minimize offset voltages. The technique also corrects for offset errors caused by common-mode voltage swings and power supply variations. This results in superb CMRR and PSRR figures in excess of 130 dB. Because the autocorrection occurs continuously, these figures can be maintained across the device's entire temperature range, from –40°C to +125°C.

Maximizing Performance Through Proper Layout

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the AD857x, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 46 shows how the guard ring should be configured and Figure 47 shows the top view of how a surface mount layout can be arranged. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the noninverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

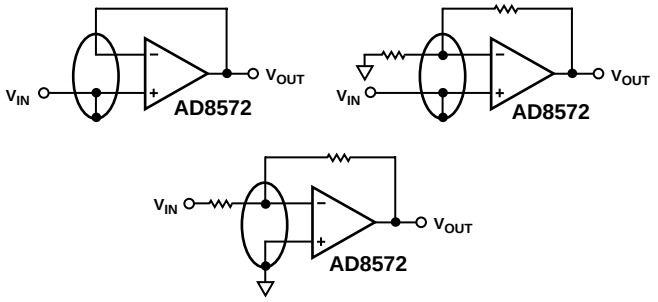


Figure 46. Guard Ring Layout and Connections to Reduce PC Board Leakage Currents

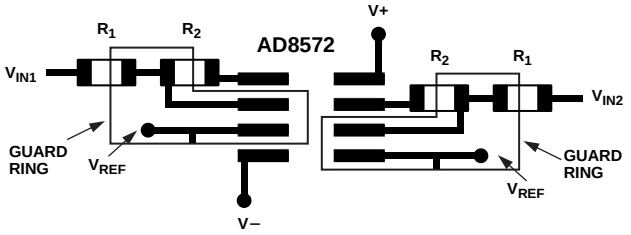


Figure 47. Top View of AD8572 SOIC Layout with Guard Rings

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. Figure 48 shows a cross-section diagram view of the thermal voltage error sources. If the temperature of the PC board at one end of the component (T_{A1}) is different from the temperature at the other end (T_{A2}), the Seebeck voltages will not be equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner will ensure both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board will further reduce this error. The use of a ground plane will help distribute heat throughout the board and will also reduce EMI noise pickup.

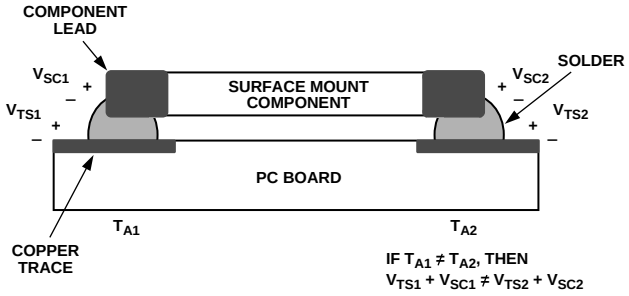
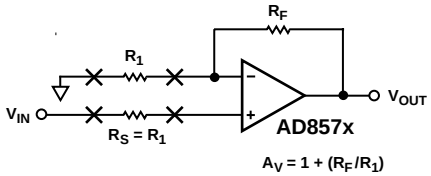


Figure 48. Mismatch in Seebeck Voltages Causes a Thermoelectric Voltage Error



NOTE: R_S SHOULD BE PLACED IN CLOSE PROXIMITY AND ALIGNMENT TO R_1 TO BALANCE SEEBECK VOLTAGES

Figure 49. Using Dummy Components to Cancel Thermoelectric Voltage Errors

1/f Noise Characteristics

Another advantage of autozero amplifiers is their ability to cancel flicker noise. Flicker noise, also known as 1/f noise, is noise inherent in the physics of semiconductor devices and increases 3 dB for every octave decrease in frequency. The 1/f corner frequency of an amplifier is the frequency at which the flicker noise is equal to the broadband noise of the amplifier. At lower frequencies, flicker noise dominates, causing higher degrees of error for sub-Hertz frequencies or dc precision applications.

Because the AD857x amplifiers are self-correcting op amps, they do not have increasing flicker noise at lower frequencies. In essence, low frequency noise is treated as a slowly varying offset error and is greatly reduced as a result of autocorrection. The correction becomes more effective as the noise frequency approaches dc, offsetting the tendency of the noise to increase exponentially as frequency decreases. This allows the AD857x to have lower noise near dc than standard low-noise amplifiers that are susceptible to 1/f noise.

Random Autozero Correction Eliminates Intermodulation Distortion

The AD857x can be used as a conventional op amp for gains up to 1 MHz. The autozero correction frequency of the device continuously varies, based on a pseudo-random generator with a uniform distribution from 2 kHz to 4 kHz. The randomization of the autocorrection clock creates a continuous randomization of intermodulation distortion (IMD) products, which show up as simple broadband noise at the output of the amplifier. This noise naturally combines with the amplifier's voltage noise in a root-squared-sum fashion, resulting in an output free of IMD. Figure 50a shows the spectral output of an AD8572 with the amplifier configured for unity gain and the input grounded. Figure 50b shows the spectral output with the amplifier configured for a gain of 60 dB.

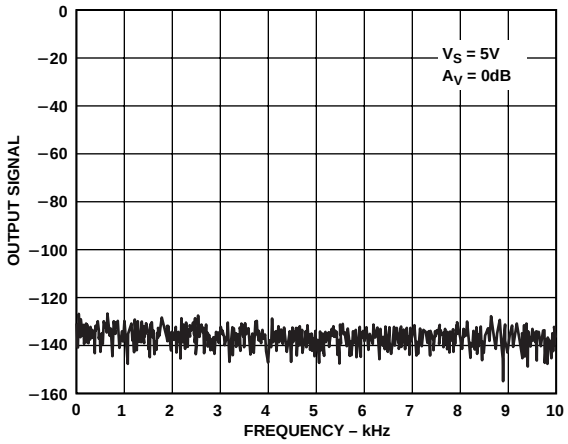


Figure 50a. Spectral Analysis of AD857x Output in Unity Gain Configuration

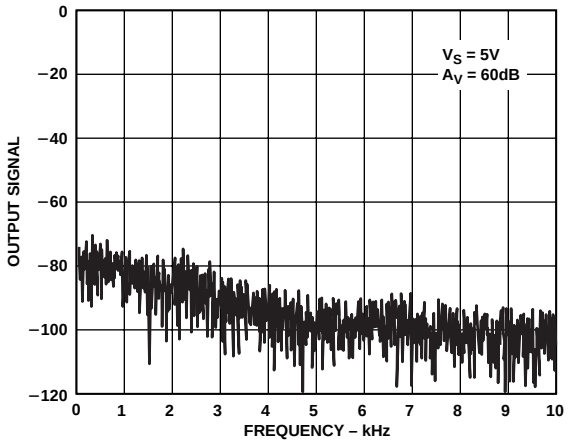


Figure 50b. Spectral Analysis of AD857x Output with 60 dB Gain

Figure 51 shows the spectral output of an AD8572 configured in a high gain (60 dB) with a 1 mV input signal applied. Note the absence of any IMD products in the spectrum. The signal-to-noise (SNR) ratio of the output signal is better than 60 dB, or 0.1%.

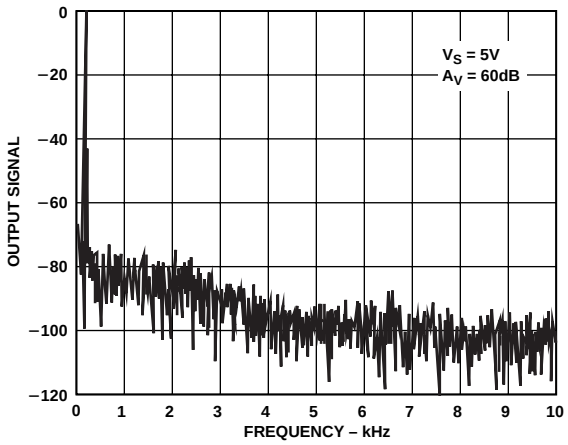


Figure 51. Spectral Analysis of AD857x in High Gain with an Input Signal

Broadband and External Resistor Noise Considerations

The total broadband noise output from any amplifier is primarily a function of three types of noise: Input voltage noise from the amplifier, input current noise from the amplifier and Johnson noise from the external resistors used around the amplifier. Input voltage noise, or e_n, is strictly a function of the amplifier used. The Johnson noise from a resistor is a function of the resistance and the temperature. Input current noise, or i_n, creates an equivalent voltage noise proportional to the resistors used around the amplifier. These noise sources are not correlated with each other and their combined noise sums in a root-squared-sum fashion. The full equation is given as:

$$e_{n,\,TOTAL} = \left[e_n^{\,2} + 4kTr_s + \left(i_n r_s\right)^2 \right]^{1/2} \qquad (15)$$

Where, e_n = The input voltage noise of the amplifier,
i_n = The input current noise of the amplifier,
r_s = Source resistance connected to the noninverting terminal,
k = Boltzmann's constant (1.38×10^{-23} J/K)
T = Ambient temperature in Kelvin (K = 273.15 + °C)

The input voltage noise density, e_n, of the AD857x is 51 nV/$\sqrt{\text{Hz}}$, and the input noise, i_n, is 2 fA/$\sqrt{\text{Hz}}$. The $e_{n,\,\text{TOTAL}}$ will be dominated by input voltage noise provided the source resistance is less than 172 kΩ. With source resistance greater than 172 kΩ, the overall noise of the system will be dominated by the Johnson noise of the resistor itself.

Because the input current noise of the AD857x is very small, i_n does not become a dominant term unless r_s is greater than 4 GΩ, which is an impractical value of source resistance.

The total noise, $e_{n,\,\text{TOTAL}}$, is expressed in volts-per-square-root Hertz, and the equivalent rms noise over a certain bandwidth can be found as:

$$e_n = e_{n,\,TOTAL} \times \sqrt{BW} \qquad (16)$$

Where BW is the bandwidth of interest in Hertz.

For a complete treatise on circuit noise analysis, please refer to the *1995 Linear Design Seminar* book available from Analog Devices.

Output Overdrive Recovery

The AD857x amplifiers have an excellent overdrive recovery of only 200 µs from either supply rail. This characteristic is particularly difficult for autocorrection amplifiers, as the nulling amplifier requires a substantial amount of time to error correct the main amplifier back to a valid output. Figure 23 and Figure 24 show the positive and negative overdrive recovery time for the AD857x.

The output overdrive recovery for an autocorrection amplifier is defined as the time it takes for the output to correct to its final voltage from an overload state. It is measured by placing the amplifier in a high gain configuration with an input signal that forces the output voltage to the supply rail. The input voltage is then stepped down to the linear region of the amplifier, usually to half-way between the supplies. The time from the input signal step-down to the output settling to within 100 µV of its final value is the overdrive recovery time. Most competitors' autocorrection amplifiers require a number of autozero clock cycles to recover from output overdrive and some can take several milliseconds for the output to settle properly.

Input Overvoltage Protection

Although the AD857x is a rail-to-rail input amplifier, care should be taken to ensure that the potential difference between the inputs does not exceed 5 V. Under normal operating conditions, the amplifier will correct its output to ensure the two inputs are at the same voltage. However, if the device is configured as a comparator, or is under some unusual operating condition, the input voltages may be forced to different potentials. This could cause excessive current to flow through internal diodes in the AD857x used to protect the input stage against overvoltage.

If either input exceeds either supply rail by more than 0.3 V, large amounts of current will begin to flow through the ESD protection diodes in the amplifier. These diodes are connected between the inputs and each supply rail to protect the input transistors against an electrostatic discharge event and are normally reverse-biased. However, if the input voltage exceeds the supply voltage, these ESD diodes will become forward-biased. Without current-limiting, excessive amounts of current could flow through these diodes causing permanent damage to the device. If inputs are subject to overvoltage, appropriate series resistors should be inserted to limit the diode current to less than 2 mA maximum.

Output Phase Reversal

Output phase reversal occurs in some amplifiers when the input common-mode voltage range is exceeded. As common-mode voltage is moved outside of the common-mode range, the outputs of these amplifiers will suddenly jump in the opposite direction to the supply rail. This is the result of the differential input pair shutting down, causing a radical shifting of internal voltages which results in the erratic output behavior.

The AD857x amplifier has been carefully designed to prevent any output phase reversal, provided both inputs are maintained within the supply voltages. If one or both inputs could exceed either supply voltage, a resistor should be placed in series with the input to limit the current to less than 2 mA. This will ensure the output will not reverse its phase.

Capacitive Load Drive

The AD857x has excellent capacitive load-driving capabilities and can safely drive up to 10 nF from a single 5 V supply. Although the device is stable, capacitive loading will limit the bandwidth of the amplifier. Capacitive loads will also increase the amount of overshoot and ringing at the output. An R-C snubber network, Figure 52, can be used to compensate the amplifier against capacitive load ringing and overshoot.

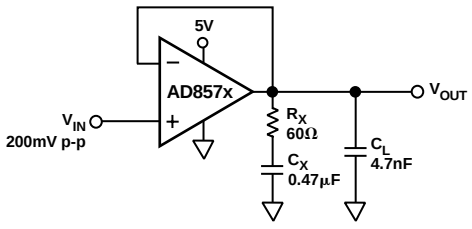


Figure 52. Snubber Network Configuration for Driving Capacitive Loads

Although the snubber will not recover the loss of amplifier bandwidth from the load capacitance, it will allow the amplifier to drive larger values of capacitance while maintaining a minimum of overshoot and ringing. Figure 53 shows the output of an AD857x driving a 1 nF capacitor with and without a snubber network.

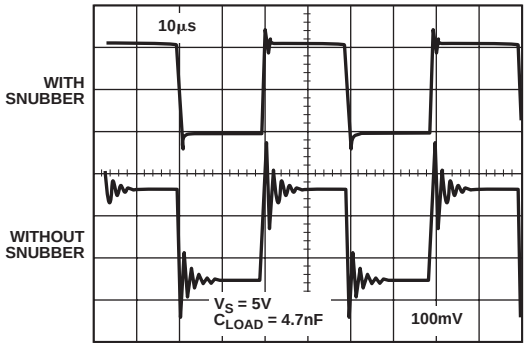


Figure 53. Overshoot and Ringing are Substantially Reduced Using a Snubber Network

The optimum value for the resistor and capacitor is a function of the load capacitance and is best determined empirically since actual C_{LOAD} will include stray capacitances and may differ substantially from the nominal capacitive load. Table I shows some snubber network values that can be used as starting points.

Table I. Snubber Network Values for Driving Capacitive Loads

C_{LOAD}	R_X	C_X
1 nF	200 Ω	1 nF
4.7 nF	60 Ω	0.47 μF
10 nF	20 Ω	10 μF

Power-Up Behavior

On power-up, the AD857x will settle to a valid output within 5 μs. Figure 54a shows an oscilloscope photo of the output of the amplifier along with the power supply voltage, and Figure 54b shows the test circuit. With the amplifier configured for unity gain, the device takes approximately 5 μs to settle to its final output voltage. This turn-on response time is much faster than most other autocorrection amplifiers, which can take hundreds of microseconds or longer for their output to settle.

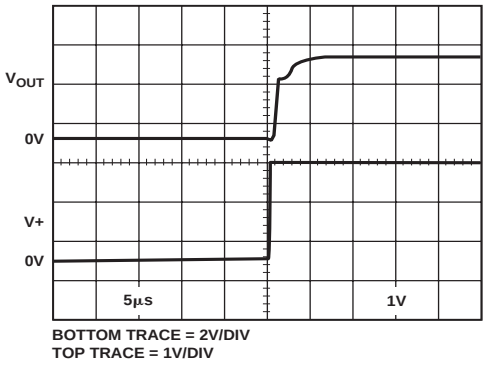


Figure 54a. AD857x Output Behavior on Power-Up

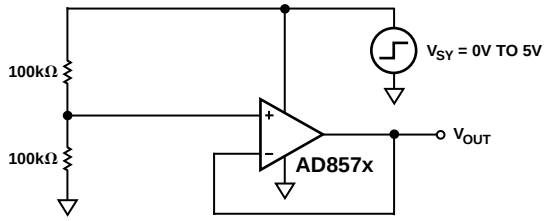


Figure 54b. AD857x Test Circuit for Turn-On Time

APPLICATIONS

A 5 V Precision Strain-Gage Circuit

The extremely low offset voltage of the AD8572 makes it an ideal amplifier for any application requiring accuracy with high gains, such as a weigh scale or strain-gage. Figure 55 shows a configuration for a single supply, precision strain-gage measurement system.

A REF192 provides a 2.5 V precision reference voltage for A2. The A2 amplifier boosts this voltage to provide a 4.0 V reference for the top of the strain-gage resistor bridge. Q1 provides the current drive for the 350 Ω bridge network. A1 is used to amplify the output of the bridge with the full-scale output voltage equal to:

$$\frac{2\times\left(R_1+R_2\right)}{R_B} \tag{17}$$

Where R_B is the resistance of the load cell. Using the values given in Figure 55, the output voltage will linearly vary from 0 V with no strain to 4 V under full strain.

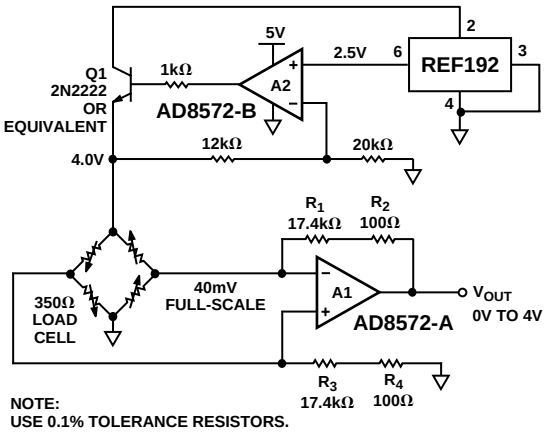


Figure 55. A 5 V Precision Strain-Gage Amplifier

3 V Instrumentation Amplifier

The high common-mode rejection, high open-loop gain, and operation down to 3 V of supply voltage makes the AD857x an excellent choice of op amp for discrete single supply instrumentation amplifiers. The common-mode rejection ratio of the AD857x is greater than 120 dB, but the CMRR of the system is also a function of the external resistor tolerances. The gain of the difference amplifier shown in Figure 56 is given as:

$$V_{OUT}=V1\left(\frac{R_4}{R_3+R_4}\right)\left(1+\frac{R_1}{R_2}\right)-V2\left(\frac{R_2}{R_1}\right) \tag{18}$$

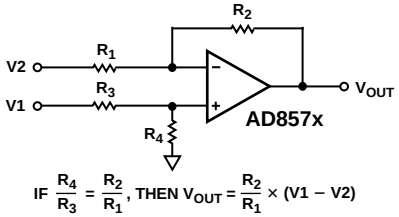


Figure 56. Using the AD857x as a Difference Amplifier

In an ideal difference amplifier, the ratio of the resistors are set exactly equal to:

$$A_V=\frac{R_2}{R_1}=\frac{R_4}{R_3} \tag{19}$$

Which sets the output voltage of the system to:

$$V_{OUT}=A_V\left(V1-V2\right) \tag{20}$$

Due to finite component tolerance the ratio between the four resistors will not be exactly equal, and any mismatch results in a reduction of common-mode rejection from the system. Referring to Figure 56, the exact common-mode rejection ratio can be expressed as:

$$CMRR=\frac{R_1R_4+2R_2R_4+R_2R_3}{2R_1R_4-2R_2R_3} \tag{21}$$

In the 3 op amp instrumentation amplifier configuration shown in Figure 57, the output difference amplifier is set to unity gain with all four resistors equal in value. If the tolerance of the resistors used in the circuit is given as δ, the worst-case CMRR of the instrumentation amplifier will be:

$$CMRR_{MIN}=\frac{1}{2\delta} \tag{22}$$

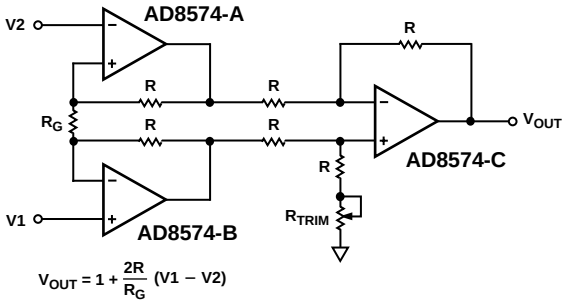


Figure 57. A Discrete Instrumentation Amplifier Configuration

Thus, using 1% tolerance resistors would result in a worst-case system CMRR of 0.02, or 34 dB. Therefore either high precision resistors or an additional trimming resistor, as shown in Figure 57, should be used to achieve high common-mode rejection. The value of this trimming resistor should be equal to the value of R multiplied by its tolerance. For example, using 10 kΩ resistors with 1% tolerance would require a series trimming resistor equal to 100 Ω.

A High Accuracy Thermocouple Amplifier

Figure 58 shows a K-type thermocouple amplifier configuration with cold-junction compensation. Even from a 5 V supply, the AD8571 can provide enough accuracy to achieve a resolution of better than 0.02°C from 0°C to 500°C. D1 is used as a temperature measuring device to correct the cold-junction error from the thermocouple and should be placed as close as possible to the two terminating junctions. With the thermocouple measuring tip immersed in a zero-degree ice bath, R_6 should be adjusted until the output is at 0 V.

Using the values shown in Figure 58, the output voltage will track temperature at 10 mV/°C. For a wider range of temperature measurement, R_9 can be decreased to 62 kΩ. This will create a 5 mV/°C change at the output, allowing measurements of up to 1000°C.

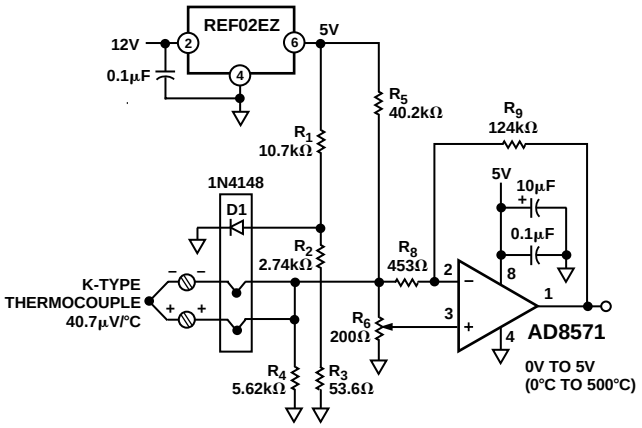


Figure 58. A Precision K-Type Thermocouple Amplifier with Cold-Junction Compensation

Precision Current Meter

Because of its low input bias current and superb offset voltage at single supply voltages, the AD857x is an excellent amplifier for precision current monitoring. Its rail-to-rail input allows the amplifier to be used as either a high-side or low-side current monitor. Using both amplifiers in the AD8572 provides a simple method to monitor both current supply and return paths for load or fault detection.

Figure 59 shows a high-side current monitor configuration. Here, the input common-mode voltage of the amplifier will be at or near the positive supply voltage. The amplifier's rail-to-rail input provides a precise measurement, even with the input common-mode voltage at the supply voltage. The CMOS input structure does not draw any input bias current, ensuring a minimum of measurement error.

The 0.1 Ω resistor creates a voltage drop to the noninverting input of the AD857x. The amplifier's output is corrected until this voltage appears at the inverting input. This creates a current through R_1, which in turn flows through R_2. The Monitor Output is given by:

$$Monitor\ Output = R_2 \times \left(\frac{R_{SENSE}}{R_1} \right) \times I_L \qquad (23)$$

Using the components shown in Figure 59, the Monitor Output transfer function is 2.5 V/A.

Figure 60 shows the low-side monitor equivalent. In this circuit, the input common-mode voltage to the AD8572 will be at or near ground. Again, a 0.1 Ω resistor provides a voltage drop proportional to the return current. The output voltage is given as:

$$V_{OUT} = V + -\left(\frac{R_2}{R_1} \times R_{SENSE} \times I_L \right) \qquad (24)$$

For the component values shown in Figure 60, the output transfer function decreases from V at –2.5 V/A.

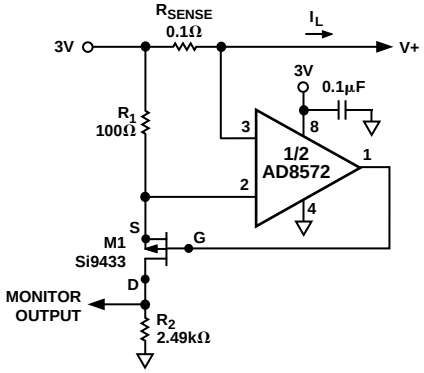


Figure 59. A High-Side Load Current Monitor

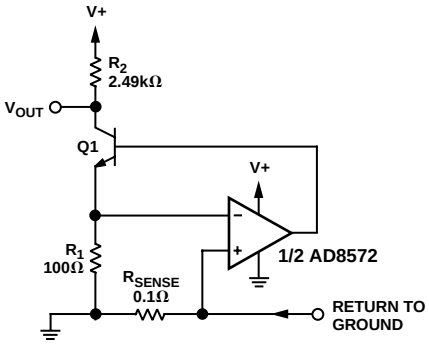


Figure 60. A Low-Side Load Current Monitor

Precision Voltage Comparator

The AD857x can be operated open-loop and used as a precision comparator. The AD857x has less than 50 µV of offset voltage when run in this configuration. The slight increase of offset voltage stems from the fact that the autocorrection architecture operates with lowest offset in a closed-loop configuration, that is, one with negative feedback. With 50 mV of overdrive, the device has a propagation delay of 15 µs on the rising edge and 8 µs on the falling edge.

Care should be taken to ensure the maximum differential voltage of the device is not exceeded. For more information, please refer to the section on Input Overvoltage Protection.

SPICE Model

The SPICE macro-model for the AD857x amplifier is given in Listing 1. This model simulates the typical specifications for the AD857x, and it can be downloaded from the Analog Devices website at **http://www.analog.com.** The schematic of the macro-model is shown in Figure 61.

Transistors M1 through M4 simulate the rail-to-rail input differential pairs in the AD857x amplifier. The EOS voltage source in series with the noninverting input establishes not only the 1 μV offset voltage, but is also used to establish common-mode and power supply rejection ratios and input voltage noise. The differential voltages from nodes 14 to 16 and nodes 17 to 18 are reflected to E1, which is used to simulate a secondary pole-zero combination in the open-loop gain of the amplifier.

The voltage at node 32 is then reflected to G1, which adds an additional gain stage and, in conjunction with CF, establishes the slew rate of the model at 0.5 V/μs. M5 and M6 are in a common-source configuration, similar to the output stage of the AD857x amplifier. EG1 and EG2 fix the quiescent current in these two transistors at 100 μA, and also help accurately simulate the V_{OUT} vs. I_{OUT} characteristic of the amplifier.

The network around ECM1 creates the common-mode voltage error, with CCM1 setting the corner frequency for the CMRR roll-off. The power supply rejection error is created by the network around EPS1, with CPS3 establishing the corner frequency for the PSRR roll-off. The two current loops around nodes 80 and 81 are used to create a 51 nV/√Hz noise figure across RN2. All three of these error sources are reflected to the input of the op amp model through EOS. Finally, GSY is used to accurately model the supply current versus supply voltage increase in the AD857x.

This macro-model has been designed to accurately simulate a number of specifications exhibited by the AD857x amplifier, and is one of the most true-to-life macro-models available for any op amp. It is optimized for operation at 27°C. Although the model will function at different temperatures, it may lose accuracy with respect to the actual behavior of the AD857x.

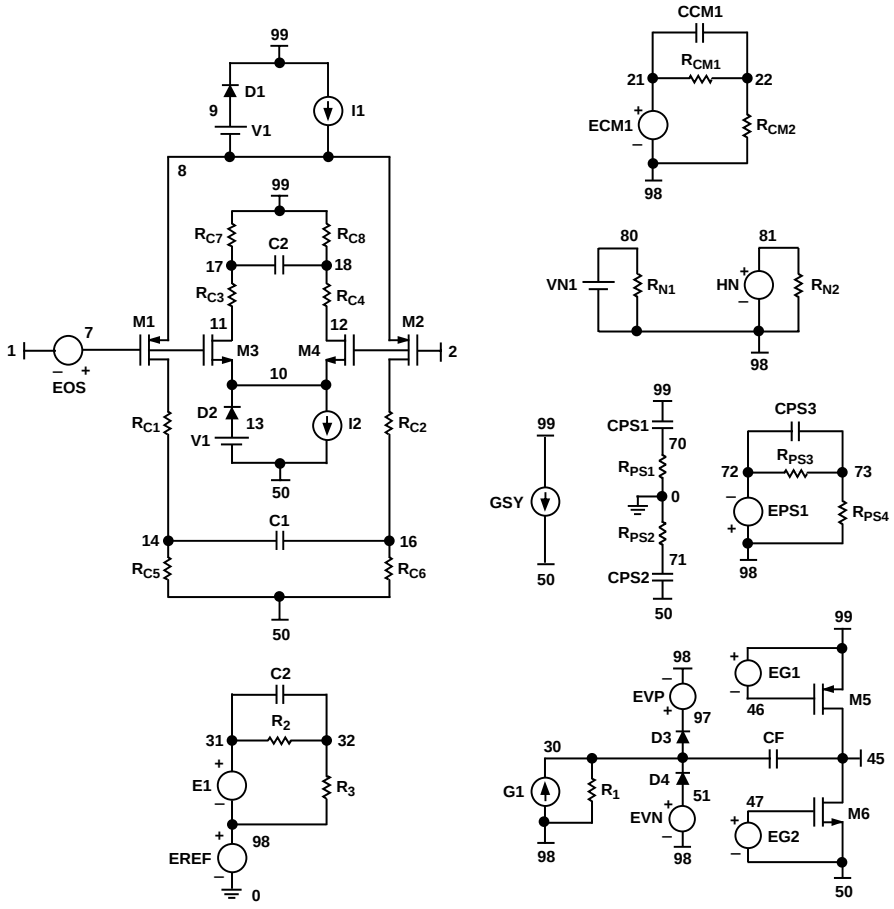


Figure 61. Schematic of the AD857x SPICE Macro-Model

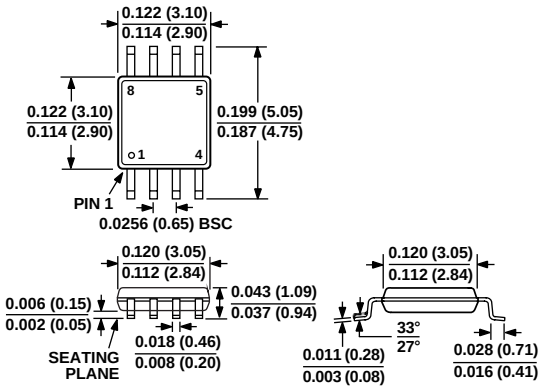
SPICE macro-model for the AD857x

```
* AD8572 SPICE Macro-model
* Typical Values
* 7/99, Ver. 1.0
* TAM / ADSC
*
* Copyright 1999 by Analog Devices
*
* Refer to "README.DOC" file for License
* Statement.  Use of this model indicates
* your acceptance of the terms and
* provisions in the License Statement.
*
* Node Assignments
*                noninverting input
*                |  inverting input
*                |  |  positive supply
*                |  |  |  negative supply
*                |  |  |  |  output
*                |  |  |  |  |
*                |  |  |  |  |
.SUBCKT AD8572   1  2  99 50 45
*
* INPUT STAGE
*
M1   4  7  8  8 PIX L=1E-6 W=355.3E-6
M2   6  2  8  8 PIX L=1E-6 W=355.3E-6
M3  11  7 10 10 NIX L=1E-6 W=355.3E-6
M4  12  2 10 10 NIX L=1E-6 W=355.3E-6
RC1  4 14 9E+3
RC2  6 16 9E+3
RC3 17 11 9E+3
RC4 18 12 9E+3
RC5 14 50 1E+3
RC6 16 50 1E+3
RC7 99 17 1E+3
RC8 99 18 1E+3
C1  14 16 30E-12
C2  17 18 30E-12
I1  99  8 100E-6
I2  10 50 100E-6
V1  99  9 0.3
V2  13 50 0.3
D1   8  9 DX
D2  13 10 DX
EOS  7  1 POLY(3) (22,98) (73,98) (81,98)
+ 1E-6 1 1 1
IOS  1  2 2.5E-12
*
* CMRR 120dB, ZERO AT 20Hz
*
ECM1 21 98 POLY(2) (1,98) (2,98) 0 .5 .5
RCM1 21 22 50E+6
CCM1 21 22 159E-12
RCM2 22 98 50
*
* PSRR=120dB, ZERO AT 1Hz
*
RPS1 70  0 1E+6
RPS2 71  0 1E+6
CPS1 99 70 1E-5
CPS2 50 71 1E-5
EPSY 98 72 POLY(2) (70,0) (0,71) 0 1 1
RPS3 72 73 15.9E+6
CPS3 72 73 10E-9
RPS4 73 98 16
*
* VOLTAGE NOISE REFERENCE OF 51nV/rt(Hz)
*
VN1 80 98 0
RN1 80 98 16.45E-3
HN  81 98 VN1 51
RN2 81 98 1
*
* INTERNAL VOLTAGE REFERENCE
*
EREF 98  0 POLY(2) (99,0) (50,0) 0 .5 .5
GSY  99 50 (99,50) 48E-6
EVP  97 98 (99,50) 0.5
EVN  51 98 (50,99) 0.5
*
* LHP ZERO AT 7MHz, POLE AT 50MHz
*
E1 32 98 POLY(2) (4,6) (11,12) 0 .5814 .5814
R2 32 33 3.7E+3
R3 33 98 22.74E+3
C3 32 33 1E-12
*
* GAIN STAGE
*
G1 98 30 (33,98) 22.7E-6
R1 30 98 259.1E+6
CF 45 30 45.4E-12
D3 30 97 DX
D4 51 30 DX
*
* OUTPUT STAGE
*
M5  45 46 99 99 POX L=1E-6 W=1.111E-3
M6  45 47 50 50 NOX L=1E-6 W=1.6E-3
EG1 99 46 POLY(1) (98,30) 1.1936 1
EG2 47 50 POLY(1) (30,98) 1.2324 1
*
* MODELS
*
.MODEL POX PMOS (LEVEL=2,KP=10E-6,
+ VTO=-1,LAMBDA=0.001,RD=8)
.MODEL NOX NMOS (LEVEL=2,KP=10E-6,
+ VTO=1,LAMBDA=0.001,RD=5)
.MODEL PIX PMOS (LEVEL=2,KP=100E-6,
+ VTO=-1,LAMBDA=0.01)
.MODEL NIX NMOS (LEVEL=2,KP=100E-6,
+ VTO=1,LAMBDA=0.01)
.MODEL DX D(IS=1E-14,RS=5)
.ENDS AD8572
```

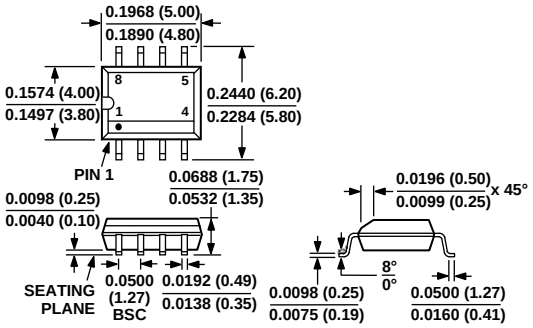
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

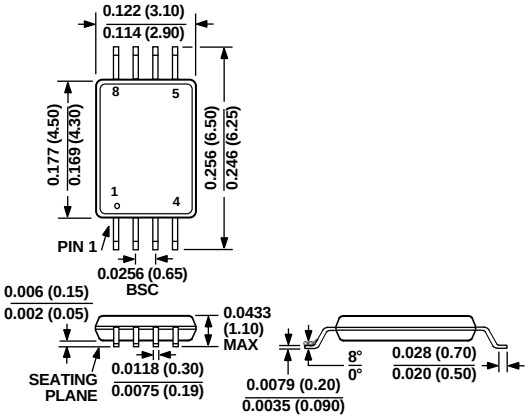
8-Lead MSOP
(RM Suffix)



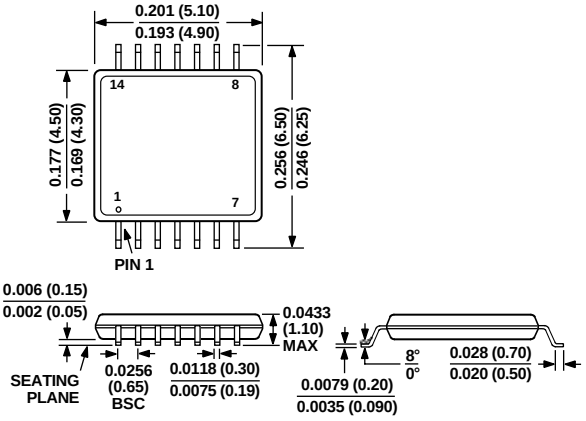
8-Lead SOIC
(R Suffix)



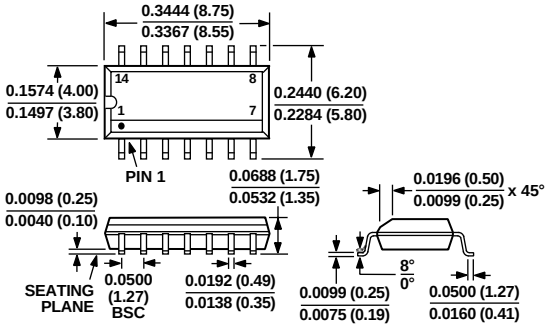
8-Lead TSSOP
(RU Suffix)



14-Lead TSSOP
(RU Suffix)



14-Lead SOIC
(R Suffix)



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