12-Bit, 20 MSPS A/D Converter

AD9034

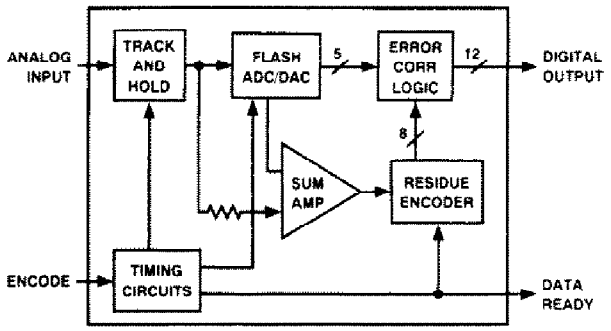
FEATURES

20 MSPS Conversion Speeds
On-Board T/H, References, Timing
Low Power: 4.5 W
Single 40-Pin Package
76 dB Spurious-Free Dynamic Range to 10 MHz A_{IN}
Bipolar Input: ±1.024 V

APPLICATIONS

Radar
Signal Intelligence
Digital Spectrum Analyzers
Medical Imaging
Electro-Optics

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9034 is a complete high speed 12-bit analog-to-digital converter (ADC) which includes on-board T/H, voltage references, and timing circuits. The AD9034 uses a subranging converter architecture to achieve sample rates from dc to 20 MSPS. Packaged in a single 40-pin hybrid, the AD9034 is pin-compatible with the AD9032, which operates at word rates up to 25 MSPS.

This ECL-compatible ADC requires only +5 V and −5.2 V supplies, an analog input, and a stable ECL clock to obtain the best dynamic performance available in a 12-bit ADC. This kind of performance is achieved with advanced bipolar circuits, custom designed and manufactured by Analog Devices. The latest in monolithic track-and-hold technology insures accurate sampling of high frequency analog inputs.

Dynamic performance has been optimized to achieve SNR of 66 dB and a spurious-free dynamic range (SFDR) of 76 dB for analog bandwidths up to 10 MHz. All dynamic performance is guaranteed for sample rates from dc to 20.48 MSPS.

The AD9034 is available in either a 40-pin ceramic DIP or leaded flatpack. The two versions operate over an industrial (−25°C to +85°C) or military (−55°C to +125°C) temperature range.

REV. 0

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AD9034—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = −5.2 V; Encode = 20.48 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9034AD/AZ Min	AD9034AD/AZ Typ	AD9034AD/AZ Max	AD9034BD/BZ Min	AD9034BD/BZ Typ	AD9034BD/BZ Max	AD9034TD/TZ Min	AD9034TD/TZ Typ	AD9034TD/TZ Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		0.65	1.25		0.5	1.0		0.5	1.0	LSB
	Full	VI			1.5			1.25			1.25	LSB
Integral Nonlinearity	+25°C	V		1.0			1.0			1.0		LSB
	Full	V		2.0			2.0			2.0		LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Offset Error	+25°C	I		5	15		5	15		5	15	mV
	Full	VI			25			25			30	mV
Gain Error	+25°C	I		±0.5	±1.0		±0.5	±1.0		±0.5	±1.0	% FS
	Full	VI			±2.5			±2.5			±2.5	% FS
ANALOG INPUT												
Input Voltage Range	+25°C	V		±1.024			±1.024			±1.024		V
Input Bias Current[1]	+25°C	I			100			100			100	μA
	Full	VI			200			200			200	μA
Input Resistance	+25°C	VI	50	350		50	350		50	350		kΩ
Input Capacitance	+25°C	IV		7	10		7	10		7	10	pF
Analog Bandwidth	+25°C	IV	110	150		110	150		110	150		MHz
SWITCHING PERFORMANCE[2]												
Conversion Rate	Full	VI	dc		20.48	dc		20.48	dc		20.48	MSPS
Aperture Delay (t_A)	Full	IV	1	3	5	1	3	5	1	4	7	ns
Aperture Uncertainty (Jitter)	Full	IV		5	10		5	10		5	10	ps, rms
Output Delay (t_{OD})	Full	IV	7	10	13	7	10	13	7	10	13	ns
Data Ready Delay (t_{DR})	Full	IV	3.5	7.5	10.5	3.5	7.5	10.5	3.5	7.5	10.5	ns
Output Time Skew	Full	IV		1	2		1	2		1	2	ns
ENCODE INPUT												
Logic "1" Voltage	Full	IV	−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	IV			−1.5			−1.5			−1.5	V
Logic "1" Current	Full	VI		150	300		150	300		150	300	μA
Logic "0" Current	Full	VI		150	300		150	300		150	300	μA
Input Capacitance	+25°C	V		10			10			10		pF
Pulse Width (High)	+25°C	IV	13			13			13			ns
Pulse Width (Low)	+25°C	IV	13			13			13			ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	IV		15	30		15	30		15	30	ns
Overvoltage Recovery Time	+25°C	IV		25	40		25	40		25	40	ns
Harmonic Distortion												
Analog Input												
@ 1.2 MHz	+25°C	I	70	80		74	80		74	80		dBc
@ 1.2 MHz	Full	VI	68			70			70			dBc
@ 4.3 MHz	+25°C	V		75			77			77		dBc
@ 9.6 MHz	+25°C	I	67	74		70	76		70	76		dBc
@ 9.6 MHz	Full	VI	64			67			67			dBc
Signal-to-Noise Ratio[3]												
Analog Input												
@ 1.2 MHz	+25°C	I	65	67		65	67		65	67		dB
@ 1.2 MHz	Full	VI	64			64			64			dB
@ 4.3 MHz	+25°C	V		66			66			66		dB
@ 9.6 MHz	+25°C	I	63	66		63	66		63	66		dB
@ 9.6 MHz	Full	VI	62			62			62			dB
Two-Tone Intermodulation Distortion Rejection[4]	+25°C	V		68			70			70		dBc

Parameter (Conditions)	Temp	Test Level	AD9034AD/AZ Min	Typ	Max	AD9034BD/BZ Min	Typ	Max	AD9034TD/TZ Min	Typ	Max	Units
DIGITAL OUTPUTS[2]												
Logic "1" Voltage	Full	VI	−1.1			−1.1			−1.1			V
Logic "0" Voltage	Full	VI			1.5			−1.5			1.5	V
Output Coding				2s Complement			2s Complement			2s Complement		
POWER SUPPLY												
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
$+V_S$ Supply Current	Full	VI		200	230		200	230		200	230	mA
$-V_S$ Supply Voltage	Full	VI	−5.45	−5.2	−4.95	−5.45	−5.2	−4.95	−5.45	−5.2	−4.95	V
$-V_S$ Supply Current	Full	VI		680	760		680	760		680	760	mA
Power Dissipation	Full	VI		4.5	5.1		4.5	5.1		4.5	5.1	W
Power Supply Rejection Ratio (PSRR)[5]	Full	VI		2.5	8.0		2.5	8.0		2.5	8.0	mV/V

NOTES
[1]Measured with analog input = 0 V.
[2]Outputs terminated through 510 Ω to −5.2 V; C_L < 4 pF. Typical values are valid for +25°C ambient.
[3]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.
[4]Intermodulation measured with analog input frequencies of 9.3 MHz and 9.6 MHz at 7 dB below full scale.
[5]PSRR is sensitivity of offset error to power supply variations within the 5% limits shown.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ . . . . . +6 V
$-V_S$ . . . . . −6 V
Analog Inputs . . . . . $-V_S$ to $+V_S$
Digital Inputs . . . . . $-V_S$ to 0 V
Digital Output Current . . . . . 20 mA
Gain Adjust . . . . . $-V_S$ to $+V_S$
Offset Adjust . . . . . $-V_S$ to $+V_S$
Operating Temperature Range
AD9034AD/BD/AZ/BZ . . . . . −25°C to +85°C
AD9034TD/TZ . . . . . −55°C to +125°C
Maximum Junction Temperature[2] . . . . . +175°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Storage Temperature Range . . . . . −65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: θ_{CA} = 13°C/W; T_J−T_C = 10°C max (worst case die junction temperature rise). See Thermal Management section.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

ORDERING GUIDE

Model	Temperature Range	Package Description
AD9034AD	−25°C to +85°C	40-Pin Ceramic DIP, Industrial Temperature
AD9034AZ*	−25°C to +85°C	40-Pin Leaded Flatpack, Industrial Temperature
AD9034BD	−25°C to +85°C	40-Pin Ceramic DIP, Industrial Temperature
AD9034BZ*	−25°C to +85°C	40-Pin Leaded Flatpack, Industrial Temperature
AD9034TD	−55°C to +125°C	40-Pin Ceramic DIP, Military Temperature
AD9034TZ*	−55°C to +125°C	40-Pin Leaded Flatpack, Military Temperature
AD9034/PWB	Printed Circuit Board (Only) of Evaluation Circuit	
AD9034/PCB	Complete Evaluation Board, Assembled and Tested (Order AD9034 DIP Separately)	

*Surface mount leaded packages are tested and shipped with unformed leads. Consult the factory for availability.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay (t_A)
The delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Data Ready Delay (t_{DR})
The delay between the 50% point of the change in output data and the 50% point of the rising edge of DATA READY.

Differential Nonlinearity (DNL)
The deviation of any code width from an ideal 1 LSB step.

Harmonic Distortion
The rms value of the fundamental divided by the rms value of the worst harmonic.

Integral Nonlinearity (INL)
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Output Delay (t_{OD})
The delay between the 50% point of the rising edge of the ENCODE command and the 50% point of the next change in output data.

Output Time Skew
Bit-to-bit time variations among D_0 to D_{11} outputs. Time skew includes HIGH-to-LOW and LOW-to-HIGH transitions of the digital output bits.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 12-bit accuracy after an analog input signal 150% of full scale is reduced to the midscale of the converter.

Power Supply Rejection Ratio
The ratio of a change in power supply voltage which results in a change in input offset voltage.

Pulse Width (High and Low)
Rated performance of the ADC is assured when stated restrictions on ENCODE pulse width shown in Specifications table are observed.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

Spurious Free Dynamic Range (SFDR)
The rms value of the fundamental divided by the rms value of the highest spurious signal. This is generally specified as a function of input signal level.

Transient Response
The time required for the converter to achieve 12-bit accuracy when a full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of two input signals to the power of the strongest third-order IMD signal.

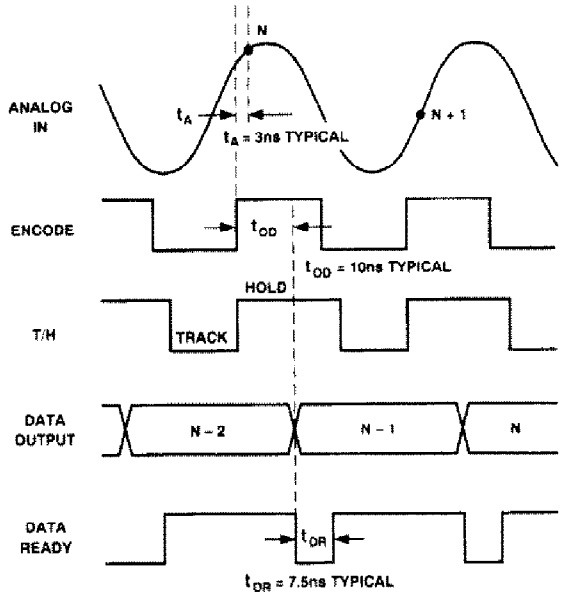
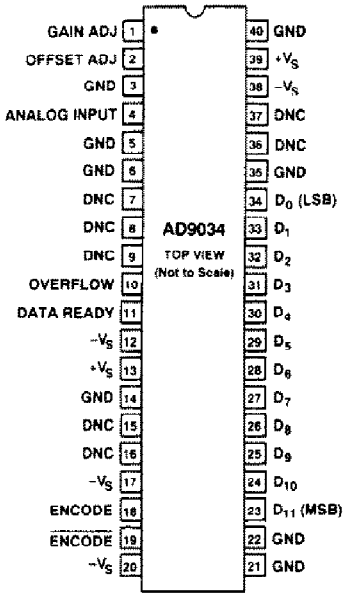


Figure 1. Timing Diagram

PIN CONFIGURATION



PIN DESCRIPTIONS

Pin	Name	Description
1	GAIN ADJUST	Can be used to null out initial gain error of ADC. Normally open.
2	OFFSET ADJUST	Can be used to null out initial offset error of ADC. Normally open.
3, 5, 6, 14, 21 22, 35, 40	GROUND	All ground pins should be connected together and to low impedance ground plane near AD9034.
4	ANALOG INPUT	Analog input to ADC. ±1.024 V input range; 350 kΩ input resistance; 7 pF input capacitance.
7, 8, 9, 15, 16, 36, 37	DNC	Do not connect. Internal test points.
10	OVERFLOW	ECL-compatible output; normally low. High when analog input > +FS.
11	DATA READY	ECL-compatible output. Rising edge of signal suitable for externally latching D_0–D_{11}.
12, 17, 20, 38	$-V_S$	−5.2 V supply voltage.
13, 39	$+V_S$	+5.0 V supply voltage.
18	ENCODE	Differential ECL convert command.
19	$\overline{\text{ENCODE}}$	Sampling occurs on rising edge; no internal terminations.
23–34	D_0–D_{11}	ECL-compatible digital outputs; 2s complement coding.

Analog Input	D_{11}	D_{10}–D_0
≥ +1.024 V	0	1
≤ −1.024 V	1	0

THEORY OF OPERATION

The AD9034 is a digitally corrected subranging analog-to-digital converter (ADC) optimized for fast sampling rates and dynamic range. As shown in the block diagram on the first page, the AD9034 is a vertically integrated structure consisting of a track-and-hold (T/H) amplifier, a combined flash ADC and digital-to-analog (DAC), a summation amplifier, digital error correction logic, and timing circuits. Reference circuits to generate stable dc voltages and currents which maintain the static accuracy of the device are also included, but are not shown on the block diagram.

Internally, the monolithic T/H (AD9100) provides fast settling and acquisition times while minimizing distortion introduced by the sampling process. The unique design of the sampling bridge allows accurate sampling of high slew rate signals with negligible distortion. The effects of jitter and other aperture errors have been reduced to provide dynamic performance previously unavailable in monolithic and discrete designs.

At the output of the T/H amplifier, the analog input is converted by the first (5-bit) ADC. This 5-bit representation of the input value is stored in the digital error correction logic and also converted back to an analog signal by the 14-bit- accurate DAC on the same chip with the ADC. The 32 DAC current sources are steered directly by the outputs of the 32 input comparators on the 5-bit ADC. This minimizes propagation delay through the DAC, and allows the summation of the DAC signal and the held output of the T/H to settle as early as possible. The hold time of the T/H is optimized to allow sufficient settling time without sacrificing the acquisition time necessary to acquire the next sample.

The residue signal, representing the difference between the 5-bit conversion (DAC output) and the input signal held by the T/H, is amplified by the summation amplifier. During the tracking period of the T/H, this residue signal can be much larger than the input range of the 8-bit ADC and would saturate the output stage of a normal amplifier. To protect the ADC and maintain fast settling times under all conditions, the summation amplifier is a custom design with clamping circuits which prevent saturation, limit the output voltage, and preserve settling time.

The 8-bit flash ADC determines the 7 least significant bits (LSBs) of the 12-bit conversion and generates a correction bit for any small errors created by inaccuracies in the first 5-bit conversion. This 8-bit signal is combined with the 5-bit quantization to obtain a 12-bit-accurate representation of the analog input voltage.

USING THE AD9034

Layout Information

Preserving the accuracy and dynamic performance of the AD9034 requires that designers pay special attention to the layout of the printed circuit board. Signal paths should be impedance matched and properly terminated at or near the package connections. Analog signal paths should be isolated from digital signal paths. Capacitive and inductive coupling of digital signals into analog signal sections can degrade the overall performance of the A/D converter.

Analog Input

The analog input pin of the AD9034 connects directly to the monolithic track-and-hold amplifier. The high input impedance (350 kΩ, 7 pF) eliminates the need for external signal conditioning in many applications. The analog input range of the AD9034 is factory trimmed for a ±10.024 V input. When the amplitude

bandwidth, or dc level of the analog input requires external signal conditioning, the selection of the input amplifier is of particular concern. The noise and distortion of the amplifier must be taken into account to preserve the dynamic range of the AD9034. The AD9617 wideband, current feedback amplifier is an excellent choice for most applications.

Timing

Internal timing for the AD9034 has been trimmed at the factory to simplify use. Care should be taken to insure that the encode command to the AD9034 is free from jitter which can degrade dynamic performance. Differential ECL inputs to the AD9034 can be derived from a single-ended source using a fast comparator such as the AD96685. The encode source should be located and terminated as close to the AD9034 as possible.

The ECL-compatible digital outputs are latched to provide valid data for the entire conversion period (less the transition region of latch). This data should be latched into external ECL registers located as near as possible to the AD9034. External termination resistors are required (512 Ω recommended). The data can be latched by using either the encode command or the data ready signal provided on the AD9034. The rising edge of the data ready signal occurs typically 7.5 ns after the data changes.

Gain and Offset Adjustment

Gain and offset pins are normally not connected. Rated performance is guaranteed without any external connection to these pins. In most applications, wide variations in input signal range and offset can be accommodated using external amplifiers. However, in those applications where a vernier adjustment is required (such as nulling out factory trim limits), the gain and offset pins will provide sufficient adjustment range.

Both inputs offer a 20 kΩ input resistance which can be driven from a voltage source (DAC, amplifier) or the center tap of a potentiometer. The offset pin provides a −12 mV/V sensitivity to input offset while the gain pin offers −120 mV/V adjustment of the full-scale input range of the ADC. The adjustment range for offset is limited to 12 millivolts and for gain is 20 mV without introducing potential dynamic errors or restricting the operating temperature range of the part.

Power Supplies

The unique design of the AD9034 provides excellent dynamic performance without a need for high voltage power supplies. Two supplies (+5 V and −5.2 V) are all that are required to achieve rated performance. Careful layout and decoupling of power supplies used in conjunction with a low impedance analog ground plane will reduce supply-related noise components.

Separate analog and digital supplies are not required nor recommended. In applications where only limited analog supply current is available, a separate digital supply source can be used for the −5.2 V supply on Pin 20. This supply typically requires 310 mA (330 mA max) and may be shared with other ECL logic devices when isolated with bypass capacitors and/or ferrite bead inductors. A separate digital ground is not available.

Each power supply pin should be capacitively decoupled to the ground plane through a good high frequency ceramic capacitor (0.1 μF) and a single large value capacitor (tantalum 10 μF). Isolation of switching noise generated by the AD9034 and suppression of noise from other devices is improved by placing ferrite bead inductors (Fair-Rite Products Corporation Part #2743001111, Wallkill, NY) between the supply source and the part.

For optimum performance, "clean" linear supplies are recommended to insure that switching noise on the supplies does not introduce distortion products during the encoding process. Recognizing, however, that switching power supplies may be required in power-sensitive applications, decoupling recommendations outlined above are critically important for using switching supplies effectively. Elsewhere in this data sheet, a graph shows the PSRR of the AD9034 as a function of the ripple frequency present on the AD9034 supplies. Clearly, if they must be used, switching power supplies with the lowest possible frequency should be selected.

Thermal Management

The AD9034 has been designed to minimize power dissipation; however, the ADC does typically require 4.5 watts (5.1 W max) to operate. To insure long life and reliable operation, the maximum junction temperature in the AD9034 must be limited to +175°C.

Within the hybrid, the hottest discrete die has a case to junction temperature rise of 10°C (max). Therefore, the case temperature of the AD9034 should not exceed +165°C under worst case operating conditions. Without airflow, the θ_{CA} of the hybrid package is 13°C/W. Assuming maximum power dissipation, this causes a 66°C rise in case temperature over the ambient air temperature. The maximum still air temperature, therefore, is equal to +99°C.

Rated performance of the AD9034 is guaranteed for case operating temperatures of +85°C (AD9034A/B) and +125°C (AD9034T). This equates to a maximum operating ambient temperature of +19°C and +59°C, respectively, in still air. In most applications, airflow is recommended. The following improvements in the thermal characteristics of the system assume that the AD9034 is soldered to a PC board.

The θ_{CA} of the hybrid is reduced to 5°C/W with 500 LFPM airflow. This will extend the rated performance to ambient operating ranges of +59°C for the AD9034A/B and +99°C for the AD9034T. The addition of a heat sink (Thermalloy #6087B, Dallas, Texas; phone 214-243-0839) will further improve the thermal transfer of the hybrid to 3°C/W @ 500 LFPM. Using a heat sink with airflow, the total case to ambient temperature rise is only 16°C, which results in a maximum ambient environment of +69°C (AD9034A/B) and +109°C (AD9034T).

DIGITAL RECEIVER APPLICATIONS

Applications as diverse as ultrasound, radar, communications, and signal intelligence can take advantage of the sampling bandwidth of the AD9034. Classic receivers utilizing in-phase and quadrature (I & Q) detection methods are being replaced increasingly with digital demodulation techniques.

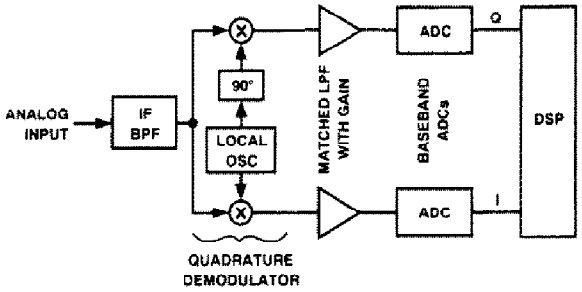


Figure 2. Classic Analog Receiver

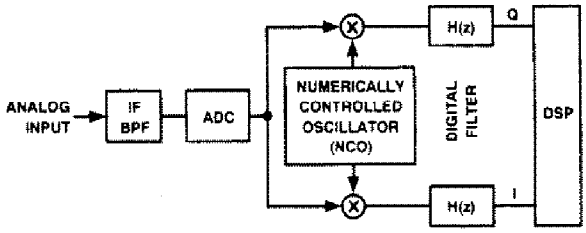


Figure 3. Digital Receiver

Classic receiver architecture depends on gain and phase matching of the mixers, amplifiers, and filters used in the quadrature demodulator. Maintaining this matching, and the 90-degree phase shift, over time and temperature extremes can be extremely difficult. But the problems caused by these difficulties can be solved by using digital receiver techniques. The inherent stability and repeatability of a digital demodulator and filters offer cost and performance advantages in a variety of applications.

In a digital receiver, the burden of performance is passed on to the ADC; its dynamic performance at the bandpass IF frequency establishes the performance limits of the system. The user must be careful to evaluate the linearity (harmonic distortion) and noise (SNR) of the converter at the highest frequency of interest. The AD9034 is designed to provide the widest possible dynamic range for analog input frequencies extending well beyond the Nyquist bandwidth of the converter. Graphs shown elsewhere in this data sheet illustrate the AD9034's SNR and harmonic distortion versus analog input frequency.

The sample rate in a digital receiver is determined by the analog *bandwidth* of the input signal, not the analog *frequency*. The theoretical minimum sample rate for a sampled analog signal is shown in the following graph.

Actual sample rates are higher than those which are shown to simplify analog and digital filter requirements, and may be increased further to improve SNR by using digital filtering and decimation techniques. Jitter is also an important concern as analog input frequency increases; the effects of jitter become more pronounced as the slew rate (i.e., analog frequency) of the input signal increases.

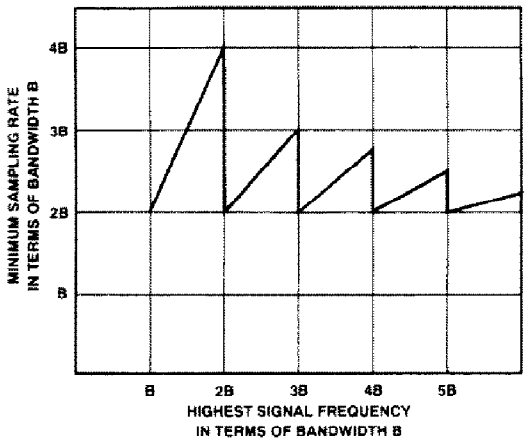
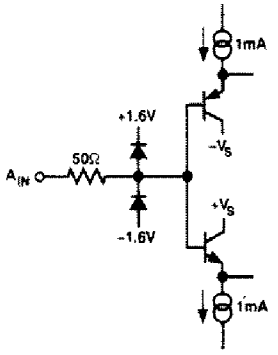
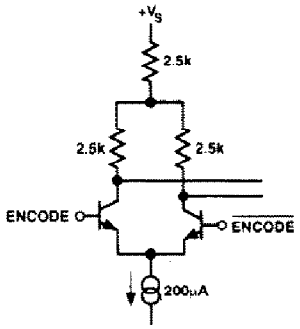


Figure 4. Theoretical Minimum Sampling vs. Sampled Analog Frequency

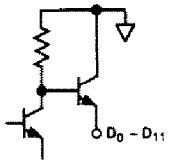
Judicious choices of sample rates and IF frequencies can be combined with careful attention to the encode source to produce a digital receiver with superior performance. Higher speeds and lower prices for digital signal processing (DSP) hardware, coupled with the wide bandwidth of sampling ADCs like the AD9034 can lower the cost and improve the reliability of systems.



a. Equivalent Analog Input Circuit



b. Equivalent Encode Input Circuit



c. Equivalent Digital Output Circuit

Figure 5. Equivalent Circuits

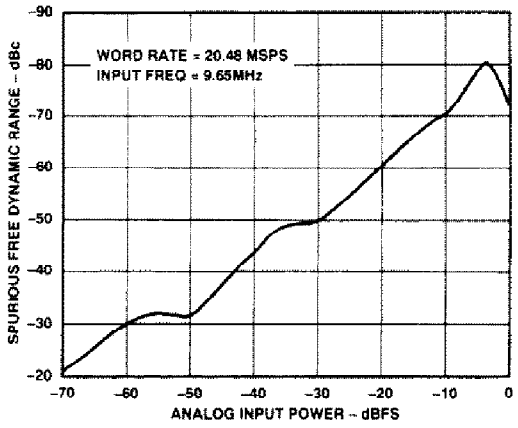


Figure 6. SFDR vs. A_{IN} Power

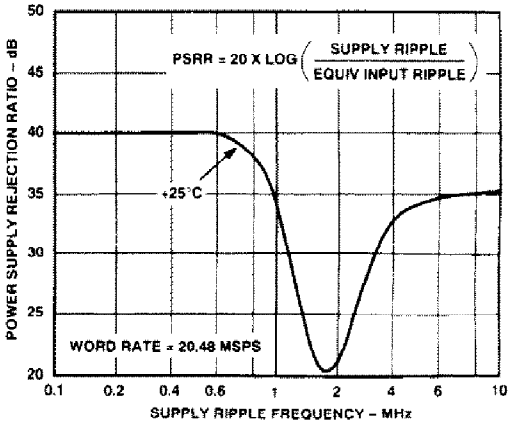


Figure 7. PSRR vs. Supply Ripple Frequency

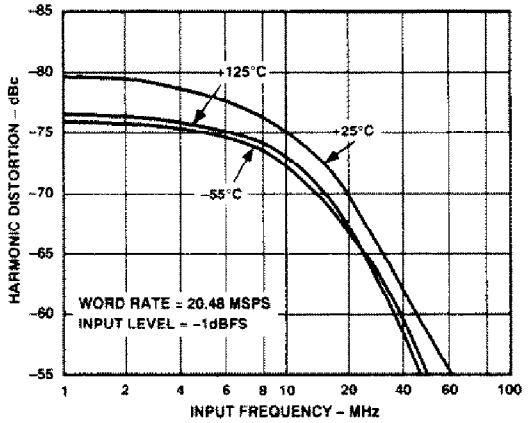


Figure 8. Harmonic Distortion vs. Analog Input

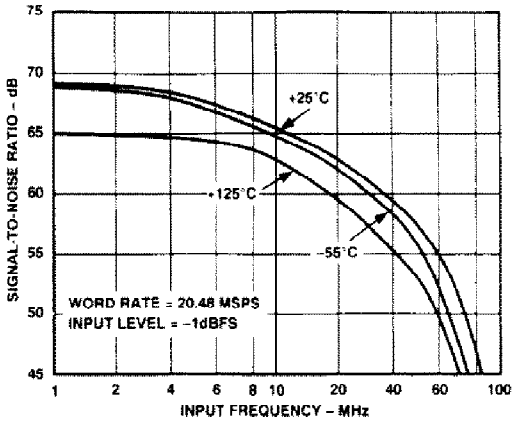


Figure 9. SNR vs. Analog Input

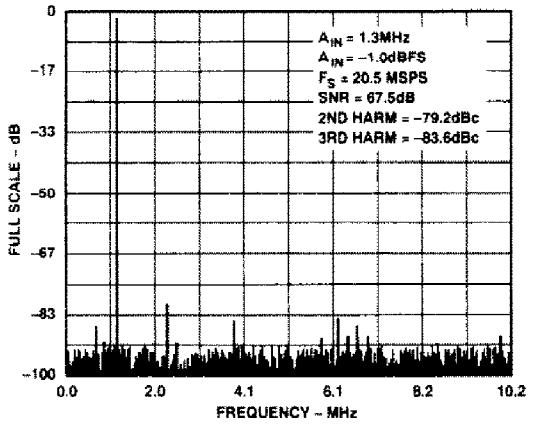


Figure 10a.

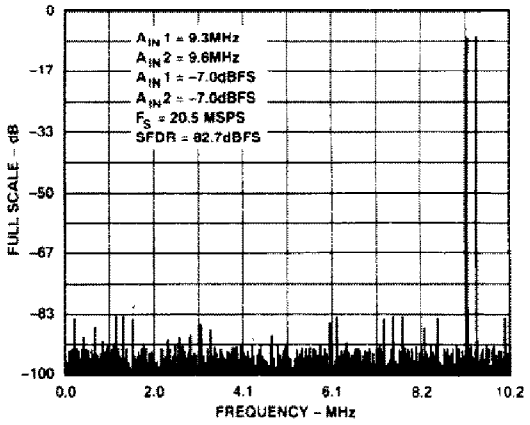


Figure 10b.

Figure 10. Spectral Performance
Five-Sample Average of 2,048-Point FFTs; All Harmonics Are Aliased.

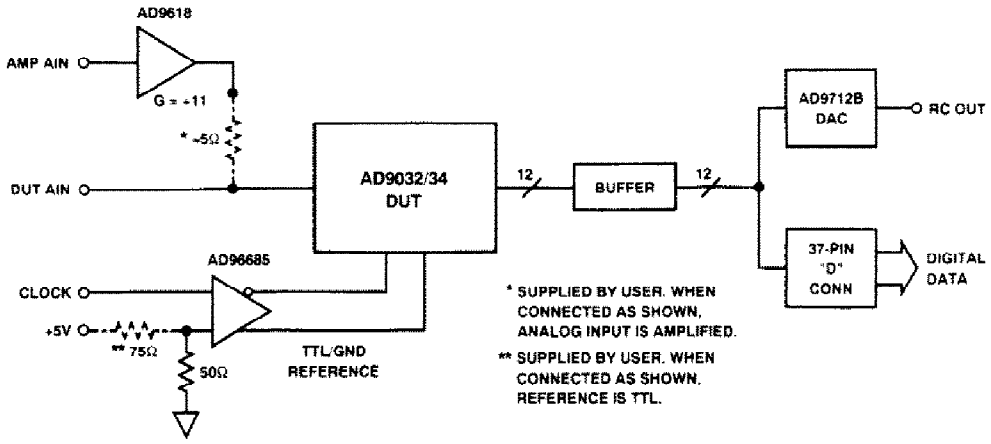


Figure 11. AD9034/PCB Functional Block Diagram

AD9034 EVALUATION BOARD

The evaluation board for the AD9034 (AD9034/PCB) provides an easy and flexible method for evaluating the ADC's performance without (or prior to) developing a user-specific printed circuit board. The board includes a reconstruction DAC, analog input amplifier, and digital output interface. The 7.25 × 6 inch two-sided board uses the layout and applications suggestions outlined above.

Generous space is provided near the analog input and digital outputs to support additional signal processing components the user may wish to add. These two prototyping areas include through holes with 100 mil centers to support a variety of component additions.

Input/Output/Supply Information

Power supply, analog input, clock connections, and reconstructed output (RC OUT) are identified by labels on the evaluation board. Operation of the evaluation board should conform to the following characteristics:

Parameter	Typical	Units
Supply Current		
+5 V	350	mA
−5 V	1500	mA
AMP AIN		
Impedance	50	Ω
Voltage Range	±0.1	V
DUT AIN		
Impedance	100	Ω
Voltage Range	±1.024	V
CLOCK		
Impedance	50	Ω
Frequency	20	MSPS
RC OUT		
Impedance	0.1	Ω
Voltage Range	±1.024	V

Analog Input

Analog input signals can be fed directly into the Device Under Test (DUT AIN) input or amplified using the AD9618 amplifier provided on-board the AD9034/PCB board. The DUT input is terminated at the device with a 100 Ω resistor.

To use the on-board amplifier, a small value resistor (R4) should be inserted in the space provided on the board. This resistor (approximately 5 Ω) provides isolation between the amplifier and the AD9034. The amplifier is set for a noninverting gain of 11 with a 51 Ω termination on the noninverting input of the amplifier.

DAC Reconstruction

The AD9034 evaluation board provides an on-board reconstruction DAC (AD9712B) for observing the digitized analog input signal. The current output DAC is applied to a current-to-voltage converter (AD9617 amplifier) to provide a 2 V p–p signal at the output (RC OUT).

Output Data

The output data bits are terminated to −5.2 V through 510 Ω resistors and recovered by ECL line receivers. The line receivers drive a 12-bit DAC and a 37-pin edge connector. The differential data and the data ready signal are available on the edge connector per the pin assignments shown on the schematic. The output data, latched in the AD9034, is valid on the rising edge of the data ready signal.

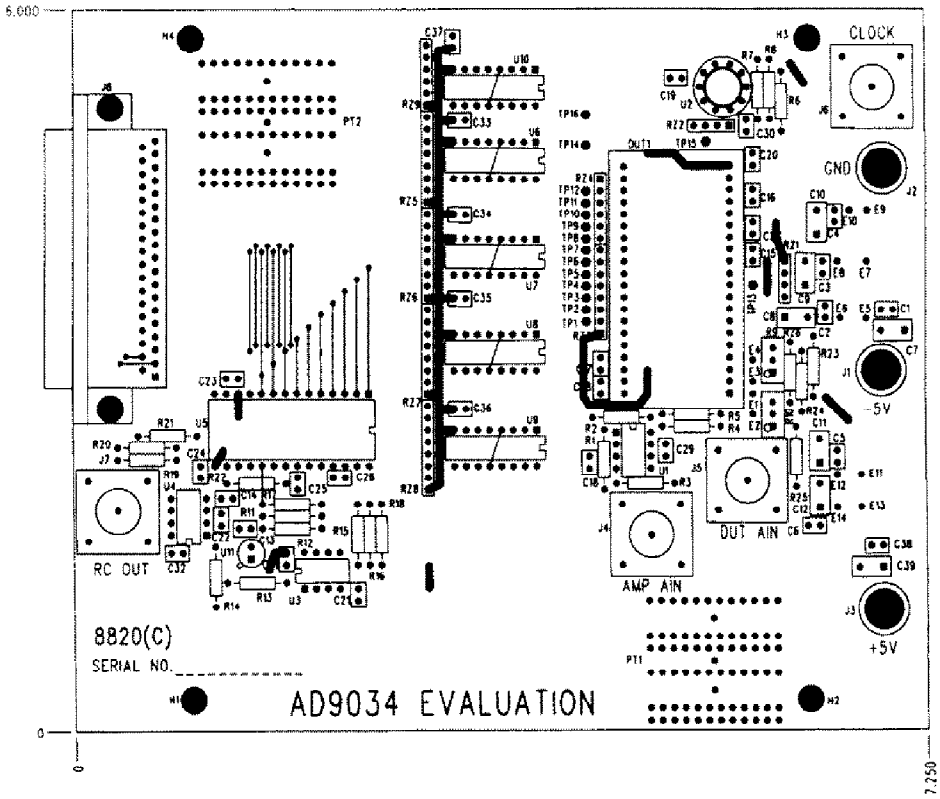


Figure 12. Top of Board

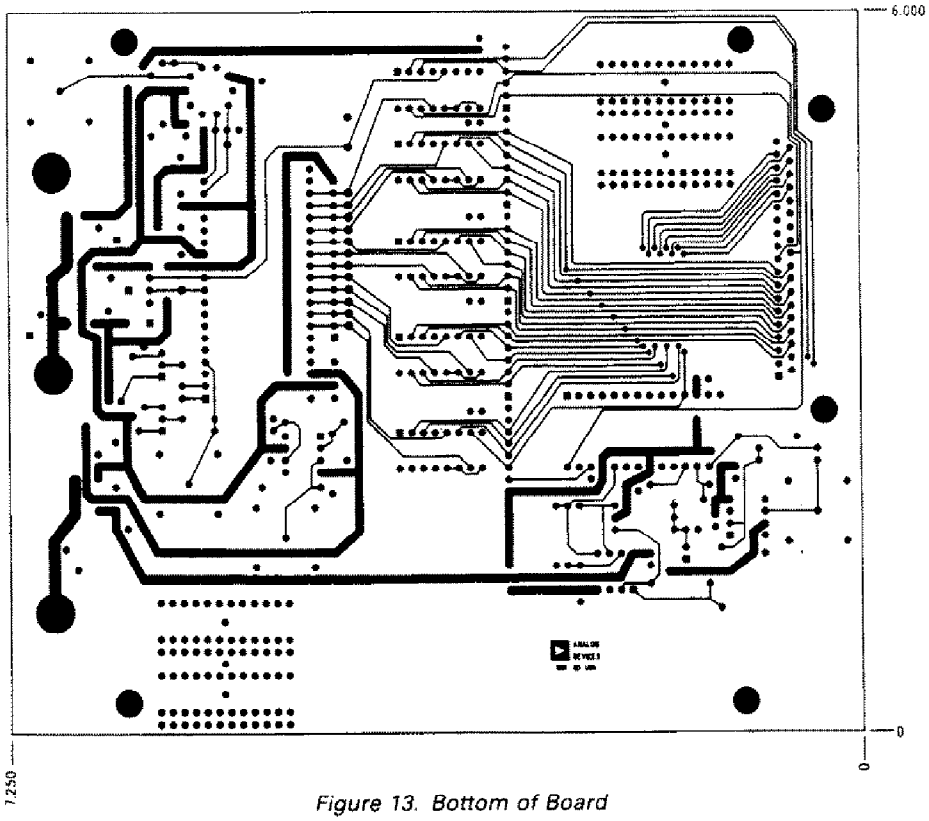
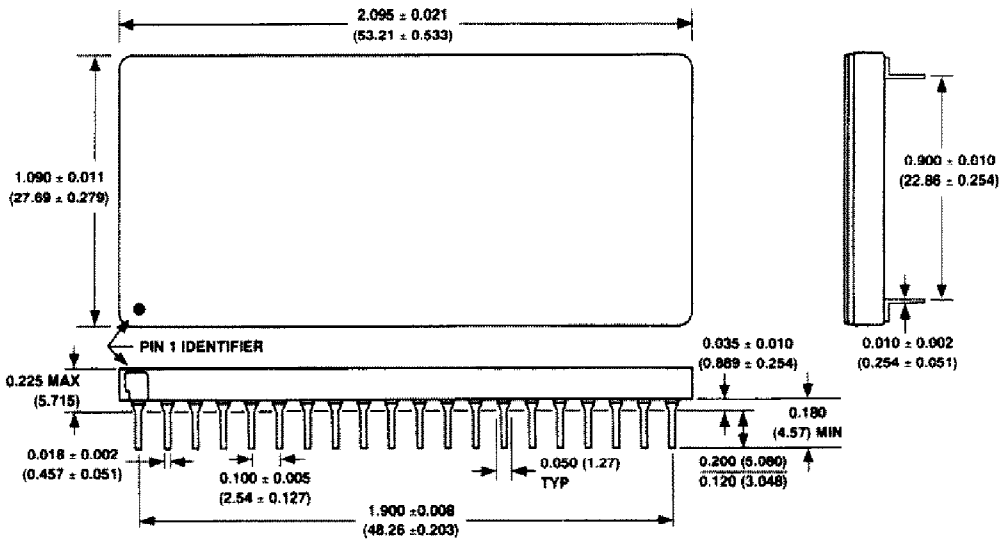


Figure 13. Bottom of Board

MECHANICAL INFORMATION

Dimensions shown in inches and (mm).

40-Lead Bottom Brazed Ceramic DIP



40-Pin Leaded Flatpack