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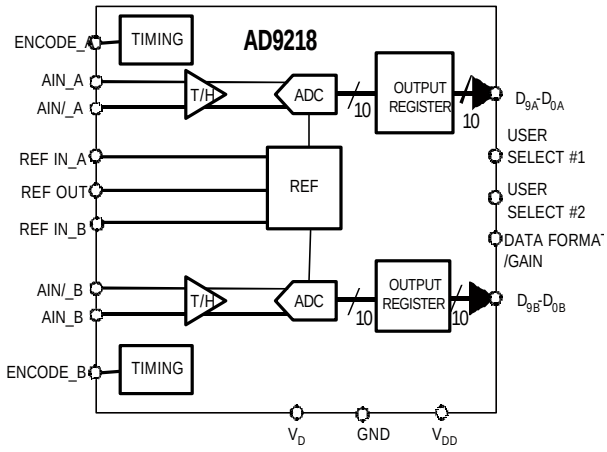
10–Bit, 40/65/80/105 MSPS Dual A/D Converter

Preliminary Technical Data AD9218

FEATURES
Dual 10–Bit, 40,65, 80, and 105 Msps ADC
Low Power: 260 mW at 105 Msps per channel
On–Chip Reference and Track/Holds
300 MHz Analog Bandwidth each channel
SNR = 54 dB @ 49MHz (105Msps)
1Vp–p or 2Vp-p Analog Input Range each channel
Single +3.0V Supply Operation (2.7V – 3.6V)
Power Down Mode for single channel operation
Two's complement or Offset Binary Output Mode
Output Data Alignment Mode
Pin Compatible with 8-Bit AD9288

APPLICATIONS
Battery Powered Instruments
Hand-Held Scopemeters
Low Cost Digital Oscilliscopes
I&Q Communications
Ultrasound Equipment

Functional Block Diagram



PRODUCT HIGHLIGHTS

GENERAL DESCRIPTION

The AD9218 is a dual 10-bit monolithic sampling analog–to–digital converter with on–chip track–and–hold circuits and is optimized for low cost, low power, small size and ease of use. The product operates at a 105 Msps conversion rate with outstanding dynamic performance over its full operating range. Each channel can be operated independently.

The ADC requires only a single 3.0V (2.7V to 3.6V) power supply and an encode clock for full–performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3V or 2.5V logic.

The encoder input is TTL/CMOS compatible and the 10-bit digital outputs can be operated from +3.0V (2.5V to 3.6V) supplies. User selectable options are available to offer a combination of power down modes, digital data formats and digital data timing schemes. In power-down mode, the digital outputs are driven to a high-impedence state.

Fabricated on an advanced CMOS process, the AD9218 is available in a 48 pin surface mount plastic package (7x7mm LQFP) specified over the industrial temperature range (–40°C to +85°C).

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AD9218—TARGET SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = 3.0V, V_D = 3.0V; external reference, unless otherwise noted)

Parameter	Temp	Test Level	AD9218BST-40/65 Min	AD9218BST-40/65 Typical	AD9218BST-40/65 Max	AD9218BST-80/105 Min	AD9218BST-80/105 Typical	AD9218BST-80/105 Max	Units
RESOLUTION				10			10		bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		±0.5			±0.5		LSB
	Full	VI							LSB
Integral Nonlinearity	+25°C	I		±0.75			±0.75		LSB
	Full	VI							LSB
No Missing Codes	Full	VI		GNT			GNT		
Gain Error [1]	+25°C	I		±2.5			±2.5		% FS
	Full	VI							% FS
Gain Tempco[1]	Full	VI		80			80		ppm/°C
Gain Matching	+25°C	V		±1.5			±1.5		% FS
Voltage Matching	+25°C	V		±15			±15		mV
ANALOG INPUT									
Input Voltage Range (with respect to AIN)	Full	V		1 or 2			1 or 2		V p–p
Common Mode Voltage	Full	V		V_D/3			V_D/3		V
Input Offset Voltage	+25°C	I		±10			±10		mV
	Full	VI		±40			±40		mV
Reference Voltage	Full	VI		1.25			1.25		V
Reference Tempco	Full	VI							ppm/°C
Input Resistance	+25°C	I		10			10		kΩ
	Full	VI							kΩ
Input Capacitance	+25°C	V		2			2		pF
Analog Bandwidth, Full Power	+25°C	V		300			300		MHz
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	40/65			80/105			Msps
Minimum Conversion Rate	+25°C	IV			10			10	Msps
Encode Pulse Width High(t_{EH})	+25°C	IV		12.5/7.7			6.3/4.7		ns
Encode Pulse Width Low(t_{EL})	+25°C	IV		12.5/7.7			6.3/4.7		ns
Aperature Delay(t_A)	+25°C	V		900			900		ps
Aperature Uncertainty(Jitter)	+25°C	V		5			5		ps rms
Output Valid Time(t_V) [2]	Full	VI		2			2		ns
Output Propagation Delay(t_{PD}) [2]	Full	VI		5			5		ns
Power Up Time	+25°C	IV		75			60		cycles
DIGITAL INPUTS[3]									
Logic "1" Voltage	Full	VI	2.0			2.0			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			±1			±1	µA
Logic "0" Current	Full	VI			±1			±1	µA
Input Capacitance	+25°C	V		4.5			4.5		pF
DIGITAL OUTPUTS[3]									
Logic "1" Voltage	Full	VI	2.45			2.45			V
Logic "0" Voltage	Full	VI			0.05			0.05	V
POWER SUPPLY									
Power Dissipation[4]	Full	VI		338/381			534/573		mW
Power Supply Rejection Ratio (PSRR)[7]	+25°C	I			18			18	mV/V

Parameter	Temp	Test Level	AD9218BST-40/65 Min	AD9218BST-40/65 Typical	AD9218BST-40/65 Max	AD9218BST-80/105 Min	AD9218BST-80/105 Typical	AD9218BST-80/105 Max	Units
DYNAMIC PERFORMANCE[6]									
Transient Response	+25°C	V		tbd			tbd		ns
Overvoltage Recovery Time	+25°C	V		tbd			tbd		ns
Signal-to-Noise Ratio (SNR) (Without Harmonics)									
fin = 10.3 MHz	+25°C	I		59/57			58/55		dB
fin = Nyquist	+25°C	I		59/56			57/54		dB
Singal-to-Noise Ratio (SINAD) (With Harmonics)									
fin = 10.3 MHz	+25°C	I		59/56			58/53		dB
fin = Nyquist	+25°C	I		59/55			57/53		dB
Effective Number of Bits									
fin = 10.3 MHz	+25°C	I		9.5/9			9.3/8.5		bits
fin = Nyquist	+25°C	I		9.5/8.8			9.2/8.5		bits
2nd Harmonic Distortion									
fin = 10.3 MHz	+25°C	I		-89/-77			-77/-68		dBc
fin = Nyquist	+25°C	I		-89/-72			-71/-66		dBc
3rd Harmonic Distortion									
fin = 10.3 MHz	+25°C	I		-79/-68			-71/-63		dBc
fin = Nyquist	+25°C	I		-78/-62			-76/-69		dBc
Two-Tone Intermod Distortion (IMD)									
fin1,2 = 10 and 11 MHz	+25°C	V		-70					dBc
fin1,2 = 40 and 41 MHz	+25°C	V					-65		dBc

NOTES

1. Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.25V external reference).
2. t_V and t_{PD} are measured from the 1.5V level of the ENCODE input to the 10% / 90% levels of the digital outputs swing. The digital output load during test is not to exceed an AC load of 5pF or a DC current of +/-40µA.
3. Digital supply current based on V_{DD} = +3.0V output drive with <5pF loading under dynamic test conditions.
4. Power dissipation is measured under the following conditions: Encode = Fs_{MAX} for grade, analog input is 10.3MHz, –0.7dBfs, both channels in operation.
5. Power-down dissipation calculated with encode clock in operation and with an analog input of 10.3MHz, 10.3MHz sine wave.
6. SNR / harmonics based on an analog input voltage of –0.7 dBfs referenced to a 1.0Vp-p full–scale input range for the 80 and 105 Msps versions and to a 2.0Vp-p for the 40 and 65 Msps version.

ABSOLUTE MAXIMUM RATINGS*

V_D ,V_{DD} ..... +4 V
Analog Inputs ..... -0.5V to V_D + 0.5 V
Digital Inputs ..... -0.5V to V_{DD} + 0.5 V
VREF IN ..... -0.5V to V_D + 0.5 V
Digital Output Current ..... 20 mA
Operating Temperature ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Maximum Junction Temperature ..... +175°C
Maximum Case Temperature ..... +150°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I 100% production tested.

II 100% production tested at +25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9218BST –40, -65, -80, -105	–40°C to +85°C	ST–48
AD9218/PCB	+25°C	Evaluation Board

*ST = Metric Quad Flat Pack (1.4mm thick: LQFP).

PIN DESCRIPTIONS

PIN #	Name	Description
1,12,16,27,29,32,34,45	GND	Ground
2	$A_{IN}A$	Analog input for Channel A
3	$A_{IN}A$/	Analog input for Channel A (complementary)
4	DFS/GAIN	Data Format Select and analog input gain mode: (Low = Offset binary output available , 1Vp-p supported; High = Two's complement output available , 1Vp-p supported; Floating = Offset binary output available, 2Vp-p supported; Set to Vref = Two's complement output available, 2Vp-p supported)
5	$REF_{IN}A$	Reference voltage input for Channel A
6	REF_{OUT}	Internal reference voltage
7	$REF_{IN}B$	Reference voltage input for Channel B
8	S1	User Select #1 (refer to Table 1), Tied with respect to V_D
9	S2	User Select #2 (refer to Table 1), Tied with respect to V_D
10	$A_{IN}B$/	Analog input for Channel B (complementary)
11	$A_{IN}B$	Analog input for Channel B
13,30,31,48	V_D	Analog Supply (3.0V)
14	ENC_B	Clock input for Channel B
15,28,33,46	V_{DD}	Digital Supply (2.5V to 3.6V)
17-26	$D9_B$-$D0_B$	Digital Output for Channel B ($D9_B$ = msb)
35-44	$D0_A$-$D9_A$	Digital Output for Channel A ($D9_A$ = msb)
47	ENC_A	Clock input for Channel A

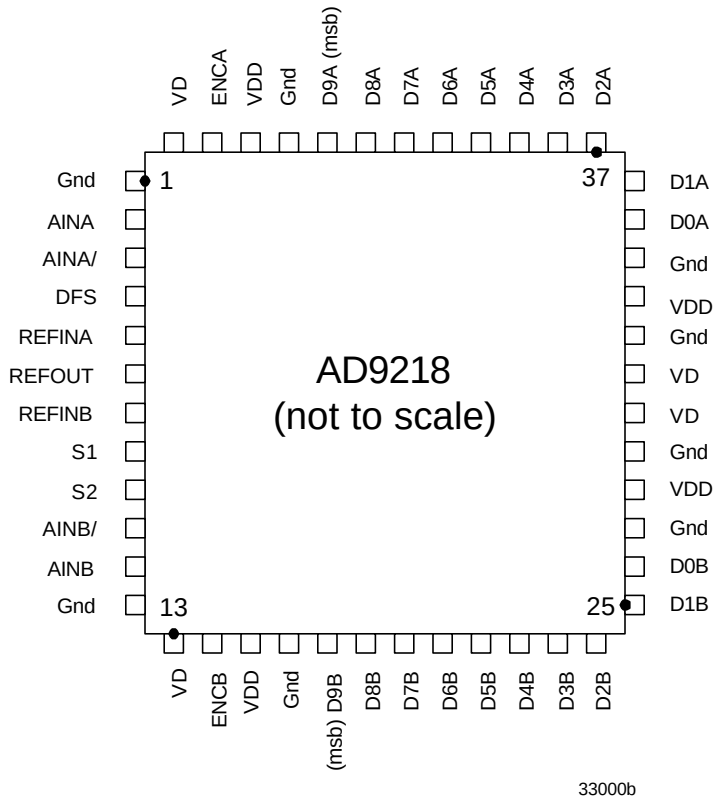

Figure 1. Pin Configuration

S1	S2	User Select Options
0	0	Power down both Channel A and Channel B
0	1	Power down Channel B only
1	0	Normal operation (Data align disabled).
1	1	Data align enabled (data from both channels available on rising edge of clock A. Channel B data is delayed by a ½ clock cycle)

Table 1. User Select Modes

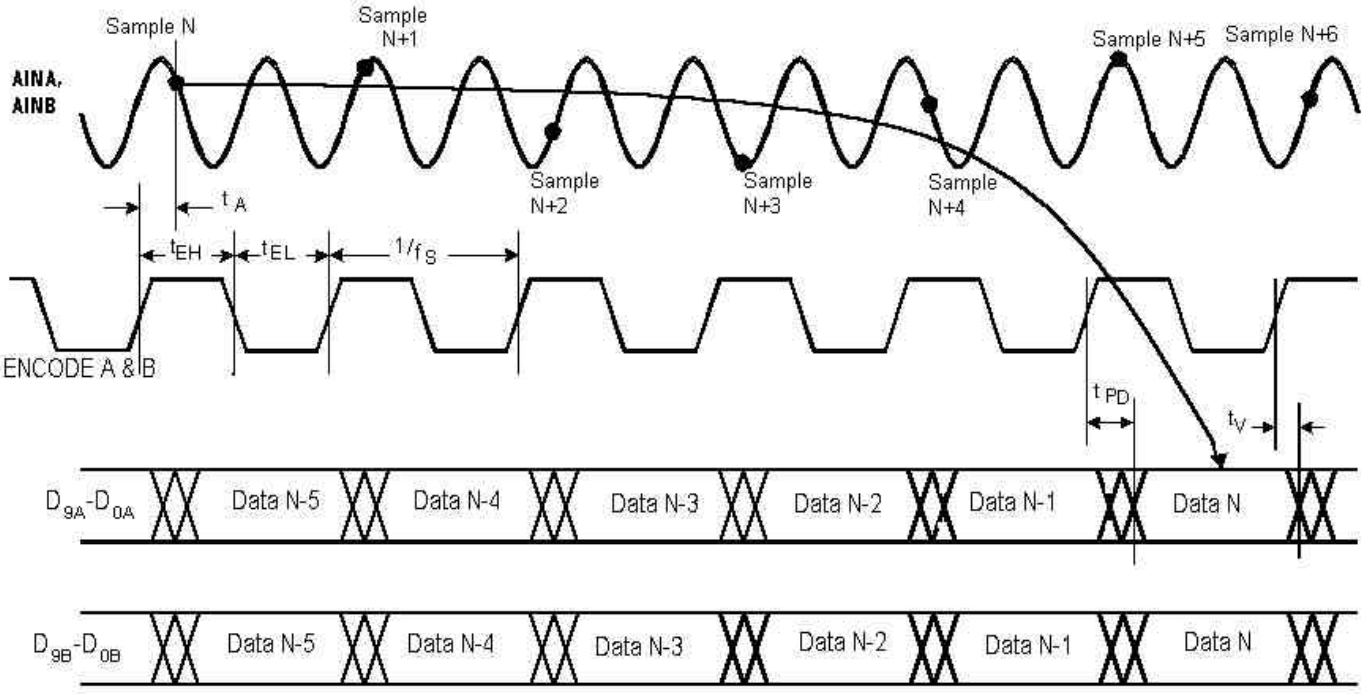

Figure 2. . Normal Operation, Same Clock (S1 =1, S2 = 0) Channel Timing

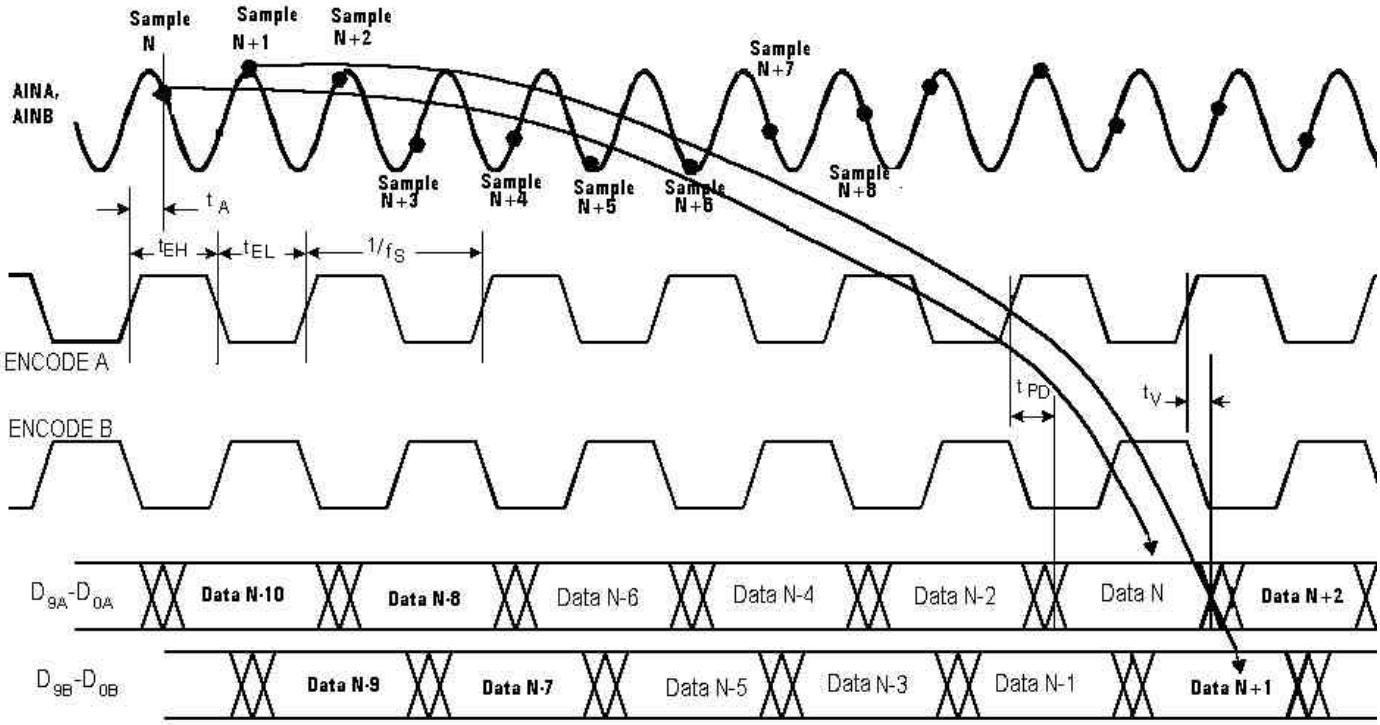

Figure 3. Normal Operation with Two Clock Sources (S1 = 1, S2 = 0) Channel Timing

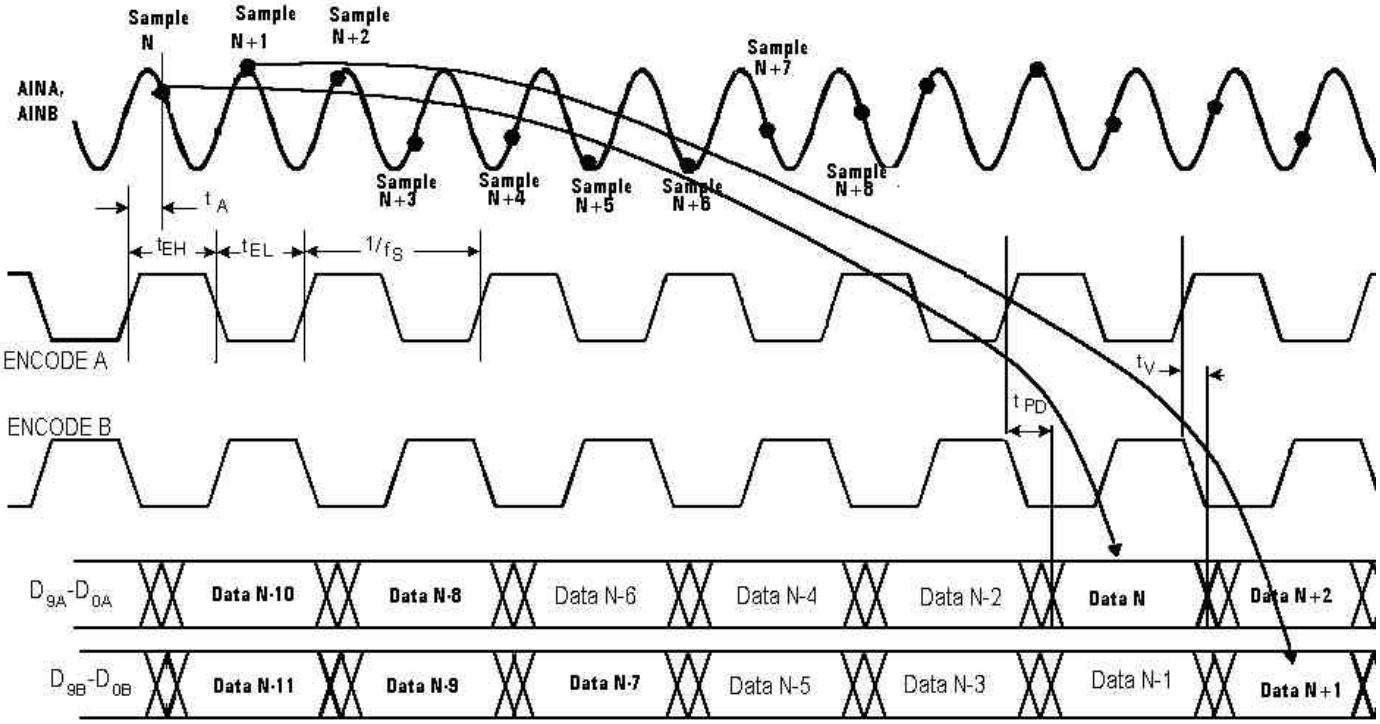

Figure 4. Data Align with Two Clock Sources (S1 = 1, S2 = 1) Channel Timing

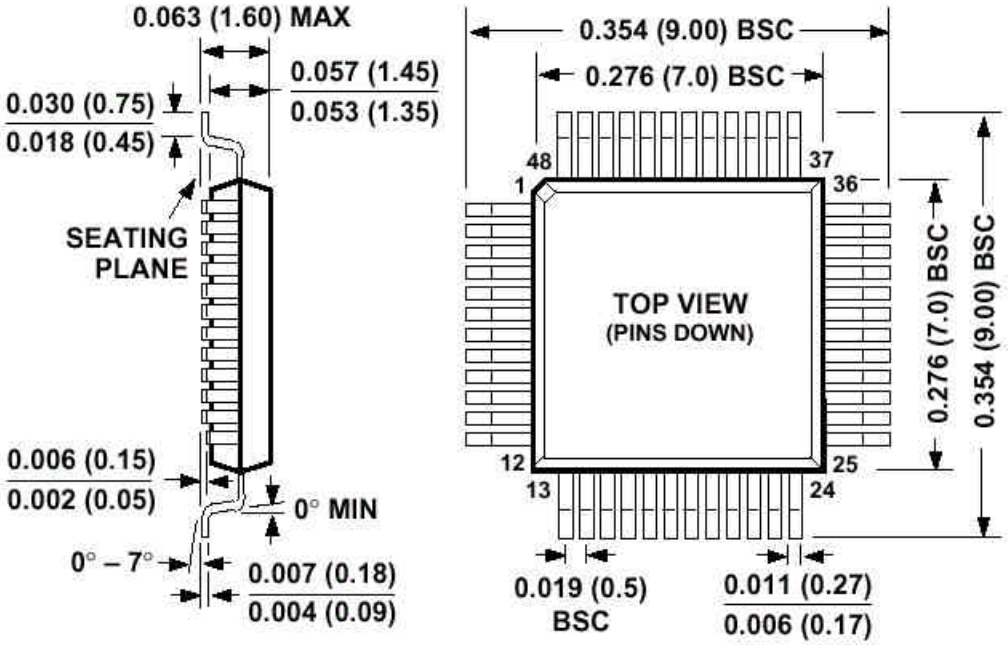

Figure 5. Package Outline (48-LQFP 7x7 - 1.4mm thick)

APPLICATION NOTES

THEORY OF OPERATION

The AD9218 ADC architecture is a bit per stage pipeline type converter utilizing switch capacitor techniques. These stages determine the 7 MSBs and drive a three bit flash. Each stage provides sufficient overlap and error correction allowing optimization of comparator accuracy. The input buffers are differential and both sets of inputs are internally biased. This allows the most flexible use of AC or DC and differential or single ended input modes. The output staging block aligns the data, carries out the error correction and feeds the data to output buffers. The set of output buffers are powered from a separate supply allowing adjustment of the output voltage swing. There is no discernible difference in performance between the two channels.

USING THE AD9218

ENCODE Input

Any high-speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A Track/Hold circuit is essentially a mixer. Any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9218, and the user is advised to give commensurate thought to the clock source. The ENCODE input is fully TTL/CMOS compatible.

Digital Outputs

The digital outputs are TTL/CMOS compatible for lower power consumption. During powerdown, the output buffers transition to a high impedance state. A data format selection option supports either two's complement (set high) or offset binary output (set low) formats.

Analog Input

The analog input to the AD9218 is a differential buffer. For best dynamic performance, impedance at AIN and AIN\ should match. Special care was taken in the design of the analog input section of the AD9218 to prevent damage and corruption of data when the input is overdriven. The nominal input range is 1.024 Vp–p.

Voltage Reference

A stable and accurate 1.25 V voltage reference is built into the AD9218 (VREF OUT). In normal operation, the internal reference is used by strapping pins 5 (ref in) and 7 (ref in) to pin 6 (ref out). The input range can be adjusted by varying the reference voltage applied to the AD9218. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full–scale range of the ADC tracks reference voltage, which changes linearly.

Timing

The AD9218 provides latched data outputs, with five pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command *(see Figure 2. . Normal Operation, Same* Clock (S1 =1, S2 = 0) Channel Timing *)*. The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9218. These transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD9218 is 10 MSPS. At clock rates below 10 MSPS, dynamic performance will degrade.

User Select Options

Two pins are available for a combination of operational modes. These options allow the user to power down channel B only or channel A and B, excluding the reference, reducing power consumption. In this mode the A and B channel output buffers are in a in a high impedance state.

The other option allows the user to skew the B channel output data by ½ a clock cycle. In other words, if two clocks are fed to the AD9218 and are 180° out of phase, enabling the data align will allow channel B output data to be available at the rising edge of Clock A. If the same encode clock is provided to both channels and the data align pin is enabled, then output data from channel B will be 180° out of phase with respect to channel A. If the same encode clock is provided to both channels and the data align pin is disabled, then both outputs are delivered on the same rising edge of the clock.

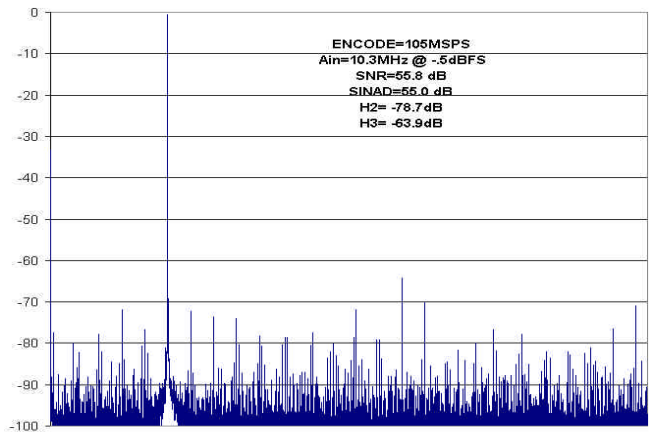

Fig 6 *Measured FFT Performance Ain=10.3MHz at 105Msps*

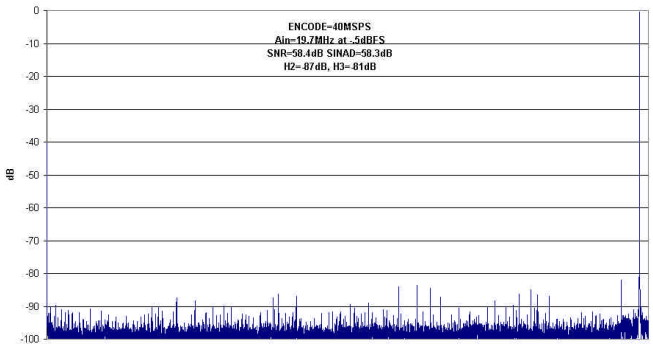

Fig 7 *Measured FFT Performance Ain=19.7MHz at 40Msps*