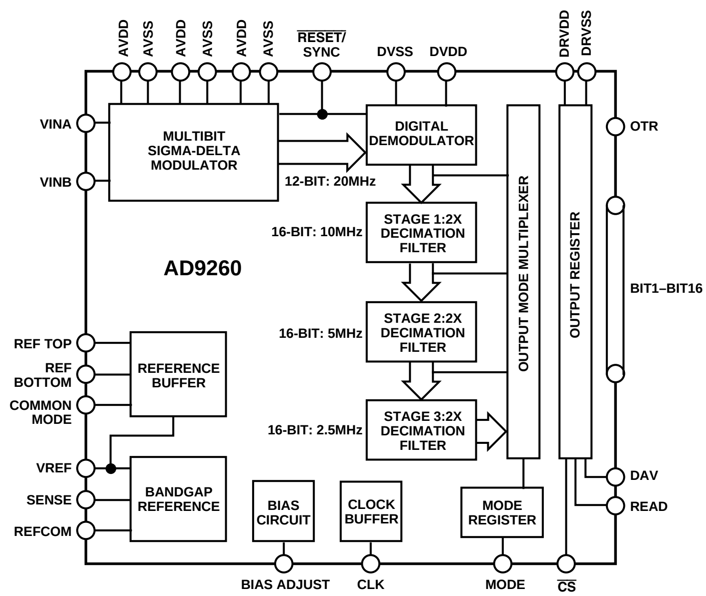
High Speed Oversampling CMOS ADC w/16-Bit Resolution at a 2.5 MHz Output Word Rate

ANALOG DEVICES

AD9260

FEATURES
- Monolithic 16-Bit, Oversampled A/D Converter
- 8× Oversampling Mode, 20 MSPS Clock
- 2.5 MHz Output Word Rate
- 1.01 MHz Signal Passband w/0.004 dB Ripple
- Signal-to-Noise Ratio: 88.5 dB
- Total Harmonic Distortion: –96 dB
- Spurious Free Dynamic Range: 100 dB
- Input Referred Noise: 0.6 LSB
- Selectable Oversampling Ratio: 1×, 2×, 4×, 8×
- Selectable Power Dissipation: 150 mW to 585 mW
- 85 dB Stopband Attenuation
- 0.004 dB Passband Ripple
- Linear Phase
- Single +5 V Analog Supply, +5 V/+3 V Digital Supply
- Synchronize Capability for Parallel ADC Interface
- Twos-Complement Output Data
- 44-Lead MQFP

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9260 is a 16-bit, high speed oversampled analog-to-digital converter (ADC) that offers exceptional dynamic range over a wide bandwidth. The AD9260 is manufactured on an advanced CMOS process. High dynamic range is achieved with an oversampling ratio of 8× through the use of a proprietary technique that combines the advantages of sigma-delta and pipeline converter technologies.

The AD9260 is a switched-capacitor ADC with a nominal full-scale input range of 4 V. It offers a differential input with 60 dB of common-mode rejection of common-mode signals. The signal range of each differential input is ±1 V centered on a 2.0 V common-mode level.

The on-chip decimation filter is configured for maximum performance and flexibility. A series of three half-band FIR filter stages provide 8× decimation filtering with 85 dB of stopband attenuation and 0.004 dB of passband ripple. An onboard digital multiplexer allows the user to access data from the various stages of the decimation filter.

The on-chip programmable reference and reference buffer amplifier are configured for maximum accuracy and flexibility. An external reference can also be chosen to suit the users specific dc accuracy and drift requirements.

The AD9260 operates on a single +5 V supply, typically consuming 585 mW of power. A power scaling circuit is provided allowing the AD9260 to operate at power consumption levels as low as 150 mW at reduced clock and data rates. The AD9260 is available in a 44-lead MQFP package and is specified to operate over the industrial temperature range.

PRODUCT HIGHLIGHTS

The AD9260 is fabricated on a very cost effective CMOS process. High speed, precision mixed-signal analog circuits are combined with high density digital filter circuits.

The AD9260 offers a complete single-chip 16-bit sampling ADC with a 2.5 MHz output data rate in a 44-lead MQFP.

Selectable Internal Decimation Filtering—The AD9260 provides a high performance decimation filter with 0.004 dB passband ripple and 85 dB of stopband attenuation. The filter is configurable with options for 1×, 2×, 4×, and 8× decimation.

Power Scaling—The AD9260 consumes a low 585 mW of power at 16-bit resolution and 2.5 MHz output data rate. Its power can be scaled down to as low as 150 mW at reduced clock rates.

Single Supply— Both of the analog and digital portions of the AD9260 can operate off of a single +5 V supply simplifying system power supply design. The digital logic will also accommodate a single +3 V supply for reduced power.

REV. A

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AD9260–SPECIFICATIONS

CLOCK INPUT FREQUENCY RANGE

Parameter—Decimation Factor (N)	AD9260 (8)	AD9260 (4)	AD9260 (2)	AD9260 (1)	Units
CLOCK INPUT (Modulator Sample Rate, f_{CLOCK})	1 20	1 20	1 20	1 20	kHz min MHz max
OUTPUT WORD RATE (FS = f_{CLOCK}/N)	0.125 2.5	0.250 5	0.500 10	1 20	kHz min MHz max

Specifications subject to change without notice

DC SPECIFICATIONS (AVDD = +5 V, DVDD = +3 V, DRVDD = +3 V, f_{CLOCK} = 20 MSPS, V_{REF} = +2.5 V, Input CML = 2.0 V T_{MIN} to T_{MAX} unless otherwise noted, R_{BIAS} = 2 kΩ)

Parameter—Decimation Factor (N)	AD9260 (8)	AD9260 (4)	AD9260 (2)	AD9260 (1)	Units
RESOLUTION	16	16	16	12	Bits min
INPUT REFERRED NOISE (TYP)					
1.0 V Reference	1.40	2.4	6.0	1.3	LSB rms typ
2.5 V Reference[1]	0.68 (90.6)	1.2 (86)	3.7 (76)	1.0 (63.2)	LSB rms typ (dB typ)
ACCURACY					
Integral Nonlinearity (INL)	±0.75	±0.75	±0.75	±0.3	LSB typ
Differential Nonlinearity (DNL)	±0.50	±0.50	±0.50	±0.25	LSB typ
No Missing Codes	16	16	16	12	Bits Guaranteed
Offset Error	0.9 (0.5)	(0.5)	(0.5)	(0.5)	% FSR max (typ @ +25°C)
Gain Error[2]	2.75 (0.66)	(0.66)	(0.66)	(0.66)	% FSR max (typ @ +25°C)
Gain Error[3]	1.35 (0.7)	(0.7)	(0.7)	(0.7)	% FSR max (typ @ +25°C)
TEMPERATURE DRIFT					
Offset Error	2.5	2.5	2.5	2.5	ppm/°C typ
Gain Error[2]	22	22	22	22	ppm/°C typ
Gain Error[3]	7.0	7.0	7.0	7.0	ppm/°C typ
POWER SUPPLY REJECTION					
AVDD, DVDD, DRVDD (+5 V ± 0.25 V)	0.06	0.06	0.06	0.06	% FSR max
ANALOG INPUT					
Input Span					
V_{REF} = 1.0 V	1.6	1.6	1.6	1.6	V p-p Diff. max
V_{REF} = 2.5 V	4.0	4.0	4.0	4.0	V p-p Diff. max
Input (VINA or VINB) Range	+0.5	+0.5	+0.5	+0.5	V min
	+AVDD – 0.5	+AVDD – 0.5	+AVDD – 0.5	+AVDD – 0.5	V max
Input Capacitance	10.2	10.2	10.2	10.2	pF typ
INTERNAL VOLTAGE REFERENCE					
Output Voltage (1 V Mode)	1	1	1	1	V typ
Output Voltage Error (1 V Mode)	±14	±14	±14	±14	mV max
Output Voltage (2.5 V Mode)	2.5	2.5	2.5	2.5	V typ
Output Voltage Error (2.5 V Mode)	±35	±35	±35	±35	mV max
Load Regulation[4]					
1 V REF	0.5	0.5	0.5	0.5	mV max
2.5 V REF	2.0	2.0	2.0	2.0	mV max
REFERENCE INPUT RESISTANCE	8	8	8	8	kΩ

Parameter—Decimation Factor (N)	AD9260 (8)	AD9260 (4)	AD9260 (2)	AD9260 (1)	Units
POWER SUPPLIES					
Supply Voltages					
AVDD	+5	+5	+5	+5	V (±5%)
DVDD and DRVDD	+5.5	+5.5	+5.5	+5.5	V max
	+2.7	+2.7	+2.7	+2.7	V min
Supply Current					
IAVDD	115	115	115	115	mA typ
				134	mA max
IDVDD	12.5	10.3	6.5	2.4	mA typ
				3.5	mA max
IDRVDD	0.450	0.850	1.7	2.6	mA typ
POWER CONSUMPTION	613	608	600	585	mW typ
				630	mW max

NOTES
[1]VINA and VINB Connect to DUT CML.
[2]Including Internal 2.5 V reference.
[3]Excluding Internal 2.5 V reference.
[4]Load regulation with 1 mA load Current (in addition to that required by AD9260).

Specifications subject to change without notice.

AC SPECIFICATIONS (AVDD = +5 V, DVDD = +3 V, DRVDD = +3 V, f_{CLOCK} = 20 MSPS, V_{REF} = +2.5 V, Input CML = 2.0 V T_{MIN} to T_{MAX} unless otherwise noted, R_{BIAS} = 2 kΩ)

Parameter—Decimation Factor (N)	AD9260(8)	AD9260(4)	AD9260(2)	AD9260(1)	Units
DYNAMIC PERFORMANCE					
INPUT TEST FREQUENCY: 100 kHz (typ)					
Signal-to-Noise Ratio (SNR)					
Input Amplitude = –0.5 dBFS	88.5	82	74	63	dB typ
Input Amplitude = –6.0 dBFS	82.5	78	68	58	dB typ
SNR and Distortion (SINAD)					
Input Amplitude = –0.5 dBFS	87.5	82	74	63	dB typ
Input Amplitude = –6.0 dBFS	82	77.5	69	58	dB typ
Total Harmonic Distortion (THD)					
Input Amplitude = –0.5 dBFS	–96	–96	–97	–98	dB typ
Input Amplitude = –6.0 dBFS	–93	–98	–96	–98	dB typ
Spurious Free Dynamic Range (SFDR)					
Input Amplitude = –0.5 dBFS	100	98	98	88	dB typ
Input Amplitude = –6.0 dBFS	94	100	94	84	dB typ
INPUT TEST FREQUENCY: 500 kHz					
Signal-to-Noise Ratio (SNR)					
Input Amplitude = –0.5 dBFS	86.5	82	74	63	dB typ
	80.5				dB min
Input Amplitude = –6.0 dBFS	82.5	77	68	58	dB typ
SNR and Distortion (SINAD)					
Input Amplitude = –0.5 dBFS	86.0	81	74	63	dB typ
	80.0				dB min
Input Amplitude = –6.0 dBFS	82.0	77	68	58	dB typ
Total Harmonic Distortion (THD)					
Input Amplitude = –0.5 dBFS	–97.0	–92	–89	–86	dB typ
	–90.0				dB max
Input Amplitude = –6.0 dBFS	–95.5	–96	–89	–86	dB typ
Spurious Free Dynamic Range (SFDR)					
Input Amplitude = –0.5 dBFS	99.0	92	91	88	dB typ
	90.0				dB max
Input Amplitude = –6.0 dBFS	98	100	91	82	dB typ

AD9260–SPECIFICATIONS

AC SPECIFICATIONS (Continued)

Parameter—Decimation Factor (N)	AD9260 (8)	AD9260 (4)	AD9260 (2)	AD9260 (1)	Units
DYNAMIC PERFORMANCE (*Continued*)					
INPUT TEST FREQUENCY: 1.0 MHz (typ)					
Signal-to-Noise Ratio (SNR)					
Input Amplitude = –0.5 dBFS	85	82	74	63	dB typ
Input Amplitude = –6.0 dBFS	80	76	68	58	dB typ
SNR and Distortion (SINAD)					
Input Amplitude = –0.5 dBFS	84.5	81	74	63	dB typ
Input Amplitude = –6.0 dBFS	80	76	69	58	dB typ
Total Harmonic Distortion (THD)					
Input Amplitude = –0.5 dBFS	–102	–96	–82	–79	dB typ
Input Amplitude = –6.0 dBFS	–96	–94	–84	–77	dB typ
Spurious Free Dynamic Range (SFDR)					
Input Amplitude = –0.5 dBFS	105	98	83	80	dB typ
Input Amplitude = –6.0 dBFS	98	96	87	80	dB typ
INPUT TEST FREQUENCY: 2.0 MHz (typ)					
Signal-to-Noise Ratio (SNR)					
Input Amplitude = –0.5 dBFS		82	74	63	dB typ
Input Amplitude = –6.0 dBFS		76	68	58	dB typ
SNR and Distortion (SINAD)					
Input Amplitude = –0.5 dBFS		81	73	62	dB typ
Input Amplitude = –6.0 dBFS		76	69	58	dB typ
Total Harmonic Distortion (THD)					
Input Amplitude = –0.5 dBFS		–101	–80	–75	dB typ
Input Amplitude = –6.0 dBFS		–95	–80	–76	dB typ
Spurious Free Dynamic Range (SFDR)					
Input Amplitude = –0.5 dBFS		104	80	78	dB typ
Input Amplitude = –6.0 dBFS		100	83	79	dB typ
INPUT TEST FREQUENCY: 5.0 MHz (typ)					
Signal-to-Noise Ratio (SNR)					
Input Amplitude = –0.5 dBFS				59	dB typ
Input Amplitude = –6.0 dBFS				57	dB typ
SNR and Distortion (SINAD)					
Input Amplitude = –0.5 dBFS				58	dB typ
Input Amplitude = –6.0 dBFS				57	dB typ
Total Harmonic Distortion (THD)					
Input Amplitude = –0.5 dBFS				–58	dB typ
Input Amplitude = –6.0 dBFS				–67	dB typ
Spurious Free Dynamic Range (SFDR)					
Input Amplitude = –0.5 dBFS				59	dB typ
Input Amplitude = –6.0 dBFS				70	dB typ
INTERMODULATION DISTORTION					
$f_{IN}1$ = 475 kHz, $f_{IN}2$ = 525 kHz	–93	–91	–91	–83	dBFS typ
$f_{IN}1$ = 950 kHz, $f_{IN}2$ = 1.050 MHz	–95	–86	–85	–83	dBFS typ
DYNAMIC CHARACTERISTICS					
Full Power Bandwidth	75	75	75	75	MHz typ
Small Signal Bandwidth (A_{IN} = –20 dBFS)	75	75	75	75	MHz typ
Aperture Jitter	2	2	2	2	ps rms typ

Specifications subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

Parameter	AD9260	Units
8× DECIMATION (N = 8)		
Passband Ripple	0.00125	dB max
Stopband Attenuation	82.5	dB min
Passband	0	MHz min
	0.605 × (f_{CLOCK}/20 MHz)	MHz max
Stopband	1.870 × (f_{CLOCK}/20 MHz)	MHz min
	18.130 × (f_{CLOCK}/20 MHz)	MHz max
Passband/Transition Band Frequency		
(–0.1 dB Point)	0.807 × (f_{CLOCK}/20 MHz)	MHz max
(–3.0 dB Point)	1.136 × (f_{CLOCK}/20 MHz)	MHz max
Absolute Group Delay[1]	8.20 × (20 MHz/f_{CLOCK})	µs max
Group Delay Variation	0	µs max
Settling Time (to ±0.0007%)[1]	13.35 × (20 MHz/f_{CLOCK})	µs max
4× DECIMATION (N = 4)		
Passband Ripple	0.001	dB max
Stopband Attenuation	82.5	dB min
Passband	0	MHz min
	1.24 × (f_{CLOCK}/20 MHz)	MHz max
Stopband	3.75 × (f_{CLOCK}/20 MHz)	MHz min
	16.25 × (f_{CLOCK}/20 MHz)	MHz max
Passband/Transition Band Frequency		
(–0.1 dB Point)	1.61 × (f_{CLOCK}/20 MHz)	MHz max
(–3.0 dB Point)	2.272 × (f_{CLOCK}/20 MHz)	MHz max
Absolute Group Delay[1]	2.90 × (20 MHz/f_{CLOCK})	µs max
Group Delay Variation	0	µs max
Settling Time (to ±0.0007%)[1]	5.05 × (20 MHz/f_{CLOCK})	µs max
2× DECIMATION (N = 2)		
Passband Ripple	0.0005	dB max
Stopband Attenuation	85.5	dB min
Passband	0	MHz min
	2.491 × (f_{CLOCK}/20 MHz)	MHz max
Stopband	7.519 × (f_{CLOCK}/20 MHz)	MHz min
	12.481 × (f_{CLOCK}/20 MHz)	MHz max
Passband/Transition Band Frequency		
(–0.1 dB Point)	3.231 × (f_{CLOCK}/20 MHz)	MHz max
(–3.0 dB Point)	4.535 × (f_{CLOCK}/20 MHz)	MHz max
Absolute Group Delay[1]	0.80 × (20 MHz/f_{CLOCK})	µs max
Group Delay Variation	0	µs max
Settling Time (to ±0.0007%)[1]	1.40 × (20 MHz/f_{CLOCK})	µs max
1× DECIMATION (N = 1)		
Propagation Delay: t_{PROP}	13	ns max
Absolute Group Delay	(225 × (20 MHz/f_{CLOCK})) + t_{PROP}	ns max

NOTES

[1]To determine "overall" Absolute Group Delay and/or Settling Time inclusive of delay from the sigma-delta modulator, add Absolute Group Delay and/or Settling Time pertaining to specific decimation mode to the Absolute Group Delay specified in 1× decimation.

Specifications subject to change without notice.

AD9260–Digital Filter Characteristics

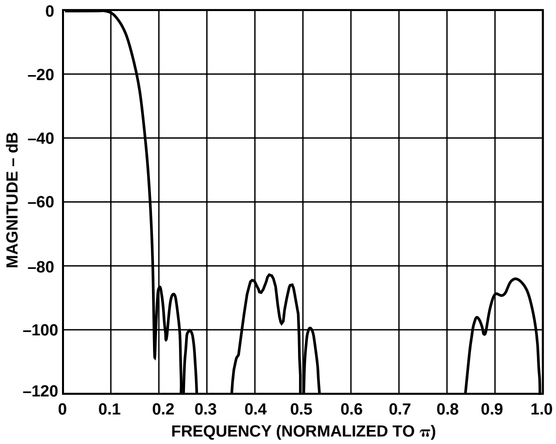


Figure 1a. 8× FIR Filter Frequency Response

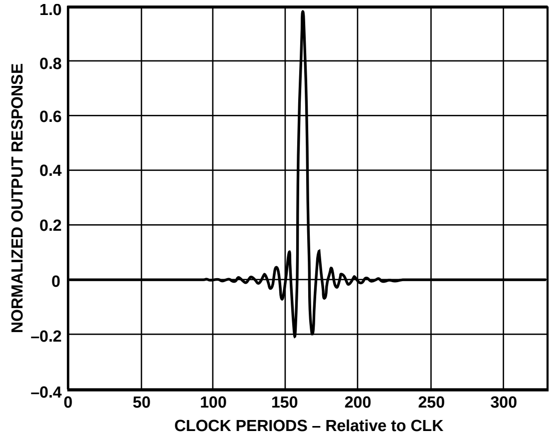


Figure 1b. 8× FIR Filter Impulse Response

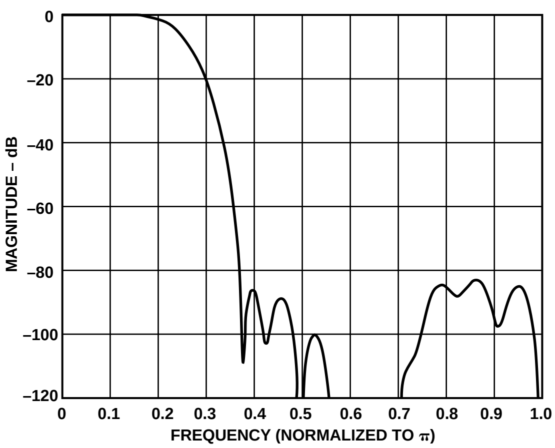


Figure 2a. 4× FIR Filter Frequency Response

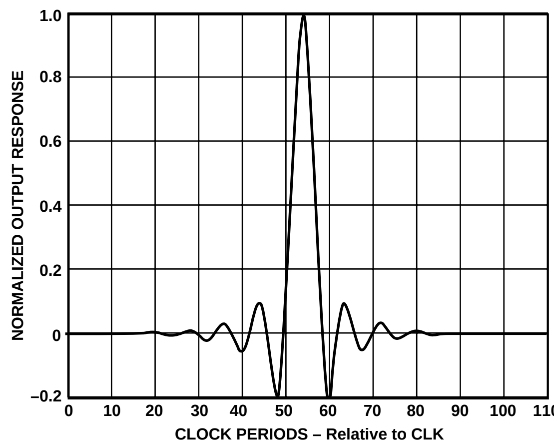


Figure 2b. 4× FIR Filter Impulse Response

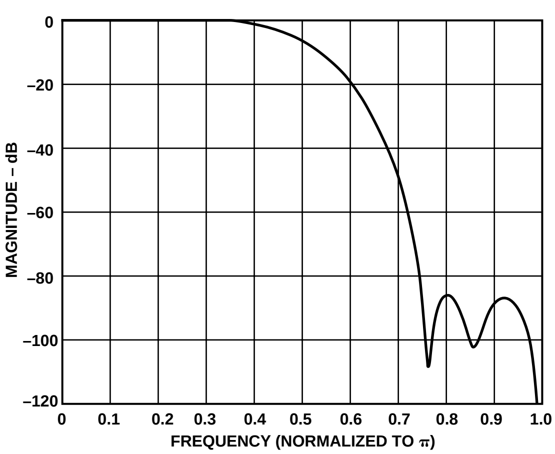


Figure 3a. 2× FIR Filter Frequency Response

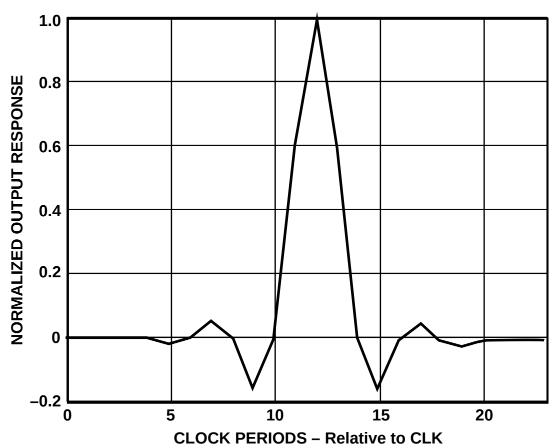


Figure 3b. 2× FIR Filter Impulse Response

Table I. Integer Filter Coefficients for First Stage Decimation Filter (23-Tap Halfband FIR Filter)

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(23)	–1
H(2)	H(22)	0
H(3)	H(21)	13
H(4)	H(20)	0
H(5)	H(19)	–66
H(6)	H(18)	0
H(7)	H(17)	224
H(8)	H(16)	0
H(9)	H(15)	–642
H(10)	H(14)	0
H(11)	H(13)	2496
H(12)		4048

Table II. Integer Filter Coefficients for Second Stage Decimation Filter (43-Tap Halfband FIR Filter)

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(43)	3
H(2)	H(42)	0
H(3)	H(41)	–12
H(4)	H(40)	0
H(5)	H(39)	35
H(6)	H(38)	0
H(7)	H(37)	–83
H(8)	H(36)	0
H(9)	H(35)	172
H(10)	H(34)	0
H(11)	H(33)	–324
H(12)	H(32)	0
H(13)	H(31)	572
H(14)	H(30)	0
H(15)	H(29)	–976
H(16)	H(28)	0
H(17)	H(27)	1680
H(18)	H(26)	0
H(19)	H(25)	–3204
H(20)	H(24)	0
H(21)	H(23)	10274
H(22)		16274

NOTE: The composite filter coefficients (i.e., impulse response) in the 4× decimation mode can be determined by convolving the first stage filter taps with a "zero stuffed" version of the second stage filter taps. Similarly, the composite filter coefficients in the 8× decimation mode can be determined by convolving the taps of the composite 4× decimation mode (as previously determined) with a "zero stuffed" version of the third stage filter taps.

Table III. Integer Filter Coefficients for Third Stage Decimation Filter (107-Tap Halfband FIR Filter)

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(107)	–1
H(2)	H(106)	0
H(3)	H(105)	2
H(4)	H(104)	0
H(5)	H(103)	–2
H(6)	H(102)	0
H(7)	H(101)	3
H(8)	H(100)	0
H(9)	H(99)	–3
H(10)	H(98)	0
H(11)	H(97)	1
H(12)	H(96)	0
H(13)	H(95)	3
H(14)	H(94)	0
H(15)	H(93)	–12
H(16)	H(92)	0
H(17)	H(91)	27
H(18)	H(90)	0
H(19)	H(89)	–50
H(20)	H(88)	0
H(21)	H(87)	85
H(22)	H(86)	0
H(23)	H(85)	–135
H(24)	H(84)	0
H(25)	H(83)	204
H(26)	H(82)	0
H(27)	H(81)	–297
H(28)	H(80)	0
H(29)	H(79)	420
H(30)	H(78)	0
H(31)	H(77)	–579
H(32)	H(76)	0
H(33)	H(75)	784
H(34)	H(74)	0
H(35)	H(73)	–1044
H(36)	H(72)	0
H(37)	H(71)	1376
H(38)	H(70)	0
H(39)	H(69)	–1797
H(40)	H(68)	0
H(41)	H(67)	2344
H(42)	H(66)	0
H(43)	H(65)	–3072
H(44)	H(64)	0
H(45)	H(63)	4089
H(46)	H(62)	0
H(47)	H(61)	–5624
H(48)	H(60)	0
H(49)	H(59)	8280
H(50)	H(58)	0
H(51)	H(57)	–14268
H(52)	H(56)	0
H(53)	H(55)	43520
H(54)		68508

AD9260–SPECIFICATIONS

DIGITAL SPECIFICATIONS (AVDD = +5 V, DVDD = +5 V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD9260	Units
CLOCK[1] AND LOGIC INPUTS		
High Level Input Voltage		
(DVDD = +5 V)	+3.5	V min
(DVDD = +3 V)	+2.1	V max
Low Level Input Voltage		
(DVDD = +5 V)	+1.0	V min
(DVDD = +3 V)	+0.9	V max
High Level Input Current (V_{IN} = DVDD)	±10	µA max
Low Level Input Current (V_{IN} = 0 V)	±10	µA max
Input Capacitance	5	pF typ
LOGIC OUTPUTS (with DRVDD = 5 V)		
High Level Output Voltage (I_{OH} = 50 µA)	+4.5	V min
High Level Output Voltage (I_{OH} = 0.5 mA)	+2.4	V min
Low Level Output Voltage[2] (I_{OL} = 0.3 mA)	+0.4	V max
Low Level Output Voltage (I_{OL} = 50 µA)	+0.1	V max
Output Capacitance	5	pF typ
LOGIC OUTPUTS (with DRVDD = 3 V)		
High Level Output Voltage (I_{OH} = 50 µA)	+2.4	V min
Low Level Output Voltage (I_{OL} = 50 µA)	+0.7	V max

NOTES
[1]Since CLK is referenced to AVDD, +5 V logic input levels only apply.
[2]The AD9260 is not guaranteed to meet V_{OL} = 0.4 V max for standard TTL load of I_{OL} = 1.6 mA.

Specifications subject to change without notice.

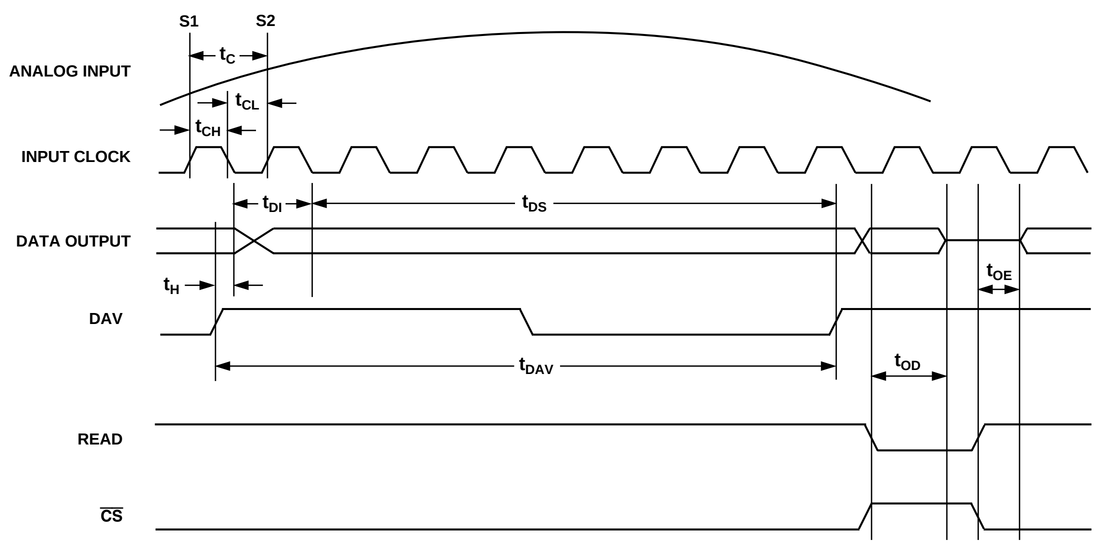


Figure 4. Timing Diagram

SWITCHING SPECIFICATIONS (AVDD = +5 V, DVDD = +5 V, C_L = 20 pF, T_{MIN} to T_{MAX} unless otherwise noted)

Parameters	Symbol	AD9260	Units
Clock Period	t_C	50	ns min
Data Available (DAV) Period	t_{DAV}	$t_C \times$ Mode	ns min
Data Invalid	t_{DI}	40% t_{DAV}	ns max
Data Setup Time	t_{DS}	$t_{DAV} - t_H - t_{DI}$	ns min
Clock Pulsewidth High	t_{CH}	22.5	ns min
Clock Pulsewidth Low	t_{CL}	22.5	ns min
Data Hold Time	t_H	3.5	ns min
Three-State Output Disable Time	t_{OD}	8	ns typ
Three-State Output Enable Time	t_{OE}	45	ns typ

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	AVSS	–0.3	+6.5	V
DVDD	DVSS	–0.3	+6.5	V
AVSS	DVSS	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
DRVDD	DRVSS	–0.3	+6.5	V
DRVSS	AVSS	–0.3	+0.3	V
REFCOM	AVSS	–0.3	+0.3	V
CLK, $\overline{\text{MODE}}$, READ, $\overline{\text{CS}}$, $\overline{\text{RESET}}$	DVSS	–0.3	DVDD + 0.3	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
VINA, VINB, CML, BIAS	AVSS	–0.3	AVDD + 0.3	V
VREF	AVSS	–0.3	AVDD + 0.3	V
SENSE	AVSS	–0.3	AVDD + 0.3	V
CAPB, CAPT	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9260AS	–40°C to +85°C	44-Lead MQFP	S-44
AD9260EB		Evaluation Board	

*S = Metric Quad Flatpack.

THERMAL CHARACTERISTICS

Thermal Resistance
44-Lead MQFP
θ_{JA} = 53.2°C/W
θ_{JC} = 19°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9260 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DEFINITIONS OF SPECIFICATION

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 14-bit resolution indicates that all 16384 codes, respectively, must be present over all operating ranges.

NOTE: Conventional INL and DNL measurements don't really apply to ΣΔ converters: the DNL looks continually better if longer data records are taken. For the AD9260, INL and DNL numbers are given as representative.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

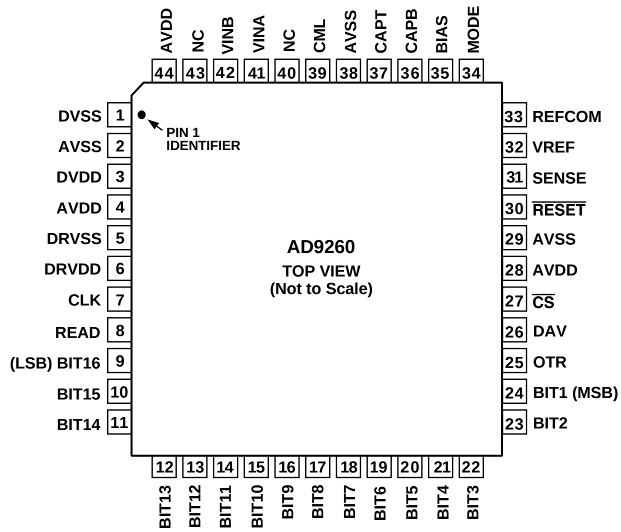
SPURIOUS FREE DYNAMIC RANGE (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

TWO-TONE SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

PIN CONFIGURATION



NC = NO CONNECT

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	DVSS	Digital Ground.
2, 29, 38	AVSS	Analog Ground.
3	DVDD	+3 V to +5 V Digital Supply.
4, 28, 44	AVDD	+5 V Analog Supply.
5	DRVSS	Digital Output Driver Ground.
6	DRVDD	+3 V to +5 V Digital Output Driver Supply.
7	CLK	Clock Input.
8	READ	Part of DSP Interface—Pull Low to Disable Output Bits.
9	BIT16	Least Significant Data Bit (LSB).
10–23	BIT15–BIT2	Data Output Bit.
24	BIT1	Most Significant Data Bit (MSB).
25	OTR	Out of Range—Set When Converter or Filter Overflows.
26	DAV	Data Available.
27	$\overline{\text{CS}}$	Chip Select ($\overline{\text{CS}}$): Active LOW.
30	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$: Active LOW.
31	SENSE	Reference Amplifier SENSE: Selects REF Level.
32	VREF	Input Span Select Reference I/O.
33	REFCOM	Reference Common.
34	MODE	Mode Select—Selects Decimation Mode.
35	BIAS	Power Bias.
36	CAPB	Noise Reduction Pin—Decouples Reference Level.
37	CAPT	Noise Reduction Pin—Decouples Reference Level.
39	CML	Common-Mode Level (AVDD/2.5).
40, 43	NC	No Connect (Ground for Shielding Purposes).
41	VINA	Analog Input Pin (+).
42	VINB	Analog Input Pin (–).

AD9260–Typical Performance Characteristics

(AVDD = DVDD = DRVDD = +5.0 V, 4 V Input Span, Differential DC Coupled Input with CML = 2.0 V, f_{CLOCK} = 20 MSPS, Full Bias)

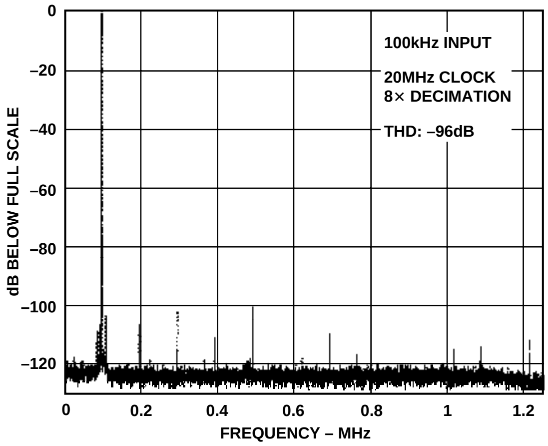


Figure 5. Spectral Plot of the AD9260 at 100 kHz Input, 20 MHz Clock, 8× OSR (2.5 MHz Output Data Rate)

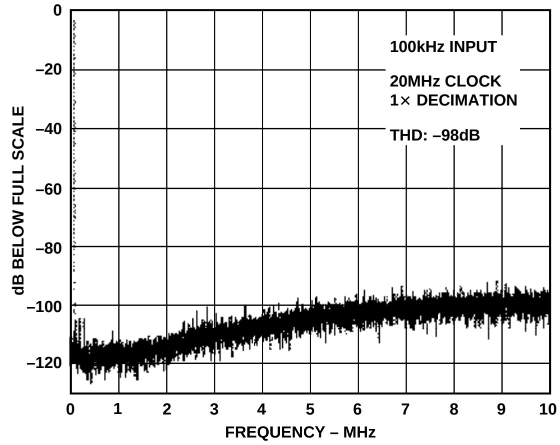


Figure 8. Spectral Plot of the AD9260 at 100 kHz Input, 20 MHz Clock, Undecimated (20 MHz Output Data Rate)

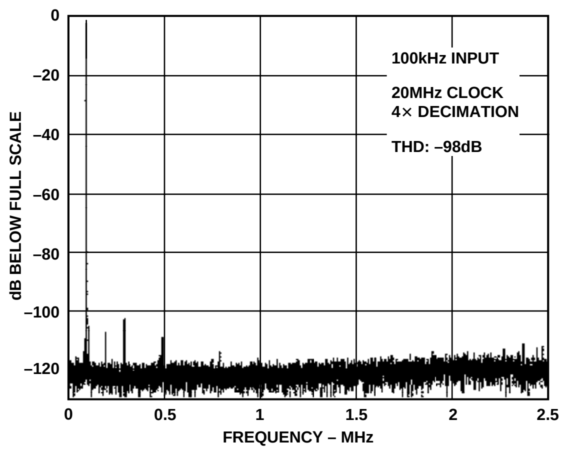


Figure 6. Spectral Plot of the AD9260 at 100 kHz Input, 20 MHz Clock, 4× OSR (5 MHz Output Data Rate)

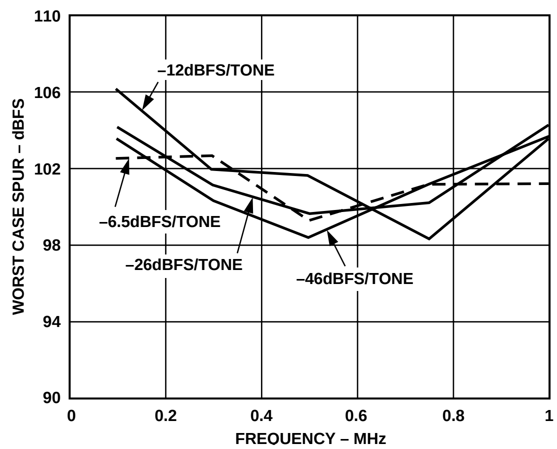


Figure 9. Dual Tone SFDR vs. Input Frequency ($F_1 = F_2$, ($F_1 - F_2$, Span = 10% Center Frequency, Mode = 8×)

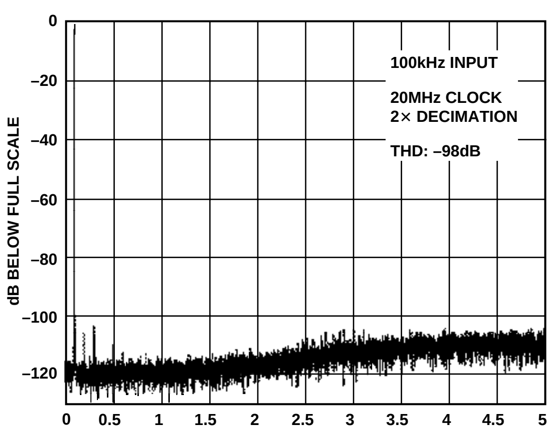


Figure 7. Spectral Plot of the AD9260 at 100 kHz Input, 20 MHz Clock, 2× OSR (10 MHz Output Data Rate)

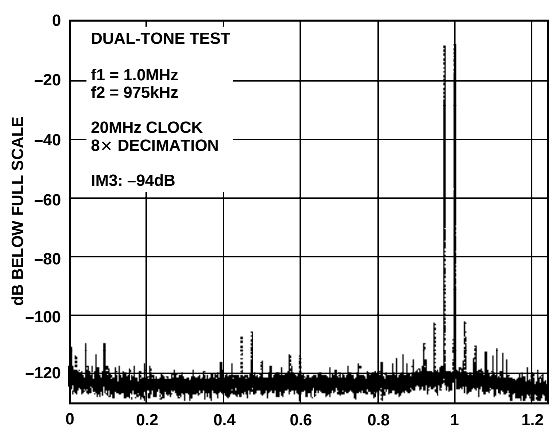


Figure 10. Two-Tone Spectral Performance of the AD9260 Given Inputs at 9 75 kHz and 1.0 MHz, 20 MHz Clock, 8× Decimation

Typical AC Characterization Curves vs. Decimation Mode

(AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, Differential DC Coupled Input with CML = 2 V, A_{IN} = 0.5 dBFS Full Bias)

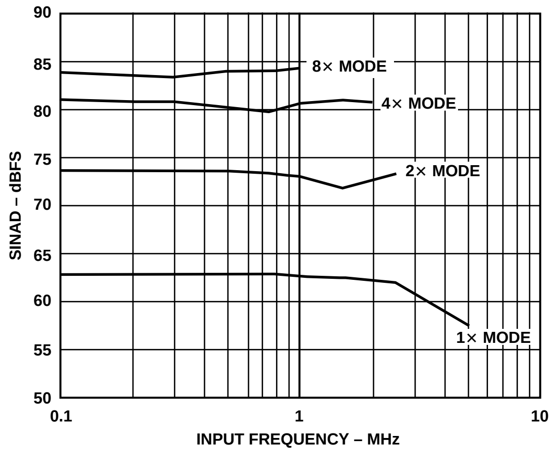


Figure 11. SINAD vs. Input Frequency (f_{CLOCK} = 20 MSPS)[1]

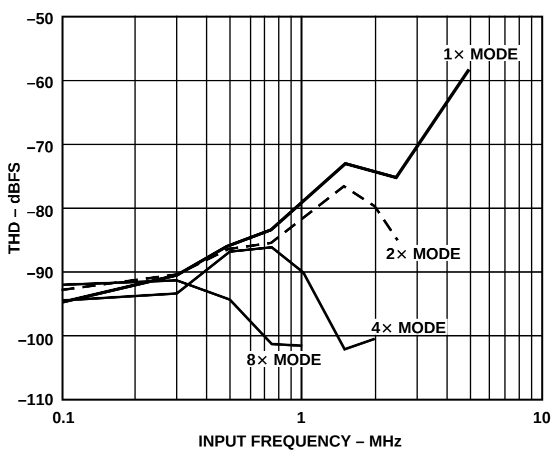


Figure 12. THD vs. Input Frequency (f_{CLOCK} = 20 MSPS)

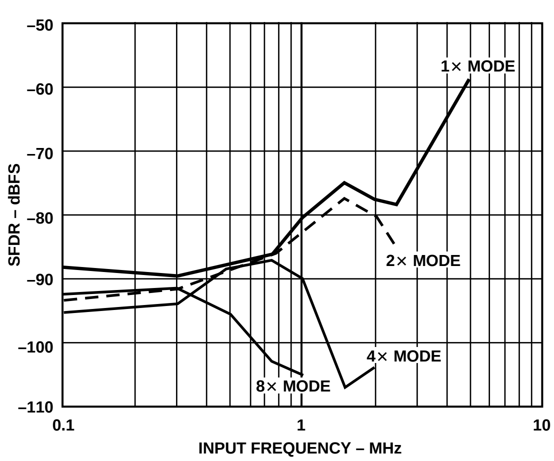


Figure 13. SFDR vs. Input Frequency (f_{CLOCK} = 20 MSPS)

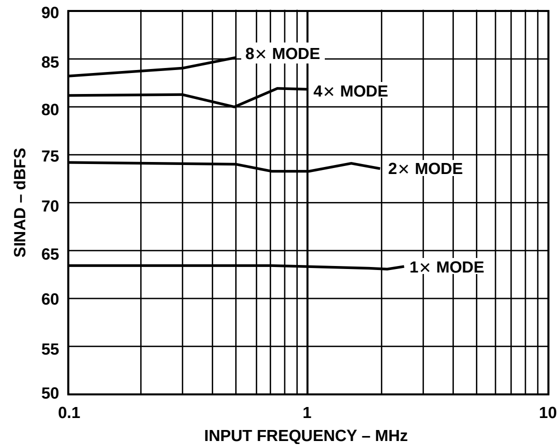


Figure 14. SINAD vs. Input Frequency (f_{CLOCK} = 10 MSPS)[1]

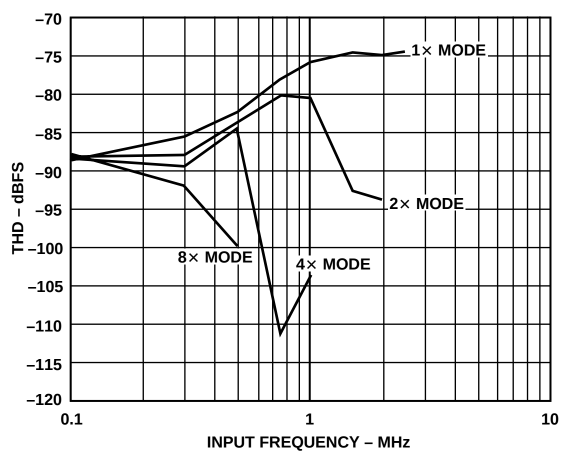


Figure 15. THD vs. Input Frequency (f_{CLOCK} = 10 MSPS)

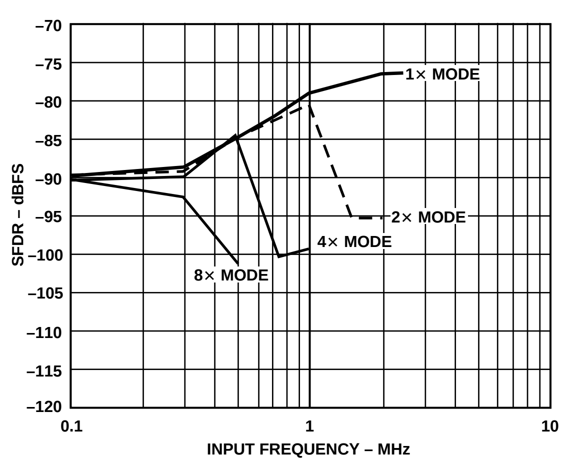


Figure 16. SFDR vs. Input Frequency (f_{CLOCK} = 10 MSPS)

[1]8× SINAD performance limited by noise contribution of input differential op amp driver.

Typical AC Characterization Curves for 8× Mode

(AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, Differential DC Coupled Input with CML = 2 V, Full Bias)

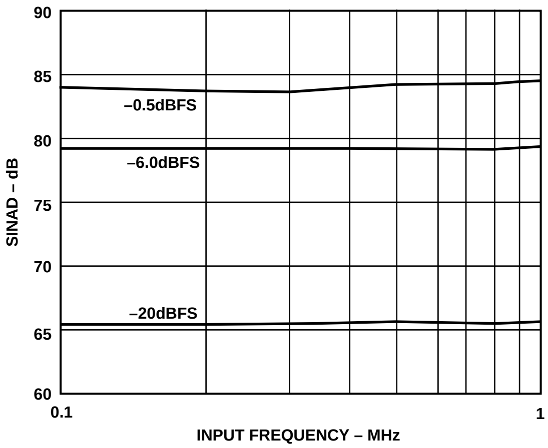


Figure 17. SINAD vs. Input Frequency (f_{CLOCK} = 20 MSPS)[1]

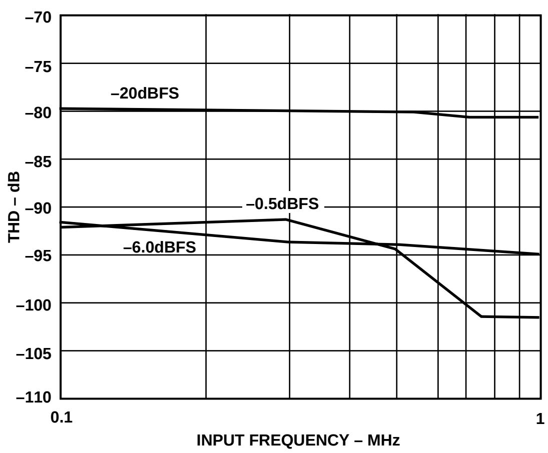


Figure 18. THD vs. Input Frequency (f_{CLOCK} = 20 MSPS)

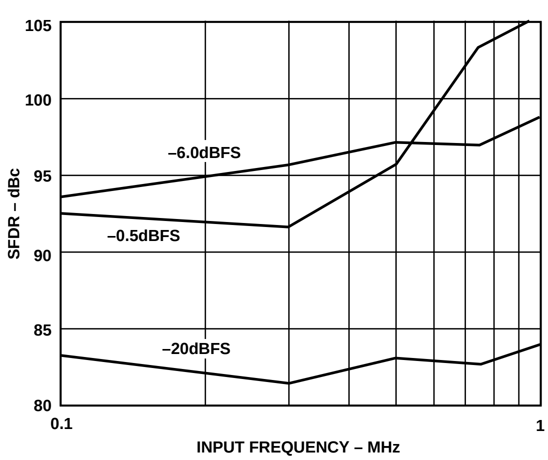


Figure 19. SFDR vs. Input Frequency (f_{CLOCK} = 20 MSPS)

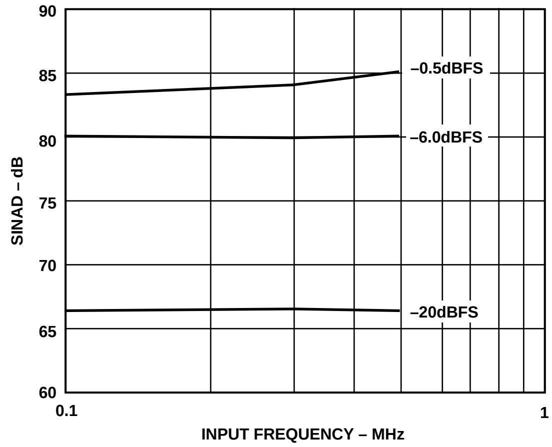


Figure 20. SINAD vs. Input Frequency (f_{CLOCK} = 10 MSPS)[1]

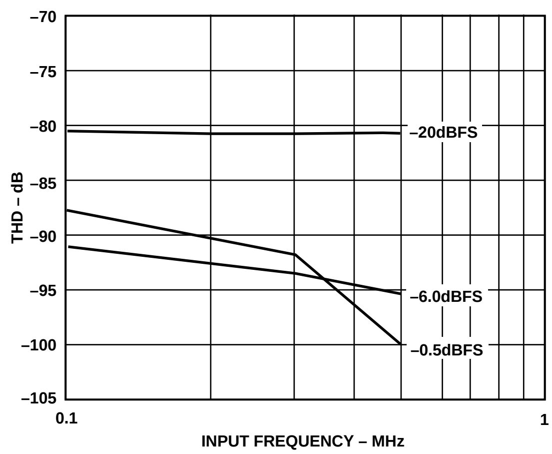


Figure 21. THD vs. Input Frequency (f_{CLOCK} = 10 MSPS)

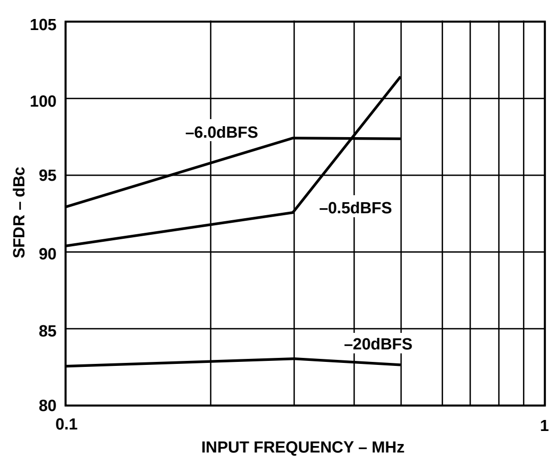


Figure 22. SFDR vs. Input Frequency (f_{CLOCK} = 10 MSPS)

[1]SINAD performance limited by noise contribution of input differential op amp driver.

Typical AC Characterization Curves for 4× Mode

(AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, Differential DC Coupled Input with CML = 2 V, Full Bias)

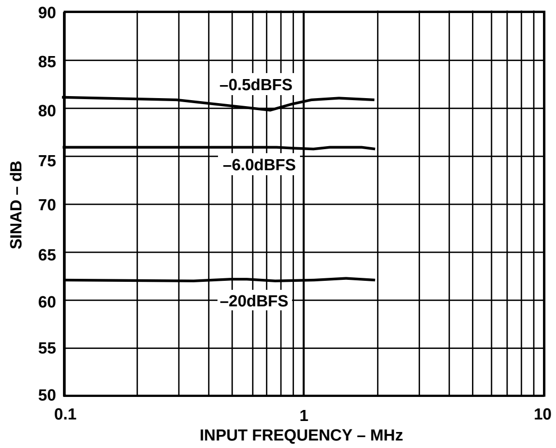


Figure 23. SINAD vs. Input Frequency (f_{CLOCK} = 20 MSPS)

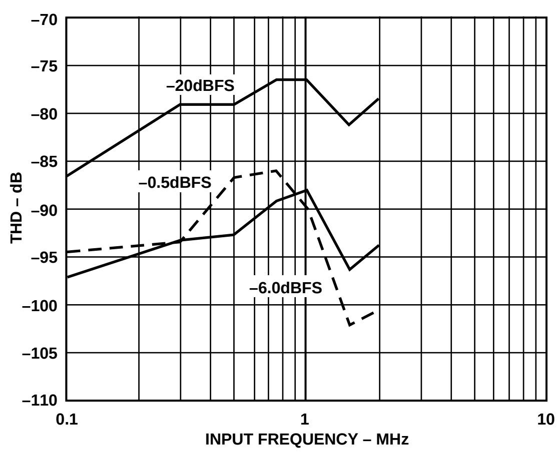


Figure 24. THD vs. Input Frequency (f_{CLOCK} = 20 MSPS)

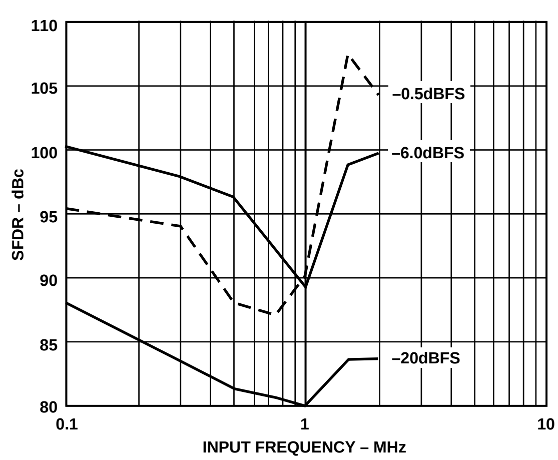


Figure 25. SFDR vs. Input Frequency (f_{CLOCK} = 20 MSPS)

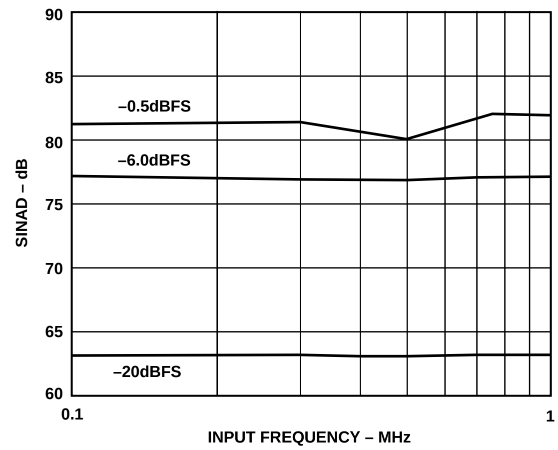


Figure 26. SINAD vs. Input Frequency (f_{CLOCK} = 10 MSPS)

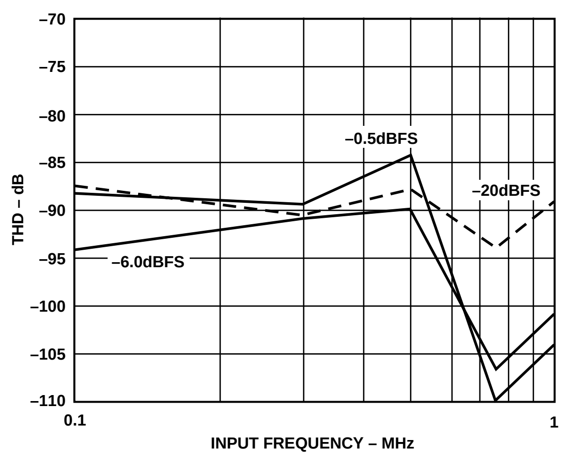


Figure 27. THD vs. Input Frequency (f_{CLOCK} = 10 MSPS)

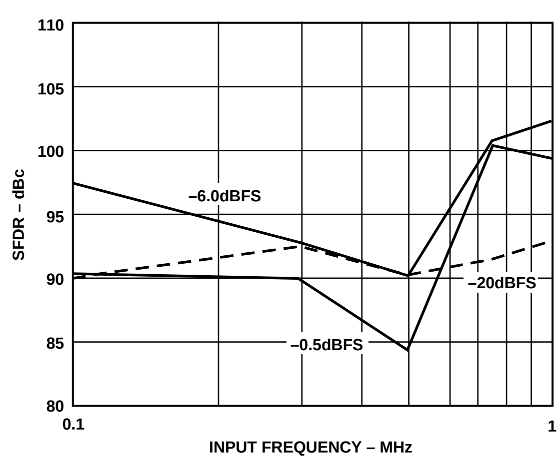


Figure 28. SFDR vs. Input Frequency (f_{CLOCK} = 10 MSPS)

Typical AC Characterization Curves for 2× Mode

(AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, Differential DC Coupled Input with CML = 2 V, Full Bias)

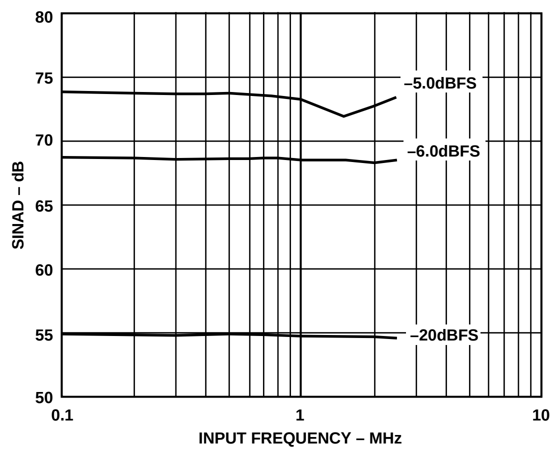


Figure 29. SINAD vs. Input Frequency (f_{CLOCK} = 20 MSPS)

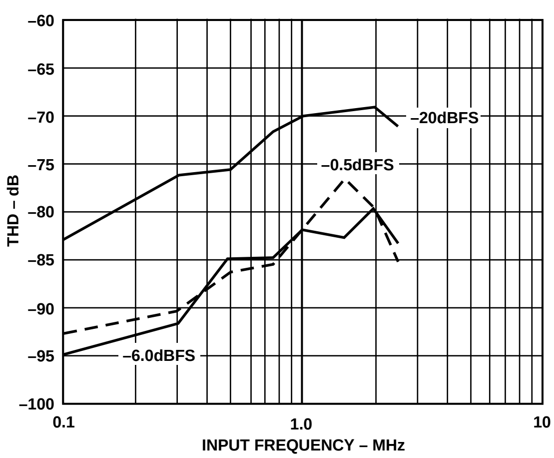


Figure 30. THD vs. Input Frequency (f_{CLOCK} = 20 MSPS)

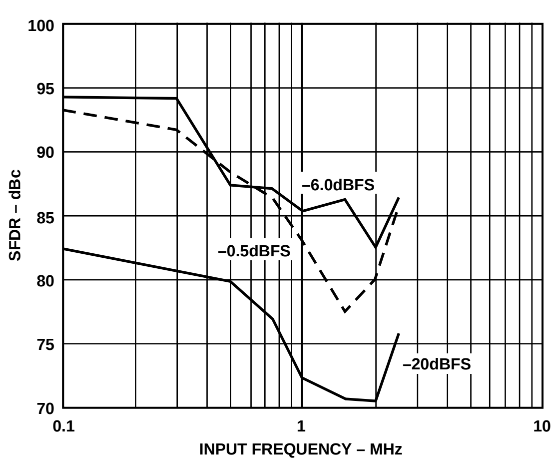


Figure 31. SFDR vs. Input Frequency (f_{CLOCK} = 20 MSPS)

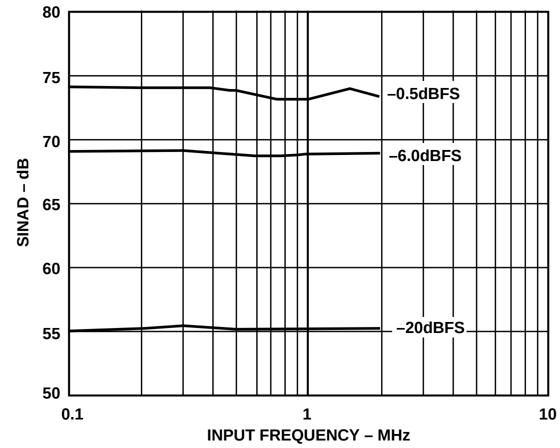


Figure 32. SINAD vs. Input Frequency (f_{CLOCK} = 10 MSPS)

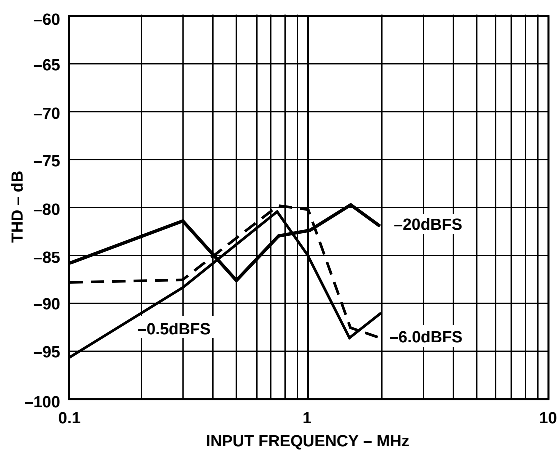


Figure 33. THD vs. Input Frequency (f_{CLOCK} = 10 MSPS)

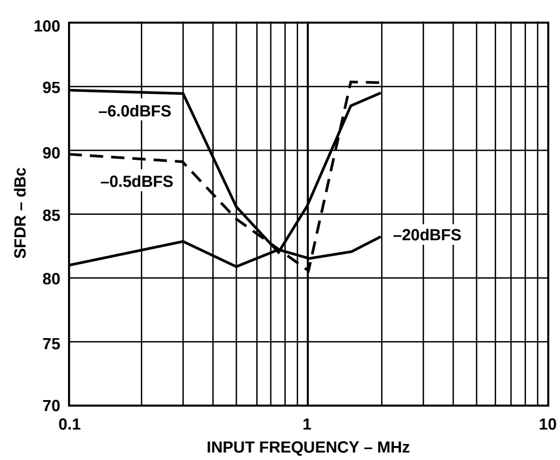


Figure 34. SFDR vs. Input Frequency (f_{CLOCK} = 10 MSPS)

Typical AC Characterization Curves for 1× Mode

(AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, Differential DC Coupled Input with CML = 2 V, Full Bias)

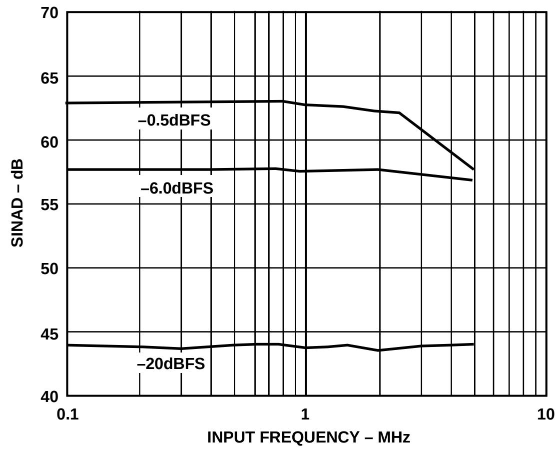


Figure 35. SINAD vs. Input Frequency (f_{CLOCK} = 20 MSPS)

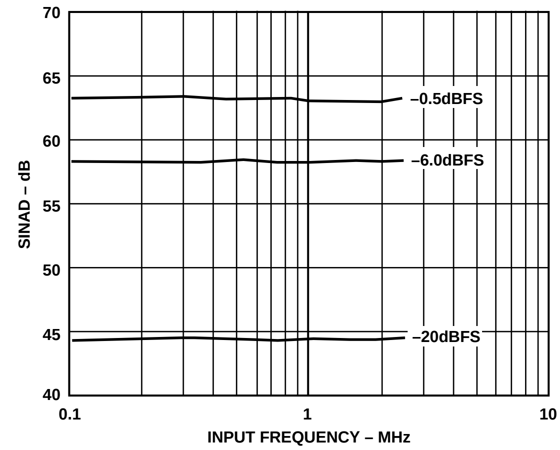


Figure 38. SINAD vs. Input Frequency (f_{CLOCK} = 10 MSPS)

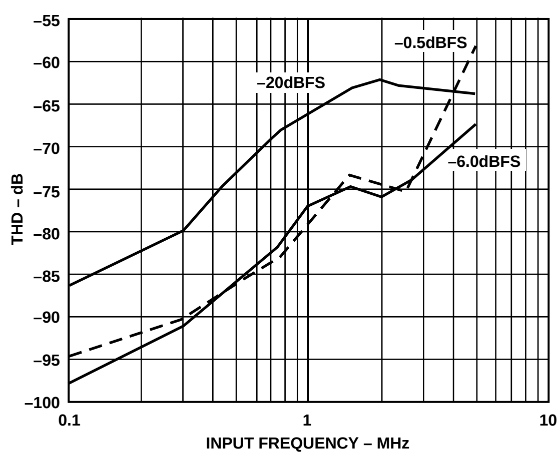


Figure 36. THD vs. Input Frequency (f_{CLOCK} = 20 MSPS)

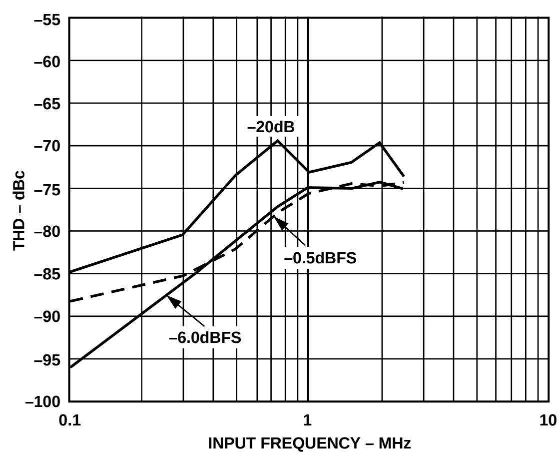


Figure 39. THD vs. Input Frequency (f_{CLOCK} = 10 MSPS)

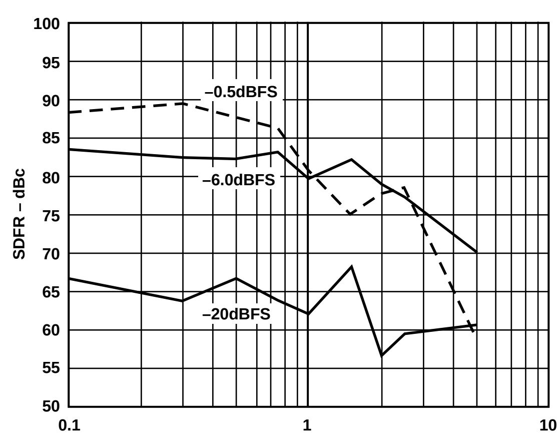


Figure 37. SFDR vs. Input Frequency (f_{CLOCK} = 20 MSPS)

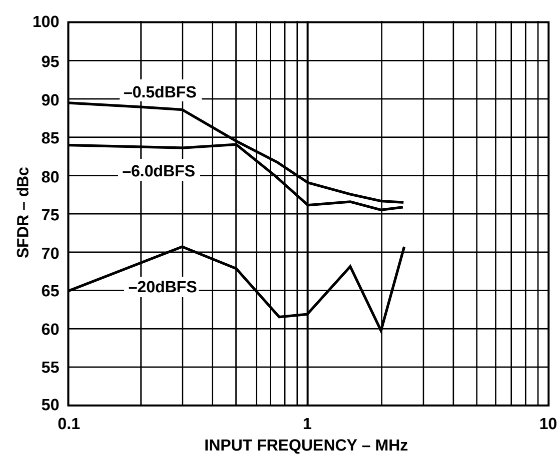


Figure 40. SFDR vs. Input Frequency (f_{CLOCK} = 10 MSPS)

Typical AC Characterization Curves

(AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, A_{IN} = –0.5 dBFS, Differential DC Coupled Input with CML = 2 V)

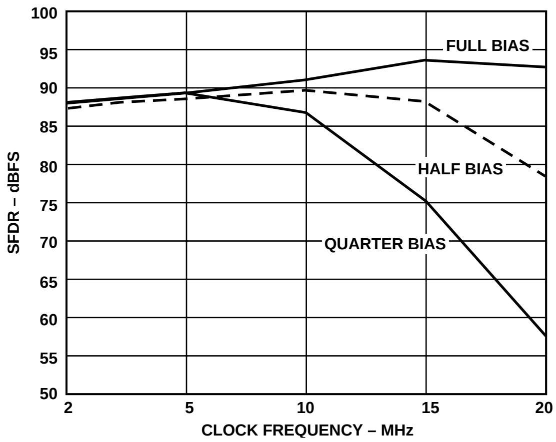


Figure 41. SFDR vs. Clock Rate (f_{IN} = 100 kHz in 8× Mode)

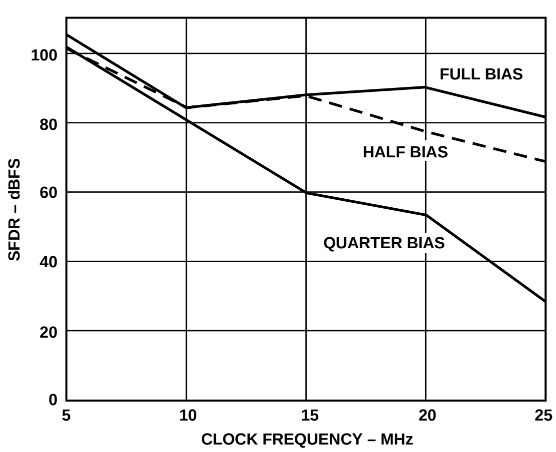


Figure 42. SFDR vs. Clock Rate (f_{IN} = 500 kHz in 4× Mode)

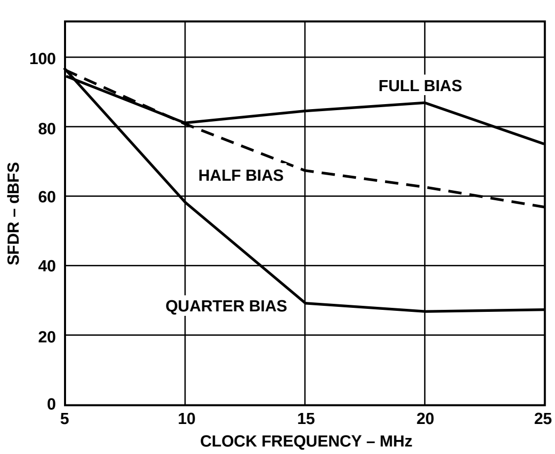


Figure 43. SFDR vs. Clock Rate (f_{IN} = 1.0 MHz in 2× Mode)

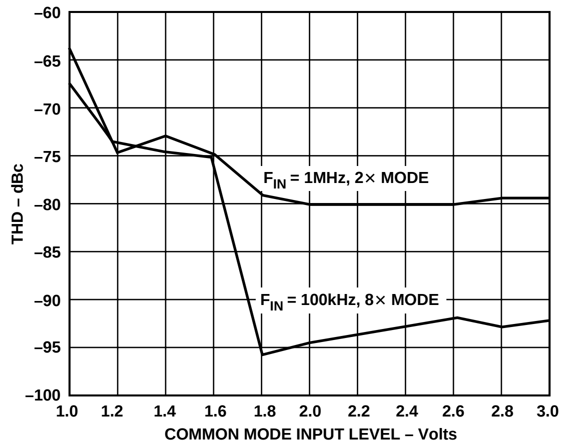


Figure 44. THD vs. Common-Mode Input Level (CML)

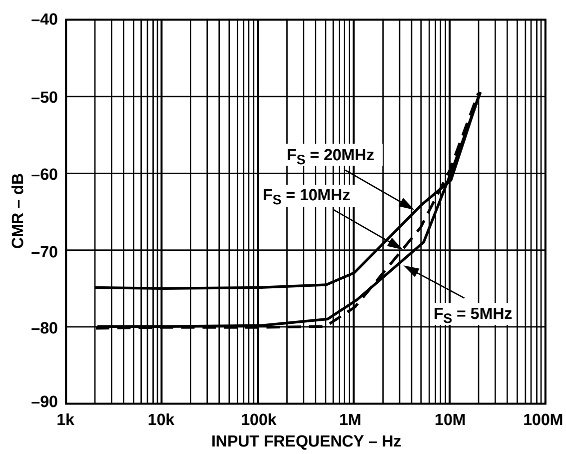


Figure 45. CMR vs. Input Frequency (V_{CML} = 2 V p-p, 1× Mode)

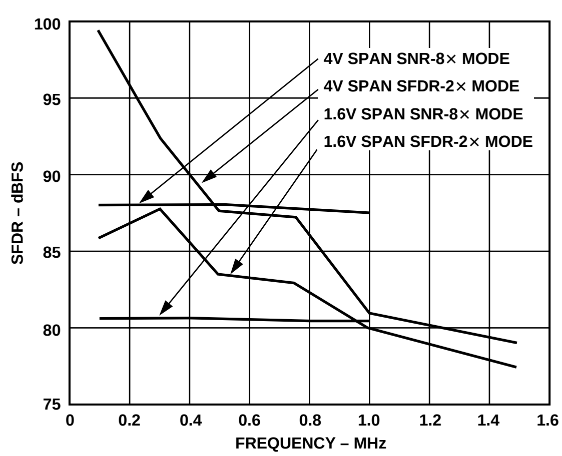


Figure 46. 4 V vs. 1.6 V Span SNR/SFDR (f_{CLOCK} = 20 MSPS)

Additional AC Characterization Curves

(AVDD = DVDD = DRVDD = +5 V, 4 V Input Span, A_{IN} = –0.5 dBFS, Differential DC Coupled Input with CML = 2 V, Full Bias, unless otherwise noted)

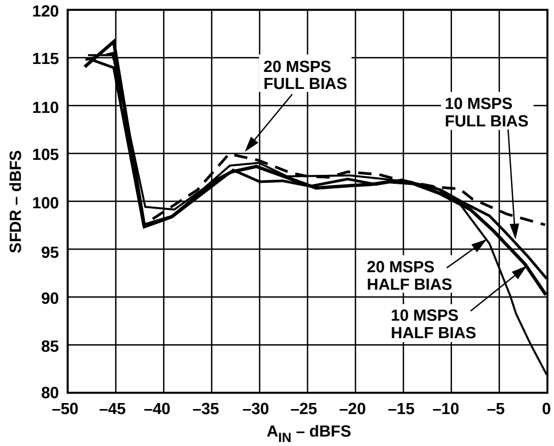


Figure 47. Single-Tone SFDR vs. Amplitude (f_{IN} =100 kHz, 8× Mode)

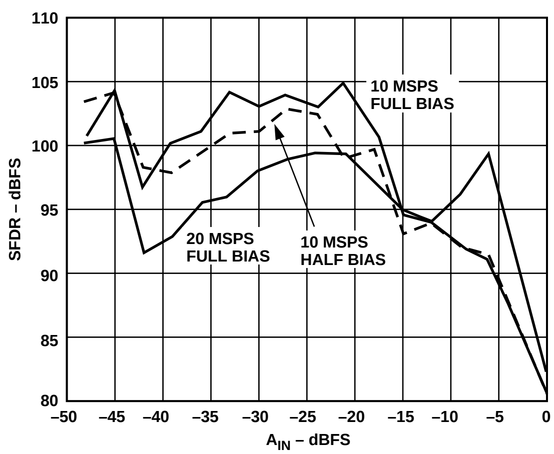


Figure 48. Single-Tone SFDR vs. Amplitude (f_{IN} =1.0 MHz, 2× Mode)

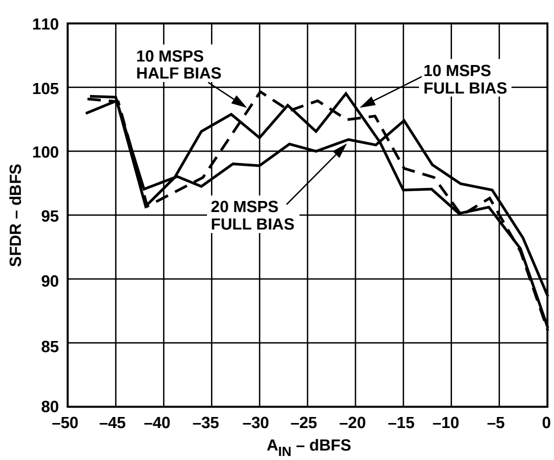


Figure 49. Single-Tone SFDR vs. Amplitude (f_{IN} = 500 kHz, 2× Mode)

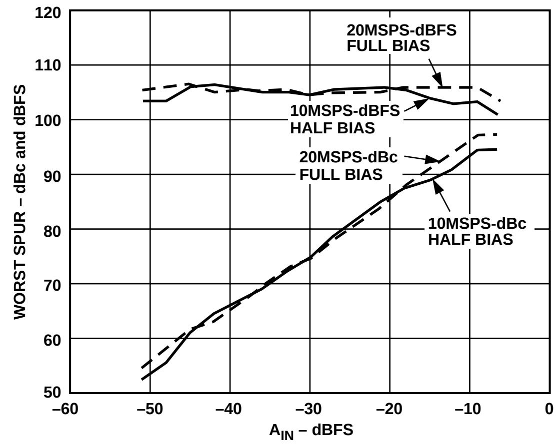


Figure 50. Two-Tone SFDR (F_1 = 475 kHz, F_2 = 525 MHz, 8× Mode)

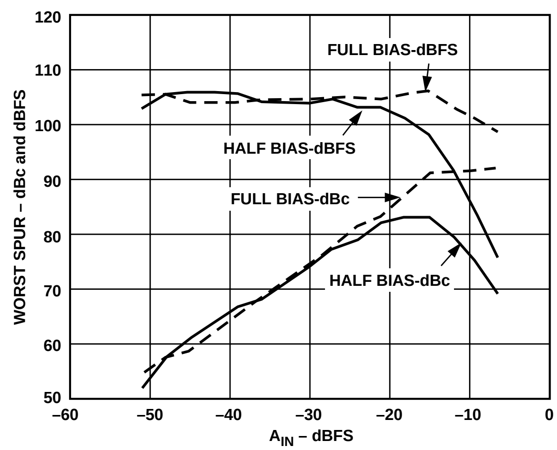


Figure 51. Two-Tone SFDR (F_1 = 0.95 kHz, F_2 = 1.05 MHz, 8× Mode 20 MSPS)

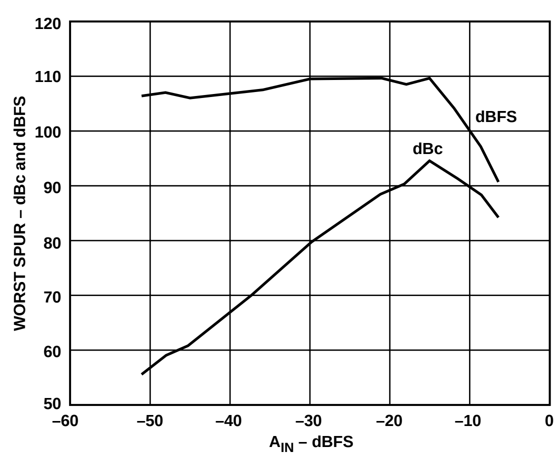


Figure 52. Two-Tone SFDR (F_1 = 1.9 MHz, F_2 = 2.1 MHz, 4× Mode 20 MSPS)

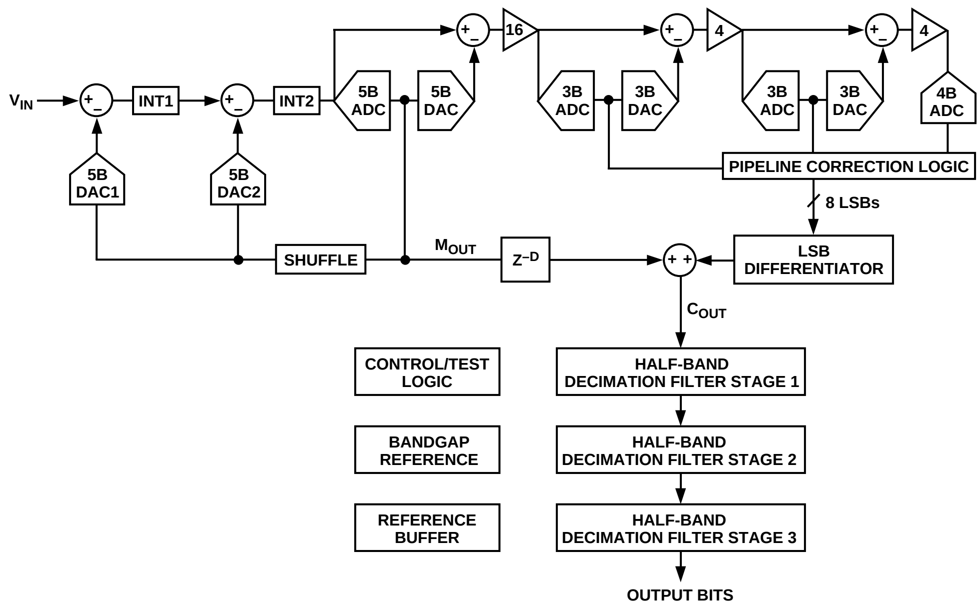


Figure 53. Simplified Block Diagram

THEORY OF OPERATION

The AD9260 utilizes a new analog-to-digital converter architecture to combine sigma-delta techniques with a high speed, pipelined A/D converter. This topology allows the AD9260 to offer the high dynamic range associated with sigma-delta converters while maintaining very wide input signal bandwidth (1.25 MHz) at a very modest 8× oversampling ratio. Figure 53 provides a block diagram of the AD9260. The differential analog input is fed into a second order, multibit sigma-delta modulator. This modulator features a 5-bit flash quantizer and 5-bit feedback. In addition, a 12-bit pipelined A/D quantizes the input to the 5-bit flash to greater accuracy. A special digital modulation loop combines the output of the 12-bit pipelined A/D with the delayed output of the 5-bit flash to produce the equivalent response of a second order loop with a 12-bit quantizer and 12-bit feedback. The combination of a second order loop and multibit feedback provides inherent stability: the AD9260 is not prone to idle tones or full-scale idiosyncracies sometimes associated with higher order single bit sigma-delta modulators.

The output of this 12-bit modulator is fed into the digital decimation filter. The voltage level on the MODE pin establishes the configuration for the digital filter. The user may bring the data out undecimated (at the clock rate), or at a decimation factor of 2×, 4×, or a full 8×. The spectra for these four cases are shown in Figures 5, 6, 7 and 8, all for a 100 kHz full-scale input and 20 MHz clock. The spectra of the undecimated output clearly shows the second order shaping characteristic of the quantization noise as it rises at frequencies above 1.25 MHz.

The on-chip decimation filter provides excellent stopband rejection to suppress any stray input signal between 1.25 MHz and 18.75 MHz, substantially easing the requirements on any anti-aliasing filter for the analog input path. The decimation filters are integrated with symmetric FIR filter structures, providing a linear phase response and excellent passband flatness.

The digital output driver register of the AD9260 features both READ and CHIP SELECT pins to allow easy interfacing. The digital supply of the AD9260 is designed to operate over a 2.7 V to 5.25 V supply range, though 3 V supplies are recommended to minimize digital noise on the board. A DATA AVAILABLE pin allows the user to easily synchronize to the converter's decimated output data rate. OUT-OF-RANGE (OTR) indication is given for an overflow in the pipelined A/D converter or digital filters. A RESETB function is provided to synchronize the converter's decimated data and clear any overflow condition in the analog integrators.

An on-chip reference and reference buffer are included on the AD9260. The reference can be configured in either a 2.5 V mode (providing a 4 V pk-pk differential input full scale), a 1 V mode (providing a 1.6 V pk-pk differential input full scale), or programmed with an external resistor divider to provide any voltage level between 1 V and 2.5 V. *However, optimum noise and distortion performance for the AD9260 can only be achieved with a 2.5 V reference as shown in Figure 46.*

For users wishing to operate the part at reduced clock frequencies, the bias current of the AD9260 is designed to be scalable. This scaling is accomplished through use of the proper external resistor tied to the BIAS pin: the power can be reduced roughly proportionately to clock frequency by as much as 75% (for clock rates of 5 MHz). Refer to Figures 41–43 and 47–51 for characterization curves showing performance tradeoffs.

ANALOG INPUT AND REFERENCE OVERVIEW

Figure 54, a simplified model of the AD9260, highlights the relationship between the analog inputs, VINA, VINB and the reference voltage VREF. Like the voltage applied to the top of the resistor ladder in a flash A/D converter, the value VREF defines the maximum input voltage to the A/D converter. An internal reference buffer in the AD9260 scales the reference voltage VREF before it is applied internally to the AD9260

A/D core. The scale factor of this reference buffer is 0.8. Consequently, the maximum input voltage to the A/D core is $+0.8 \times VREF$. The minimum input voltage to the A/D core is automatically defined to be $-0.8 \times VREF$. With this scale factor, the maximum differential input span of 4 V p-p is obtained with a VREF voltage of 2.5 V. A smaller differential input span may be obtained by using a VREF voltage of less than 2.5 V at the expense of ac performance (refer to Figure 46).

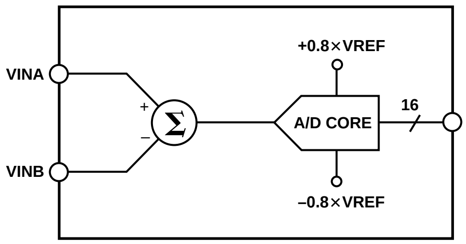


Figure 54. Simplified Input Model

INPUT SPAN

The AD9260 is implemented with a differential input structure. This structure allows the common-mode level (average voltage of the two input pins) of the input signal to be varied independently of the input span of the converter over a wide range, as shown in Figure 44. Specifically, the input to the A/D core is the difference of the voltages applied at the VINA and VINB input pins. Therefore, the equation,

$$VCORE = VINA - VINB \tag{1}$$

defines the output of the differential input stage and provides the input to the A/D core.

The voltage, *VCORE*, must satisfy the condition,

$$-0.8 \times VREF \leq VCORE \leq +0.8 \times VREF \tag{2}$$

where *VREF* is the voltage at the VREF pin.

INPUT COMPLIANCE RANGE

In addition to the limitations on the differential span of the input signal indicated in Equation 2, an additional limitation is placed on the inputs by the analog input structure of the AD9260. The analog input structure bounds the valid operating range for VINA and VINB. The condition,

$$\begin{aligned} AVSS + 0.5\ V < VINA < AVDD - 0.5\ V \\ AVSS + 0.5\ V < VINB < AVDD + 0.5\ V \end{aligned} \tag{3}$$

where *AVSS* is nominally 0 V and *AVDD* is nominally +5 V, defines this requirement. Thus the valid inputs for *VINA* and *VINB* are any combination that satisfies both Equations 2 and 3. Note, the clock clamping method used in the differential driver circuit shown in Figure 57 is sufficient for protecting the AD9260 in an undervoltage condition.

For additional information showing the relationships between VINA, VINB, VREF and the digital output of the AD9260, see Table V.

Refer to Table IV for a summary of the various analog input and reference configurations.

ANALOG INPUT OPERATION

The analog input structure of the AD9260 is optimized to meet the performance requirements for some of the most demanding communication and data acquisition applications. This input structure is composed of a switched-capacitor network that samples the input signal applied to pins VINA and VINB on every rising edge of the CLK pin. The input switched capacitors are charged to the input voltage during each period of CLK. The resulting charge, q, on these capacitors is equal to $C \times V_{IN}$, where C is the input capacitor. The change in charge on these capacitors, delta q, as the capacitors are charged from a previous sample of the input signal to the next sample, is approximated in the following equation,

$$delta\ q \sim C \times delta V_N = C \times (V_N - V_{N-2}) \tag{4}$$

where V_N represents the present sample of the input signal and V_{N-2} represents the sample taken two clock cycles earlier. The average current flow into the input (provided from an external source) is given in the following equation,

$$I = delta\ q/T \sim C \times (V_N - V_{N-2}) \times f_{CLOCK} \tag{5}$$

where T represents the period of CLK and f_{CLOCK} represents the frequency of CLK. Equations 4 and 5 provide simplifying approximations of the operation of the analog input structure of the AD9260. A more exact, detailed description and analysis of the input operation is provided below.

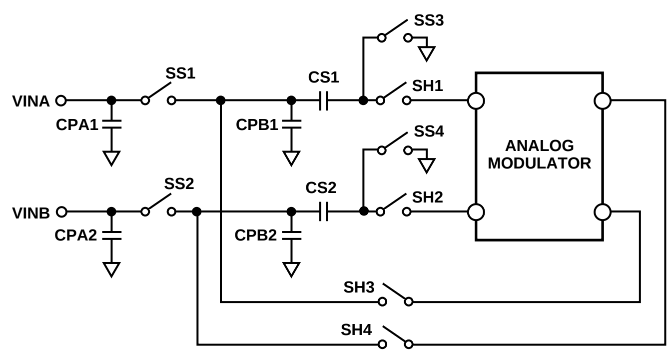


Figure 55. Detailed Analog Input Structure

Figure 55 illustrates the analog input structure of the AD9260. For the moment, ignore the presence of the parasitic capacitors CPA and CPB. The effects of these parasitic capacitors will be discussed near the end of this section. The switched capacitors, CS1 and CS2, sample the input voltages applied on pins VINA and VINB. These capacitors are connected to input pins VINA and VINB when CLK is low. When CLK rises, a sample of the input signal is taken on capacitors CS1 and CS2. When CLK is high, capacitors CS1 and CS2 are connected to the Analog Modulator. The modulator precharges capacitors CS1 and CS2 to minimize the amount of charge required from any circuit used in combination with the AD9260 to drive input pins VINA and VINB. This reduces the input drive requirements of the analog circuitry driving pins VINA and VINB. The Analog Modulator precharges the voltages across capacitors CS1 and CS2, approximately equal to a delayed version of the input signal. When capacitors CS1 and CS2 are connected to input pins VINA and VINB, the differential charge, Q(n), on these capacitors is given in the following equation,

$$Q(n) = q1 - q2 = CS \times VCORE \tag{6}$$

where $q1$ and $q2$ are the individual charges stored on capacitors CS1 and CS2 respectively, and CS is the capacitance value of CS1 and CS2. When capacitors CS1 and CS2 are connected to the Analog Modulator during the preceding "precharge" clock phase, the capacitors are precharged equal to an approximation of a previous sample of the input signal. Consequently the differential charge on these capacitors while CLK is high is given in the following equation,

$$Q(n-1) = CS \times VCORE(delay) + CS \times Vdelta \tag{7}$$

where $VCORE(delay)$ is the value of VCORE sampled during a previous period of CLK, and $Vdelta$ is the sigma-delta error voltage left on the capacitors. Vdelta is a natural artifact of the sigma-delta feedback techniques utilized in the Analog Modulator of the AD9260. It is a small random voltage term that changes every clock period and varies from 0 to $\pm 0.05 \times$ VREF.

The analog circuitry used to drive the input pins of the AD9260 must respond to the charge glitch that occurs when capacitors CS1 and CS2 are connected to input pins VINA and VINB. This circuitry must provide additional charge, qdelta, to capacitors CS1 and CS2, which is the difference between the precharged value, Q(n–1), and the new value, Q(n), as given in the following equation,

$$Qdelta = Q(n) - Q(n-1) \tag{8}$$

$$Qdelta = CS \times [VCORE - VCORE(delay) + Vdelta] \tag{9}$$

DRIVING THE INPUT

Transient Response

The charge glitch occurs once at the beginning of every period of the input CLK (falling edge), and the sample is taken on capacitors CS1 and CS2 exactly one-half period later (rising edge). Figure 56 presents a typical input waveform applied to input Pins VINA and VINB of the AD9260.

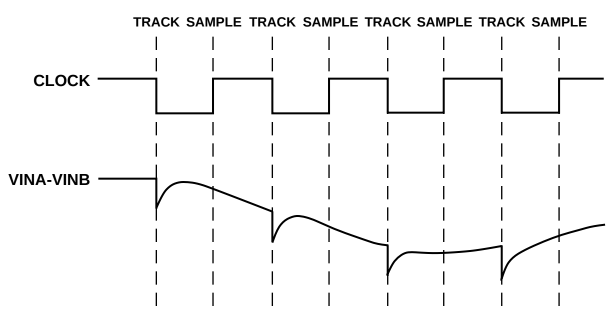


Figure 56. Typical Input Waveform

Figure 56 illustrates the effect of the charge glitch when a source with nonzero output impedance is used to drive the input pins. This source must be capable of settling from the charge glitch in one-half period of the CLK. Unfortunately, the MOS switches used in any CMOS-switched capacitor circuit (including those in the AD9260) include nonlinear parasitic junction capacitances connected to their terminals. Figure 55 also illustrates the parasitic capacitances, Cpa1, Cpb1, Cpa2 and Cpb2, associated with the input switches.

Parasitic capacitor Cpa1 and Cpa2 are always connected to Pins VINA and VINB and therefore do not contribute to the glitch energy. Parasitic capacitors Cpb1 and Cpb2, on the other hand, cause a charge glitch that adds to that of input capacitors CS1 and CS2 when they are connected to input Pins VINA and VINB. The nonlinear junction capacitance of Cpb1 and Cpb2 cause charge glitch energy that is nonlinearly related to the input signal. Therefore, linear settling is difficult to achieve unless the input source completely settles during one-half period of CLK. A portion of the glitch impulse energy "kicked" back at the source is not linearly related to the input signal. Therefore, the best way to ensure that the input signal settles linearly is to use wide bandwidth circuitry, which settles as completely as possible from the glitch during one-half period of the CLK.

The AD9260 utilizes a proprietary clock-boosted boot-strapping technique to reduce the nonlinear parasitic capacitances of the internal CMOS switches. This technique improves the linearity of the input switches and reduces the nonlinear parasitic capacitance. Thus, this technique reduces the nonlinear glitch energy. The capacitance values for the input capacitors and parasitic capacitors for the input structure of the AD9260, as illustrated in Figure 55, are listed as follows.

CS = 3.2 pF, Cpa = 6 pF, Cpb = 1 pF (where CS is the capacitance value of capacitors CS1 and CS2, Cpa is the value of capacitors Cpa1 and Cpa2, and Cpb is the value of capacitors Cpb1 and Cpb2). The total capacitance at each input pin is C_{IN} = CS + Cpa + Cpb = 10.2 pF.

Input Driver Considerations

The optimum noise and distortion performance of the AD9260 can ONLY be achieved when the AD9260 is driven differentially with a 4 V input span . Since not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion. In the case of the AD9260, a single-ended-to-differential conversion is best realized using a differential op amp driver. Although a transformer will perform a similar function for ac signals, its usefulness is precluded by its inability to directly drive the AD9260 and thus the additional requirement of an active low noise, low distortion buffer stage.

Single-Ended to Differential Op Amp Driver

There are two particular single-ended-to-differential op amp driver circuits useful for driving the AD9260. The first driver circuit shown in Figure 57 is optimized for dc coupling applications requiring optimum distortion performance. This differential op amp driver circuit is configured to convert and level shift a 2 V p-p single-ended, ground referenced signal to a 4 V p-p differential signal centered at the common-mode level of the AD9260. The circuit is based on two op amps which are configured as matched unity gain difference amplifiers. The single-ended input signal is applied to opposing inputs of the difference amplifiers, thus providing differential outputs. The common-mode offset voltage is applied to the noninverting resistor leg of each difference amplifier providing the required offset voltage. This offset voltage is derived from the common-mode level (CML) pin of the AD9260 via a low output impedance buffer amplifier capable of driving a 1 μF capacitive load. The common-mode offset can be varied over a 1.8 V to 2.5 V span without any serious degradation in distortion performance as shown in Figure 44, thus providing some flexibility in improving output compression distortion from some ±5 op amps with limited positive voltage swing.

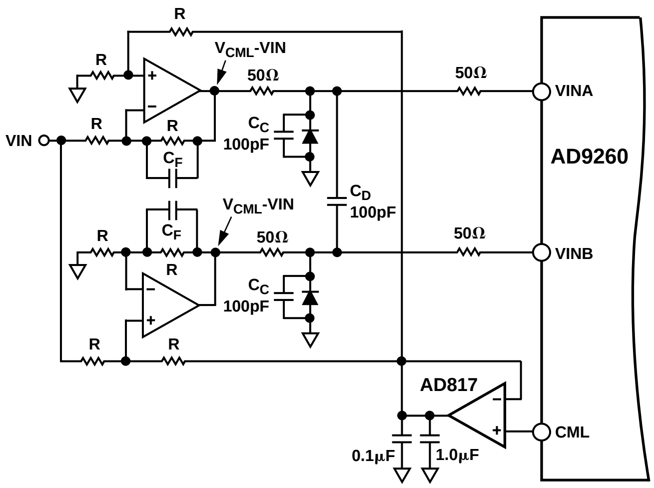


Figure 57. DC-Coupled Differential Driver with Level-Shifting

To protect the AD9260 from an undervoltage fault condition from op amps specified for ±5 V operation, two 50 Ω series resistors and a diode to AGND are inserted between each op amp output and the AD9260 inputs. The AD9260 will inherently be protected against any overvoltage condition if the op amps share the same positive power supply (i.e., AVDD) as the AD9260. Note, the gain accuracy and common-mode rejection of each difference amplifier in this driver circuit can be enhanced by using a matched thin-film resistor network (i.e., Ohmtek ORNA5000F) for the op amps. Resistor values should be 500 Ω or less to maintain the lowest possible noise. Recall, the AD9260's small signal bandwidth is 75 MHz, hence any noise falling within the baseband bandwidth of the AD9260 defined by its sample and decimation rate, as well as "images" of its baseband response occurring at multiples of the sample rate, will degrade its overall noise performance.

The noise performance of each unity gain differential driver circuit is limited by its inherent noise gain of two. For unity gain op amps ONLY, the noise gain can be reduced from two to one beyond the input signals passband by adding a shunt capacitor, C_F, across each op amp's feedback resistor. This will essentially establish a low-pass filter which reduces the noise gain to one beyond the filter's $f_{-3\ dB}$ while simultaneously bandlimiting the input signal to $f_{-3\ dB}$. Note, the pole established by this filter can also be used as the real pole of an antialiasing filter. Since the noise contribution of two op amps from the same product family are typically equal but uncorrelated, the total output-referred noise of each op amp will add root-sum square leading to a further 3 dB degradation in the circuit's noise performance. Further out-of-band noise reduction can be realized with the addition of single-ended and differential capacitors, C_S and C_D.

The distortion and noise performance of the two op amps within the signal path are critical in achieving the AD9260's optimum performance. Low noise op amps capable of providing greater than 85 dB THD at 1 MHz while swinging over a 1 V to 3 V range are a rare commodity, yet should only be considered. The AD9632 op amp was found to provide superb distortion performance in this circuit due to its ability to maintain excellent distortion performance over a wide bandwidth while swinging over a 1 V to 3 V range. Since the AD9632 is gain-of-two or greater stable, the use of the noise reduction shunt capacitors discussed above was prohibited thus degrading its noise performance slightly (1 dB–2 dB) when compared to the OPA642. A lower cost and lower power unity gain alternative is the AD8056 dual op amp which only exhibited a slight degradation (i.e., 1 dB–2 dB) in SNR and THD performance for full-scale input signals. For the lowest possible noise performance while maintaining excellent distortion performance, the unity gain OPA642 should be considered. Note, the majority of the AD9260 test and characterization data presented in this data sheet was taken using the AD9632 op amp in this dc coupled driver circuit. This driver circuit is also provided on the AD9260 evaluation board.

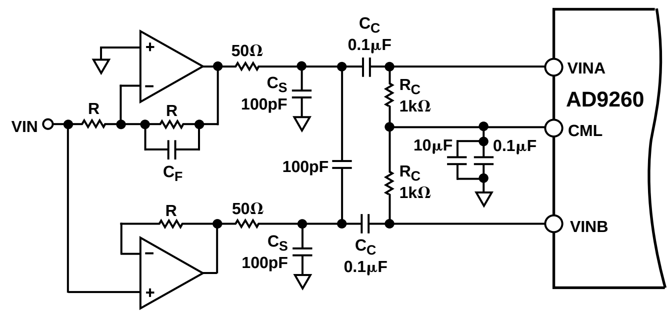


Figure 58. AC Coupled, Low Noise Differential Driver

The lowest possible noise and distortion performance can be achieved using an ac coupled circuit shown in Figure 58. The circuit simply consists of two low noise, high speed op amps configured as an inverting gain of one and a unity gain buffer. In this configuration, the noise performance is dominated by the inverting op amp topology due to its noise gain of two. Excellent distortion is achieved due to both op amps' outputs being centered around AGND. The group delay mismatch between the inverting and noninverting op amps caused only a slight degradation in the distortion performance of this circuit using the recommended wide bandwidth, low distortion op amps.

Table IV. Reference Configuration Summary

Reference Operating Mode	Input Span (VINA–VINB) (V p-p)	Required VREF (V)	Connect	To
INTERNAL	1.6	1	SENSE	VREF
INTERNAL	4.0	2.5	SENSE	REFCOM
INTERNAL	1.6 ≤ SPAN ≤ 4.0 and	1 ≤ VREF ≤ 2.5 and	R1	VREF and SENSE
	SPAN = 1.6 × VREF	VREF = (1+R1/R2)	R2	SENSE and REFCOM
EXTERNAL	1.6 ≤ SPAN ≤ 4.0	1 ≤ VREF ≤ 2.5	SENSE	AVDD
			VREF	EXT. REF.

The outputs of each op amp are ac coupled via a small series resistor and capacitor (i.e., 50 Ω and 0.1 µF) to the respective inputs of the AD9260. Similar to the dc coupled driver, further out-of-band noise reduction can be realized with the addition of 100 pF single-ended and differential capacitors, C_S and C_D. The lower-cutoff frequency of this ac coupled circuit is determined by R_C and C_C in which R_C is tied to the common-mode level pin, CML, of the AD9260 for proper biasing of the inputs. Although the OPA642 was found to provide the lowest overall noise and distortion performance (i.e., 88.8 dB and 96 dB THD @ 100 kHz), the AD8055 (or dual AD8056) suffered only a 0.5 dB to 1.5 dB degradation in overall performance. It is worth noting that given the high-level of performance attainable by the AD9260, special consideration must be given to both the quality of the test equipment and test setup in its evaluation.

Common-Mode Level

The CML pin is an internal analog bias point used internally by the AD9260. This pin must be decoupled to analog ground with at least a 0.1 µF capacitor as shown in Figure 59. The dc level of CML is approximately AVDD/2.5. This voltage should be buffered if it is to be used for any external biasing.

Note: the common-mode voltage of the input signal applied to the AD9260 need not be at the exact same level as CML. While this level is recommended for optimal performance, the AD9260 is tolerant of a range of input common-mode voltages around AVDD/2.5.

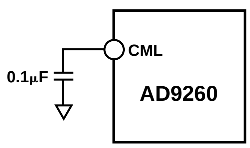


Figure 59. CML Decoupling

REFERENCE OPERATION

The AD9260 contains an onboard bandgap reference and internal reference buffer amplifier. The onboard reference provides a pin-strappable option to generate either a 1 V or 2.5 V output. With the addition of two external resistors, the user can generate reference voltages other than 1 V and 2.5 V. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance. See Table IV for a summary of the pin-strapping options for the AD9260 reference configurations. *Note, the optimum noise and distortion can only be achieved with a 2.5 V reference.*

Figure 60 shows a simplified model of the internal voltage reference of the AD9260. A pin-strappable reference amplifier buffers a 1 V fixed reference. The output from the reference amplifier, A1, appears on the VREF pin and MUST be decoupled with 0.1 µF and 10 µF capacitor to REFCOM. The voltage on the VREF pin determines the full-scale input span of the A/D. This input span equals:

$$\textit{Full-Scale Input Span} = 1.6 \times \textit{VREF}$$

The voltage appearing at the VREF pin, as well as the state of the internal reference amplifier, A1, are determined by the voltage appearing at the SENSE pin. The logic circuitry contains two comparators that monitor the voltage at the SENSE pin. The comparator with the lowest set point (approximately 0.3 V) controls the position of the switch within the feedback path of A1. If the SENSE pin is tied to REFCOM, the switch is connected to the internal resistor network, thus providing a VREF of 2.5 V. If the SENSE pin is tied to the VREF pin via a short or resistor, the switch is connected to the SENSE pin. A short will provide a VREF of 1.0 V while an external resistor network will provide an alternative VREF SPAN between 1.0 V and 2.5 V. The external resistor network may, for example, be implemented as a resistor divider circuit. This divider circuit could consist of a resistor (R1) connected between VREF and SENSE and another resistor (R2) connected between SENSE and REFCOM. The other comparator controls internal circuitry that will disable the reference amplifier if the SENSE pin is tied to AVDD. Disabling the reference amplifier allows the VREF pin to be driven by an external voltage reference.

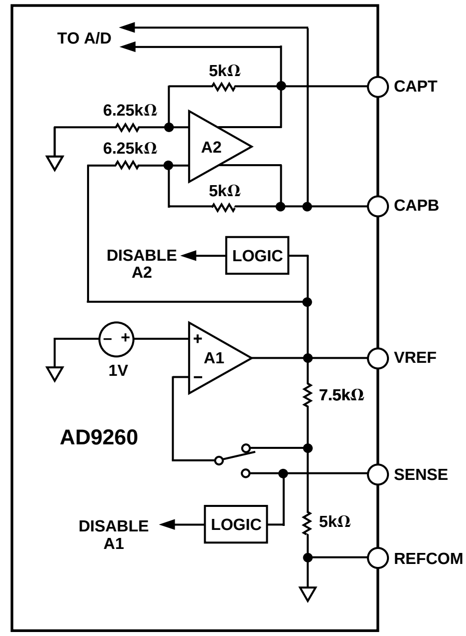


Figure 60. Simplified Reference

The reference buffer circuit, level shifts the reference to an appropriate common-mode voltage for use by the internal circuitry. The on-chip buffer provides the low impedance necessary for driving the internal switched capacitor circuits and eliminates the need for an external buffer op amp.

The actual reference voltages used by the internal circuitry of the AD9260 appear on the CAPT and CAPB pins. If VREF is configured for 2.5 V, thus providing a 4 V full-scale input span, the voltages appear at CAPT and CAPB are 3.0 V and 1.0 V respectively. For proper operation when using the internal or an external reference, it is necessary to add a capacitor network to decouple the CAPT and CAPB pins. Figure 61 shows the recommended decoupling network. This capacitive network performs the following three functions: (1) along with the reference amplifier, A2, it provides a low source impedance over a large frequency range to drive the A/D internal circuitry, (2) it provides the necessary compensation for A2, and (3) it bandlimits the noise contribution from the reference. The turn-on time of the reference voltage appearing between CAPT and CAPB is approximately 15 ms and should be evaluated in any power-down mode of operation.

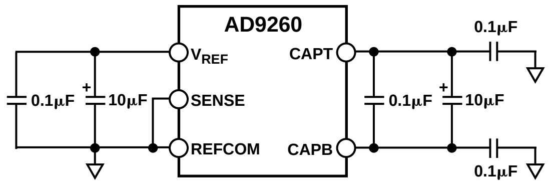


Figure 61. Recommended Reference Decoupling Network

DIGITAL INPUTS AND OUTPUTS

Digital Outputs

The AD9260 output data is presented in a twos complement format. Table V indicates the output data formats for various input ranges and decimation modes. A straight binary output data format can be created by inverting the MSB.

Table V. Output Data Format

Input (V)	Condition (V)	Digital Output
8× Decimation Mode		
VINA–VINB	< –0.8 × VREF	1000 0000 0000 0000
VINA–VINB	= –0.8 × VREF	1000 0000 0000 0000
VINA–VINB	= 0	0000 0000 0000 0000
VINA–VINB	= +0.8 × VREF – 1 LSB	0111 1111 1111 1111
VINA–VINB	>= + 0.8 × VREF	0111 1111 1111 1111
4× Decimation Mode		
VINA–VINB	< –0.825 × VREF	1000 0001 0001 1100
VINA–VINB	= –0.825 × VREF	1000 0001 0000 1100
VINA–VINB	= 0	0000 0000 0000 0000
VINA–VINB	= +0.825 × VREF – 1 LSB	0111 1110 1110 0011
VINA–VINB	>= + 0.825 × VREF	0111 1110 1110 0011
2× Decimation Mode		
VINA–VINB	< –0.825 × VREF	1000 0000 0100 0001
VINA–VINB	= –0.825 × VREF	1000 0000 0100 0001
VINA–VINB	= 0	0000 0000 0000 0000
VINA–VINB	= +0.825 × VREF – 1 LSB	0111 1111 1011 1110
VINA–VINB	>= + 0.825 × VREF	0111 1111 1011 1110

The slight different ± full-scale input voltage conditions and their corresponding digital output code for the 4× and 2× decimation modes can be attributed to the different digital scaling factors applied to each of the AD9260's FIR decimation stages for filter optimization purposes. Thus, a + full-scale reading of 0111 1111 1111 1111 and – full-scale reading of 1000 0000 0000 0000 is unachievable in the 2× and 4× decimation mode. As a result, a digital overrange condition can never exist in the 2× and 4× decimation mode and thus OTR being set high indicates an overrange condition in the analog modulator.

The output data format in 1× decimation differs from that in 2×, 4× and 8× decimation modes. In 1× decimation mode the output data remains in a twos complement format, but the digital numbers are scaled by a factor of 7/128. This factor of 7/128 is the product of an internal scale factor of 7/8 in the analog modulator and a 1/16 scale factor caused by LSB justification of the 12-bit modulator data.

$\overline{\text{CS}}$ AND READ PINS

The $\overline{\text{CS}}$ and READ pins control the state of the output data pins (Bit 1–Bit 16) on the AD9260. The $\overline{\text{CS}}$ pin is active low and the READ pin is active high. When $\overline{\text{CS}}$ and READ are both active the ADC data is driven on the output data pins, otherwise the output data pins are in a high impedance (Hi-Z) state. Table VI indicates the relationship between the $\overline{\text{CS}}$ and READ pins and the state of Pins Bit 1–Bit 16.

Table VI. $\overline{\text{CS}}$ and READ Pin Functionality

$\overline{\text{CS}}$	READ	Condition of Data Output Pins
Low	Low	Data Output Pins in Hi-Z State
Low	High	ADC Data on Output Pins
High	Low	Data Output Pins in Hi-Z State
High	High	Data Output Pins in Hi-Z State

DAV PIN

The DAV pin indicates when the output data of the AD9260 is valid. Digital output data is updated on the rising edge of DAV. The data hold time (t_H) is dependent on the external loading of DAV and the digital data output pins (BIT1–BIT16) as well as the particular decimation mode. The internal DAV driver is sized to be larger than the drivers pertaining to the digital data outputs to ensure that rising edge of DAV occurs before the data transitions under similar loading conditions (i.e., fanout) regardless of mode. Note that minimum data hold (t_H) of 3.5 ns is specified in the Figure 4 timing diagram from the 50% point of DAV's rising edge to the 50% of data transition using a capacitive load of 20 pF for DAV and BIT1–BIT16. Applications interfacing to TTL logic and/or having larger capacitive loading for DAV than BIT1–BIT16 should consider latching data on the falling edge of DAV since the falling edge of DAV occurs well after the data has transitioned in the case of the 2×, 4× and 8× modes. The duty cycle of DAV is approximately 50% and it remains active independent of $\overline{\text{CS}}$ and READ.

$\overline{\text{RESET}}$ PIN

The $\overline{\text{RESET}}$ pin is an asynchronous digital input that is active low. Upon asserting $\overline{\text{RESET}}$ low, the clocks in the digital decimation filters are disabled, the DAV pin goes low and the data on the digital output data pins (Bit 1–Bit 16) is invalid. In addition, the analog modulator in the AD9260 and internal clock dividers used in the decimation filters are reset and will remain reset as long as $\overline{\text{RESET}}$ is maintained low. In the 2×, 4×, or 8× mode, the $\overline{\text{RESET}}$ must remain low for at least a clock period to ensure all the clock dividers and analog modulator are reset. Upon bringing $\overline{\text{RESET}}$ high, the internal clock dividers will begin to count again on the next rising edge of CLK.

The state of the internal decimation filters in the AD9260 remains unchanged when $\overline{\text{RESET}}$ is asserted low. Consequently, when $\overline{\text{RESET}}$ is pulsed low, this resets the analog modulator but does not clear all the data in the digital filters. The data in the filters is corrupted by the effect of resetting the analog modulator (this causes an abrupt change at the input of the digital filter and this change is unrelated to the signal at the input of the A/D converter). For this reason, following a pulse on the $\overline{\text{RESET}}$ pin, the decimation filters must be flushed of their data. These filters have a memory length, hence delay, equal to the number of filter taps times the clock rate of the converter. This memory length may be interpreted in terms of a number of samples stored in the decimation filter. For example, if the part is in 8× decimation mode, the delay is 321/f_{CLOCK}. This corresponds to 321 samples stored in the decimation filter. These 321 samples must be flushed from the AD9260 after $\overline{\text{RESET}}$ is pulsed high prior to reusing the data from the AD9260. That is, the AD9260 should be allowed to clock for 321 samples as the corrupted data is flushed from the filters. If the part is in 4× or 2× decimation mode, then the relatively smaller group delays of the 4× and 2× decimation filters result fewer samples that must be flushed from the filters (108 sample- and 23 samples respectively)

In 2×, 4× or 8× mode, $\overline{\text{RESET}}$ may be used to synchroniz multiple AD9260s clocked with the same clock. The decimatio filters in the AD9260 are clocked with an internal clock divider The state of this clock divider determines when the output dat becomes available (relative to CLK). In order to synchroniz multiple AD9260s clocked with the same clock, it is necessar that the clock dividers in each of the individual AD9260s ar all reset to the same state. When $\overline{\text{RESET}}$ is asserted low, thes clock dividers are cleared. On the next falling edge of CLK following the rising edge of $\overline{\text{RESET}}$, the clock dividers begin countin and the clock is applied to the digital decimation filters

OTR PI

The OTR pin is a synchronous output that is updated eac CLK period. It indicates that an overrange condition has occurred within the AD9260. Ideally, OTR should be latched o the falling edge of CLK to ensure proper setup-and-hold time However, since an overrange condition typically extends wel beyond one clock cycle (i.e., does not toggle at the CLK rate) OTR typically remains high for more than a clock cycle, allowing it to be successfully detected on the rising edge of CL or monitored asynchronou

ly. An overrange condition must be carefully handled becaus of the group delays in the low-pass digital decimation filters in the output stages of the AD9260. When the input signal exc eds the full-scale range of the converter, this can have a variet of effects upon the operation of the AD9260, depending on the duration and amplitude of this overrange condition. A s ort duration overrange condition (<< filter group delay) may c use the analog modulator to briefly overrange without causing the data in the low pass digital filters to exceed full scale. The analog modulator is actually capable of processing signals slig tly (3%) beyond the full-scale range of the AD9260 without internally clipping. A long duration overrange condition will c use the digital filter data to exceed full scale. For this reason, the OTR signal is generated using two separate internal out -of-range detect

rs. The first of these out-of-range detectors is placed at the ou put of the analog modulator and indicates whether the modul tor output signal has extended 3% beyond the full-scale rang of the converter. If the modulator output signal exceeds 3%- beyond full scale, the digital data is hard-limited (i.e., clipped) o a number that is 3% larger than full scale. Due to the delay of the switched capacitor analog modulator, the OTR signal is del yed 3 1/2 clock cycles relative to the clock edge in which the o er- ranged analog input signal was samp

ed. The second out-of-range detector is placed at the output of the stage three decimation filter and detects whether the low ass filtered data has exceeded full scale. When this occurs, the fi ter output data is hard limited to full scale. The OTR signal s a logical OR function of the signals from these two internal out-of-range detectors. If either of these detectors produces an out-of-range signal, the OTR pin goes high and the data ma be seriously corrupt

If the AD9260 is used in a system that incorporates automatic gain control (AGC), the OTR signal may be used to indicate that the signal amplitude should be reduced. This may be particularly effective for use in maximizing the signal dynamic range if the signal includes high frequency components that occasionally exceed full scale by a small amount. If, on the other hand, the signal includes large amplitude low frequency components that cause the digital filters to overrange, this may cause the low pass digital filter to overrange. In this case the data may become seriously corrupted and the digital filters may need to be flushed. See the $\overline{\text{RESET}}$ pin function description above for an explanation of the requirements for flushing the digital filters.

OTR should be sampled with the falling edge of CLK. This signal is invalid while CLK is HIGH.

MODE OPERATION

The Mode Select Pin (MODE) allows the user to select one of four available digital filter modes using a single pin. Each mode configures the internal decimation filter to decimate at: 1×, 2×, 4× or 8×. Refer to Table VII for mode pin ranges.

The mode selection is performed by using a set of internal comparators, as illustrated in Figure 62, so that each mode corresponds to a voltage range on the input of the MODE pin. The output of the comparators are fed into encoding logic where, on the falling edge of the clock, the encoded data is latched.

Table VII. Recommended Mode Pin Ranges and Configurations

Mode Pin Range	Typical Mode Pin	Decimation Mode
0 V–0.5 V	GND	8×
0.5 V–1.5 V	VREF/2	2×
1.5 V–3.0 V	CML	4×
3.0 V–5.0 V	AVDD	1×

BIAS PIN OPERATION

The Bias Select Pin (BIAS) gives the user, who is able to operate the AD9260 at a slower clock rate, the added flexibility of running the device in a lower, power consumption mode when it is clocked at less than 20 MHz.

This is accomplished by scaling the bias current of the AD9260 as illustrated in Figure 63. The bias amplifier drives a source follower and forces 1 V across R_{EXT}, which sets the bias current. This effectively adjusts the bias current in the modulator amplifiers and FLASH preamplifiers. When a large value of R_{EXT} is used, a smaller bias current is available to the internal amplifier circuitry. As a result these amplifiers need more time to settle, thus dictating the use of a slower clock as the power is reduced. Refer to the characterization curves shown in Figures 41–48 revealing the performance tradeoffs.

The scaling is accomplished by properly attaching an external resistor to the BIAS pin of the AD9260 as shown in Table IX. R_{EXT} is normally 2 kΩ for a clock speed of 20 MHz and scales inversely with clock rate. Because BIAS is an external pin, minimization of capacitance to this pin is recommended in order to prevent instability of the bias pin amplifier.

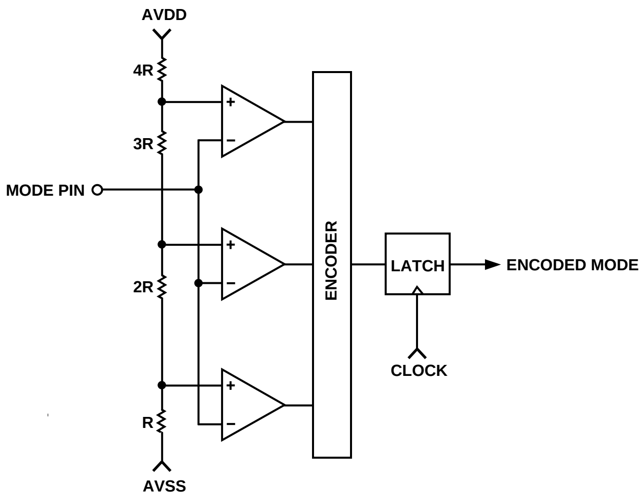


Figure 62. Simplified Mode Pin Circuitry

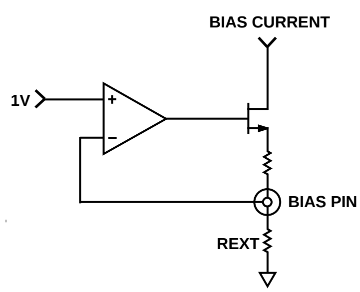


Figure 63. Simplified Bias Pin Circuitry

POWER DISSIPATION CONSIDERATIONS

The power dissipation of the AD9260 is dependent on its application-specific configuration and operating conditions. The analog power dissipation as shown in Figure 64 is primarily a function of its power bias setting and sample rate. It remains insensitive to the particular input waveform being digitized or digital filter MODE setting. The digital power dissipation is primarily a function of the digital supply setting (i.e., +3 V to +5 V), the sample rate and, to a lesser extent, the MODE setting and input waveform. Figures 65a and 65b show the total current dissipation of the "combined" digital (DVDD) and digital driver supply (DRVDD) for +3 V and +5 V supplies. Note, DVDD and DRVDD are typically derived from the same supply bus since no degradation in performance results. A 1 MHz full-scale sine wave was used to ensure maximum digital activity in the digital filters and the digital drivers had a fanout of one. Note also that a twofold decrease in digital supply current results when the digital supply is reduced form +5 V to +3 V.

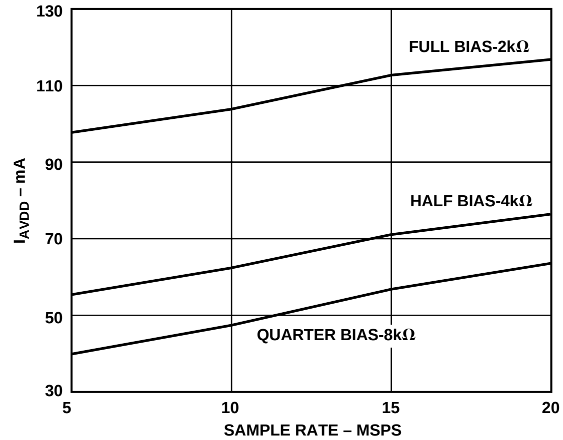


Figure 64. I_{AVDD} vs. Sample Rate (AVDD = +5 V, Mode 1×–4×)

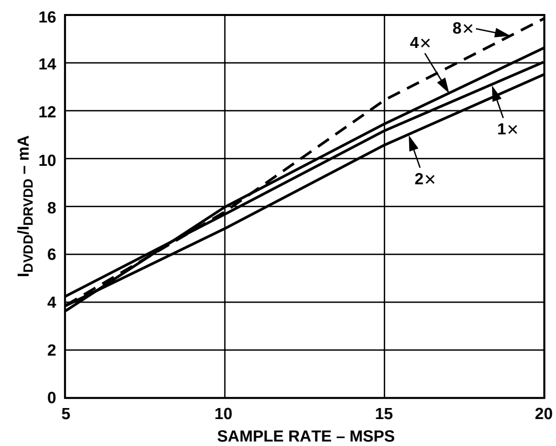


Figure 65a. I_{DVDD}/I_{DRVDD} vs. Sample Rate (DVDD = DRVDD = 3 V, f_{IN} = 1 MHz)

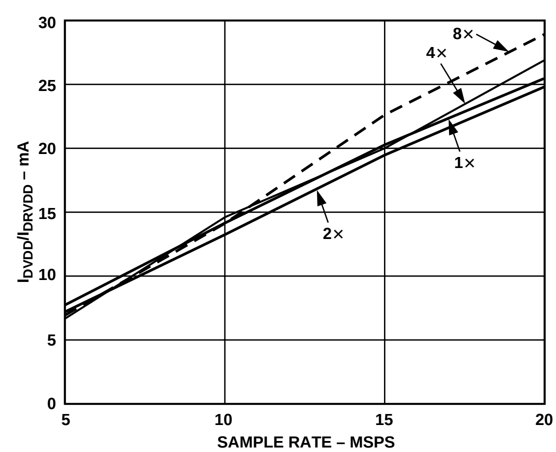


Figure 65b. I_{DVDD}/I_{DRVDD} vs. Sample Rate (DVDD = DRVDD = 5 V, f_{IN} = 1 MHz)

Digital Output Driver Considerations (DRVDD)

The AD9260 output drivers can be configured to interface with +5 V or 3.3 V logic families by setting DRVDD to +5 V or 3.3 V respectively. The AD9260 output drivers in each mode are appropriately sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect SINAD performance. Applications requiring the AD9260 to drive large capacitive loads or large fanout may require additional decoupling capacitors on DRVDD. The addition of external buffers or latches helps reduce output loading while providing effective isolation from the databus.

Clock Input and Considerations

The AD9260 internal timing uses the two edges of the clock input to generate a variety of internal timing signals. The clock input must meet or exceed the minimum specified pulse width high and low (t_{CH} and t_{CL}) specifications for the given A/D as defined in the Switching Specifications at the beginning of the data sheet to meet the rated performance specifications. For example, the clock input to the AD9260 operating at 20 MSPS may have a duty cycle between 45% to 55% to meet this timing requirement since the minimum specified t_{CH} and t_{CL} is 22.5 ns. For clock rates below 20 MSPS, the duty cycle may deviate from this range to the extent that both t_{CH} and t_{CL} are satisfied.

All high speed high resolution A/Ds are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{IN}) due to only aperture jitter (t_A) can be calculated with the following equation:

$$SNR = 20 \log_{10} [1/(2 \pi f_{IN} t_A)]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum square of all the jitter sources which include the clock input, analog input signal, and A/D aperture jitter specification. For example, if a 500 kHz full-scale sine wave is sampled by an A/D with a total rms jitter of 15 ps, the SNR performance of the A/D will be limited to 86.5 dB.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9260. In fact, the CLK input buffer is internally powered from the AD9260's analog supply, AVDD. Thus the CLK logic high and low input voltage levels are +3.5 V and +1.0 V, respectively. Supplies for clock drivers should be separated from the A/D output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other method), it should be retimed by the original clock at the last step.

GROUNDING AND DECOUPLING

Analog and Digital Grounding

Proper grounding is essential in any high speed, high resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. While the AD9260 features separate analog and digital ground pins, it should be treated as an analog component. *The AVSS, DVSS and DRVSS pins must be joined together directly under the AD9260.* A solid ground plane under the A/D is acceptable if the power and ground return currents are managed carefully. Alternatively, the ground plane under the A/D may contain serrations to *steer* currents in predictable directions where cross-coupling between analog and digital would otherwise be unavoidable. The AD9260/EB ground layout, shown in Figure 76, depicts the serrated type of arrangement. The analog and digital grounds are connected by a jumper below the A/D.

Analog and Digital Supply Decoupling

The AD9260 features separate analog, digital, and driver supply and ground pins, helping to minimize digital corruption of sensitive analog signals.

Figure 66 shows the power supply rejection ratio vs. frequency for a 200 mV p-p ripple applied to AVDD, DVDD, and DAVDD.

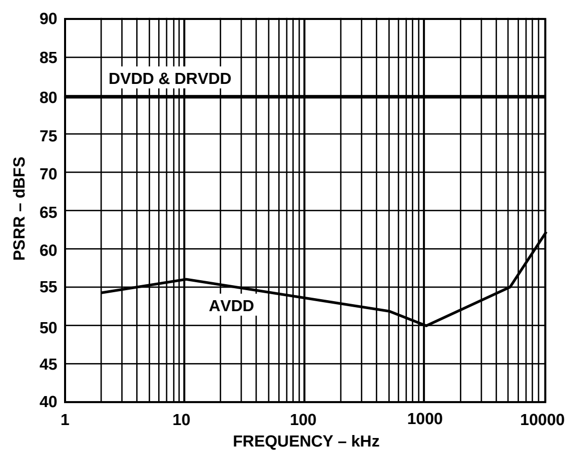


Figure 66. AD9260 PSRR vs. Frequency (8 × Mode)

In general, AVDD, the analog supply, should be decoupled to AVSS, the analog common, as close to the chip as physically possible. Figure 67 shows the recommended decoupling for the analog supplies; 0.1 µF ceramic chip capacitors should provide adequately low impedance over a wide frequency range. Note that the AVDD and AVSS pins are co-located on the AD9260

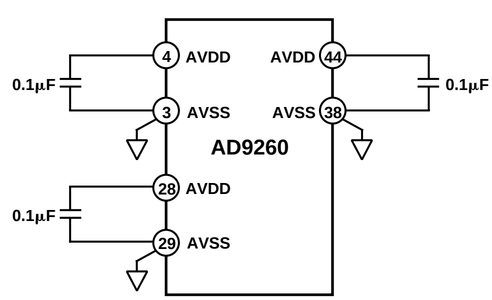


Figure 67. Analog Supply Decoupling

to simplify the layout of the decoupling capacitors and provide the shortest possible PCB trace lengths. The AD9260/EB power plane layout, shown in Figure 77 depicts a typical arrangement using a multilayer PCB.

The digital activity on the AD9260 chip falls into two general categories: digital logic, and output drivers. The internal digital logic draws surges of current, mainly during the clock transitions. The output drivers draw large current impulses while the output bits are changing. The size and duration of these currents are a function of the load on the output bits: large capacitive loads are to be avoided. Note that the digital logic of the AD9260 is referenced DVDD while the output drivers are referenced to DRVDD. Also note that the SNR performance of the AD9260 remains independent of the digital or driver supply setting.

The decoupling shown in Figure 68, a 0.1 μF ceramic chip capacitor, is appropriate for a reasonable capacitive load on the digital outputs (typically 20 pF on each pin). Applications involving greater digital loads should consider increasing the digital decoupling proportionally, and/or using external buffers/latches.

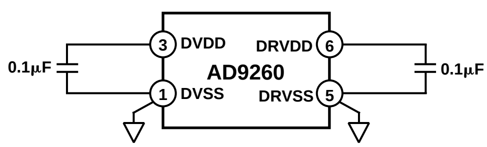


Figure 68. Digital Supply Decoupling

A complete decoupling scheme will also include large tantalum or electrolytic capacitors on the PCB to reduce low-frequency ripple to negligible levels. Refer to the AD9260/EB schematic and layouts in Figures 73–77 for more information regarding the placement of decoupling capacitors.

An alternative layout and decoupling scheme is shown in Figure 69. This layout and decoupling scheme is well suited for applications in which multiple AD9260s are located on the same PC board and/or the AD9260 is part of a multicard mixed signal system in which grounds are tied back at the system supplies (i.e., star ground configuration). In this case, the AD9260 is treated as an analog component in which its analog (i.e., AVDD) and digital (DVDD and DRVDD) supplies are derived from the systems +5 V analog supply and all of the AD9260's ground pins are tied directly to the analog ground plane which resides directly underneath the IC.

Referring to Figure 69, each supply pin is directly decoupled to their respective ground pin or analog ground plane via a ceramic 0.1 μF chip capacitor. Surface mount ferrite beads are used to isolate the analog (AVDD), digital (DVDD), and driver supplies (DRVDD) of the AD9260 from the +5 V power buss. Properly selected ferrite beads can provide more than 40 dB of isolation from high frequency switching transients originating from AD9260 supply pins. Further noise immunity from noise is provided by the inherent power-supply rejection of the AD9260 as shown in Figure 64. If digital operation at 3 V is desirable for power savings and or to provide for a 3 V digital logic interface, a 5 V to 3 V linear regulator can be used to drive DVDD and/or DRVDD. A more complete discussion on this layout and decoupling scheme can be found in Chapter 7, pages 7-27 through 7-55 of the High Speed Design Techniques seminar book, which is available at *www.analog.com/support/frames/lin_frameset.hml.*

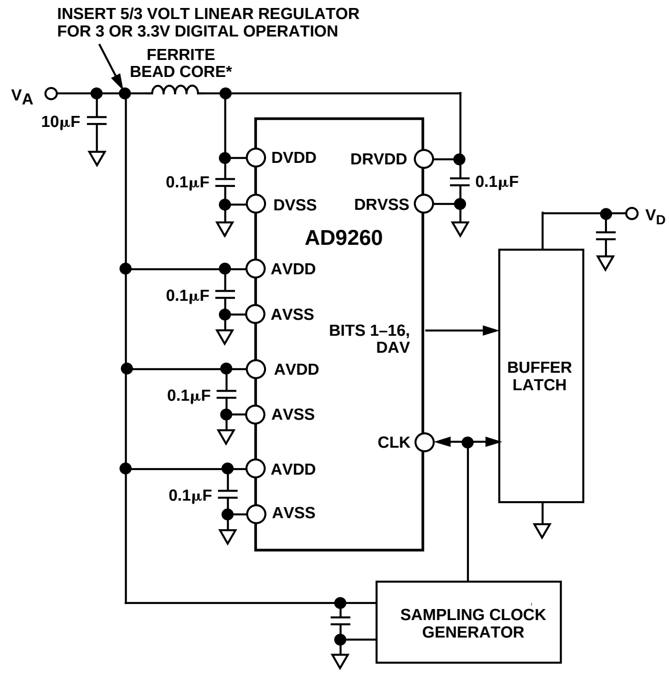


Figure 69.

AD9260 EVALUATION BOARD

GENERAL DESCRIPTION

The AD9260 Evaluation Board is designed to provide an easy and flexible method of exercising the AD9260 and demonstrate its performance to data sheet specifications. The evaluation board is fabricated in four layers: the component layer; the ground layer; the power layer and the solder layer. The board is clearly labeled to provide easy identification of components. Ample space is provided near the analog and clock inputs to provide additional or alternate signal conditioning.

FEATURES AND USER CONTROL

- **Jumper Controlled Mode/OSR Selection:** The choice of Mode/OSR can easily be varied by jumping either JP1, JP2, JP3 or JP4 as illustrated in Figure 71 within the Mode/OSR Control Block. To obtain the desired mode refer to Table VIII.

Table VIII. AD9260 Evaluation Board Mode Select

Mode/OSR	Connect Jumper
1×	JP4
2×	JP2
4×	JP3
8×	JP1

- **Selectable Power Bias:** The power consumption of the AD9260 can be scaled down if the user is able to operate the device at a lower clock frequency. As illustrated in Figure 71, pin cups are provided for the external resistor (R2) tied to the BIAS pin of the AD9260. Table IX defines the recommended resistance for a given clock speed to obtain the desired power consumption.

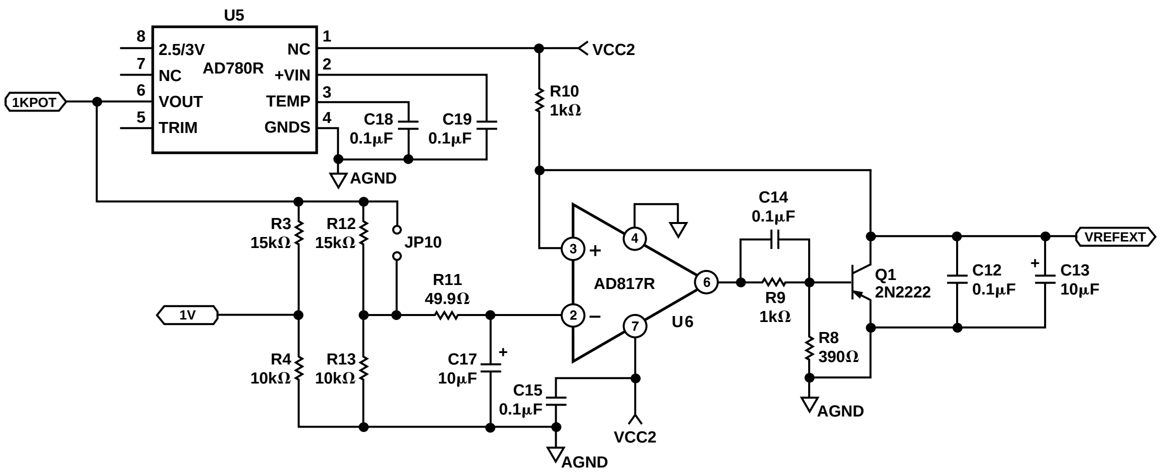


Figure 70. Evaluation Board External Reference Circuitry

Table IX. Evaluation Board Recommended Resistance Value for External Bias Resistor

Resistor Value	Clock Speed (max)	Power Consumption
2 kΩ	20 MHz	585 mW
4 kΩ	10 MHz	325 mW
8 kΩ	5 MHz	200 mW
16 kΩ	2.5 MHz	150 mW

- **Data Interfacing Controls:** The data interfacing controls (RESETB, CSB, READ, DAV) are all accessible via SMA connectors (J2–J5) as illustrated in Figure 71 within the data interfacing control block. The RESETB, CSB and READ connections are each supplied with two sets or resistor pin cups to allow the user to pull-up or pull-down each signal to a fixed state. R5, R6 and R30 will terminate to ground, while R7, R28 and R29 terminate to DRVDD. The DAV and OTR signals are also directly connected to the data output connector P1. All interfacing controls are buffered through the CMOS line driver 74HC541.
- **Buffered Output Data:** The twos complement output data is buffered through two CMOS noninverting bus transceivers (U2 and U3) and made available at pin connector P1 as illustrated in Figure 71 within the data output block.
- **Jumper Controlled Reference Source:** The choice of reference for the AD9260 can easily be varied between 1.0 V, 2.5 V or external, by using Jumpers JP5, JP6, JP7 and JP9 as illustrated in Figure 71 within the reference configuration block. To obtain the desired reference see Table X.

Table X. Evaluation Board Reference Pin Configuration

Reference Voltage	Connect Jumper	Input Voltage (pk-pk FS)
2.5 V	JP7	4.0 V
1.0 V	JP6	1.6 V
External	JP5, JP9 and JP10	4.0 V

The external reference circuitry, is illustrated in Figure 70. By connecting or disconnecting JP10, the external reference can be configured for either 1.0 V or 2.5 V. That is, by connecting JP10, the external reference will be configured to provide a 2.5 V reference. By leaving JP10 open, the external reference will be configured to provide a 1.0 V reference.

- **Flexible DC or AC Coupled External Clock Inputs:** As illustrated in Figure 71, the AD9260 Evaluation Board is designed to allow the user the flexibility of selecting how to connect the external clock source. It is also equipped with a playpen area for experimenting with optional clock drivers or crystals.
- **Selecting DC or AC Coupled External Clock:**
  DC Coupled: To directly drive the clock externally via the CLKIN connector, connect JP11 and disconnect JP12. Note: 50 Ω terminated by R27.

  AC Coupled: To ac couple the external clock and level shift it to midsupply, connect JP12 and disconnect JP11. Note: 50 Ω terminated by R27.
- **Flexible Input Signal Configuration Circuitry:** The AD9260 Evaluation Board's Input Signal Configuration Block is illustrated in Figure 72. It is comprised of an input signal summing amplifier (U7), a variable input signal common-mode generator (U10) and a pair of amplifiers (U8 and U9) that configure the input into a differential signal and drive it, through a pair of isolation resistors, into the input pins of AD9260. The user can either input a signal or dual signal into the evaluation board via the two SMA connectors (J6 and J7) labeled IN-1 or IN-2.

  The user should refer to the Driving the Input section of the data sheet for a detailed explanation of how the inputs are to be driven and what amplifier requirements are recommended.
- **Selecting Single or Dual Signal Input:** The input amplifier (U7) can either be configured as a dual input signal inverting summer or a single tone inverting buffer. This flexibility will allow for slightly better noise performance in the single tone mode due to the inherent noise gain difference in the two amplifier configurations. An optional feedback capacitor (C9) was added to allow the user additional out-of band filtering of the input signal if needed.

For two-tone input signals: The user would leave jumpers (JP8) connected and use IN-1 and IN-2 (J7 and J6) as the connectors for the input signals.

For signal tone input signal: The user would remove jumper (JP8) and use only IN-1 as the input signal connector.

- **Selectable Input Signal Common-Mode Level Source:** The input signal's common-mode level (CML) can be set by U10.

  To use the Input CML generated by U10: Disconnect jumper JP13 and Connect resistors RX3 and RX4. The CML generated by U10 is variable and adjustable using the 1 kΩ trimpot R35.

SHIPMENT CONFIGURATION AND QUICK SETUP

- The AD9260 Evaluation Board is configured as follows when shipped:

1. 2.5 V external reference/4.0 V differential full-scale input: JP5, JP9 and JP10 connected, JP6 and JP7 disconnected.
2. 8× Mode/OSR: JP1 connected, JP2, JP3, and JP4 disconnected.
3. Full Speed Power Bias: R2 = 2 kΩ and connected.
4. CSB pulled low: R6 = 49.9 Ω and connected, R29 disconnected.
5. RESETB pulled high: R7 = 10 kΩ and connected, R30 disconnected.
6. READ pulled high: R28 = 10 kΩ and connected, R5 disconnected.
7. Single Tone Input: JP8 removed, input applied via IN-1 (J7).
8. Input signal common-mode level set by Trimpot R35 to 2.0 V: Jumper JP12 is disconnected and resistors Rx4 and Rx3 are connected.
9. AC Coupled Clock: JP12 connected and JP11 disconnected. Note: 50 Ω terminated by R27.

QUICK SETUP

1. Connect the required power supplies to the Evaluation Board as illustrated in Figure 22:
   ⇒ ±5 VA supplies to P5—Analog Power
   ⇒ +5 VA supply to P4—Analog Power
   ⇒ +5 VD supply to P3—Digital Power
   ⇒ +5 VD supply to P2—Driver Power
2. Connect a Clock Source to CLKIN (J1): Note: 50 Ω terminated by R1.
3. Connect an Input Signal Source to the IN-1 (J7).
4. Turn On Power!
5. The AD9260 Evaluation Board is now ready for use.

APPLICATION TIPS

1. The ADC analog input should not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6 dB to prevent "hard limiting" on peaks.
3. Bandpass filtering of test signal generators is absolutely necessary for SNR, THD and IMD tests. Note, a low noise signal generator along with a high Q bandpass filter is often necessary to achieve the attainable noise performance of the AD9260.
4. Test signal generators must have exceptional noise performance to achieve accurate SNR measurements. Good generators, together with fifth-order elliptical bandpass filters, are recommended for SNR tests. Narrow bandwidth crystal filters can also be used to filter generator broadband noise, but they should be carefully tested for operation at high signal levels.
5. The analog inputs of the AD9260 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50 Ω or 75 Ω), or it should be driven by a low output impedance buffer. Short leads are necessary to prevent digital noise pickup.
6. A low noise (jitter) clock signal generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance particularly at higher input frequencies. A high frequency generator, based on a clock source (e.g., crystal source), is recommended. Frequency-synthesized clock generators should generally be avoided because they typically provide poor jitter performance. See Note 8 if a crystal-based clock generator is used during FFT testing.

A low jitter clock may be generated by using a high-frequency clock source and dividing this frequency down with a low noise clock divider to obtain the AD9260 input CLK. Maintaining a large amplitude clock signal may also be very beneficial in minimizing the effects of noise in the digital gates of the clock generation circuitry.

Finally, special care should be taken to avoid coupling noise into any digital gates preceding the AD9260 CLK pin. Short leads are necessary to preserve fast rise times and careful decoupling should be used with these digital gates and the supplies for these digital gates should be connected to the same supplies as that of the internal AD9260 clock circuitry (Pins 44 and 38).

7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits.
8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies.
9. A well designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but if carefully designed, a two-sided PC board with large heavy (20 oz. foil) ground planes can give excellent results.
10. Prototype "plug-boards" or wire-wrap boards will not be satisfactory.

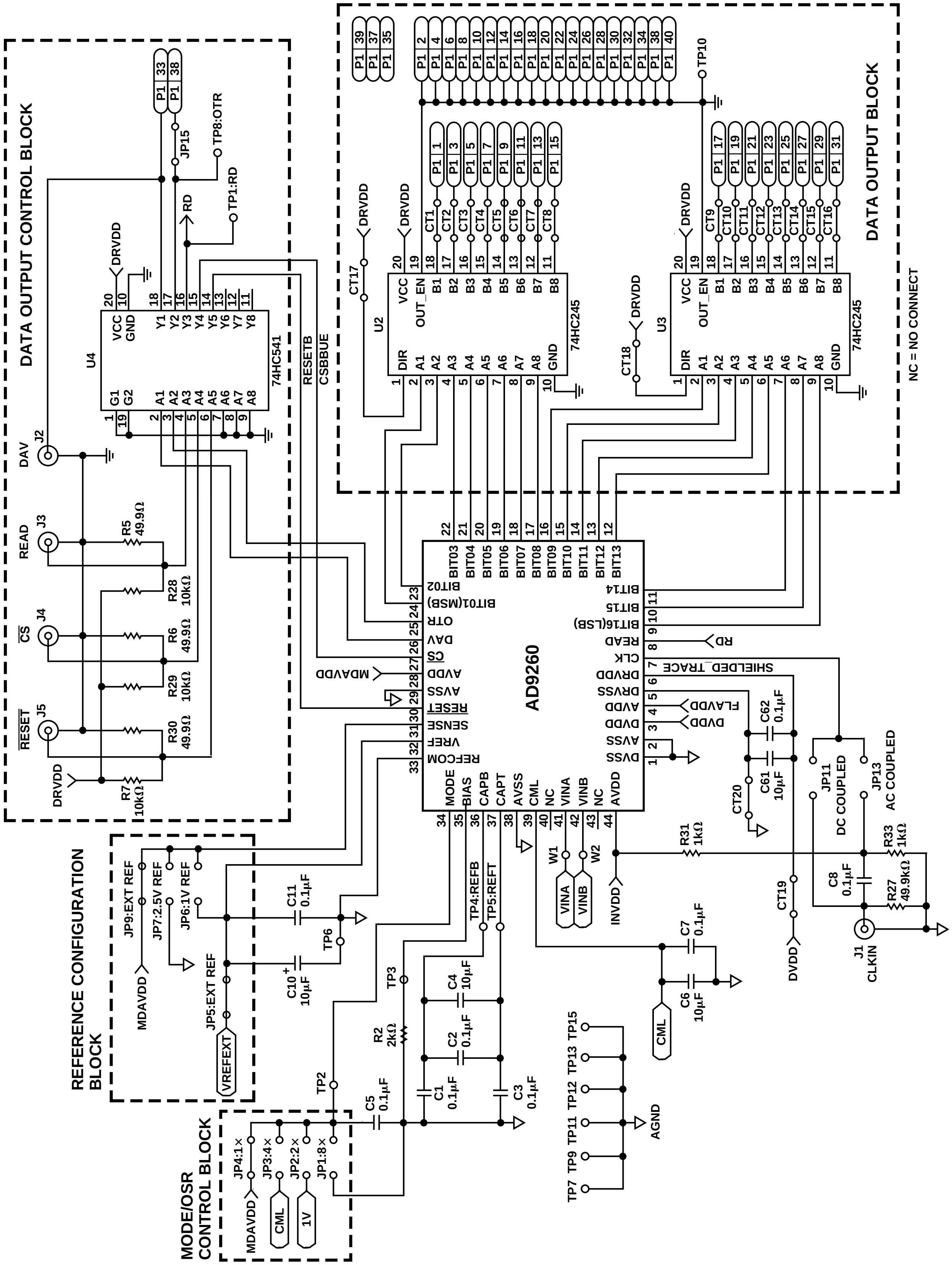


Figure 71. Evaluation Board Top Level Schematic

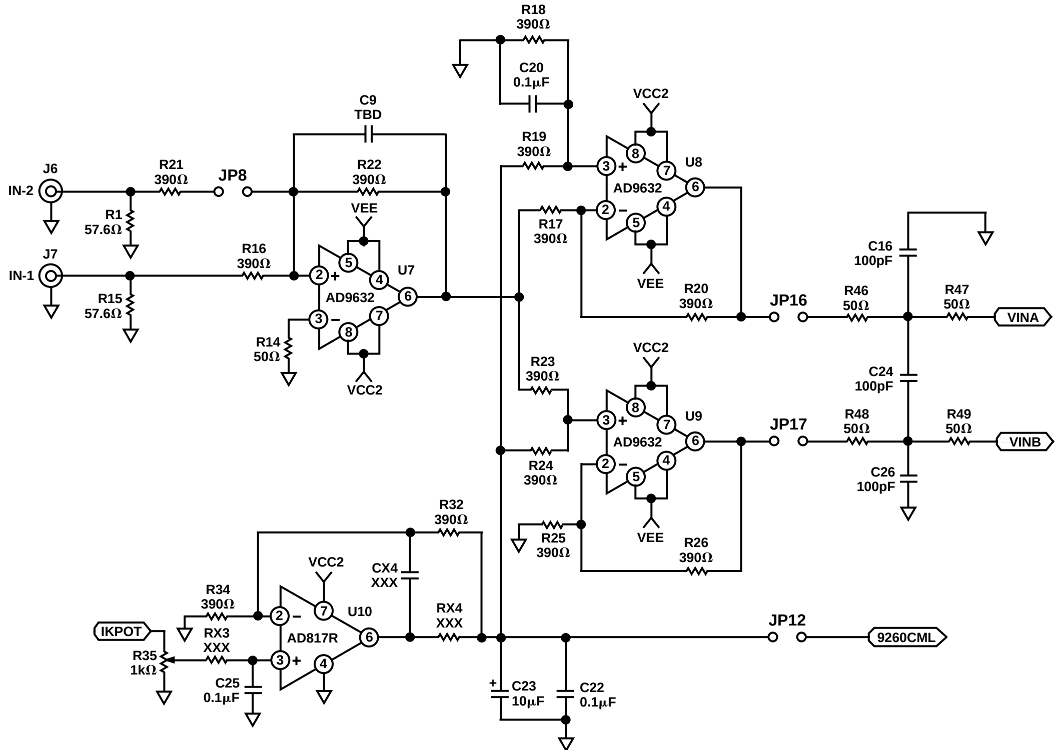


Figure 72. Evaluation Board Input Configuration Block

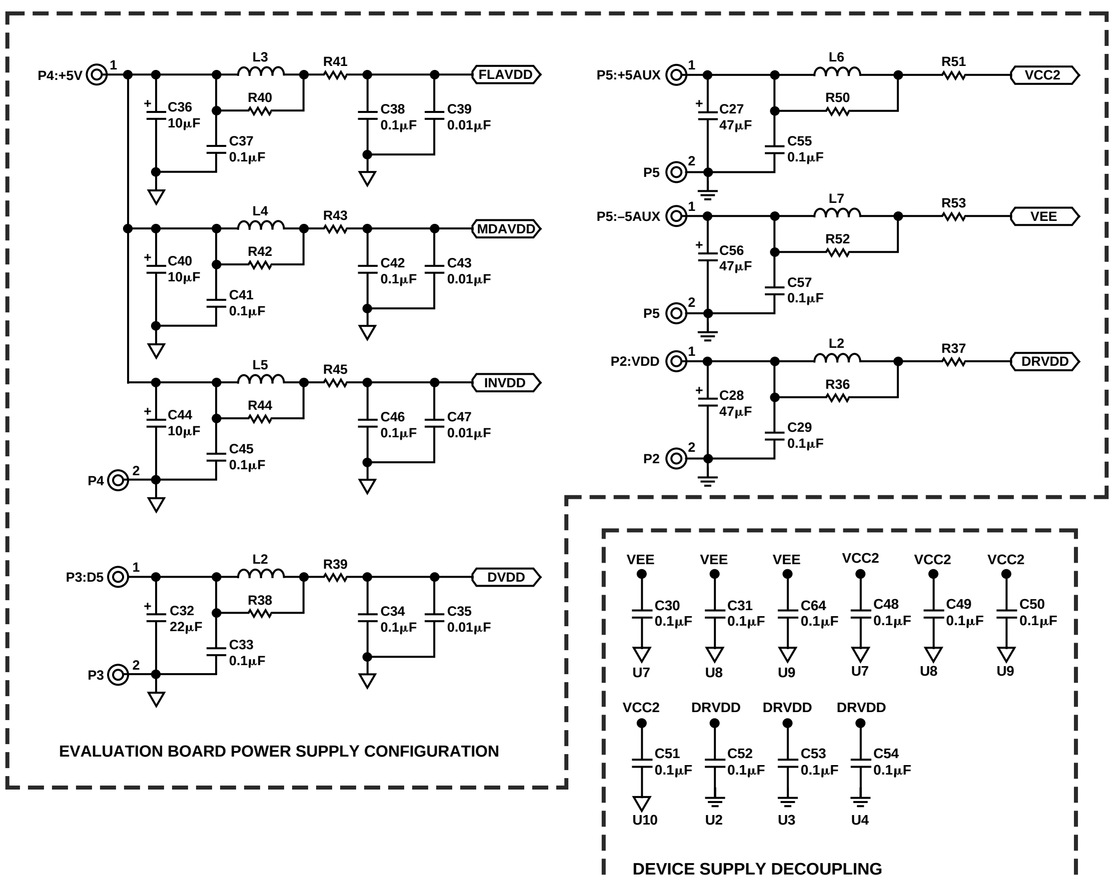


Figure 73. Evaluation Board Power Supply Configuration and Coupling

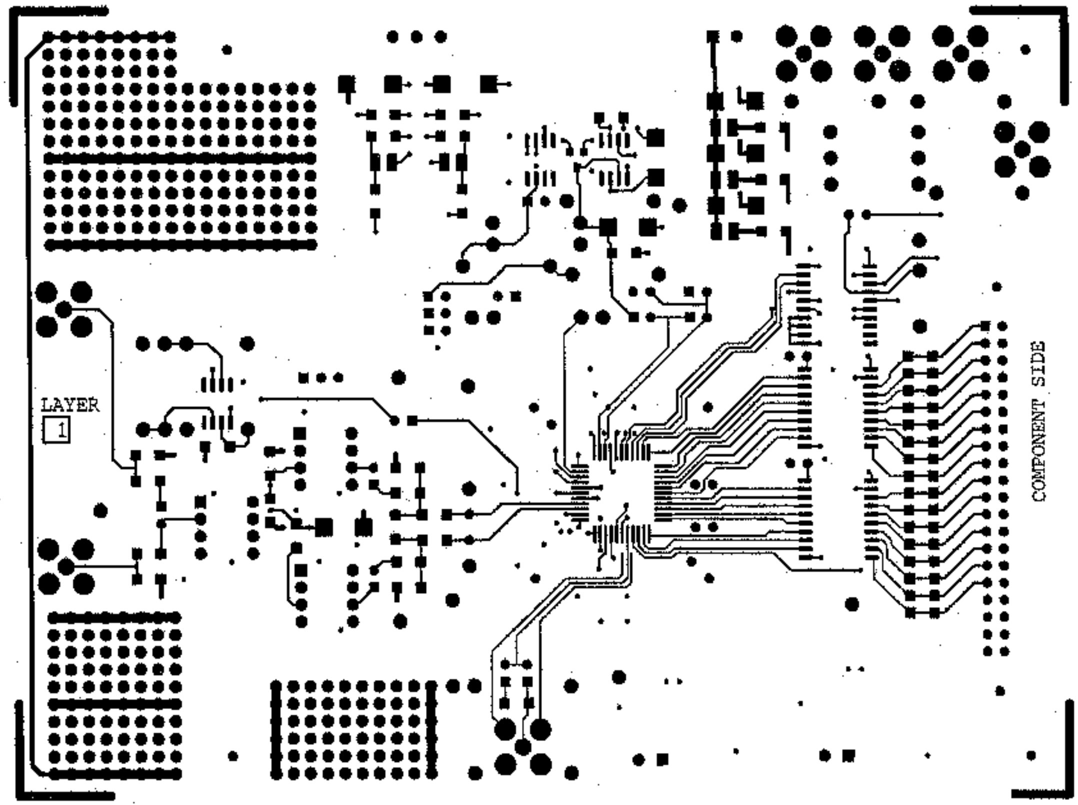


Figure 74. Evaluation Board Component Side Layout (Not to Scale)

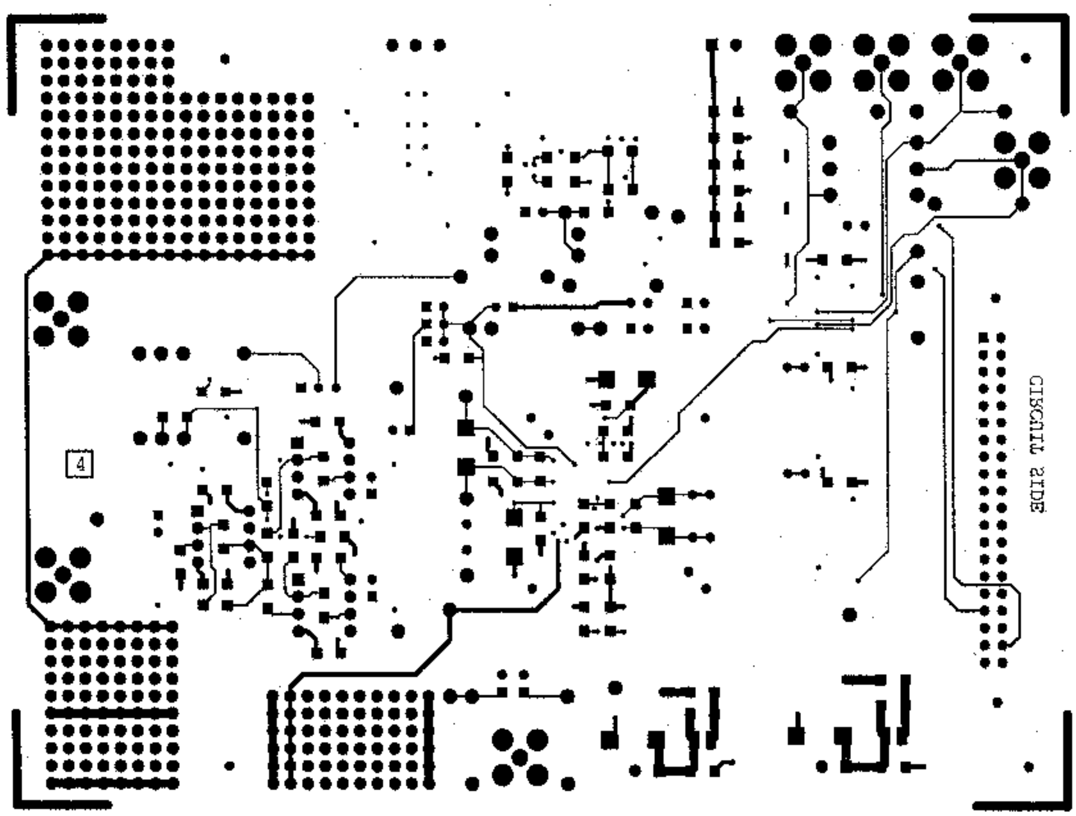


Figure 75. Evaluation Board Solder Side Layout (Not to Scale)

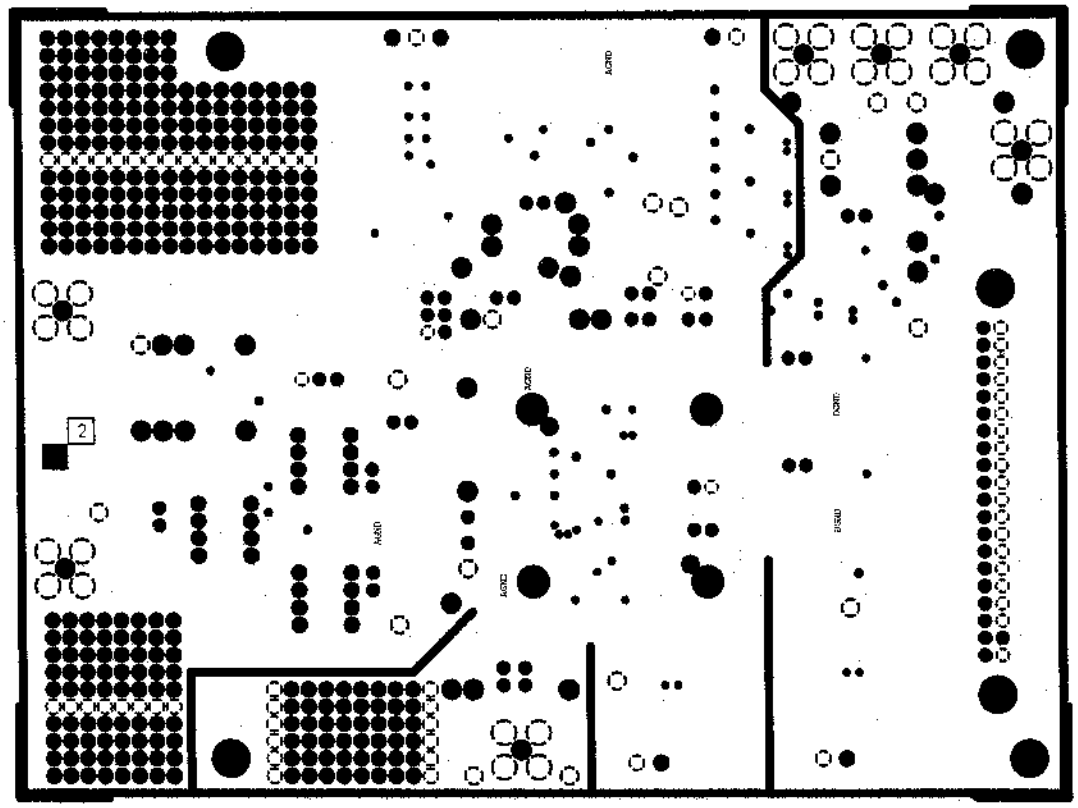


Figure 76. Evaluation Board Ground Plane Layout (Not to Scale)

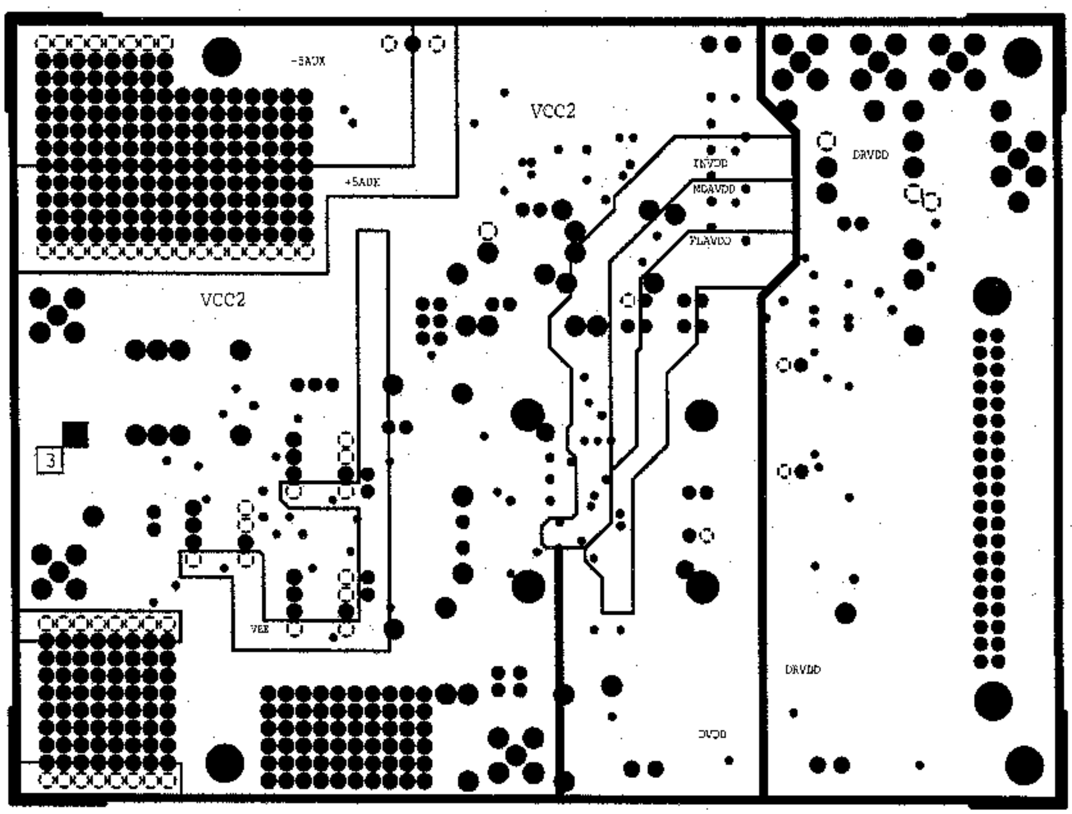
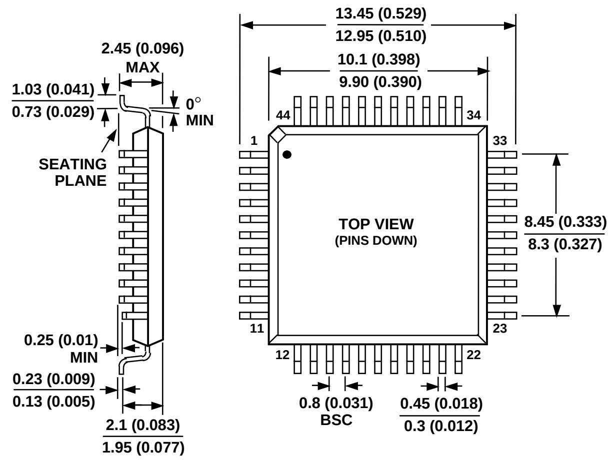


Figure 77. Evaluation Board Power Plane Layout (Not to Scale)

OUTLINE DIMENSIONS

Dimensions shown in millimeters and (inches).

44-Lead MQFP (S-44)



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