a

12-Bit, 170/210 MSPS A/D Converter

AD9430

FEATURES

SNR = 66dB @ Fin up to 65MHz at 170Msps
ENOB of 10.3 @ Fin up to 65MHz at 170 Msps (-1dBFs)
SFDR = -80dBc @ Fin up to 65MHz at 170Msps (-1dBFs)
Excellent Linearity:
- **DNL = +/- 0.3 lsb (typ)**
- **INL = +/- 0.5 lsb (typ)**

Two Output Data options
- **Demultiplexed 3.3V CMOS outputs each at 105 Msps**
- **LVDS at 210Msps**

700 MHz Full Power Analog Bandwidth
On–chip reference and track/hold
Power dissipation = 1.3W typical at 210Msps
1.5V Input voltage range
+3.3V Supply Operation
Output data format option
Data Sync input and Data Clock output provided
Interleaved or parallel data output option
Clock Duty Cycle Stabilizer.

APPLICATIONS

Wireless and Wired Broadband Communications
- **Wideband carrier frequency systems**
- **Cable Reverse Path**

Communications Test Equipment
Radar and Satellite sub-systems

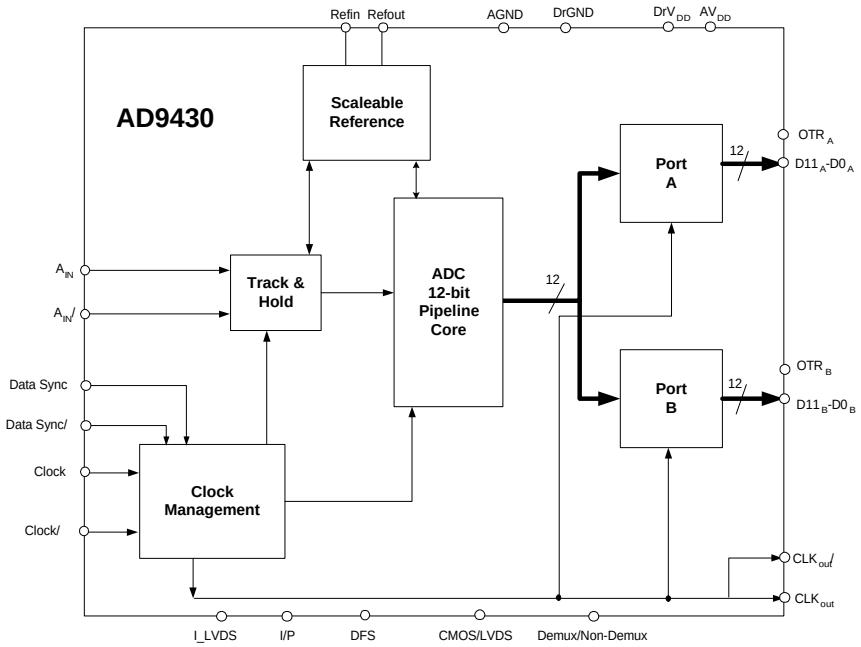
PRODUCT DESCRIPTION

The AD9430 is a 12-bit monolithic sampling analog–to–digital converter with an on–chip track–and–hold circuit and is optimized for low cost, low power, small size and ease of use. The product operates up to 210 Msps conversion rate and is optimized for outstanding dynamic performance in wideband carrier systems.

The ADC requires a +3.3V power supply and a differential encode clock for full performance operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS or LVDS compatible. Separate output power supply pins support interfacing with 3.3V CMOS logic.

An output data format select option of two's complement or offset binary is supported. Two output buses support demultiplexed data up to 105 Msps rates. A data sync input is supported for proper output data port alignment and a data clock output is available for proper output data timing.

Fabricated on an advanced BiCMOS process, the AD9430 is available in an 100 pin surface mount plastic package (100 LQFP) specified over the industrial temperature range (–40°C to +85°C).



AD9430 FUNCTIONAL BLOCK DIAGRAM

AD9430

DC SPECIFICATIONS (AV_{DD}= 3.3V, DrV_{DD} = 3.3V; T_{MIN} = -40°C, T_{MAX} = +85°C, Fin = -0.5dBFS, 1.235V External reference)

Parameter	Temp	Test Level	AD9430BST-210 Min	AD9430BST-210 Typ	AD9430BST-210 Max	AD9430BST-170 Min	AD9430BST-170 Typ	AD9430BST-170 Max	Units
RESOLUTION				12			12		Bits
ACCURACY									
No Missing Codes	Full	I		Guaranteed			Guaranteed		
Offset Error	25°C	I		tbd			tbd		mV
Gain Error	25°C	I		tbd			tbd		% FS
Differential Nonlinearity (DNL)	25°C	I		+/-0.3			+/-0.3		LSB
Integral Nonlinearity (INL)	25°C	I		+/-0.5			+/-0.5		LSB
TEMPERATURE DRIFT									
Offset Error	Full	V		tbd			tbd		ppm/°C
Gain Error	Full	V		tbd			tbd		ppm/°C
POWER SUPPLY REJECTION	Full	V		± tbd			± tbd		mV/V
REFERENCE OUT (V_{REF})	Full	V		1.235			1.235		V
ANALOG INPUTS (AIN, $\overline{AIN}$)									
Input Voltage Range (AIN– $\overline{AIN}$)	Full	V		.768			.768		V_{P-P}
Input Common Mode Voltage	Full	V		2.8			2.8		V
Input Resistance	Full	V		3			3		kΩ
Input Capacitance	Full	V		5			5		pF
POWER SUPPLY									
Supply Voltages									
AV_{DD}	Full	V	3.0	3.3	3.6	3.0	3.3	3.6	V
DrV_{DD}	Full	V	3.0	3.3	3.6	3.0	3.3	3.6	V
Supply Current									
I_{ANALOG} (AV_{DD}= 3.3V)[1]	Full	V		340			300		mA
$I_{DIGITAL}$ (DrVDD = 3.3V)[1]	Full	V		60			60		mA
POWER CONSUMPTION[2]	Full	V		1.1			1.0		W

NOTES

[1] I_{AVDD} and I_{DrVDD} are measured with an analog input of 10.3MHz, -0.5dBFs, sine wave, rated Encode rate and in Demux output mode. See Typical Performance Characteristics and Applications section for I_{DrVDD}.

[2] Power Consumption is measured with a DC input at rated Encode rate in Demux output mode.

DIGITAL SPECIFICATIONS (AV_{DD}= 3.3V, DrV_{DD} = 3.3V; T_{MIN} = -40°C, T_{MAX} = +85°C)

Parameter (Conditions)	Temp	Test Level	AD9430BST-210 Min	AD9430BST-210 Typ	AD9430BST-210 Max	AD9430BST-170 Min	AD9430BST-170 Typ	AD9430BST-170 Max	Units
ENCODE AND DATA SYNC INPUTS (ENC, $\overline{ENC}$, DS, DS/)									
Differential Input Voltage[1]	Full	IV	0.2			0.2			V
V_{IH}	Full	IV			2.6			2.6	V
V_{IL}	Full	IV	.9			.9			V
Input Resistance	Full	IV		5.5			5.5		kΩ
Input Capacitance	Full	IV		4			4		pF
LOGIC INPUTS (S1,S2,S3,S4,S5)									
Logic '1' Voltage	Full	IV	2.0			2.0			V
Logic '0' Voltage	Full	IV			.8			.8	V
Input Resistance	Full	IV		30			30		kΩ
Input Capacitance	Full	IV		4			4		pF
LOGIC OUTPUTS (Demux Mode)									
Logic "1" Voltage[2]	Full	IV	DrV_{DD}-0.05			DrV_{DD}-0.05			V
Logic "0" Voltage[2]	Full	IV			0.05			0.05	V
LOGIC OUTPUTS (LVDS Mode)[2,3]									
V_{OD} Differential Output Voltage	Full	IV	247		454	247		454	mV
V_{OS} Output Offset Voltage	Full	IV	1.125		1.375	1.125		1.375	V
Output Coding	Full	IV	Two's Comp or Binary			Two's Comp or Binary			

NOTES [1]All AC specifications tested by driving ENCODE and $\overline{ENCODE}$ differentially | ENCODE - $\overline{ENCODE}$ | > 200mV

[2]Digital Output Logic Levels: DrV_{DD}= 3.3V, C_{LOAD} = 10pF. [3] LVDS Rl=100 ohms, LVDS Output Swing Set Resistor = TBD

AC SPECIFICATIONS[1] (AV_{DD}= 3.3 V, DrV_{DD} = 3.3V; ENCODE = Maximum Conversion Rate ; T_{MIN} = -40°C, T_{MAX} = +85°C, Internal voltage reference)

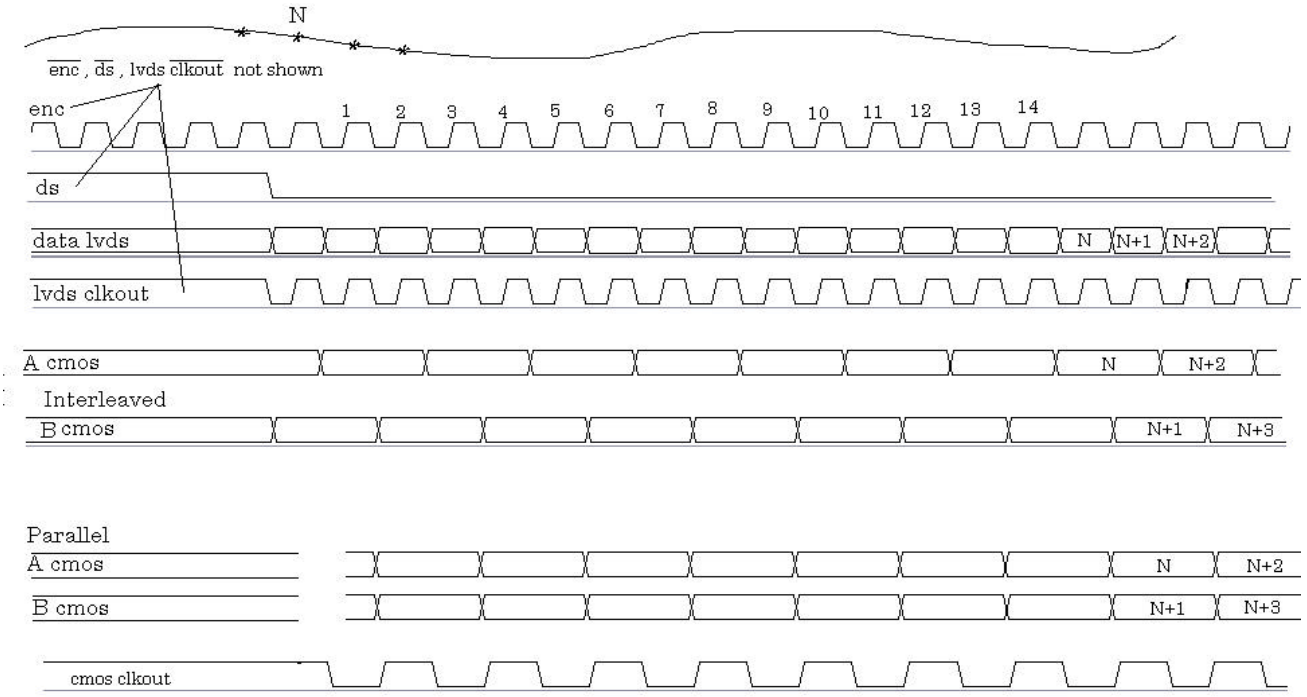
Parameter (Conditions)	Temp	Test Level	AD9430BST-210 Min	AD9430BST-210 Typ	AD9430BST-210 Max	AD9430BST-170 Min	AD9430BST-170 Typ	AD9430BST-170 Max	Units
SNR									
Analog Input 10 MHz	25°C	I		66			66.5		dB
@ -0.5dBFS 65 MHz	25°C	I		65			66		dB
100 MHz	25°C	V		64			65		dB
240 MHz	25°C	V		60			61		dB
SINAD									
Analog Input 10 MHz	25°C	I		65.5			66		dB
@ -0.5dBFS 65 MHz	25°C	I		64.5			65.5		dB
100 MHz	25°C	V		63.5			64.5		dB
240 MHz	25°C	V		TBD			TBD		dB
Worst Harmonic (2^{nd} or 3^{rd})									
Analog Input 10 MHz	25°C	I		-83			-85		dBc
@ -0.5dBFS 65 MHz	25°C	I		-80			-82		dBc
100 MHz	25°C	V		-78			-80		dBc
240 MHz	25°C	V		TBD			TBD		dBc
Worst Harmonic (4^{th} or higher)									
Analog Input 10 MHz	25°C	I		-85			-90		dBc
@ -0.5dBFS 65 MHz	25°C	I		-85			-90		dBc
100 MHz	25°C	V		-85			-90		dBc
240 MHz	25°C	V		-85			-90		dBc
Two-tone IMD[2]									
F1, F2 @ -7 dBFS	Full	V		-70			-75		dBc
Analog Input Bandwidth	25°C	V		700			700		MHz

NOTES
[1] All AC specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially.
2 F1 = 64.1 MHz, F2 = 65.1 MHz

SWITCHING SPECIFICATIONS (AV_{DD}= 3.3 V, DrV_{DD} = 3.3V; ENCODE = Maximum Conversion Rate ; T_{MIN} = -40°C, T_{MAX} = +85°C)

Parameter (Conditions)	Temp	Test Level	AD9430BST-210 Min	AD9430BST-210 Typ	AD9430BST-210 Max	AD9430BST-170 Min	AD9430BST-170 Typ	AD9430BST-170 Max	Units
Maximum Conversion Rate	Full	I	210			170			MSPS
Minimum Conversion Rate	Full	V			100			100	MSPS
Encode Pulse Width High (t_{EH})[1]	Full	V	2			2			ns
Encode Pulse Width Low (t_{EL})[1]	Full	V	2			2			ns
Encode Period[1]	Full	V							ns

NOTES
[1] All AC specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially.



Notes:
1) LVDS clockout True will be same physical pin as CMOS Clkout Bar
LVDS clockout Bar will be same physical pin as CMOS Clkout True
2) Clkout True (LVDS or CMOS) will be DC out of phase with encode True
3) Data Outputs and Clkout pins are held static when DS is high
4) Latency --> 14 cycles

AD9430 Preliminary Timing Diagram **10/12/2000** GH

AD9430 Timing Diagram

SWITCHING SPECIFICATIONS (cont'd)

Parameter	Temp	Test Level	AD9430BST-210 Min	AD9430BST-210 Typ	AD9430BST-210 Max	AD9430BST-170 Min	AD9430BST-170 Typ	AD9430BST-170 Max	Units
OUTPUT Parameters in Demux Mode									
Valid Time (t_V)	Full	IV							ns
Propagation Delay (t_{PD})	Full	IV		3.5			3.5		ns
Rise Time (t_R)	25°C	V							ns
Fall Time (t_F)	25°C	V							ns
DCO Propagation Delay (t_{CPD})	Full	VI							ns
Data to DCO Skew ($t_{PD} - t_{CPD}$)	Full	IV							ns
DS Setup Time (t_{SDS})	Full	IV							ns
DS Hold Time (t_{HDS})	Full	IV							ns
Interleaved Mode (A, B Latency)	Full	VI							Cycles
Parallel Mode (A, B Latency)	Full	VI							Cycles
OUTPUT Parameters in LVDS Mode									
Valid Time (t_V)	Full	IV							ns
Propagation Delay (t_{PD})	Full	IV		3.5			3.5		ns
Rise Time (t_R)	25°C	V							ns
Fall Time (t_F)	25°C	V							ns
DCO Propagation Delay (t_{CPD})	Full	VI							ns
Data to DCO Skew ($t_{PD} - t_{CPD}$)	Full	IV							ns
DS Setup Time (t_{SDS})	Full	IV							ns
DS Hold Time (t_{HDS})	Full	IV							ns
Pipeline Latency	Full	VI							Cycles
Aperture Delay (t_A)	25°C	V							ps
Aperture Uncertainty (Jitter, t_J)	25°C	V		0.25			0.25		ps rms

Table 1. AD9430 Output Select Coding (rev B – 2/13/01 jhh)

S1 (Data Format Select)[1]	**S2** (LVDS/CMOS Output Mode Select)[2]	**S3** (Dual Mode Select)[3]	**S4** (Select Interleaved or Parallel Mode)[4]	**S5** (Gain)	**Mode**
1	X	X	X	X	2's Complement
0	X	X	X	X	Offset Binary
X	0	0	1	X	Dual Mode CMOS Interleaved
X	0	0	0	X	Dual Mode CMOS Parallel
X	0	1	X	X	Single Mode CMOS
X	1	X	X	X	LVDS Mode
X	X	X	X	1	Gain enabled
X	X	X	X	0	No Gain

Notes:
[1] S1 Pin is independent of S2-S5 and sets output coding for all states of S2,S3,S4,S5
[2] S2 =1 sets LVDS Mode independent of S1,S3,S4,S5 - S2=0 sets CMOS Mode
[3] S3 used in CMOS Mode only (S2=0)
[4] S4 used in CMOS Mode only (S2=0)

In interleaved mode output data on port A is offset from output data changes on port B by ½ output clock cycle.

Interleaved mode  Parallel Mode 

S1-S5 all have 30K resistive pulldowns on chip.