ANALOG DEVICES

12-Bit, 160 MSPS TxDAC+® with 2×/4×/8× Interpolation and Signal Processing

Preliminary Technical Data AD9782

FEATURES

12-Bit Resolution, 160 MSPS Input Data Rate
Selectable 2×/4×/8× Interpolating Filters
Selectable $f_{DAC}/2$,$f_{DAC}/4$,$f_{DAC}/8$ Modulation Modes
Single or Dual Channel Signal Processing
Selectable Image Rejection Hilbert Transform
Flexible Calibration Engine
Direct IF Transmission Features
Serial Control Interface
Versatile Clock and Data Interface
SFDR 82dBc @10MHz
W-CDMA ACPR -67dB @16.384 Offset
DNL < +/-2 LSBs
Power Dissipation <1W
3.3 V Analog, 2.5V Digital Supply
3.3V Compatible Digital Interface
On-chip 1.2 V Reference
80-Lead LQFP

APPLICATIONS

Digital Quadrature Modulation Architectures
W-CDMA, Multi-Carrier GSM, TDMA, DCS, PCS, CDMA Systems

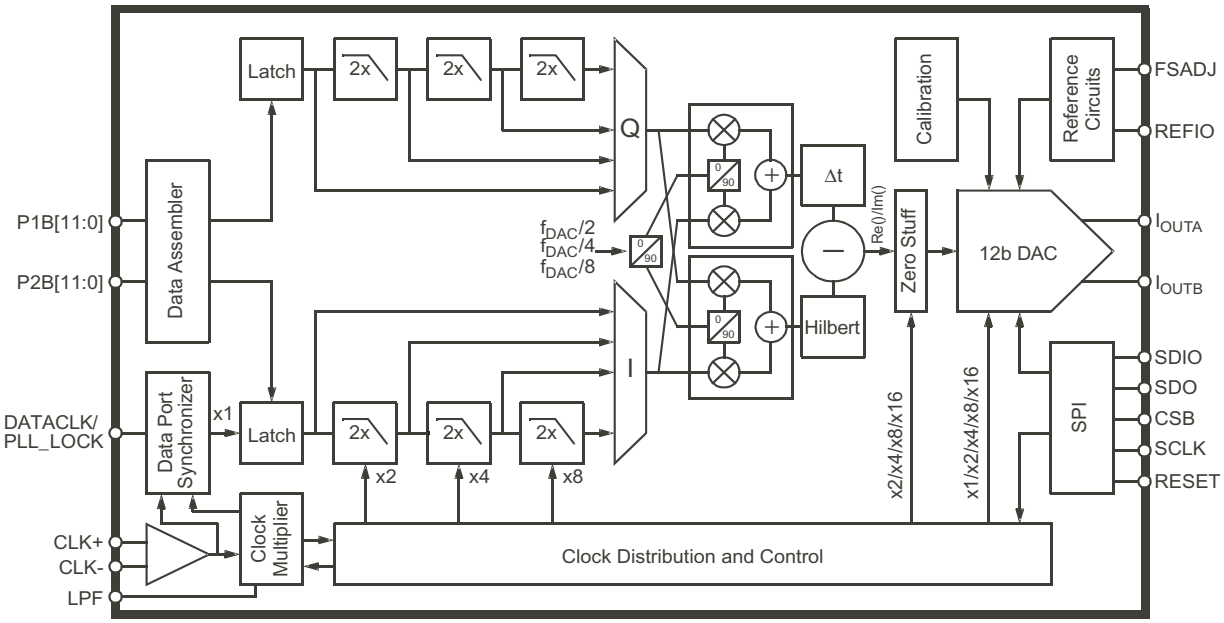
PRODUCT DESCRIPTION

The AD9782 is a 12 bit, high speed, CMOS DAC with 2×/4×/8× interpolation and signal processing features tuned for communications applications. It offers state of the art distortion and noise performance. The AD9782 was developed to meet the demanding performance requirements of multi-carrier and third generation basestations. The selectable interpolation filters simplify interfacing to a variety of input data rates while also taking advantage of oversampling performance gains. The modulation modes allow convenient bandwidth placement and selectable sideband suppression.

The flexible clock interface accepts a variety of input types such as 1V p-p sine wave LO inputs, CMOS clock inputs, single ended or differential inputs. Internal dividers generate data rate interface clocks.

The AD9782 provides a differential current output, supporting single-ended or differential applications; it provides a nominal full-scale current from 10 to 20mA. The AD9782 is manufactured on an advanced low cost 0.25µm CMOS process consuming <1W of power.

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT HIGHLIGHTS

1. The AD9782 is a member of the high speed interpolating TxDAC+s with 16/14/12 bit resolution.

2. 2×/4×/8× user selectable interpolating filter eases data rate and output signal reconstruction filter requirements.

3. 160MSPS input data rate.

4. Ultra high speed 400 MSPS DAC conversion rate.

5. Internal PLL/clock divider provides data rate clock for easy interfacing.

6. Flexible clock input with single-ended or differential input, CMOS or 1V pk-pk LO sinewave input capability.

7. Low Power: Complete CMOS DAC function operates on <1W from a 2.7 V to 3.6 V single analog (AVDD) supply and a 2.5 V (DVDD) digital supply. The DAC full-scale current can be reduced for lower power operation, and a sleep mode is provided for low-power idle periods.

8. On-chip Voltage Reference: The AD9782 includes a 1.20 V temperature-compensated bandgap voltage reference.

AD9782–SPECIFICATIONS

DC SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD1, AVDD2 = +3.3 V, ACVDD, ADVDD, CLKVDD, DVDD, DRVDD = +2.5v, I_{OUTFS} = 20 mA, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNITS
RESOLUTION		12		bits
DC Accuracy[1]				
Integral Non-Linearity		2.0		LSB
Differential Non-Linearity		1.5		LSB
ANALOG OUTPUT				
Offset Error				% of FSR
Gain Error (Without Internal Reference)				% of FSR
Gain Error (With Internal Reference)				% of FSR
Full-Scale Output Current[2]	10		20	mA
Output Compliance Range	–1.0		+1.0	V
Output Resistance		500		kΩ
Output Capacitance		3		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		1		µA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance (ext reference mode)		10		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Unipolar Offset Drift				ppm of FSR/°C
Gain Drift (Without Internal Reference)				ppm of FSR/°C
Gain Drift (With Internal Reference)				ppm of FSR/°C
Reference Voltage Drift				ppm/°C
POWER SUPPLY				
AVDD1, AVDD2				
Voltage Range	3.1	3.3	3.5	V
Analog Supply Current (I_{AVDD1})				mA
Analog Supply Current (I_{AVDD2})				mA
I_{AVDD1} in SLEEP Mode				mA
ACVDD, ADVDD				
Voltage Range	2.35	2.5	2.65	V
Analog Supply Current (I_{ACVDD})				mA
Analog Supply Current (I_{ADVDD})				mA
CLKVDD				
Voltage Range	2.35	2.5	2.65	V
Clock Supply Current (I_{CLKVDD})				mA
DVDD				
Voltage Range	2.35	2.5	2.65	V
Digital Supply Current (I_{DVDD})				mA
DRVDD				
Voltage Range	2.35	2.5/3.3	3.5	V
Digital Supply Current (I_{DRVDD})				mA
Nominal Total Power Dissipation		<1		W
OPERATING RANGE	–40		+85	°C

NOTES

[1]Measured at I_{OUTA} driving a virtual ground.

[2]Nominal full-scale current, I_{OUTFS}, is 32× the I_{REF} current.

[3]Use an external amplifier to drive any external load.

Specifications subject to change without notice.

AD9782–SPECIFICATIONS

DYNAMIC SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD1, AVDD2 = +3.3 V, ACVDD, ADVDD, CLKVDD, DVDD, DRVDD = +2.5v, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50Ω Doubly Terminated, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DYNAMIC PERFORMANCE				
Maximum DAC Output Update Rate (f_{DAC})	400			MSPS
Output Settling Time (t_{ST}) (to 0.025%)				ns
Output Propagation Delay[1] (t_{PD})				ns
Output Rise Time (10% to 90%)[2]				ns
Output Fall Time (90% to 10%)[2]				ns
Output Noise (I_{OUTFS} = 20 mA)				pA√Hz
AC LINEARITY–BASEBAND MODE				
Spurious-Free Dynamic Range (SFDR) to Nyquist (f_{OUT} = 0 dBFS)				
f_{DATA} = 160 MSPS; f_{OUT} = 1 MHz		87		dBc
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
f_{DATA} = MSPS; f_{OUT} = MHz				dBc
Two-Tone Intermodulation (IMD) to Nyquist (f_{OUT1} = f_{OUT2} = –6 dBFS)				
f_{DATA} = 160 MSPS; f_{OUT1} = 25 MHz; f_{OUT2} = 31 MHz		72		dBc
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
f_{DATA} = MSPS; f_{OUT1} = MHz; f_{OUT2} = MHz				dBc
Total Harmonic Distortion (THD)				
f_{DATA} = MSPS; f_{OUT} = MHz; 0 dBFS				dB
f_{DATA} = MSPS; f_{OUT} = MHz; 0 dBFS				dB
Signal-to-Noise Ratio (SNR)				
f_{DATA} = MSPS; f_{OUT} = MHz; 0 dBFS				dB
f_{DATA} = MSPS; f_{OUT} = MHz; 0 dBFS				dB
Adjacent Channel Power Ratio (ACPR)				
WCDMA with MHz BW, MHz Channel Spacing				
IF = 16 MHz, f_{DATA} = 65.536 MSPS				dBc
IF = 32 MHz, f_{DATA} = 131.072 MSPS				dBc
Four-Tone Intermodulation				
MHz, MHz, MHz and MHz at –12 dBFS				dBFS
(f_{DATA} = MSPS, Missing Center)				
AC LINEARITY–IF MODE				
Four-Tone Intermodulation at IF = MHz				
MHz, MHz, MHz and MHz at dBFS				dBFS
f_{DATA} = MSPS, f_{DAC} = MHz				

NOTES

[1]Propagation delay is delay from CLK input to DAC update.

[2]Measured single-ended into 50 Ω load.

Specifications subject to change without notice.

AD9782–SPECIFICATIONS

DIGITAL SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD1, AVDD2 = +3.3 V, ACVDD, ADVDD, CLKVDD, DVDD = +2.5v, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage	DRVDD-0.9	DRVDD		V
Logic "0" Voltage		0	0.9	V
Logic "1" Current[1]	–10		+10	µA
Logic "0" Current	–10		+10	µA
Input Capacitance		5		pF
CLOCK INPUTS				
Input Voltage Range	0		2.65	V
Common-Mode Voltage	0.75	1.5	2.25	V
Differential Voltage	0.5	1.5		V
PLL CLOCK ENABLED				
Input Setup Time (t_S)				ns
Input Hold Time (t_H)				ns
Latch Pulsewidth (t_{LPW})				ns
PLL CLOCK DISABLED				
Input Setup Time (t_S)				ns
Input Hold Time (t_H)				ns
Latch Pulsewidth (t_{LPW})				ns
CLK to PLLLOCK Delay (t_{OD})				ns

Pin Function Descriptions

Clock

Pin Number	Pin Name	Direction	Description		
	CLK+,CLK-	I	Differential clock input		
	LPF	I/O	PLL LOOP FILTER		
	DATACLK/ PLL_LOCK	I/O	PLOCKEXT 00h[0]	EXDCLK 02h[3]	Mode
			0	0	Pin configured for input of channel data rate or synchronizer clock. Internal clock synchronizer may be turned on or off with DCKDLLEN (02h[4])
			0	1	Pin configured for output of channel data rate or synchronizer clock
			1	X	Internal clock PLL status output 0: Internal clock PLL is not locked 1: Internal clock PLL is locked
	CLKVDD	-	Clock domain 2.5V		
	CLKCOM	-	Clock domain 0V		

Analog

Pin Number	Pin Name	Direction	Description
	REFIO	A	Reference
	FSADJ	A	Full scale adjust
	IOUTB, IOUTA	A	Differential DAC output currents
	NC	-	Do not connect
	ADVDD	-	Analogue domain digital content 2.5V
	ADCOM	-	Analogue domain digital content 0V
	ACVDD	-	Analogue domain clock content 2.5V
	ACCOM	-	Analogue domain clock content 0V
	AVDD2	-	Analogue domain switching 3.3V
	ACOM2	-	Analogue domain switching 0V
	AVDD1	-	Analogue domain quiet 3.3V
	ACOM1	-	Analogue domain quiet 0V

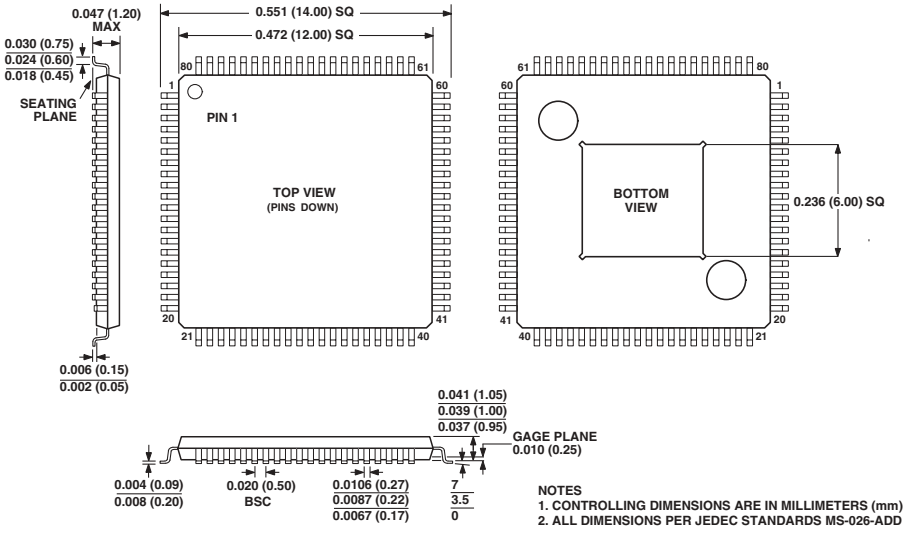
Data

Pin Number	Pin Name	Direction	Description			
	P1B11-P1B0	I	Input data port one			
			ONEPORT 02h[6]	Mode		
			0	Latched data routed for I channel processing		
			1	Latched data demultiplexed by IQSEL and routed for interleaved I/Q processing		
	IQSEL/P2B11	I	ONEPORT 02h[6]	IQPOL 03h[0]	IQSEL/ P2B15	Mode (IQPOL==0)
			0	X	X	Latched data routed to Q channel bit 15(MSB) processing
			1	0	0	Latched data on data port one routed to Q channel processing
			1	0	1	Latched data on data port one routed to I channel processing
			1	1	0	Latched data on data port one routed to I channel processing
			1	1	1	Latched data on data port one routed to Q channel processing
	ONEPORTCLK/ P2B10	I/O	ONEPORT 02h[6]			
			0	Latched data routed for Q channel bit 14 processing		
			1	Pin configured for output of clock at twice the channel data rate		
	P2B9-P2B0	I	Input data port two bits 9-0			
	DRVDD	-	Digital output pin supply, 2.5V or 3.3V			
	DVDD	-	Digital domain 2.5V			
	DCOM	-	Digital domain 0V			

Serial Interface

Pin Number	Pin Name	Direction	Description		
	SDO	O	CSB	SDIODIR 00h[7]	Mode
			1	X	High Impedance
			0	0	Serial data output
			0	1	High impedance
	SDIO	I/O	CSB	SDIODIR 00h[7]	Mode
			1	X	High Impedance
			0	0	Serial data input
			0	1	Serial data input/output depending on bit 7 of the serial instruction byte
	SCLK	I	Serial interface clock		
	CSB	I	Serial interface chip select		
	RESET	I	Resets entire chip to default state		

80-Lead Thermally Enhanced TQFP
(SV-80)
Dimensions shown in inches and (mm).



NOTES
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. ALL DIMENSIONS PER JEDEC STANDARDS MS-026-ADD

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called offset error. For I_{OUTA}, 0 mA output is expected when the inputs are all 0s. For I_{OUTB}, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s, minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (+25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per degree C. For reference drift, the drift is reported in ppm per degree C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from minimum to maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured fundamental. It is expressed as a percentage or in decibels (dB).

Signal-to-Noise Ratio (SNR)
S/N is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

Interpolation Filter
If the digital inputs to the DAC are sampled at a multiple rate of f_{DATA} (interpolation rate), a digital filter can be constructed which has a sharp transition band near $f_{DATA}/2$. Images which would typically appear around f_{DAC} (output data rate) can be greatly supressed.

Passband
Frequency band in which any input applied therein passes unattenuated to the DAC output.

Stopband Rejection
The amount of attenuation of a frequency outside the passband applied to the DAC, relative to a full-scale signal applied at the DAC input within the passband.

Group Delay
Number of input clocks between an impulse applied at the device input and peak DAC output current. A half-band FIR filter has constant group delay over its entire frequency range

Impulse Response
Response of the device to an impulse applied to the input.

Adjacent Channel Power Ratio (or ACPR)
A ratio in dBc between the measured power within a channel relative to its adjacent channel.

Complex Modulation
The process of passing the real and imaginary components of a signal through a complex modulator (transfer function = e^{jwt} = coswt+jsinwt) and realizing real and imaginary components on the modulator output.

Complex Image Rejection
In a traditional two part upconversion, two images are created around the second IF frequency. These images are redundant and have the effect of wasting transmitter power and system bandwidth. By placing the real part of a second complex modulator in series with the first complex modulator, either the upper or lower frequency image near the second IF can be rejected.

(T_{MIN} to T_{MAX}, AVDD1, AVDD2 = +3.3 V, ACVDD, ADVDD, CLKVDD, DVDD, DRVDD = +2.5v, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50Ω Doubly Terminated, unless otherwise noted)

TPC 1: Single-Tone Spectrum@ FDATA=65MSPS With FOUT=FDATA/3

TPC 2: In-Band SFDR Vs FOUT @FDATA=65MSPS

TPC 3: Out of Band SFDR Vs FOUT @FDATA=65MSPS

TPC 4: Single-Tone Spectrum@ FDATA=78MSPS With FOUT=FDATA/3

TPC 5: In-Band SFDR Vs FOUT @FDATA=78MSPS

TPC 6: Out of Band SFDR Vs FOUT @FDATA=78MSPS

TPC 7: Single-Tone Spectrum@ FDATA=160MSPS With FOUT=FDATA/3

TPC 8: In-Band SFDR Vs FOUT @FDATA=160MSPS

TPC 9: Out of Band SFDR Vs FOUT @FDATA=160MSPS

(T_{MIN} to T_{MAX}, AVDD1, AVDD2 = +3.3 V, ACVDD, ADVDD, CLKVDD, DVDD, DRVDD = +2.5v, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50Ω Doubly Terminated, unless otherwise noted)

TPC 10: Third Order IMD Products Vs FOUT @FDATA=65MSPS

TPC 11: Third Order IMD Products Vs FOUT @FDATA=78MSPS

TPC 12: Third Order IMD Products Vs FOUT @FDATA=160MSPS

TPC 13: Third Order IMD Products Vs FOUT and Interpolation Rate
1×-FDATA=160MSPS
2×-FDATA=160MSPS
4×-FDATA=80MSPS
8×-FDATA=50MSPS

TPC 14: Figure 14: Third Order IMD Products Vs AOUT and Interpolation Rate FDATA=50MSPS for All Cases
1×-FDAC=50MSPS
2×-FDAC=100MSPS
4×-FDAC=200MSPS
8×-FDAC=400MSPS

TPC 15: SFDR VS AVDD @ FOUT=10MHz, FDAC=320MSPS FDATA=160MSPS

TPC 16: 3rd Order IMD Products VS AVDD @ FOUT=10MHz, FDAC=320MSPS FDATA=160MSPS

TPC 17. SNR vs. Data Rate for f_{OUT} = 5MHz

TPC 18. SFDR vs. Temperature @ $f_{OUT}=f_{DATA}/11$

(T_{MIN} to T_{MAX}, AVDD1, AVDD2 = +3.3 V, ACVDD, ADVDD, CLKVDD, DVDD, DRVDD = +2.5v, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50Ω Doubly Terminated, unless otherwise noted)

TPC19. Single Tone Spurious Performance, F_{OUT}= 10MHz, F_{DATA}=150MSPS, No Interpolation

TPC20. Two Tone IMD Performance, F_{DATA}=150MSPS, No Interpolation

TPC21. Single Tone Spurious Performance, F_{OUT}= 10MHz, F_{DATA}=150MSPS, Interpolation = 2×

TPC22. Two Tone IMD Performance, F_{DATA}=90MSPS, Interpolation = 4×

TPC23. Single Tone Spurious Performance, F_{OUT}= 10MHz, F_{DATA}=80MSPS, Interpolation = 4×

TPC24. Two Tone IMD Performance, F_{OUT}= 10MHz, F_{DATA}=50MSPS, Interpolation = 8×

TPC25. Single Tone Spurious Performance, F_{OUT}= 10MHz, F_{DATA}=50MSPS, Interpolation = 8×

TPC26. Eight Tone IMD Performance, F_{DATA}=160MSPS, Interpolation = 8×

SERIAL CONTROL INTERFACE

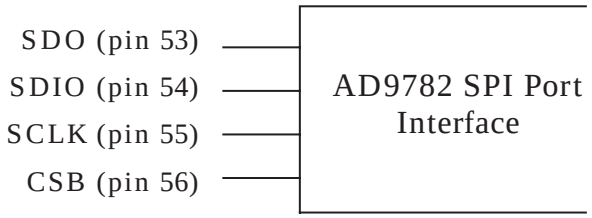


Figure 1. AD9782 SPI Port Interface

The AD9782 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI and Intel SSR protocols. The interface allows read/write access to all registers that configure the AD9782. Single or multiple byte transfers are supported as well as MSB first or LSB first transfer formats. The AD9782's serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO).

General Operation of the Serial Interface
There are two phases to a communication cycle with the AD9782. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9782, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9782 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9782.

A logic high on the CS pin, followed by a logic low, will reset the SPI port timing to the initial state of the instruction cycle. This is true regardless of the present state of the internal registers or the other signal levels present at the inputs to the SPI port. If the SPI port is in the midst of an instruction cycle or a data transfer cycle, none of the present data will be written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9782 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Normally, using one multibyte transfer is the preferred method. However, single byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change *immediately* upon writing to the last bit of each transfer byte.

Instruction Byte
The instruction byte contains the following information as shown below:

N1	N2	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

R/W- bit 7 of the instruction byte determines whether a read or a write data transfer will occur after the instruction byte write. Logic high indicates read operation . Logic zero indicates a write operation. N1, N0 -Bits 6 and 5 of the instruction byte determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in the following table:

MSB							LSB
I7	I6	I5	I4	I3	I2	I1	I0
R/W	N1	N0	A4	A3	A2	A1	A0

A4, A3, A2, A1, A0—Bits 4, 3, 2, 1, 0 of the instruction byte determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9782.

Serial Interface Port Pin Description
SCLK - Serial Clock. The serial clock pin is used to synchronize data to and from the AD9782 and to run the internal state machines. SCLK maximum frequency is 15 MHz. All data input to the AD9782 is registered on the rising edge of SCLK. All data is driven out of the AD9782 on the falling edge of SCLK.

CSB - Chip Select. Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDO and SDIO pins will go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

SDIO - Serial Data I/O. Data is always written into the AD9782 on this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 7 of register address 00h. The default is logic zero, which configures the SDIO pin as unidirectional.

SDO - Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9782 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB Transfers

The AD9782 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by register address 00h bit 6. The default is MSB first. When this bit is set active high, the AD9782 serial port is in LSB first format. That is, if the AD9782 is in LSB first mode, the instruction byte must be written from least significant bit to most significant bit. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the most significant byte. In MSB first mode, the serial port internal byte address generator decrements for each byte required of the multibyte communication cycle. Multibyte data transfers in LSB first format can be completed by writing an instruction byte that includes the register address of the least significant byte. In LSB first mode, the serial port internal byte address generator increments for each byte required of the multibyte communication cycle.

The AD9782 serial port controller address will increment from 1Fh to 00h for multibyte I/O operations if the MSB first mode is active. The serial port controller address will decrement from 00h to 1Fh for multibyte I/O operations if the LSB first mode is active.

Notes on Serial Port Operation

The AD9782 serial port configuration bits reside in bits 6 and 7 of register address 00h. It is important to note that the configuration changes *immediately* upon writing to the last bit of the register. For multibyte transfers, writing to this register may occur during the middle of communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

The same considerations apply to setting the reset bit in register address 00h. All other registers are set to their default values but the software reset doesn't affect the bits in register address 00h.

It is recommended to use only single byte transfers when changing serial port configurations or initiating a software reset.

A write to bits 1, 2 and 3 of address 00h with the same logic levels as for bits 7, 6 and 5 (bit pattern: XY1001YX binary) allows to reprogram a lost serial port configuration and to reset the registers to their default values. A second write to address 00h with Reset bit low and serial port configuration as specified above (XY) reprograms the OSC IN Multiplier setting. A changed f_{SYSCLK} frequency is stable after a maximum of 200 f_{MCLK} cycles (=Wake-Up Time).

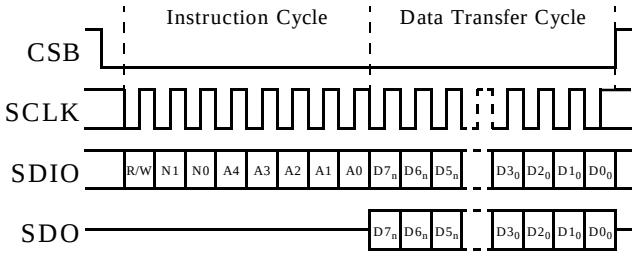


Figure 2a. Serial Register Interface Timing MSB-First

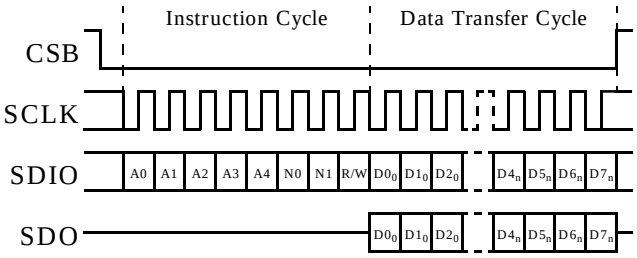


Figure 2b. Serial Register Interface Timing LSB-First

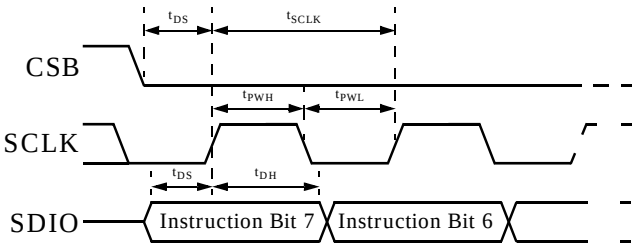


Figure 3. Timing Diagram for Register Write

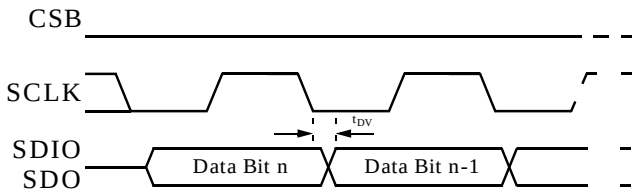


Figure 4.Timing Diagram for Register Read

Mode Control (via SPI Port)

Address	Name	Function	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	COMMCTRL	Communication control	SDIODIR	DATADIR	SWRST	SLEEP	PDN	RESERVED	PLLLOCK	PLOCKEXT
01	FILTMOD1	Filter mode 1	INTERP[1]	INTERP[0]	MOD[1]	MOD[0]	ZSTUFF	MODSING	SIDEBAND	EXREF
02	DATACTRL	Data port control	DATAFMT	ONEPORT	DCLKSTR	DCKDLLEN	EXDCLK	DLLSTAT[2]	DLLSTAT[1]	DLLSTAT[0]
03	FILTMOD2	Filter mode 2	CHANNEL	REALIMAG	HILBERT	HPFX8	HPFX4	HPFX2	DCLKPOL	IQPOL
04	PLLCHARG	PLL control	PLLON	PLLMULT[1]	PLLMULT[0]	PLLDIV[1]	PLLDIV[0]	RESERVED	RESERVED	RESERVED
05			RESERVED							
06			RESERVED							
07			RESERVED							
08			RESERVED							
09			RESERVED							
0A			RESERVED							
0B			RESERVED							
0C			RESERVED							
0D	VERSION	Silicon version					VERSION[3]	VERSION[2]	VERSION[1]	VERSION[0]
0E	CALMEMCK	Cal. memory clock ratio	MSTRFUSE		CALMEM[1]	CALMEM[0]		CALCKDIV[2]	CALCKDIV[1]	CALCKDIV[0]
0F	MEMRDWR	Cal. memory read/write	CALSTAT	CALEN	XFERSTAT	XFEREN	SMEMWR	SMEMRD	FMEMRD	UNCAL
10	MEMADDR	Cal. memory address	MEMADDR[7]	MEMADDR[6]	MEMADDR[5]	MEMADDR[4]	MEMADDR[3]	MEMADDR[2]	MEMADDR[1]	MEMADDR[0]
11	MEMDATA	Cal. memory data			MEMDATA[5]	MEMDATA[4]	MEMDATA[3]	MEMDATA[2]	MEMDATA[1]	MEMDATA[0]
12	SHUFSEED	Shuffler seed(1)		SHUFSEED[6]	SHUFSEED[5]	SHUFSEED[4]	SHUFSEED[3]	SHUFSEED[2]	SHUFSEED[1]	SHUFSEED[0]
13	SHUFCTRL	Shuffler seed(2)/control			RANDSEED[2]	RANDSEED[1]	RANDSEED[0]		RANDEN	SHUFEN
14			RESERVED							
15			RESERVED							
16			RESERVED							
17	SYNCPHAZ	Synchronizer offsets	DATADJ[3]	DATADJ[2]	DATADJ[1]	DATADJ[0]	MODSYNC	MODADJ[2]	MODADJ[1]	MODADJ[0]
18			RESERVED							
19			RESERVED							
1A			RESERVED							
1B			RESERVED							
1C			RESERVED							
1D			RESERVED							
1E			RESERVED							
1F			RESERVED							

COMMCTRL (00)	Bit	DIrection	Default	Description
SDIODIR	7	I	0	0: SDIO pin configured for input only during data transfer 1: SDIO pin configured for input or output during data transfer
DATADIR	6	I	0	0: Serial data uses MSB first format 1: Serial data uses LSB first format
SWRST	5	I	0	1: Default all serial register bits, except address 00h
SLEEP	4	I	0	1: DAC output current off
PDN	3	I	0	1: All analog and digital circuitry, except serial interface, off
RESERVED	2	O	0	RESERVED
PLLLOCK	1	O	0	0: With PLL on, indicates PLL is not locked 1: With PLL on, indicates PLL is locked
PLOCKEXT	0	I	0	0: With PLL on, DATACLK/PLL_LOCK pin configured for DATACLK input/output 1: With PLL on, DATACLK/PLL_LOCK pin configured for output of PLLLOCK

FILTMOD1 (01)	Bit	Direction	Default	Description
INTERP[1:0]	[7:6]	I	00	00: No Interpolation 01: Interpolation X2 10: Interpolation X4 11: Interpolation X8
MOD[1:0]	[5:4]	I	00	00: No Modulation 01: fs/2 Modulation 10: fs/4 Modulation 11: fs/8 Modulation
ZSTUFF	3	I	0	1: Zero stuffing on
MODSING	2	I	0	0: Modulator uses a single channel 1: Modulator uses both I and Q channels
SIDEBAND	1	I	0	0: With MODSING on, upper sideband rejected 1: With MODSING on, lower sideband rejected
EXREF	0	I	0	0: Internal bandgap reference 1: External reference

DATACTRL (02)	Bit	Direction	Default	Description
DATAFMT	7	I	0	0: 2's complement input data format 1: Unsigned binary input data format
ONEPORT	6	I	0	0: I and Q input data onto ports 1 and 2 respectively 1: I and Q input data interleaved onto port 1
DCLKSTR	5	I	0	0: DATACLK pin 12mA drive strength 1: DATACLK pin 24mA drive strength
DCKDLLEN	4	I	0	0: With PLOCKEXT off and DATACLK pin as input, DATACLK DLL off 1: With PLOCKEXT off and DATACLK pin as input, DATACLK DLL on
EXDCLK	3	I	0	0: With PLOCKEXT off, DATACLK pin inputs channel data rate or modulator synchronizer clock 1: With PLOCKEXT off, DATACLK pin outputs channel data rate or modulator synchronizer clock
DLLSTAT[2]	2	O	0	0: With DATACLK DLL on, lock has never been achieved 1: With DATACLK DLL on, lock has been achieved at some time
DLLSTAT[1]	1	O	0	0: With DATACLK DLL on, loop has not needed to slip a phase to maintain lock 1: With DATACLK DLL on, after initial lock the loop has moved phase to relock
DLLSTAT[0]	0	O	0	0: With DATACLK DLL on, loop has no cycle jitter 1: With DATACLK DLL on, loop has cycle jitter but is less than the loop bandwidth

FILTMOD2 (03)	Bit	Direction	Default	Description
CHANNEL	7	I	0	0: With MODSING off, I channel processing routed to DAC 1: With MODSING off, Q channel processing routed to DAC
REALIMAG	6	I	0	0: With MODSING on, real output routed to DAC 1: With MODSING on, imaginary output routed to DAC
HILBERT	5	I	0	0: With MODSING on, hilbert transform off 1: With MODSING on, hilbert transform on
HPFX8	4	I	0	0: X8 interpolation filter configured for low pass 1: X8 interpolation filter configured for high pass
HPFX4	3	I	0	0: X4 interpolation filter configured for low pass 1: X4 interpolation filter configured for high pass
HPFX2	2	I	0	0: X2 interpolation filter configured for low pass 1: X2 interpolation filter configured for high pass
DCLKPOL	1	I	0	0: PLOCKEXT off,DATACLK as input,DATACLK DLL off,data latched on DATACLK rising edge 1: PLOCKEXT off,DATACLK as input,DATACLK DLL off,data latched on DATACLK falling edge
IQPOL	0	I	0	0: In one port mode; IQSEL=1 latches data into I channel, IQSEL=0 latches data into Q channel 1: In one port mode; IQSEL=0 latches data into Q channel, IQSEL=1 latches data into I channel

PLLCHARG (04)	Bit	Direction	Default	Description
PLLON	7	I	0	0: PLL off 1: PLL on
PLLMULT[1:0]	[6:5]	I	00	PLL multiply factor 00: x2 01: x4 10: x8 11: x16
PLLDIV[1:0]	[4:3]	I	00	PLLMULT rate divide factor 00: /1 01: /2 10: /4 11: /8

VERSION (0D)	Bit	Direction	Default	Description
VERSION[3:0]	[3:0]	O	-	Hardware version indentifier

CALMEMCK (0E)	Bit	Direction	Default	Description
MSTRFUSE	7	O	0	0: Master fuse is blown 1: Master fuse is not blown
FUSEWR	6	I	0	1: Write fuse memory data from external parallel port
CALMEM	[5:4]	O	00	Calibration memory 00: Uncalibrated 01: Self calibration 10: Factory calibration 11: User input
CALCKDIV[2:0]	[2:0]	I	000	Calibration clock divide ratio from channel data rate 000: /32 001: /64 : 110: /2048 111: /4096

MEMRDWR (0F)	Bit	Direction	Default	Description
CALSTAT	7	O	0	0: Calibration cycle not complete 1: Calibration cycle complete
CALEN	6	I	0	1: Calibration in progress
XFERSTAT	5	O	0	0: Factory fuse transfer not complete 1: Factory fuse transfer complete
XFEREN	4	I	0	1: Fuse transfer in progress
SMEMWR	3	I	0	1: Write static memory data from external port
SMEMRD	2	I	0	1: Read static memory to external port
FMEMRD	1	I	0	1: Read fuse memory data to external port
UNCAL	0	I	0	1: Use uncalibrated

MEMADDR (10)	Bit	Direction	Default	Description
MEMADDR[7:0]	[7:0]	I/O	00000000	Address of fuse or static memory to be accessed

MEMDATA (11)	Bit	Direction	Default	Description
MEMDATA[5:0]	[5:0]	I/O	00000	Data for fuse or static memory access

SHUFSEED (12)	Bit	Direction	Default	Description
SHUFSEED[6:0]	[6:0]	I	0000000	Shuffler PN generator seed

SHUFCTRL (13)	Bit	Direction	Default	Description
RANDSEED[2:0]	[5:3]	I	000	Randomiser PN generator seed
RANDEN	1	I	0	0: Randomiser off 1: Randomiser on
SHUFEN	0	I	0	0: Shuffler off 1: Shuffler on

SYNCPHAZ (17)	Bit	Direction	Default	Description
DATADJ[3:0]	[7:4]	I	0000	Dataclock offset. Two's complement representation 0111: +7 : 0000: 0 : 1000: -8
MODSYNC	3	I	0	0: With PLOCKEXT off ,state machine clock synchronization mode 1: With PLOCKEXT off, channel data rate clock synchronization mode

MODADJ[2:0]	[2:0]	I	000		fs/8	fs/4	fs/2	Modulator coefficient offset
				000	1	1	1	
				001	$1/\sqrt{2}$	0	-1	
				010	0	-1	1	
				011	$-1/\sqrt{2}$	0	-1	
				100	-1	1	1	
				101	$-1/\sqrt{2}$	0	-1	
				110	0	-1	1	
				111	$1/\sqrt{2}$	0	-1	

DIGITAL FILTER SPECIFICATIONS

Table I: Digital Interpolation Filter Coefficients

Stage 1 Interpolation Filter Coefficients

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(43)	9
H(2)	H(42)	0
H(3)	H(41)	-27
H(4)	H(40)	0
H(5)	H(39)	65
H(6)	H(38)	0
H(7)	H(37)	-131
H(8)	H(36)	0
H(9)	H(35)	239
H(10)	H(34)	0
H(11)	H(33)	-407
H(12)	H(32)	0
H(13)	H(31)	665
H(14)	H(30)	0
H(15)	H(29)	-1070
H(16)	H(28)	0
H(17)	H(27)	1764
H(18)	H(26)	0
H(19)	H(25)	-3273
H(20)	H(24)	0
H(21)	H(23)	10358
H(22)		16384

Stage 2 Interpolation Filter Coefficients

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(19)	19
H(2)	H(18)	0
H(3)	H(17)	-120
H(4)	H(16)	0
H(5)	H(15)	436
H(6)	H(14)	0
H(7)	H(13)	-1284
H(8)	H(12)	0
H(9)	H(11)	5045
H(10)		8192

Stage 3 Interpolation Filter Coefficients

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(11)	7
H(2)	H(10)	0
H(3)	H(9)	-53
H(4)	H(8)	0
H(5)	H(7)	302
H(6)		512

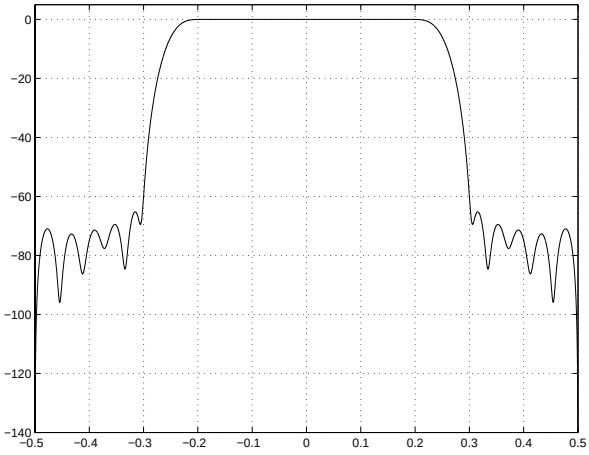


Figure 5a. x2 Interpolation Filter Response

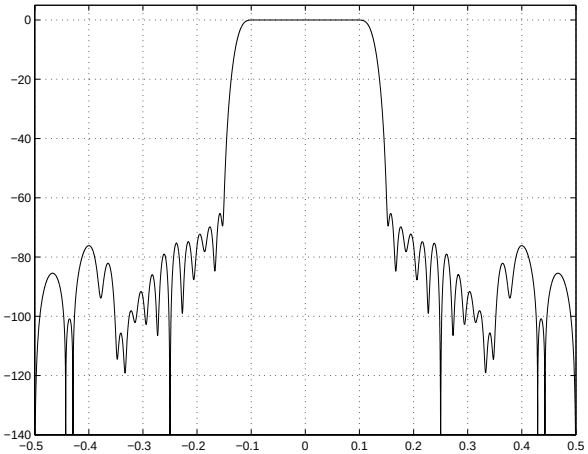


Figure 5b. x4 Interpolation Filter Response

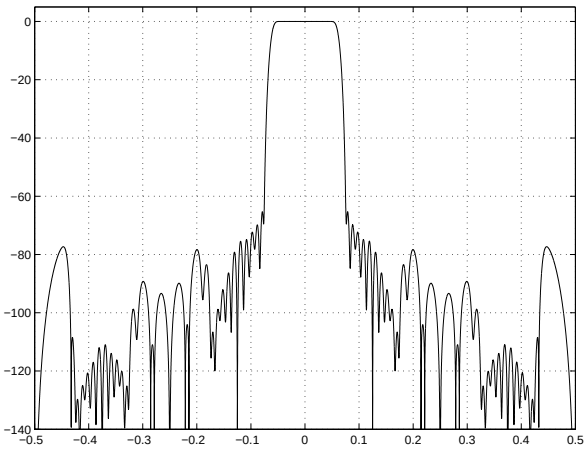


Figure 5c. x8 Interpolation Filter Response

INTERPOLATION MODES

INTERP[1]	INTERP[0]	Mode
0	0	No Interpolation
0	1	x2 Interpolation
1	0	x4 Interpolation
1	1	x8 Interpolation

Interpolation is the process of increasing the number of points in a time domain waveform by approximating points between the input data points; on a uniform time grid this produces a higher output data rate. Applied to an interpolation DAC, a digital interpolation filter is used to approximate the interpolated points, having an output data rate increased by the interpolation factor. Interpolation filter responses are achieved by cascading individual digital filter banks, whose filter coefficients are given in table I; filter responses are shown figure 5.

The digital filters frequency domain response exhibits symmetry about half the output data rate and dc. It will cause images of the input data to be shaped by the interpolation filter's frequency response. This has the advantage of causing input data images which fall in the stop band of the digital filter to be rejected by the stop band attenuation of the interpolation filter; input data images falling in the interpolation filter's passband will be passed. In bandlimited applications the images at the output of the DAC must be limited by an analog reconstruction filter. The complexity of the analog reconstruction filter is determined by the proximity of the closest image to the required signal band. Higher interpolation rates yield larger stop band regions, suppressing more input images and resulting in a much relaxed analog reconstruction filter.

A DAC shapes it's output with a sinc function, having a null at the sampling frequency of the DAC. The higher the DAC sampling rate compared to the input signal bandwidth, the less the DAC sinc function will shape the output. Figure 6 shows the interpolation filters of the AD9782 under different interpolation rates, normalised to the input data rate, fs_{in}. The higher the interpolation rate the more input data images fall in the interpolation filter stop band and are rejected; the bandwidth between passed images is larger with higher interpolation factors. The sinc function shaping is also reduced with higher interpolation factor.

Mode	sinc shaping at $0.43fs_{in}$	bandwidth to first image
No Interpolation	-2.8241dB	fs_{in}
x2 Interpolation	-0.6708dB	$2fs_{in}$
x4 Interpolation	-0.1657dB	$4fs_{in}$
x8 Interpolation	-0.0413dB	$8fs_{in}$

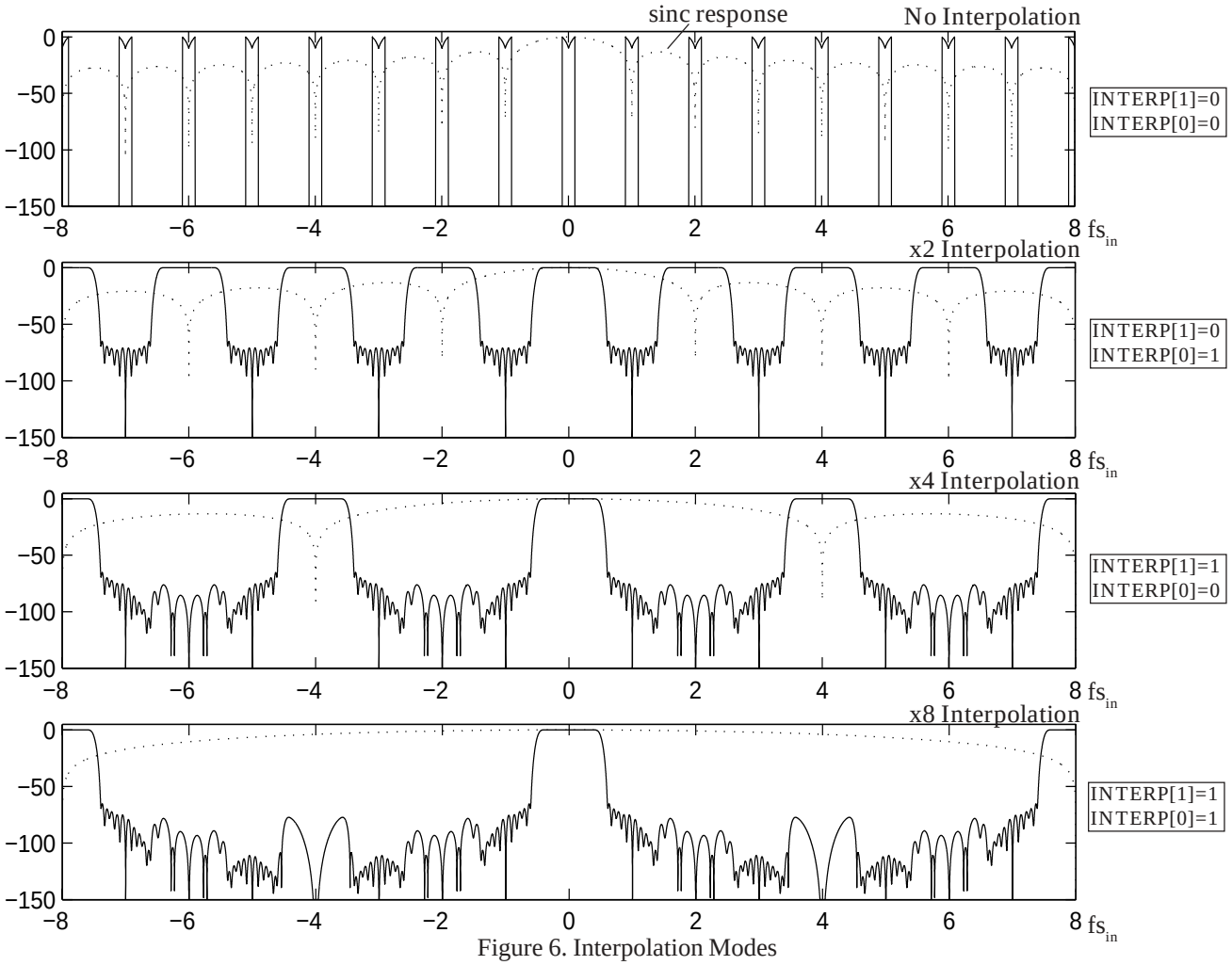
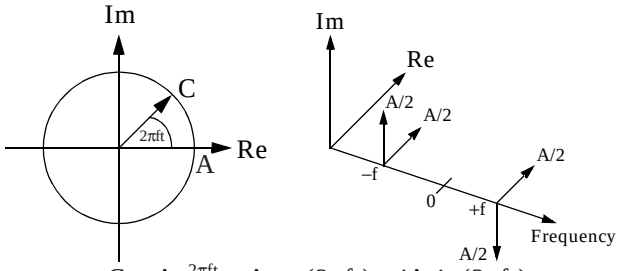


Figure 6. Interpolation Modes

REAL AND COMPLEX SIGNALS

A complex signal contains both magnitude and phase information. Given two signals at the same frequency, if a point in time can be taken such that the signal which leads in phase is cosinusoidal and the signal which lags is sinusoidal, then information pertaining to the magnitude and phase of a combination of the two signals can be derived; the combination of the two signals can be considered a complex signal. The cosine and sine can be represented as a series of exponentials; recalling that a multiplication by j is a counter clockwise rotation about the Re/Im plane, the phasor representation of a complex signal, with frequency f, can be shown figure 7.



$$C = Ae^{2\pi ft} = A\cos(2\pi ft) + jA\sin(2\pi ft)$$

$$A\cos(2\pi ft) = A\left[\frac{e^{j2\pi ft} + e^{-j2\pi ft}}{2}\right] = \frac{A}{2}\left[e^{j2\pi ft} + e^{-j2\pi ft}\right]$$

$$A\sin(2\pi ft) = A\left[\frac{e^{j2\pi ft} - e^{-j2\pi ft}}{2j}\right] = \frac{A}{2}\left[je^{j2\pi ft} - je^{-j2\pi ft}\right]$$

Figure 7. Complex Phasor Representation

The cosine term represents a signal on the real plane with mirror symmetrical about dc; this is referred to as the real, in-phase or I component of a complex signal. The sine term represents a signal on the imaginary plane with mirror asymmetrical about dc; this term is referred to as the imaginary, quadrature or Q complex signal component.

The AD9782 has two channels of interpolation filters, allowing both I and Q components to be shaped by the same filter transfer function. The interpolation filters' frequency response is a real transfer function. Two DACs are required to represent a complex signal. A single DAC can only synthesize a real signal. When a DAC synthesizes a real signal, negative frequency components fold onto the positive frequency axis. If the input to the DAC is mirror symmetrical about dc, the folded negative frequency components fold directly onto the positive frequency components in phase producing constructive signal summation. If the input to the DAC is not mirror symmetric about dc negative frequency components may not be in phase with positive frequency components and will cause destructive signal summation. Different applications may or may not benefit from either type of signal summation.

MODULATIONMODES

Single Channel Modulation

MODSING CHANNEL	MOD[1]	MOD[0]	Mode
1	0	0	0	Q Channel, no modulation
1	0	0	1	Q Channel, modulation by $f_{DAC}/2$
1	0	1	0	Q Channel, modulation by $f_{DAC}/4$
1	0	1	1	Q Channel, modulation by $f_{DAC}/8$
1	1	0	0	I Channel, no modulation
1	1	0	1	I Channel, modulation by $f_{DAC}/2$
1	1	1	0	I Channel, modulation by $f_{DAC}/4$
1	1	1	1	I Channel, modulation by $f_{DAC}/8$

Either channel of the AD9782's interpolation filter channels can be routed to the DAC and modulated. In single channel operation the input data may be modulated by a real sinusoid; the input data and the modulating sinusoid will contain both positive and negative frequency components. A double sideband output results when modulating two real signals. At the DAC output the positive and negative frequency components will add in phase resulting in constructive signal summation.

As the modulating sinusoidal frequency becomes a larger fraction of the DAC update rate, f_{DAC}, the more the sinc function of the DAC shapes the modulated signal bandwidth, and the closer the first image moves. As the AD9782 interpolation filter's passband represents a large portion of the input data's nyquist band, under certain modulation and interpolation modes it is possible

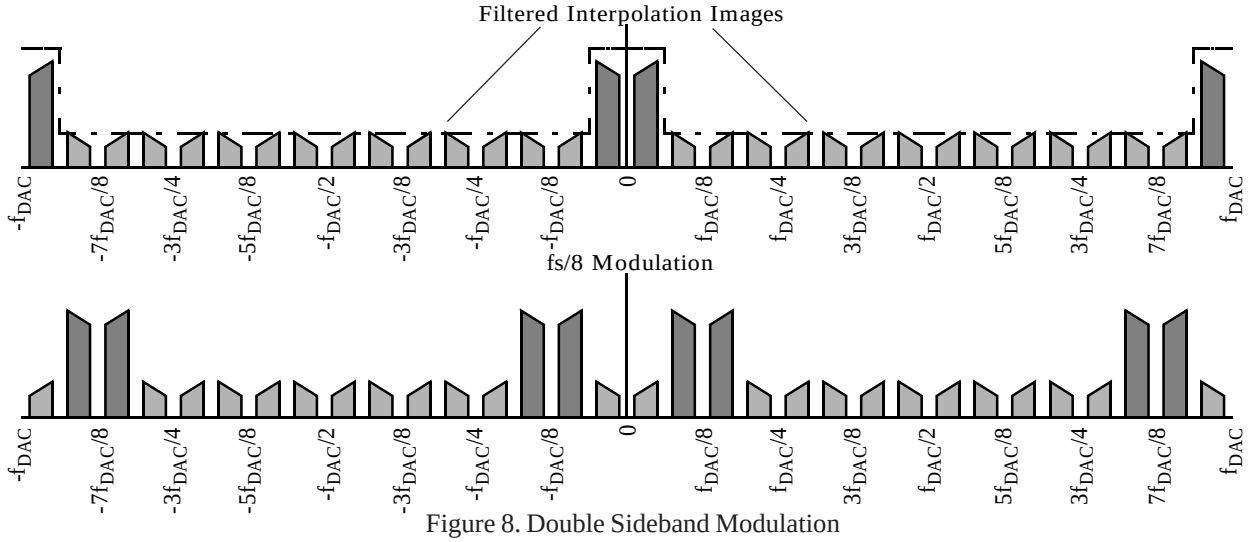


Figure 8. Double Sideband Modulation

for modulated signal bands to touch or overlap images if sufficient interpolation is not used.

Figure 9 shows the effect of real modulation under all interpolation modes. The sinc shaping at the corners of the modulated signal band and the bandwidth to the first image for those cases whose passbands do not touch or overlap are tabulated.

Modulation	Interpolation			
	none	x2	x4	x8
none	fs_{in}	$2fs_{in}$	$4fs_{in}$	$8fs_{in}$
$f_{DAC}/2$	fs_{in}	$2fs_{in}$	$4fs_{in}$	$8fs_{in}$
$f_{DAC}/4$	overlap	touching	$2fs_{in}$	$4fs_{in}$
$f_{DAC}/8$	overlap	overlap	touching	$6fs_{in}$

Bandwidth to first image

Modulation	Interpolation			
	none	x2	x4	x8
none	0	0	0	0
	-2.8241	-0.6708	-0.1657	-0.0413
$f_{DAC}/2$	-0.0701	-1.1932	-2.3248	-3.0590
	-22.5378	-9.1824	-6.1190	-4.9337
$f_{DAC}/4$	overlap	touching	-0.2921	-0.5974
			-1.9096	-1.3607
$f_{DAC}/8$	overlap	overlap	touching	-0.0727
				-0.4614

Modulated passband edges sinc shaping(lower/upper)

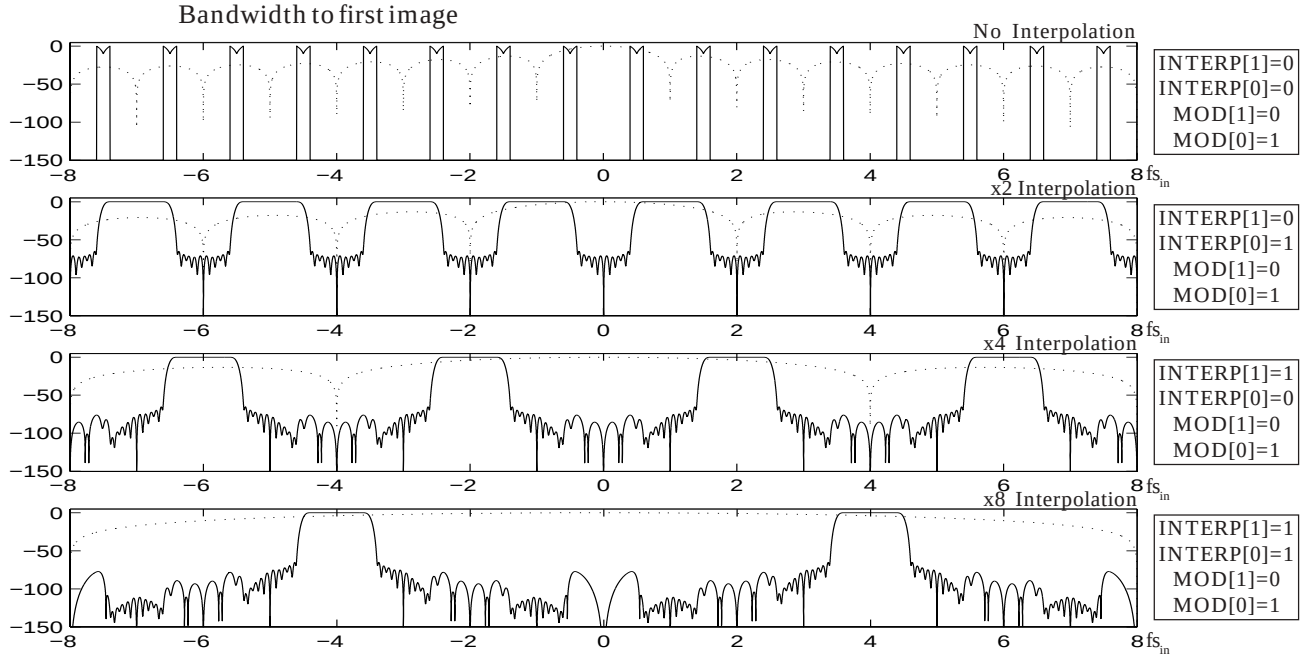


Figure 9a. Real modulation by $f_{DAC}/2$ under all interpolation modes

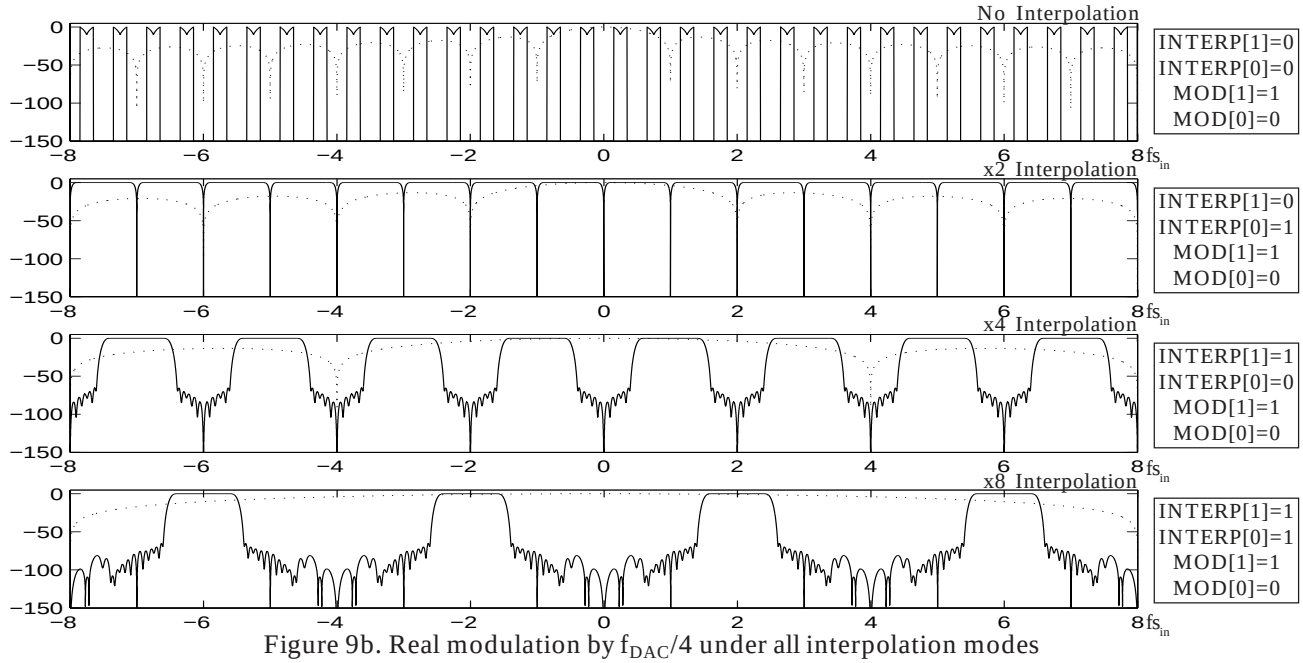


Figure 9b. Real modulation by $f_{DAC}/4$ under all interpolation modes

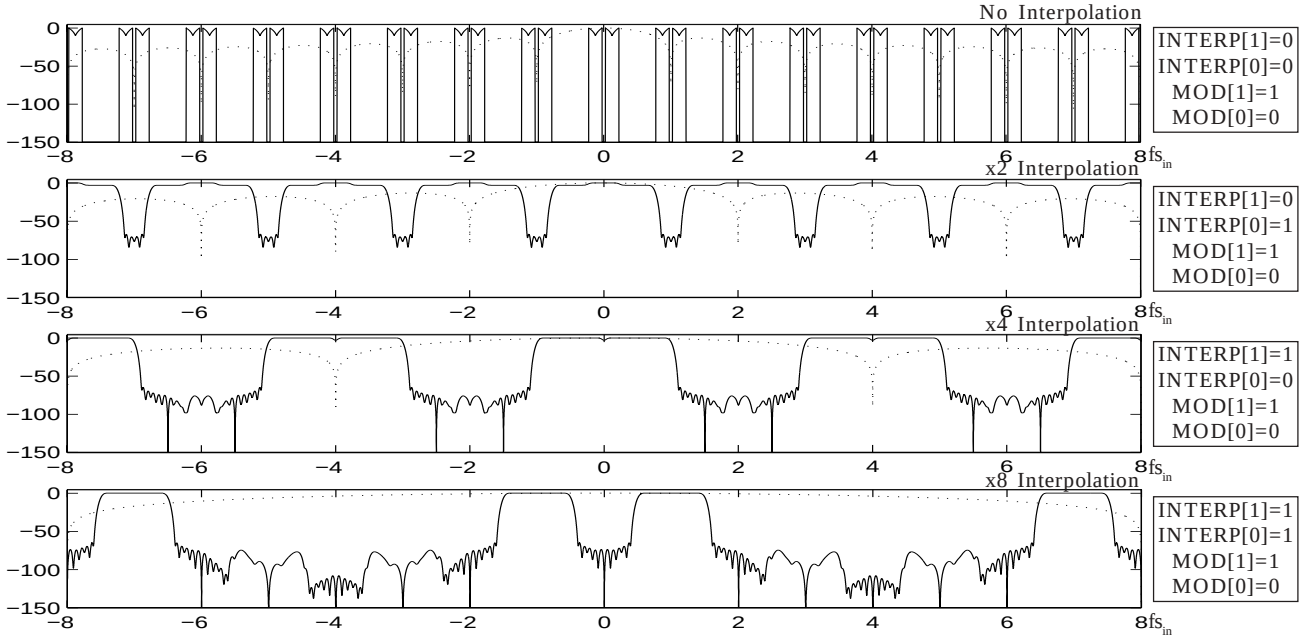


Figure 9c. Real modulation by $f_{DAC}/8$ under all interpolation modes

Dual Channel Complex Modulation

MODSING	REALIMAG	MOD[1]	MOD[0]	Mode
0	0	0	0	Real output, no modulation
0	0	0	1	Real output, modulation by $f_{DAC}/2$
0	0	1	0	Real output, modulation by $f_{DAC}/4$
0	0	1	1	Real output, modulation by $f_{DAC}/8$
0	1	0	0	Imag output, no modulation
0	1	0	1	Imag output, modulation by $f_{DAC}/2$
0	1	1	0	Imag output, modulation by $f_{DAC}/4$
0	1	1	1	Imag output, modulation by $f_{DAC}/8$

In dual channel mode the two channels may be modulated by a complex signal, with either the real or imaginary modulation result directed to the DAC. Assume initially that the complex modulating signal is defined for a positive frequency only; this causes the output spectrum to be translated in frequency by the modulation factor only. No additional sidebands are created as a result of the modulation process,and hence the bandwidth to the first image from the baseband bandwidth is the same as the output of the interpolation filters; furthermore, passbands will not overlap or touch. The sinc shaping at the corners of the modulated signal band are tabulated. Figure 11 shows the complex modulations.

Modulation	Interpolation			
	none	x2	x4	x8
none	0	0	0	0
	-2.8241	-0.6708	-0.1657	-0.0413
$f_{DAC}/2$	-0.0701	-1.1932	-2.3248	-3.0590
	-22.5378	-9.1824	-6.1190	-4.9337
$f_{DAC}/4$	-0.4680	-0.0175	-0.2921	-0.5974
	-8.0630	-3.3447	-1.9096	-1.3607
$f_{DAC}/8$	-1.3723	-0.1160	-0.0044	-0.0727
	-4.9592	-1.7195	-0.7866	-0.4614

Modulated passband edges sinc shaping(lower/upper)

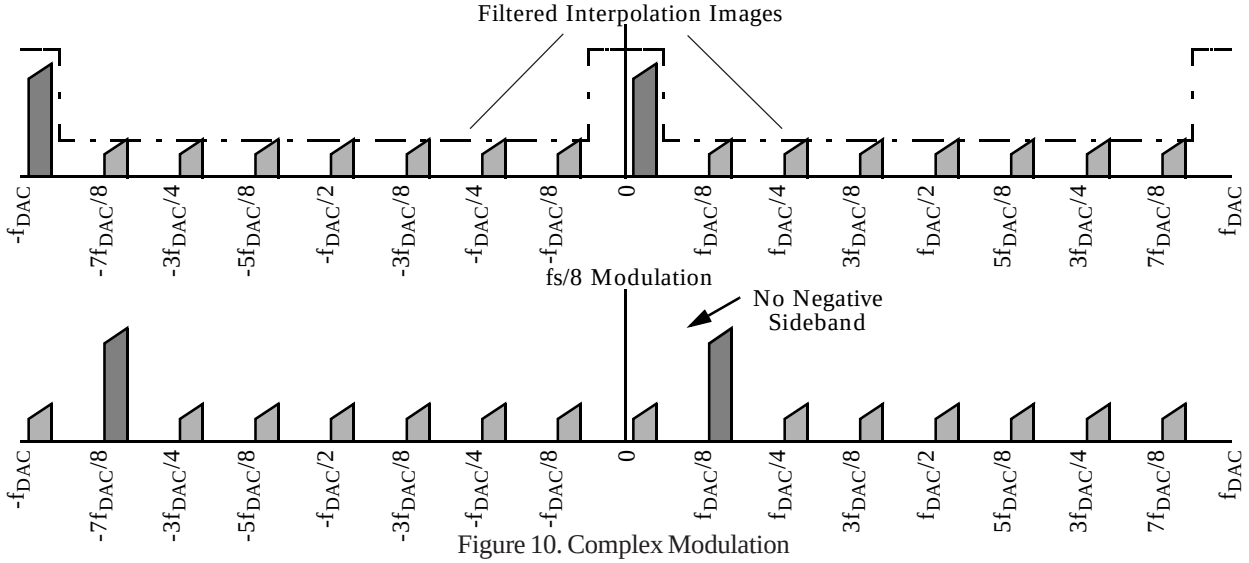


Figure 10. Complex Modulation

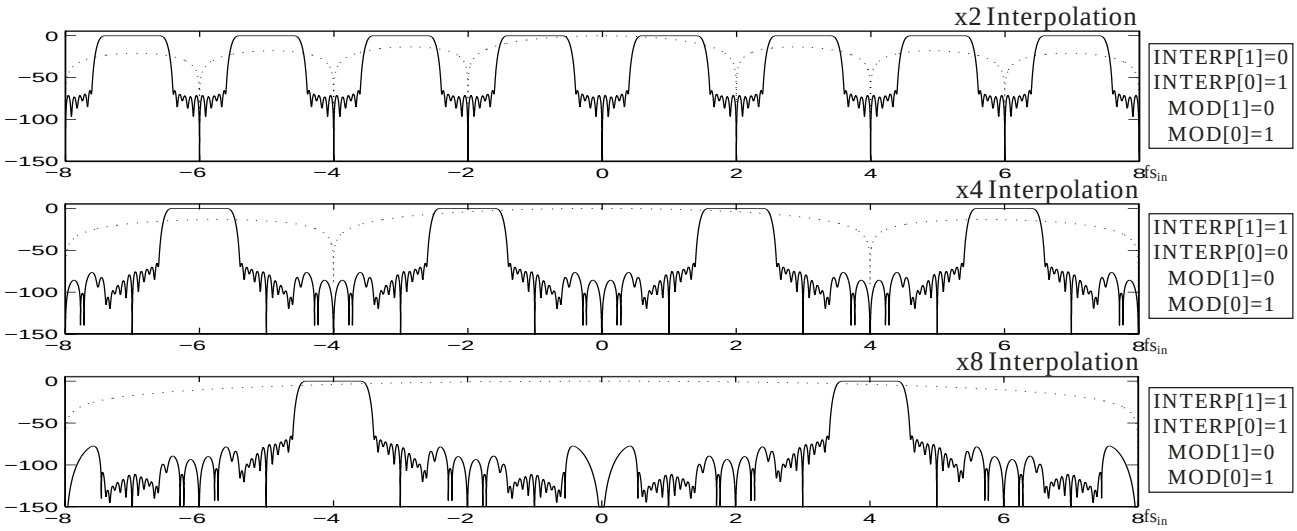


Figure 11a. Complex Modulation by $f_{DAC}/2$ under all interpolation modes

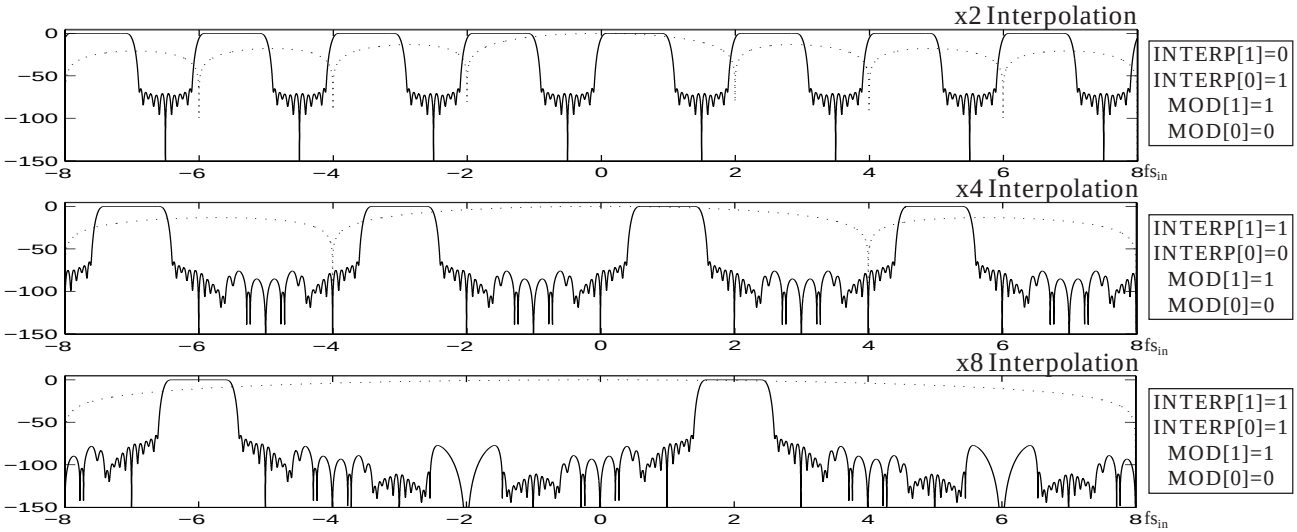


Figure 11b. Complex Modulation by $f_{DAC}/4$ under all interpolation modes

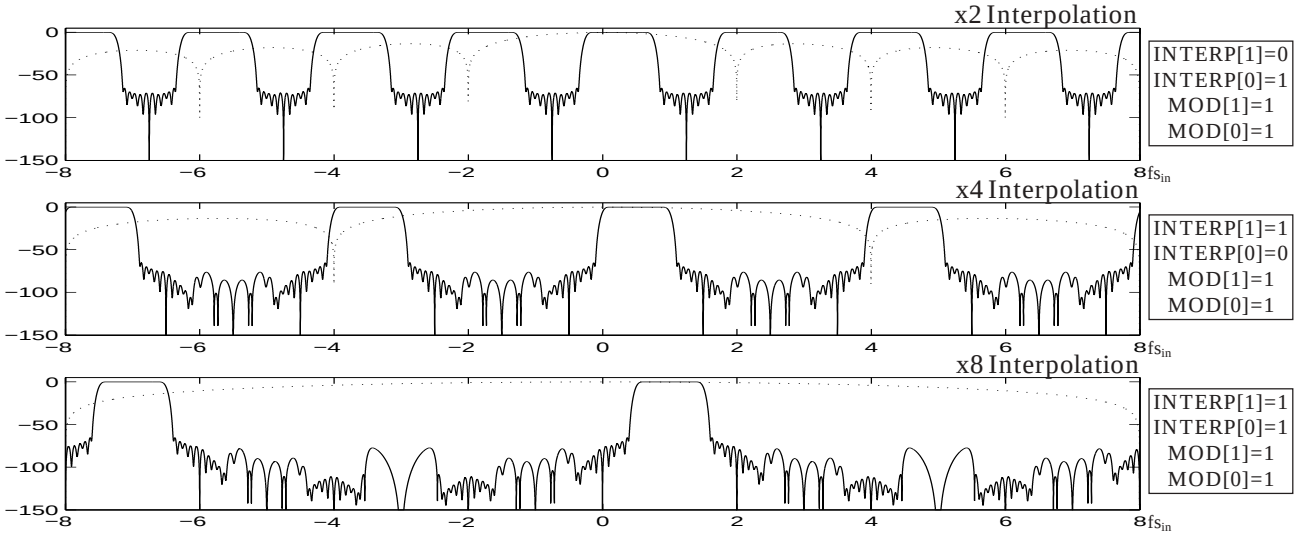


Figure 11c. Complex Modulation by $f_{DAC}/8$ under all interpolation modes

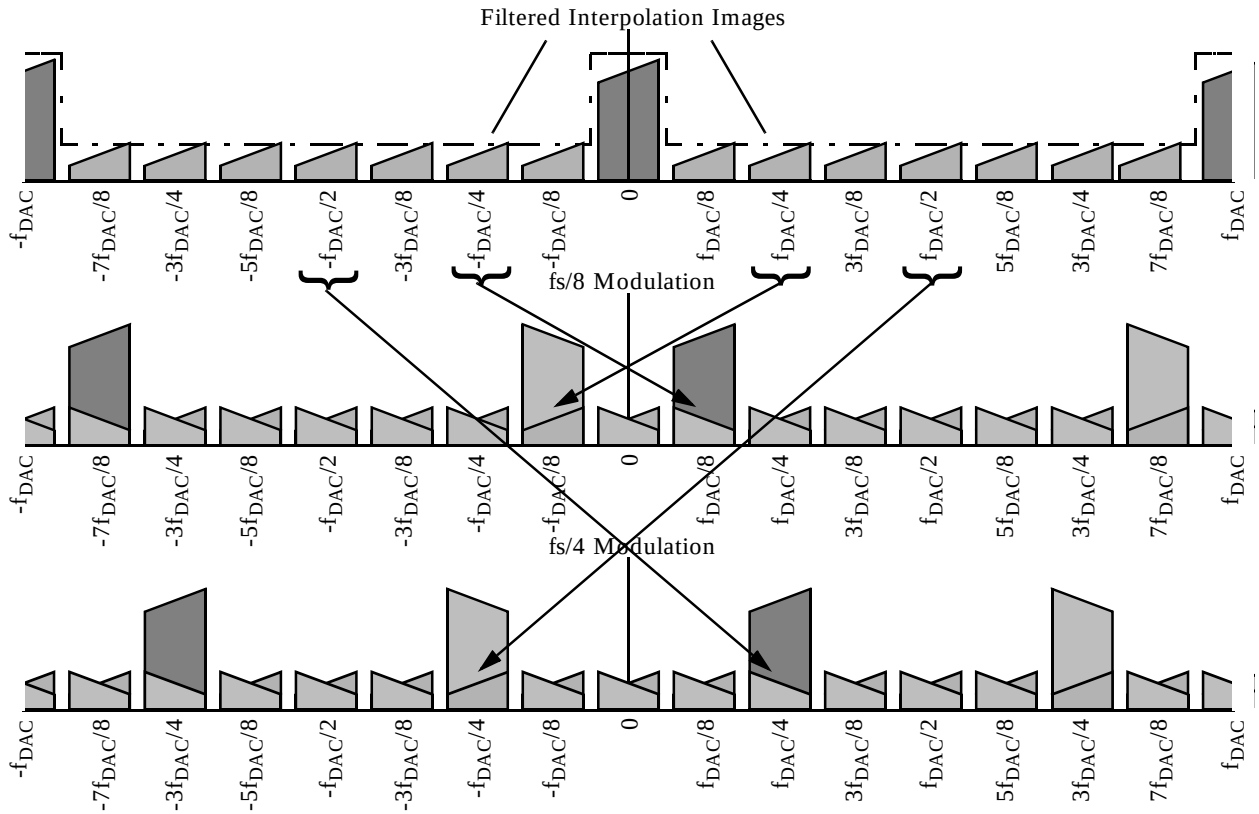


Figure 12. Complex modulation with negative frequency aliasing

Dual Channel Complex Modulation with Hilbert

HILBERT	Mode
0	Hilbert transform off
1	Hilbert transform on

When complex modulation is performed, the entire spectrum is translated by the modulation factor. If the resulting modulated spectrum is not mirror symmetric about dc,when the DAC synthesizes the modulated signal negative frequency components will fall on the positive frequency axis and can cause destructive summation of the signals. For some applications this can be seen as distorting the

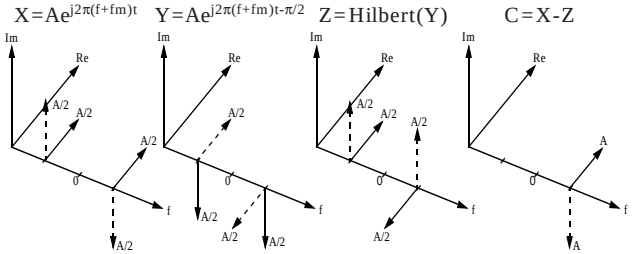


Figure 13. Negative frequency image rejection

modulated output signal. By performing a second complex modulation with a modulating signal having a fixed π/2 phase difference, figure 13(Y), relative to the original complex modulation signal, figure 13(X), taking the Hilbert transform of the new resulting complex modulation, and subtracting it from the original complex modulation output all negative frequency components can be folded in phase to the positive frequency axis before being synthesized by the DAC. When the DAC synthesizes the modulated output there are no negative frequency components to fold onto the positive frequency axis out of phase; consequently no distortion is produced as a result of the modulation process.

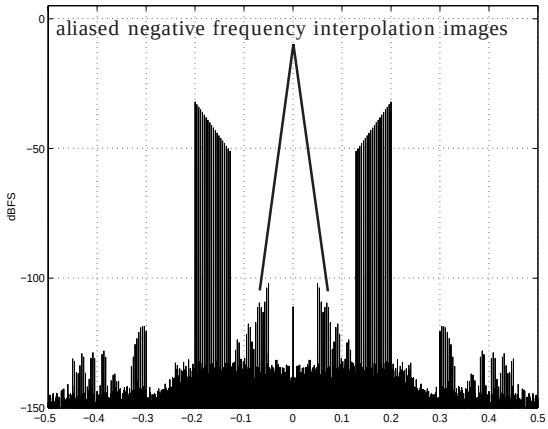


Figure 14. Negative frequency aliasing distortion

Figure 14 shows this effect at the DAC output for a mirror asymmetic signal about dc produced by complex modulation without a Hilbert transform. The signal bandwidth was narrowed to show the aliased negative frequency interpolation images.

In contrast figure 15 shows the same waveform with the Hilbert transform applied. Clearly the aliased interpolation images are not present.

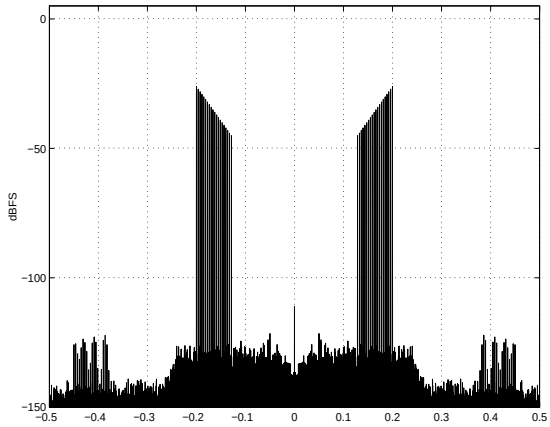


Figure 15. Effects of Hilbert transform

If the output of the AD9782 is to be used with a quadrature modulator, negative frequency images are cancelled without the need of a Hilbert transform.

Dual Channel Complex Modulation Sideband Selection

SIDEBAND	Mode
0	Upper IF sideband rejected
1	Lower IF sideband rejected

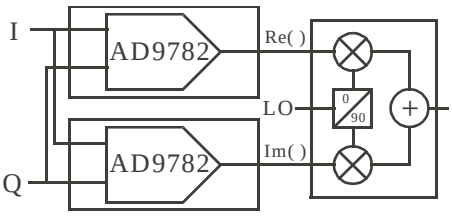


Figure 16. AD9782 Driving Quadrature Modulator

The AD9782 can be configured to drive a quadrature modulator, representatively as in figure 16. Where two AD9782 are used with one AD9782 producing the real output, the second AD9782 producing the imaginary output. By configuring the AD9782 as a complex modulator coupled to a quadrature modulator,IF image rejection is possible. The quadrature modulator acts as the real part of a complex modulation producing a double sideband spectrum at the local oscillator (LO) frequency, with mirror symmetry about dc.

A baseband double sideband signal modulated to IF increases IF filter complexity and reduces power efficiency. If the baseband signal is complex, a single sideband IF modulation can be used, relaxing IF filter complexity and increasing power efficiency.

The AD9782 has the ability to place the baseband single sideband complex signal either above the IF frequency or below it, figure 18 illustrates the baseband selection.

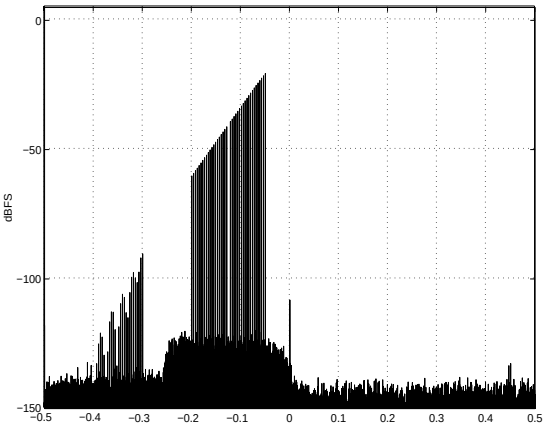


Figure 18a. Upper IF sideband rejected

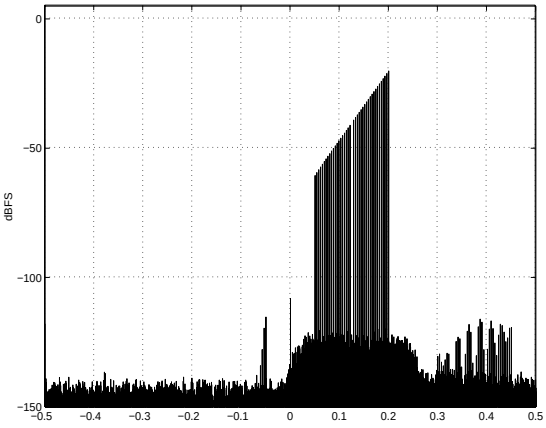


Figure 18b. Lower IF sideband rejected

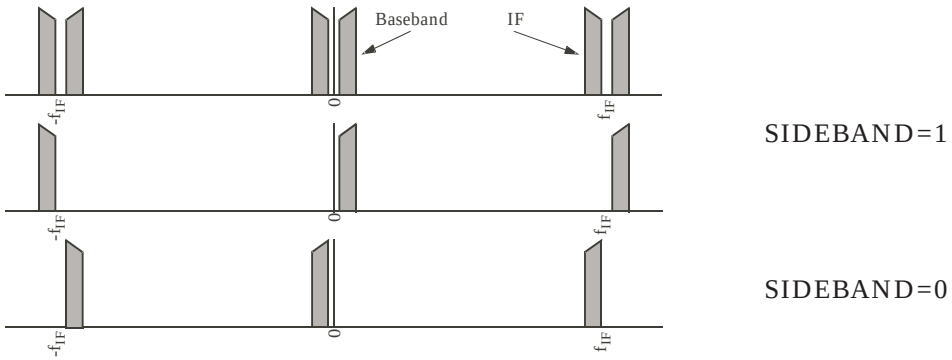


Figure 17. IF quadrature modulation of real and complex baseband signals

Data Port Synchronization

PLOCKEXT	EXDCLK	MODSYNC	DCKDLLEN	Mode	Function
1	X	X	X	PLL output	PLL locked flag output, synchronizer disabled
0	0	0	X	Dataclk Master	Channel data rate clock output
0	0	1	X	Modulator Master	Modulator synchronization clock output
0	1	0	0	Dataclk Slave	Input channel data rate clock, DLL off
0	1	0	1	Dataclk Slave	Input channel data rate clock, DLL on
0	1	1	0	Modulator Slave	Input modulator synchronizer clock, DLL off
0	1	1	1	Modulator Slave	Input modulator synchronizer clock, DLL on

In applications where two or more AD9782 are used to synthesize several digital data paths, it may be necessary to ensure that the digital inputs to each device are latched synchronously. In complex data processing applications, digital modulator phase alignment may be required between two AD9782. In order to allow data synchronisation and phase alignment, only one AD9782 should be configured as a master device, providing a reference clock for other slave configured AD9782.

With synchronisation enabled, a reference clock signal is generated on the DATACLK/PLL_LOCK pin of the master. The DATACLK/PLL_LOCK pins on the slave devices act as inputs for the reference clock generated by the master. The DATACLK/PLL_LOCK pin on the master and all slaves must be directly connected. All master and slave devices must have the same clock source connected to their respective CLK+/CLK- pins.

When configured as a master, the reference clock generated may take one of two forms. In modulator master mode, the reference clock will be a square wave with a period equal to sixteen cycles of the DAC update clock. Internal to the AD9782 is a sixteen state finite state machine, running at the DAC update rate. This state machine generates all internal and external synchronisation clocks and modulator phasings. The rising edge of the master reference clock is time aligned to the internal state machine's state zero. Slave devices use the master's reference clock to synchronise their data latching and align their modulator's phase by aligning their local state machine state zero to the master.

The second master mode, dataclk master mode, generates a reference clock which is at the channel data rate. In this mode the slave devices align their internal channel data rate clock to the master. If modulator phase alignment is needed, a concurrent serial write to all slave devices is necessary. To achieve this, the CSB pin on all slaves must be connected together and a group serial write to the MODADJ register bits performed; the modulator coefficient alignment will be updated on the next rising edge of the internal state machine following a successful serial write, figure 19. Modulator master mode does not need a concurrent serial write as slaves lock to the master phase automatically.

In a slave device, the local channel data rate clock and the digital modulator clock are created from the internal state machine. The local channel data rate clock is used by the slave to latch digital input data. At high data rates, the delay inherent in the signal path from master to slave may cause the slave to lag the master when acquiring synchronisation. To account for this, an integer number of the DAC update clock cycles may be programmed into the slave device as an offset. The value in DATADJ allows the local channel data rate clock in the slave device to advance by up to eight cycles of the DAC clock or delayed by up to seven cycles, figure 20.

The digital modulator coefficients are updated at the DAC clock rate and decoded in sequential order from the state machine according to figure 21. The MODADJ bits can be used to align a different coefficient to the finite state machine's zero state as shown in figure 22.

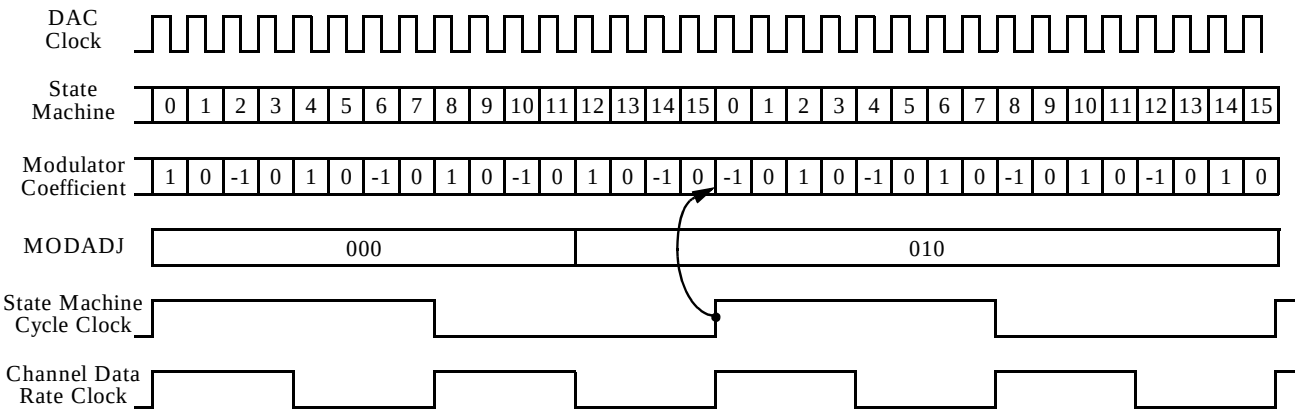


Figure 19. Synchronous Serial Modulator Phase Alignment

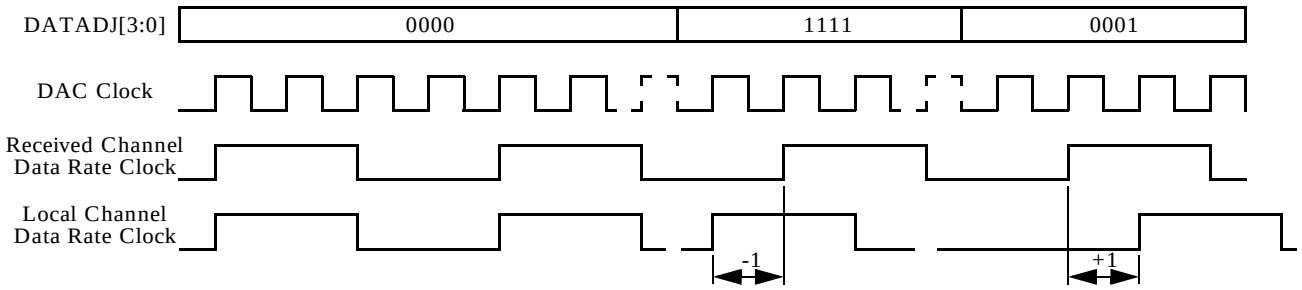


Figure 20. Local Channel Data Rate Clock Synchronised with Offset

State	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Decode	1	0	$1/\sqrt{2}$	0	0	0	$-1/\sqrt{2}$	0	-1	0	$-1/\sqrt{2}$	0	0	0	$1/\sqrt{2}$	0
fs/8	0	→	1	→	2	→	3	→	4	→	5	→	6	→	7	→
fs/4	0	→			1	→			2	→			3	→		
fs/2	0	→							1	→						

Figure 21. Digital Modulator State Machine Decode.

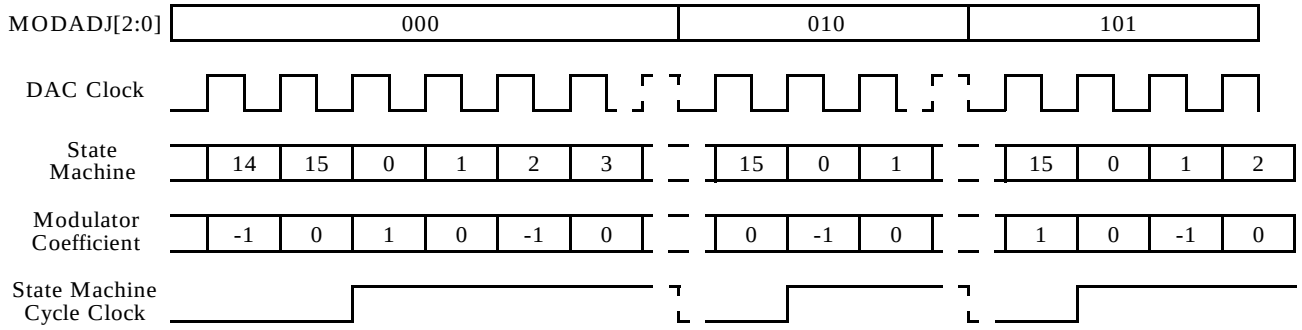


Figure 22. Local Modulator Coefficient Synchronised with Offset

When a device is configured as a master, its data clock offset value DATADJ and modulator phase adjust value MODADJ have no effect. Regardless of the synchronisation mode, the MODSYNC bit on master and slave devices must be in the same state.