Broadband Modem Mixed-Signal Front End

AD9975

FEATURES

Low Cost, 3.3 V-CMOS, Mixed Signal, Front End Converter for Broadband Modems
10-Bit D/A Converter (TxDAC+®)
- 50 MSPS Input Word Rate
- 2× Interpolating Low-Pass Transmit Filter
- 100 MSPS DAC Output Update Rate
- Wide (21 MHz) Transmit Bandwidth
- Power-Down Modes

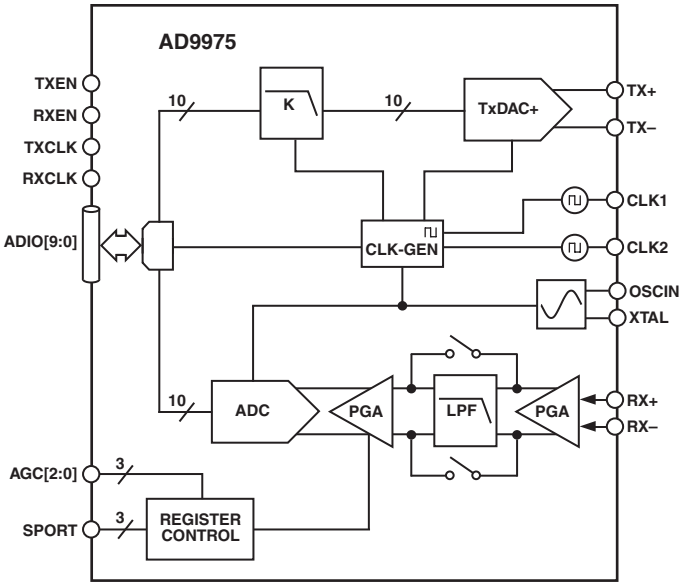
10-Bit, 50 MSPS A/D Converter
- Fourth Order LPF with Selectable Cutoff Frequency
- Dual Mode Programmable Gain Amplifier

Internal Clock Multiplier (PLL)
Two Auxiliary Clock Outputs
48-Lead LQFP Package

APPLICATIONS

Powerline Networking
Home Phone Networking

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9975 is a single-supply, broadband modem, mixed signal, front end (MxFE™) IC. The device contains a transmit path interpolation filter and DAC and a receive path PGA, LPF, and ADC required for a variety of broadband modem applications. Also on-chip is a PLL clock multiplier that provides all required clocks from a single crystal or clock input.

The TxDAC+ uses a digital 2× interpolation low-pass filter to oversample the transmit data and ease the complexity of analog reconstruction filtering. The transmit path bandwidth is 21 MHz when sampled at 100 MSPS. The 10-bit DAC provides differential current outputs. The DAC full-scale current can be adjusted from 2 to 20 mA by a single resistor, providing 20 dB of additional gain range.

The receive path consists of a PGA, LPF, and ADC. The programmable gain amplifier (PGA) has two modes of operation. One mode allows programming through the serial port and provides a gain range from –6 dB to +36 dB in 2 dB steps. The other mode allows the gain to be controlled through an asynchronous 3-pin port and offers a gain range from 0 dB to 48 dB in 8 dB steps with the use of an external gain stage. The receive path LPF cutoff frequency can be selected to either 12 MHz or 26 MHz. The filter cutoff frequency can also be tuned or bypassed where filter requirements differ. The 10-bit ADC uses a multistage differential pipeline architecture to achieve excellent dynamic performance with low power consumption.

The digital transmit and receive ports are multiplexed onto a 10-bit databus and have individual TX/RX clocks and TX/RX enable lines. This interface connects directly to Homelug 1.0 PHY/MAC chips from Intellon and Conexant.

The AD9975 is available in a space-saving 48-lead LQFP package. The device is specified over the commercial (–40°C to +85°C) temperature range.

REV. 0

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AD9975–SPECIFICATIONS

(V_S = 3.3 V ±10%, F_{OSCIN} = 50 MHz, F_{DAC} = 100 MHz, Gain = –6 dB, R_{SET} = 4.02 kΩ, 100 Ω DAC Load.)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
OSC IN CHARACTERISTICS						
Frequency Range	Full	I	10		50	MHz
Duty Cycle	25°C	II	40	50	60	%
Input Capacitance	25°C	III		3		pF
Input Impedance	25°C	III		100		MΩ
CLOCK OUTPUT CHARACTERISTICS						
CLKA Jitter (F_{CLKA} Derived from PLL)	25°C	II		14		ps rms
CLKA Duty Cycle	25°C	III		50 ±5		%
TX CHARACTERISTICS						
2× Interpolation Filter Characteristics						
TX Path Latency, 2× Interpolation	Full	II		30		F_{DAC} Cycles
Pass-Band Flatness 0 MHz to 20.7 MHz	Full	II		0.8		dB
Stop-Band Rejection @ 29.3 MHz	Full	II		35		dB
TxDAC						
Resolution	Full	II		10		Bits
Conversion Rate	Full	II	10		100	MHz
Full-Scale Output Current	Full	II	2	10	20	mA
Voltage Compliance Range (TX+ or TX– AVSS)	Full	II	–0.5		+1.5	V
Gain Error	25°C	II	–5.5	±2	+5.0	%FS
Output Offset	25°C	II	0	2	TBD	µA
Differential Nonlinearity	25°C	III		0.5		LSB
Integral Nonlinearity	25°C	II			1	LSB
Output Capacitance	25°C	III		5		pF
Phase Noise @ 1 kHz Offset, 10 MHz Signal	25°C	III		–100		dBc/Hz
Signal-to-Noise and Distortion (SINAD)						
5 MHz Analog Out (20 MHz BW)	25°C	II		–60.6		dB
Wideband SFDR (to Nyquist, 50 MHz max)	25°C	III				
5 MHz Analog Out	25°C	III		–76.2		dBc
Narrowband SFDR (3 MHz Window)						
5 MHz Analog Out	25°C	III		–77.9		dBc
IMD (f1 = 6.25 MHz, f2 = 7.8125 MHz)	25°C	III		–77		dBFS
RX PATH CHARACTERISTICS (LFP Bypassed)						
Resolution	N/A	N/A		10		Bits
Conversion Rate	Full	II	10		50	MHz
Pipeline Delay, ADC Clock Cycles	N/A	N/A		5.5		Cycles
Dynamic Performance (A_{IN} = –0.5 dBFS, f = 5 MHz)						
@ F_{OSCIN} = 50 MHz, RX LPF Bypassed						
Signal-to-Noise and Distortion Ratio (SINAD)	Full	III		–56.6		dB
Effective Number of Bits (ENOB)	Full	III		9.1		Bits
Signal-to-Noise Ratio (SNR)	Full	III		–59.2		dB
Total Harmonic Distortion (THD)	Full	III		–60.1		dB
Spurious-Free Dynamic Range (SFDR)	Full	III		–66		dB
RX PATH GAIN/OFFSET						
Minimum Programmable Gain	25°C	I		–6		dB
Maximum Programmable Gain						
Narrow Band Rx LPF or Rx LPF Bypassed	25°C	I		+36		dB
Wideband Rx LPF	25°C	I		+30		dB
Gain Step Size	25°C	I		2		dB
Gain Step Accuracy	25°C	II		±0.4		dB
Gain Range Error	Full	II		±1.0		dB
Absolute Gain Error, PGA Gain = 0 dB	Full	II		±0.8		dB
RX PATH INPUT CHARACTERISTICS						
Input Voltage Range (Gain = –6 dB)	Full	III		4		Vppd
Input Capacitance	25°C	III		4		pF
Differential Input Resistance	25°C	III		270		Ω
Input Bandwidth (–3 dB) (Rx LPF Bypassed)	25°C	III		50		MHz
Input Referred Noise (at +36 dB Gain with Filter)	25°C	III		16		µV rms
Input Referred Noise (at –6 dB Gain with Filter)	25°C	III		684		µV rms
Common-Mode Rejection	25°C	III		40		dB

Parameter	Temp	Test Level	Min	Typ	Max	Unit
RX PATH LPF (Low Cutoff Frequency)						
Cutoff Frequency	Full	III		12		MHz
Cutoff Frequency Variation	Full	III		±7		%
Attenuation @ 22 MHz	Full	III		20		dB
Pass-Band Ripple	Full	II		±1.0		dB
Group Delay Variation	Full	II		30		ns
Settling Time (to 1% FS, Min to Max Gain Change)	25°C	II		150		ns
Total Harmonic Distortion at Max Gain (THD)	Full	I		–61		dBc
RX PATH LPF (High Cutoff Frequency)						
Cutoff Frequency	Full	III		26		MHz
Cutoff Frequency Variation	Full	III		±7		%
Attenuation @ 35 MHz	Full	III		20		dB
Pass-Band Ripple	Full	II		±1.2		dB
Group Delay Variation	Full	II		15		ns
Settling Time (to 1% FS, Min to Max Gain Change)	25°C	II		80		ns
Total Harmonic Distortion at Max Gain (THD)	Full	I		–61		dBc
RX PATH DIGITAL HPF						
Latency (ADC Clock Source Cycles)				1		Cycle
Roll-Off in Stop Band				6		dB/Octave
–3 dB Frequency				f_{ADC} /400		Hz
POWER-DOWN/DISABLE TIMING						
Power-Down Delay (Active-to-Power-Down)						
DAC	25°C	II			200	ns
Interpolator	25°C	II			200	ns
Power-Up Delay (Power-Down-to-Active)						
DAC	25°C	II			10	µs
PLL	25°C	II			10	µs
ADC	25°C	II			1000	µs
PGA	25°C	II			1	µs
LPF	25°C	II			1	µs
Interpolator	25°C	II			200	ns
Minimum RESET Pulsewidth Low (t_{RL})	Full	III			5	f_{OSCIN} Cycles
ADIO PORT INTERFACE						
Maximum Input Word Rate	25°C	I	100			MHz
TX-Data Setup Time (t_{SU})	25°C	II	3.0			ns
TX-Hold Hold Time (t_{HD})	25°C	II	0			ns
RX-Data Valid Time(t_{VT})	25°C	II			3.0	ns
RX-Data Hold Time (t_{HT})	25°C	II	1.5			ns

SPECIFICATIONS (continued)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
SERIAL CONTROL BUS						
Maximum SCLK Frequency (f_{SCLK})	Full	II	25			MHz
Clock Pulsewidth High (t_{PWH})	Full	II	18			ns
Clock Pulsewidth Low (t_{PWL})	Full	II	18			ns
Clock Rise/Fall Time	Full	II			10	µs
Data/Chip-Select Setup Time (t_{DS})	Full	II	25			ns
Data Hold Time (t_{DH})	Full	II	0			ns
Data Valid Time (t_{DV})	Full	II			20	ns
CMOS LOGIC INPUTS						
Logic "1" Voltage	25°C	II	V_{DRVDD} – 0.7			V
Logic "0" Voltage	25°C	II			0.4	V
Logic "1" Current	25°C	II			12	µA
Logic "0" Current	25°C	II			12	µA
Input Capacitance	25°C	III		3		pF
CMOS LOGIC OUTPUTS (1 mA Load)						
Logic "1" Voltage	Full	II	V_{DRVDD} – 0.6			V
Logic "0" Voltage	25°C	II			0.4	V
Digital Output Rise/Fall Time	Full	II	1.5		2.5	ns
POWER SUPPLY						
All Blocks Powered Up						
I_{S_TOTAL} (Total Supply Current)	25°C	I		210	227	mA
Digital Supply Current (I_{DRVDD} + I_{DVDD})	25°C	III		22.5		mA
Clock Supply Current (I_{CLKVDD})	25°C	III		5.5		mA
Analog Supply Current (I_{AVDD})	25°C	III		182		mA
Power Consumption of Functional Blocks						
Rx LPF	25°C	III		110		mA
ADC and SPGA	25°C	III		55		mA
Rx Reference	25°C	III		2		mA
Interpolator	25°C	III		20		mA
DAC	25°C	III		18		mA
PLL-A	25°C	III		22		
All Blocks Powered Down						
I_{S_TOTAL} (Total Supply Current)	25°C	I		21	27	mA
Digital Supply Current (I_{DRVDD} + I_{DVDD})	25°C	III		10		mA
Clock Supply Current (I_{CLKVDD})	25°C	III		0		mA
Analog Supply Current (I_{AVDD})	25°C	III		11		mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Power Supply (V_S) . . . . . 3.9 V
Digital Output Current . . . . . 5 mA
Digital Inputs . . . . . –0.3 V to DRVDD + 0.3 V
Analog Inputs . . . . . –0.3 V to AVDD + 0.3 V
Operating Temperature . . . . . –40°C to +85°C
Maximum Junction Temperature . . . . . 150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . 300°C

*Absolute Maximum Ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

EXPLANATION OF TEST LEVELS

I. Devices are 100% production tested at 25°C and guaranteed by design and characterization testing for the commercial operating temperature range (–40°C to +85°C).
II. Parameter is guaranteed by design and/or characterization testing.
III. Parameter is a typical value only.

THERMAL CHARACTERISTICS

Thermal Resistance

48-Lead LQFP
θ_{JA} = 57°C/W
θ_{JC} = 28°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9975ABST	–40°C to +85°C	48-Lead LQFP	ST-48
AD9975ABSTEB	–40°C to +85°C	AD9975 EVAL Board	
AD9975ABSTRL	–40°C to +85°C	AD9975ABST Reel	

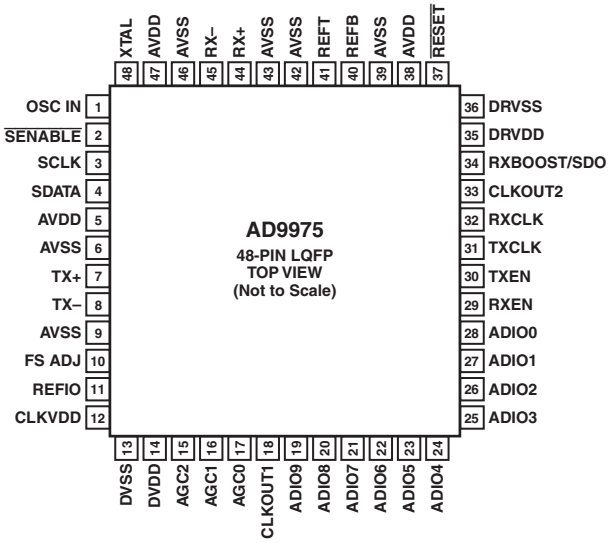
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9975 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Function
1	OSC IN	Crystal Oscillator Inverter Input
2	$\overline{\text{SENABLE}}$	Serial Bus Enable Input
3	SCLK	Serial Bus Clock Input
4	SDATA	Serial Bus Data I/O
5, 38, 47	AVDD	Analog 3.3 V Power Supply
6, 9, 39, 42, 43, 46	AVSS	Analog Ground
7	Tx+	Transmit DAC + Output
8	Tx–	Transmit DAC – Output
10	FS ADJ	DAC Full-Scale Output Current Adjust with External Resistor
11	REFIO	DAC Band Gap Decoupling Node
12	CLKVDD	Power Supply for CLKOUT1
13	DVSS	Digital Ground
14	DVDD	Digital 3.3 V Power Supply
15–17	AGC[2:0]	AGC Control Inputs
18	CLKOUT1	Auxiliary Clock Output
19–28	ADIO[9:0]	Digital Data I/O Port
29	RXEN	ADIO Direction Control Input
30	TXEN	TX Path Enable
31	TXCLK	ADIO Sample Clock Input
32	RXCLK	ADIO Request Clock Input
33	CLKOUT2	Auxiliary Clock Output
34	RXBOOST/ SDO	External Gain Control Output/ Serial Data Output
35	DRVDD	Digital I/O 3.3 V Power Supply
36	DRVSS	Digital I/O Ground
37	$\overline{\text{RESET}}$	Reset Input
40, 41	REFB, REFT	ADC Reference Decoupling Node
44	Rx+	Receive Path + Input
45	Rx–	Receive Path – Input
48	XTAL	Crystal Oscillator Inverter Output

PIN CONFIGURATION



DEFINITIONS OF SPECIFICATIONS

Clock Jitter
The clock jitter is a measure of the *intrinsic* jitter of the PLL generated clocks. It is a measure of the jitter from one rising edge of the clock with respect to another edge of the clock nine cycles later.

Differential Nonlinearity Error (DNL, No Missing Codes)
An ideal converter exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 10-bit resolution indicate that all 1024 codes, respectively, must be present over all operating ranges.

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Phase Noise
Single-sideband phase noise power density is specified relative to the carrier (dBc/Hz) at a given frequency offset (1 kHz) from the carrier. Phase noise can be measured directly on a generated single tone with a spectrum analyzer that supports noise marker measurements. It detects the relative power between the carrier and the offset (1 kHz) sideband noise and takes the resolution bandwidth (rbw) into account by subtracting 10 log(rbw). It also adds a correction factor that compensates for the implementation of the resolution bandwidth, log display, and detector characteristic.

Output Compliance Range
The range of allowable voltage at the output of a current-output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation, resulting in nonlinear performance, or breakdown.

Spurious-Free Dynamic Range (SFDR)
The difference, in dB, between the rms amplitude of the DAC's output signal (or ADC's input signal) and the peak spurious signal over the specified bandwidth (Nyquist bandwidth, unless otherwise noted).

Pipeline Delay (Latency)
The number of clock cycles between conversion initiation and the associated output data being made available.

Offset Error
First transition should occur for an analog value 1/2 LSB above negative full scale. Offset error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Input Referred Noise
The rms output noise is measured using histogram techniques. The ADC output code's standard deviation is calculated in LSB and converted to an equivalent voltage. This results in a noise figure that can directly be referred to the RX input of the AD9975.

Signal-to-Noise and Distortion Ratio (SINAD)
SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

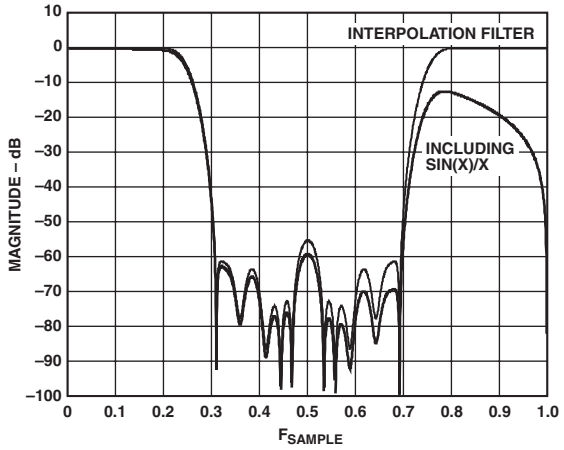
$$N = (SINAD - 1.76)\ dB / 6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits.

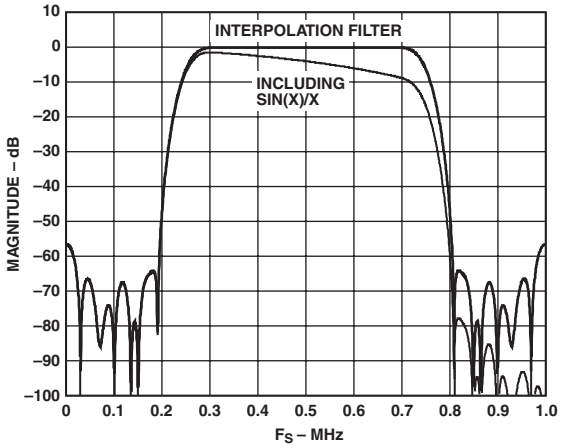
Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

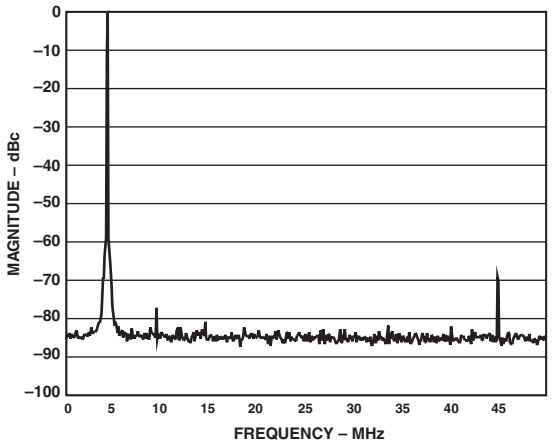
Power Supply Rejection
Power supply rejection specifies the converter's maximum full-scale change when the supplies are varied from nominal to minimum and maximum specified voltages.



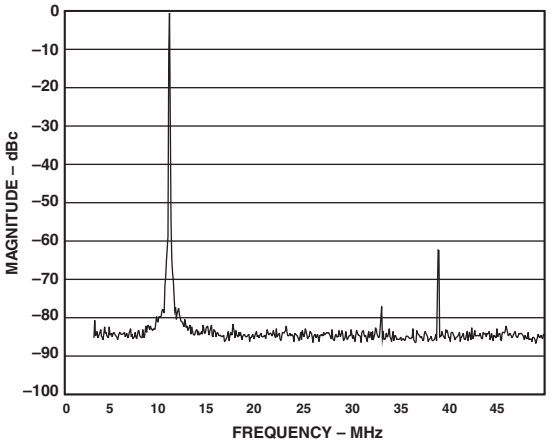
TPC 1. 2× Low-Pass Interpolation Filter



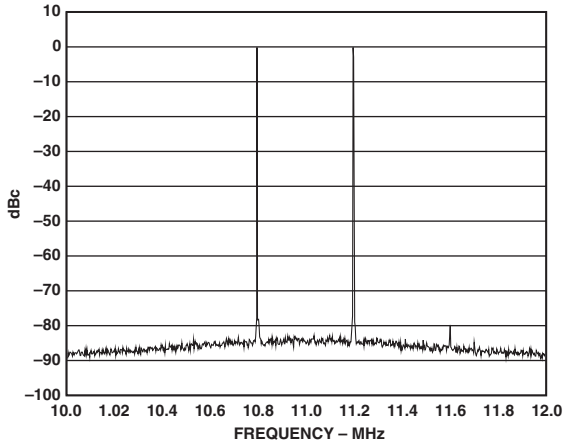
TPC 2. 2× Band-Pass Interpolation Filter, $F_S/2$ Modulation, Adjacent Image Preserved



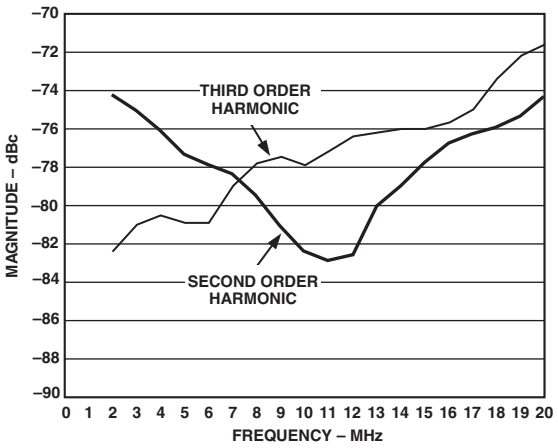
TPC 3. Single Tone Spectral Plot @ f_{DATA} = 50 MSPS, f_{OUT} = 5 MHz, 2× LPF



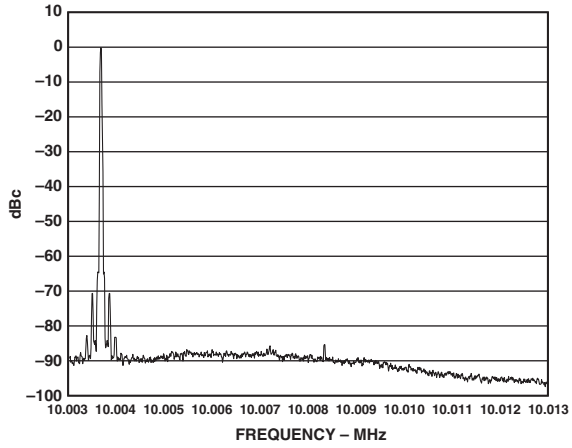
TPC 4. Single Tone Spectral Plot @ f_{DATA} = 50 MSPS, f_{OUT} = 11 MHz, 2× LPF



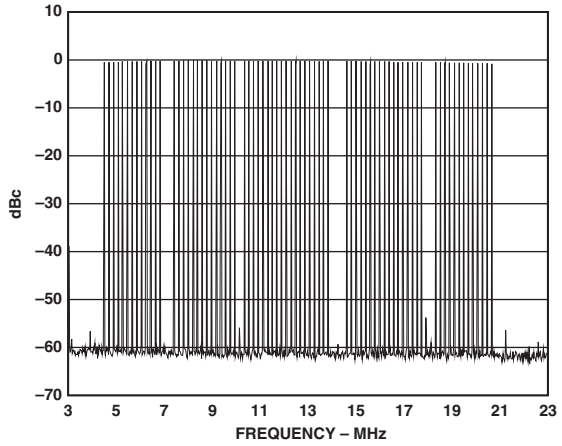
TPC 5. Dual Tone Spectral Plot @ f_{DATA} = 50 MSPS, f_{OUT} = 6.7 MHz and 7.3 MHz, 2× LPF



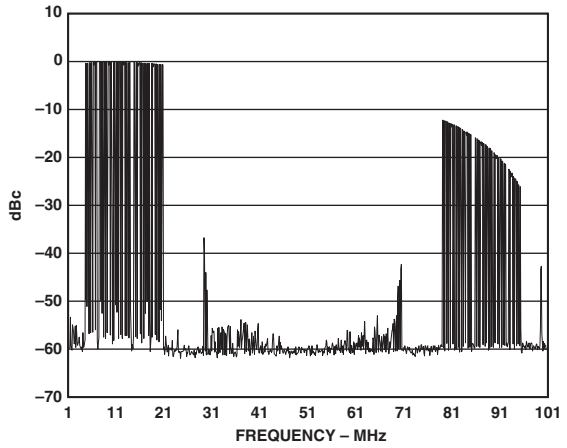
TPC 6. Harmonic Distortion vs. f_{OUT} @f_{DATA} = 50 MSPS



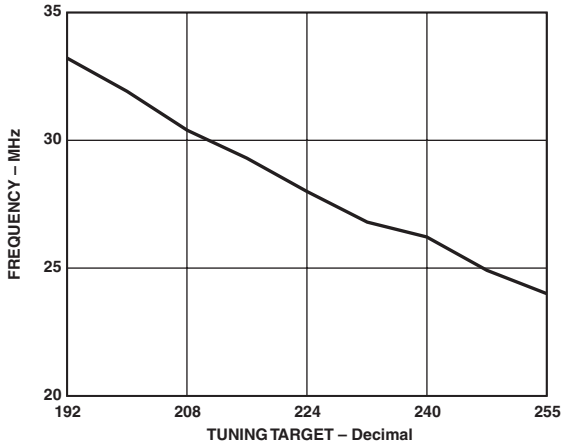
TPC 7. Phase Noise Plot @f_{DATA} 50 MSPS, f_{OUT} = 10 MHz, 2× LPF



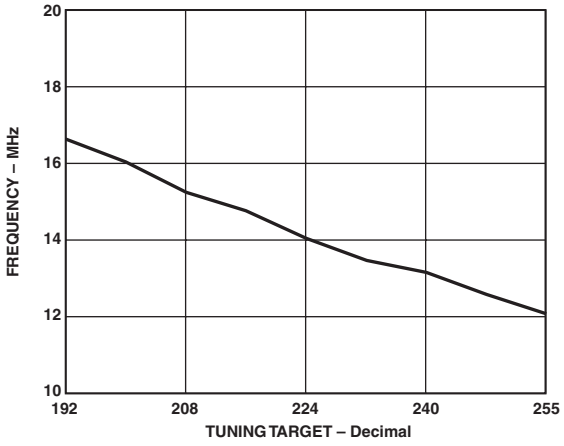
TPC 8. "In-Band" Multitone Spectral Plot @f_{DATA} = 50 MSPS, f_{OUT} = k× 195 kHz, 2× LPF



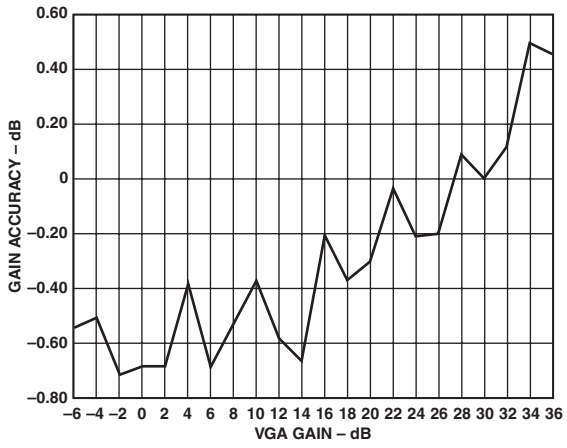
TPC 9. "Wide-Band" Multitone Spectral Plot @f_{DATA} = 50 MSPS, f_{OUT} = k× 195 kHz, 2× LPF



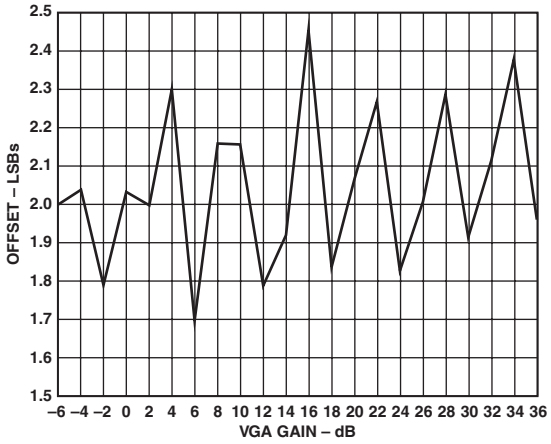
TPC 10. F_C vs. Tuning Target, F_{ADC} = 50 MHz, LPF = Wideband Rx Filter



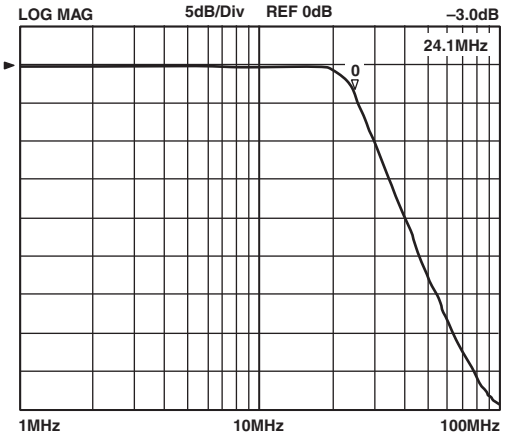
TPC 11. F_C vs. Tuning Target, F_{ADC} = 50 MHz, LPF = Narrowband Rx Filter



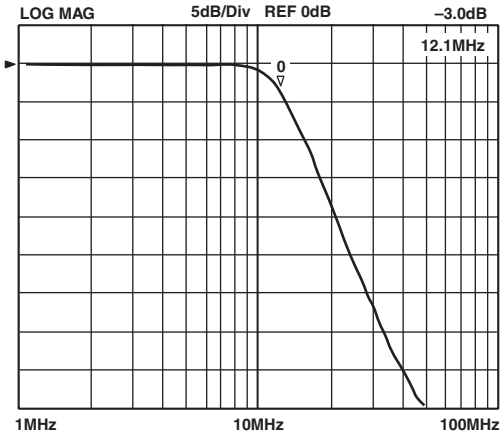
TPC 12. PGA Gain Error vs. Gain



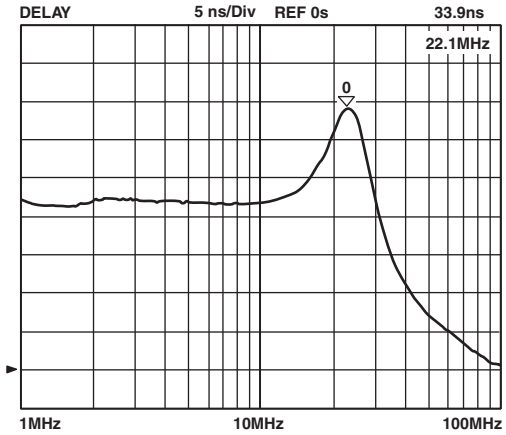
TPC 13. PGA Gain Step vs. Gain



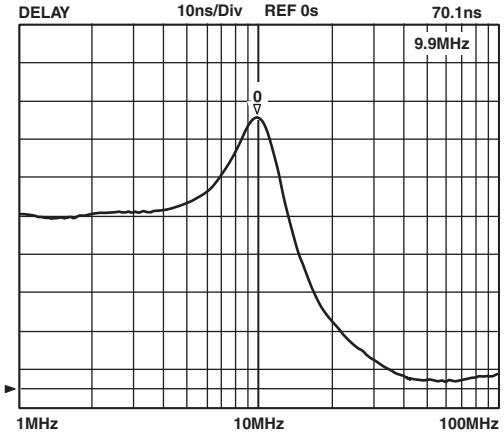
TPC 16. Rx LPF Group Delay, LPF = Narrowband Rx Filter, F_{ADC} = 50 MHz, Tuning Target = 255



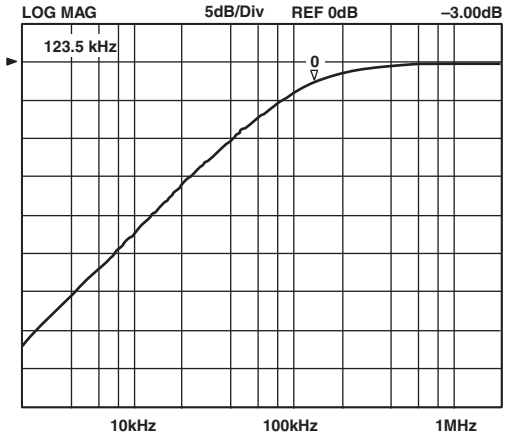
TPC 14. Rx LPF Frequency Response, LPF = Narrowband Rx Filter, F_{ADC} = 50 MHz, Tuning Target = 255



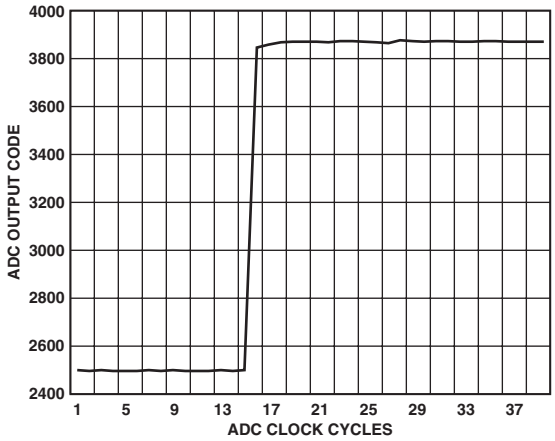
TPC 17. Rx LPF Group Delay, LPF = Wideband Rx Filter, F_{ADC} = 50 MHz, Tuning Target = 255



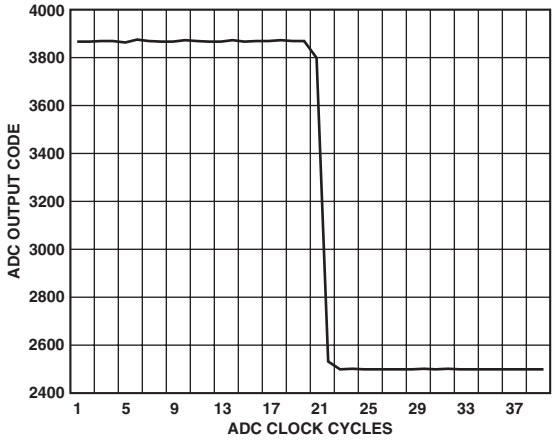
TPC 15. Rx LPF Frequency Response, LPF = Wideband Rx Filter, F_{ADC} = 50 MHz, Tuning Target = 255



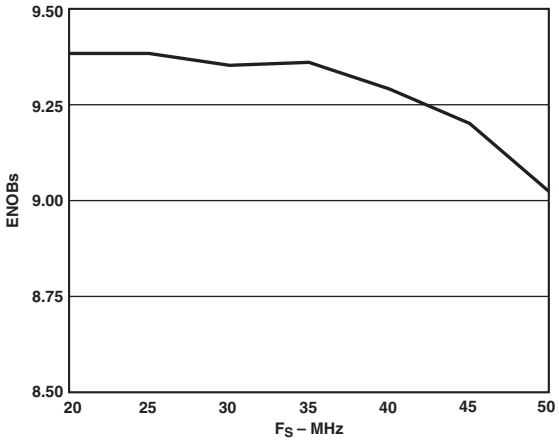
TPC 18. Rx HPF Frequency Response, F_{ADC} = 50 MHz



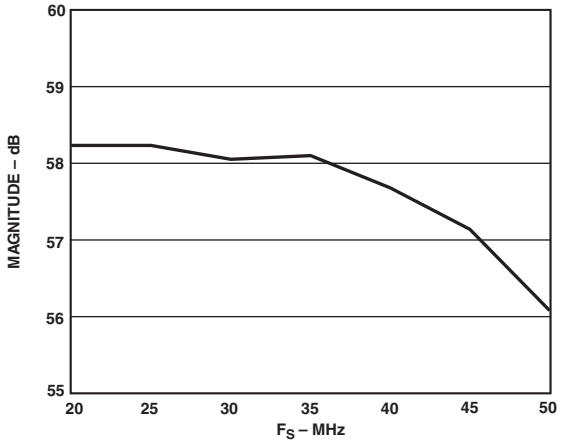
TPC 19. Rx Path Settling, 1/2 Scale Rising Step with Gain Change, LPF F_C = 26 MHz, F_{ADC} = 50 MHz



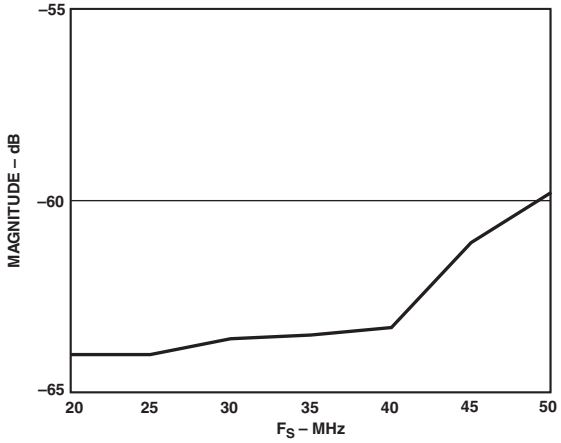
TPC 20. Rx Path Settling, 1/2 Scale Falling Step with Gain Change, LPF F_C = 26 MHz, F_{ADC} = 50 MHz



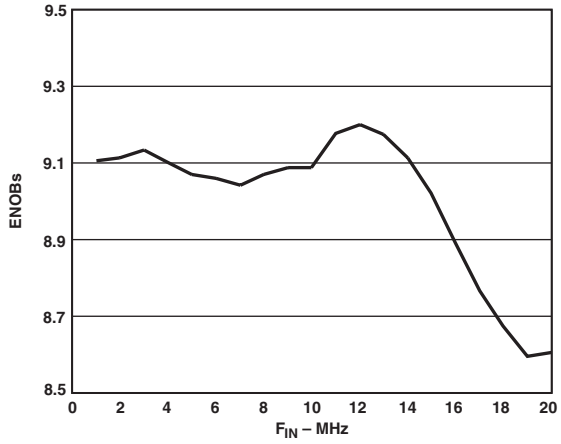
TPC 21. Rx Path ENOB vs. F_{ADC}, F_{IN} = 5 MHz, Gain = –6 dB, Rx LPF Bypassed



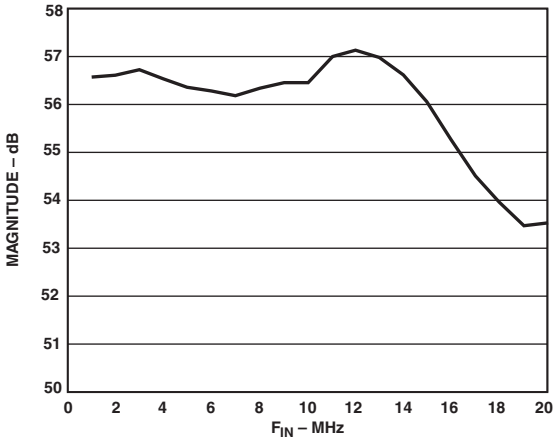
TPC 22. Rx Path SNR vs. F_{ADC}, F_{IN} = 5 MHz, Gain = –6 dB, Rx LPF Bypassed



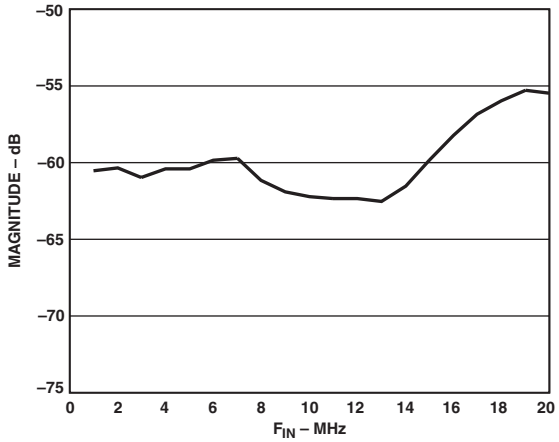
TPC 23. Rx Path THD vs. F_{ADC}, F_{IN} = 5 MHz, Gain = –6 dB, Rx LPF Bypassed



TPC 24. Rx Path ENOB vs. F_{IN}, F_{ADC} = 50 MHz, Gain = –6 dB, Rx LPF Bypassed



TPC 25. Rx Path SNR vs. F_{IN}, F_{ADC} = 50 MHz, Gain = –6 dB, Rx LPF Bypassed



TPC 26. Rx Path THD vs. F_{IN}, F_{ADC} = 50 MHz, Gain = –6 dB, Rx LPF Bypassed

TRANSMIT PATH

The AD9975 transmit path consists of a digital interface port, a bypassable 2× interpolation filter, and a transmit DAC. The clock signals required by these blocks are generated by the internal PLL. The block diagram below shows the interconnection between the major functional components of the transmit path.

INTERPOLATION FILTER

The interpolation filter can be programmed to run at a 2× upsampling ratio in either a low-pass filter or band-pass filter mode. The transfer functions of these two modes are shown in TPC 1 and TPC 2, respectively. The y-axes of the figures show the magnitude response of the filters in dB, and the x-axes show the frequency normalized to F_{DAC}. The top trace of the plot shows the discrete time transfer function of the interpolation filter. The bottom trace shows the TX path transfer function including the sin(x)/x transfer function of the DAC. In addition to the two upsampling modes, the interpolation filter can be programmed into a pass-through mode if no interpolation filtering is desired.

The table below shows the following parameters as a function of the mode in which it is programmed.

Latency – The number of clock cycles from the time a digital impulse is written to the DAC until the peak value is output at the TX+ and TX– Pins.

Flush – The number of clock cycles from the time a digital impulse is written to the DAC until the output at the TX+ and TX– Pins settles to zero.

F_{PASS} – The frequency band over which the pass-band ripple is less than the stated magnitude (i.e., 0.1 dB or 1.0 dB).

F_{STOP} – The frequency band over which the stop-band attenuation is greater than the stated magnitude (i.e., 40 dB or 50 dB).

Table I. Interpolation Filters vs. Mode

Register 7[7:4]	0x1	0x5
Mode	2× LPF	2× BPF, Adj. Image
Latency, F_{DAC} Clock Cycles	30	30
Flush, F_{DAC} Clock Cycles	48	48
F_{PASS}, 0.1 dB	<0.204	>0.296, <0.704
F_{PASS}, 1.0 dB	<0.207	>0.293, <0.707
F_{STOP}, 40 dB	<0.296	>0.204, <0.796
F_{STOP}, 50 dB	<0.302	<0.198, >0.802

DPLL-A CLOCK DISTRIBUTION

Figure 1 shows the clock signals used in the transmit path. The DAC sampling clock, f_{DAC}, is generated by DPLL-A. f_{DAC} has a frequency equal to $L \times f_{OSCIN}$, where L is the PLL clock multiplier value and f_{OSCIN} is the frequency of the input to PLL-A. The value of L is programmed through the serial interface port and can be set to 1, 2, 4, or 8. The transmit path expects a new input sample at the ADIO interface at a rate of $f_{DAC}/2$ if the interpolation filter is being used. If the interpolation filter is bypassed, the transmit path expects a new input sample at the ADIO interface at a rate of f_{DAC}.

D/A CONVERTER

The AD9975 DAC provides differential output current on the TX+ and TX– pins. The values of the output currents are complementary, meaning they will always sum to I_{FS}, the full-scale current of the DAC. For example, when the current from TX+ is at full scale, the current from TX– is zero. The two currents will typically drive a resistive load that will convert the output currents to a voltage. The TX+ and TX– output currents are inherently ground seeking and should each be connected to matching resistors, R_L, that are tied directly to AGND.

The full-scale output current of the DAC is set by the value of the resistor placed from the FS ADJ pin to AGND. The relationship between the resistor, R_{SET}, and the full-scale output current is governed by the following equation:

$$I_{FS} = 39.4 / R_{SET}$$

The full-scale current can be set from 2 to 20 mA. Generally, there is a trade-off between DAC performance and power consumption. The best DAC performance will be realized at an I_{FS} of 20 mA. However, the value of I_{FS} adds directly to the overall current consumption of the device.

The single-ended voltage outputs appearing at the TX+ and TX– nodes are:

$$V_{TX+} = I_{TX+} \times R_L$$
$$V_{TX-} = I_{TX-} \times R_L$$

Note that the full-scale voltage of V_{TX+} and V_{TX-} should not exceed the maximum output compliance range of 1.5 V to prevent signal compression. To maintain optimum distortion and linearity performance, the maximum voltages at V_{TX+} and V_{TX-} should not exceed ±0.5 V.

The single-ended full-scale voltage at either output node will be:

$$V_{FS} = I_{FS} \times R_L$$

The differential voltage, V_{DIFF}, appearing across V_{TX+} and V_{TX-} is:

$$V_{DIFF} = (I_{TX+} - I_{TX-}) \times R_L$$

and

$$V_{DIFF\_FS} = I_{FS} \times R_L$$

It should be noted that the differential output impedance of the DAC is $2 \times R_L$ and any load connected across the two output resistors will load down the output voltage accordingly.

RECEIVE PATH DESCRIPTION

The receive path consists of a two stage PGA, a continuous time, 4-pole LPF, an ADC, and a digital HPF. Also working in conjunction with the receive path is an offset correction circuit and a digital phase-locked loop. Each of these blocks will be discussed in detail in the following sections.

PROGRAMMABLE GAIN AMPLIFIER

The PGA has a programmable gain range from –6 dB to +36 dB if the narrower (approximately 12 MHz) LPF bandwidth is selected, or if the LPF is bypassed. If the wider (approximately 29 MHz) LPF bandwidth is selected, the gain range is –6 dB to +30 dB. The PGA is comprised of two sections, a continuous time PGA (CPGA), and a switched capacitor PGA (SPGA). The CPGA has possible gain settings of 0, 6, 12, 18, 24 and 30. The SPGA has possible gain settings of –6 dB, –4 dB, –2 dB, 0 dB, +2 dB, +4 dB, and +6 dB. Table II shows how the gain is distributed for each programmed gain setting.

The CPGA input appears at the device RX+ and RX– input pins. The input impedance of this stage is nominally 270 Ω differential and is not gain dependent. It is best to ac-couple the input signal to this stage and let the inputs self-bias. This will lower the offset voltage of the input signal, which is important at higher gains, since any offset will lower the output compliance range of the CPGA output. When the inputs are driven by direct coupling, the dc level should be AVDD/2. However, this could lead to larger dc offsets and reduce the dynamic range of the RX path.

There are two modes for selecting the RX path gain. The first mode is to program the PGA through the serial port. A 5-bit word determines the gain with a resolution of 2 dB per step. More detailed information about this mode is included in the Register Programming Definitions section of this data sheet.

The second mode sets the gain through the asynchronous AGC[2:0] pins. These three pins set the PGA gain and state of the RXBOOST pin according to Table II.

Table II. AGC[2:0] Gain Mapping

AGC [2:0]	Rx Path Gain	CPGA Gain	SPGA Gain	RXBOOST
0x00	–6	–6	0	0
0x01	–6	–6	0	0
0x02	2	–6	8	0
0x03	10	0	10	0
0x04	2	–6	8	1
0x05	10	0	10	1
0x06	18	12	6	1
0x07	26	18	8	1

LOW-PASS FILTER

The low-pass filter (LPF) is a programmable, three-stage, fourth order low-pass filter. The first real pole is implemented within the CPGA. The second filter stage implements a complex pair of poles. The last real pole is implemented in a buffer stage that drives the SPGA.

There are two pass band settings for the LPF. Within each pass band, the filters are tunable over about a ±15% frequency range. The formula for the cutoff frequency is:

$$F_C = F_{ADC} \times 64 / (64 + Target)$$

Where *Target* is the decimal value programmed as the tuning target in Register 5.

This filter may also be bypassed. In this case, the bandwidth of the RX path will be gain dependent and will be around 50 MHz at the highest gain settings.

ADC

The AD9975's analog-to-digital converter implements pipelined multistage architecture to achieve high sample rates while consuming low power. The ADC distributes the conversion over several smaller A/D subblocks, refining the conversion with progressively higher accuracy as it passes the results from stage to stage. As a consequence of the distributed conversion, ADCs require a small fraction of the 2^n comparators used in a traditional n-bit flash-type A/D. A sample-and-hold function within each of the stages permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Each stage of the pipeline, excluding the last, consists of a low resolution Flash A/D connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a Flash A/D.

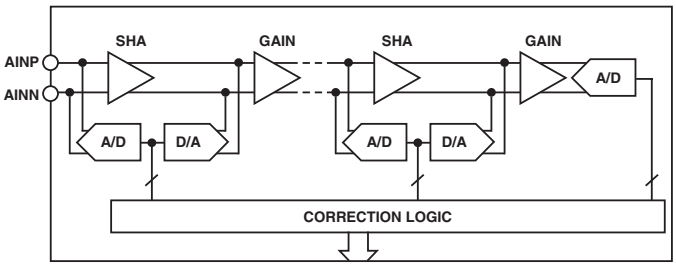


Figure 1. ADC Theory of Operation

The digital data outputs of the ADC are represented in straight binary format. They saturate to full scale or zero when the input signal exceeds the input voltage range.

The maximum value will be output from the ADC when the RX+ input is 1 V or more greater than the RX– input. The minimum value will be output from the ADC when the RX– input is 1 V or more greater than the RX+ input. This results in a full-scale ADC voltage of 2 Vppd.

The data can be translated to straight binary data format by simply inverting the most significant bit.

The timing of the interface is fully described in the Digital Interface Port Timing section.

DIGITAL HPF

Following the ADC, there is a bypassable digital HPF. The response is a single pole IIR HPF. The transfer function is approximately:

$$H(z) = (Z - 0.99994) / (Z - 0.98466)$$

where the sampling period is equal to the ADC clock period. This results in a 3 dB frequency approximately 1/400th of the ADC sampling rate. The transfer function of the digital HPF with an ADC sample rate of 50 MSPS is plotted in TPC 23.

The digital HPF introduces a 1 ADC clock cycle latency. If the HPF function is not desired, the HPF can be bypassed and the latency will not be incurred.

CLOCK AND OSCILLATOR CIRCUITRY

The AD9975 generates all internally required clocks from a single clock source. This source can be supplied in one of two ways. The first method uses the on-chip oscillator by connecting a fundamental frequency quartz crystal between the OSC IN (Pin 1) and XTAL (Pin 48) with parallel resonant load capacitors as specified by the crystal manufacturer. Alternatively, a TTL-level clock applied to OCS IN with the XTAL pin left unconnected can overdrive the internal oscillator circuit.

The PLL has a frequency capture range between 10 MHz and 50 MHz.

AGC TIMING CONSIDERATIONS

When implementing the AGC timing loop, it is important to consider the delay and settling time of the RX path in response to a change in gain. Figure 2 shows the delay the receive signal experiences through the blocks of the RX path. Whether the gain is programmed through the serial port or via the AGC[2:0] pins, the gain takes effect immediately with the delays shown in Figure 2. When gain changes do not involve the CPGA, the new gain will be evident in samples after about 7 ADC clock cycles. When the gain change does involve the CPGA, it takes an additional 45 ns to 70 ns due to the propagation delays of the buffer, LPF and PGA. Table VI in the Register Programming section details the PGA programming map.

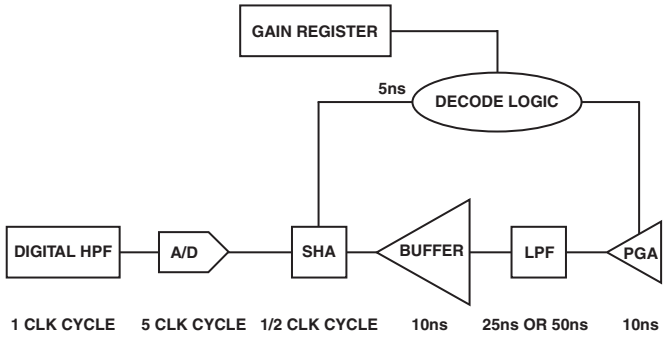


Figure 2. AGC Loop Timing

AGC PROGRAMMING

The gain in the receive path can be programmed in two ways. The default method is through the AGC[2:0] pins. In this mode, the gain is achieved using a combination of internal and external gain. The external gain is controlled by the RXBOOST output pin, which is determined by the decode of the 3-bit AGC gain value.

DIGITAL INTERFACE PORT OPERATION

The digital interface port is a 10-bit bidirectional bus shared in burst fashion between the transmit path and receive path. The MxFE acts as a slave to the digital ASIC, accepting two input enable signals, TXEN and RXEN, as well as two input clock signals, TXCLK and RXCLK. Because the sampling clocks for the DAC and ADC are derived internally from the OSC IN signal, it is required that the TXCLK and RXCLK signals are exactly the same frequency as the OSC IN signal. The phase relationships between the TXCLK, RXCLK, and OSC IN signal are arbitrary.

In order to add flexibility to the digital interface port, there are several programming options available. The data input format is straight binary by default. It is possible to independently change the data format of the transmit path and receive path to twos complement. Also, the clock timing can be independently changed on the transmit and receive paths by selecting either the rising or falling clock edge as the validating/sampling edge of the clock. The digital interface port can also be programmed into a three-state output mode allowing it to be connected onto a shared bus.

The timing of the interface is fully described in the Digital Interface Port Timing section.

CLOCK DISTRIBUTION

The DAC sampling clock, f_{DAC}, is generated by the internal digital phase-locked loop (DPLL). f_{DAC} has a frequency equal to $L \times f_{OSCIN}$, where f_{OSCIN} is the internal signal generated either by the crystal oscillator when a crystal is connected between the OSC IN and XTAL pins or by the clock that is fed into the OSC IN pin, and L is the multiplier programmed through the serial port. L can have the values of 1, 2, 4, or 8.

When the interpolation filter is enabled (either 2× LPF or 2× BPF is selected), the data rate is upsampled by a factor of two. In this case, the transmit path expects a new data input word at the rate of $f_{DAC}/2$. When the interpolation filter is bypassed, the transmit path expects a new input word at the same frequency as DAC sampling clock, f_{DAC}. Therefore, in terms of f_{OSCIN}, the TXCLK frequency should be:

$$f_{TXCLK} = L \times f_{OSCIN} / K$$

where K is the interpolation factor. The interpolation factor, K, is equal to 2 when the interpolator is enabled and is equal to 1 when the interpolator is bypassed.

The ADC sampling clock is derived from f_{OSCIN} and a new output sample is available every f_{OSCIN} clock cycle. The ADC sampling lock can be programmed to be equal to f_{OSCIN} if desired. The timing of the digital interface port is illustrated in the Figures 3 and 4.

DIGITAL INTERFACE PORT TIMING

The ADIO[9:0] bus accepts input data-words into the transmit path when the TXEN pin is high, the RXEN pin is low, and a clock is present on the TXCLK pin. Figure 3 illustrates the transmit path input timing.

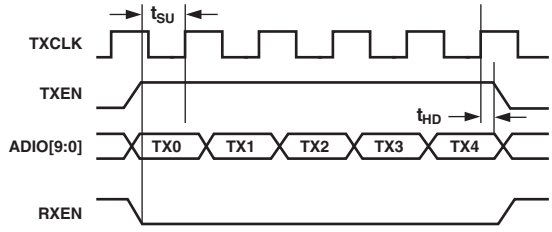


Figure 3. Transmit Data Input Timing Diagram

It should be noted that to clear the transmit path input buffers, an additional six clock cycles on the TXCLK input are required after TXEN goes low. The interpolation filters will be "flushed" with zeros if the clock signal into the TXCLK pin is present for 48 clock cycles after TXEN goes low (the data on the ADIO bus being irrelevant over this interval).

The output from the receive path will be driven onto the ADIO[9:0] bus when the RXEN pin is high, and a clock is present on the RXCLK pin. When both TXEN and RXEN are low, the ADIO[9:0] bus is three-stated. Figure 4 illustrates the receive path output timing.

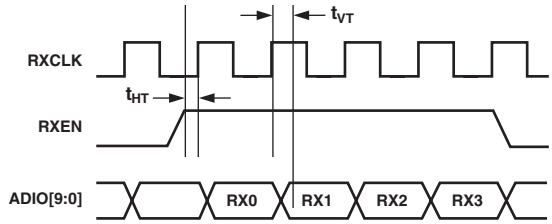


Figure 4. Receive Data Output Timing Diagram

SERIAL INTERFACE FOR REGISTER CONTROL

The serial port is a 3-wire serial communications port consisting of a clock (SCLK), chip select ($\overline{\text{SENABLE}}$), and a bidirectional data (SDATA) signal. The interface allows read/write access to all registers that configure the AD9975 internal parameters. Single or multiple byte transfers are supported as well as MSB first or LSB first transfer formats.

General Operation of the Serial Interface

Serial communication over the serial interface can be from 1 byte to 5 bytes in length. The first byte is always the instruction byte. The instruction byte establishes whether the communication is going to be a read or write access, the number of data bytes to be transferred, and the address of the first register to be accessed. The instruction byte transfer is complete immediately upon the eighth rising edge of SCLK after $\overline{\text{SENABLE}}$ is asserted. Likewise, the data registers change *immediately* upon writing to the eighth bit of each data byte.

Instruction Byte

The instruction byte contains the information shown in Table III.

Table III. Instruction Byte Bit Definitions

MSB							LSB
I7	**I6**	**I5**	**I4**	**I3**	**I2**	**I1**	**I0**
R/W	N1	N0	A4	A3	A2	A1	A0

Bit I7 – R/W

This bit determines whether a read or a write data transfer will occur after the instruction byte write. Logic high indicates a read operation, and Logic 0 indicates a write operation.

Bits I6:I5 – N1:N0

These two bits determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in Table IV.

Table IV. N1:N0 Bit Map

N1:N0	Description
0:0	Transfer 1 Byte
0:1	Transfer 2 Bytes
1:0	Transfer 3 Bytes
1:1	Transfer 4 Bytes

Bits I4:I0 - A4:A0

These bits determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9975.

Serial Interface Port Pin Description

SCLK—Serial Clock

The serial clock pin is used to synchronize data transfers to and from the AD9975 and to run the internal state machines. SCLK maximum frequency is 25 MHz. All data transmitted to the AD9975 is sampled on the rising edge of SCLK. All data read from the AD9975 is validated on the rising edge of SCLK and is updated on the falling edge.

$\overline{\text{SENABLE}}$—Serial Interface Enable

The $\overline{\text{SENABLE}}$ Pin is active low. It enables the serial communication to the device. $\overline{\text{SENABLE}}$ select should stay low during the entire communication cycle. All input on the serial port is ignored when $\overline{\text{SENABLE}}$ is inactive.

SDATA—Serial Data I/O

The signal on this line is sampled on the first eight rising edges of SCLK after $\overline{\text{SENABLE}}$ goes active. Data is then read from or written to the AD9975 depending on what was read.

Figures 5 and 6 show the timing relationships between the three SPI signals.

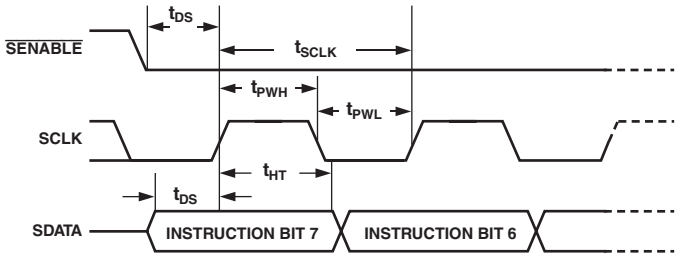


Figure 5. Timing Diagram Register Write to AD9975

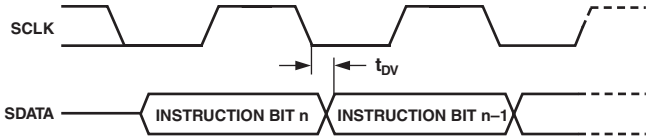


Figure 6. Timing Diagram Register Read from AD9975

MSB/LSB Transfers

The AD9975 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. The bit order is controlled by the *SPI LSB First* Bit (Register 0, Bit 6). The default value is 0, MSB first. Multibyte data transfers in MSB format can be completed by writing an instruction byte that includes the register address of the last address to be accessed. The AD9975 will automatically decrement the address for each successive byte required for the multibyte communication cycle.

When the *SPI LSB First* Bit (Register 0, Bit 6) is set high, the serial port interprets both instruction and data bytes LSB first. Multibyte data transfers in LSB format can be completed by writing an instruction byte that includes the register address of the first address to be accessed. The AD9975 will automatically increment the address for each successive byte required for the multibyte communication cycle.

Figures 7a and 7b show how the serial port words are built for each of these modes.

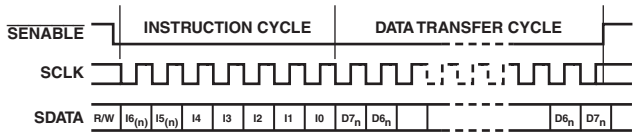


Figure 7a. Serial Register Interface Timing MSB First

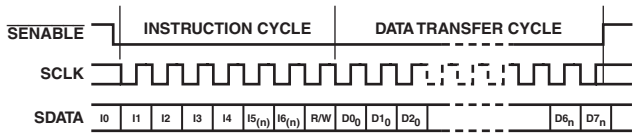


Figure 7b. Serial Register Interface Timing LSB First

Notes on Serial Port Operation

The serial port is disabled and all registers are set to their default values during a hardware reset. During a software reset, all registers except Register 0 are set to their default values. Register 0 will remain at the last value sent, with the exception that the *Software Reset* Bit will be set to 0.

Table V. Register Layout

Address (hex)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default (hex)	Type
00	Select 4-Wire SPORT	LSB/MSB First	Software Reset						00	R/W
01			Power-Down PLL-A	Power-Down DAC	Power-Down Interpolators	Power-Down RX Reference	Power-Down ADC and SPGA	Power-Down Receive Filter and CPGA	00	R/W
02									00	R/W
03		ADC Clock Source OSC IN/2					PLL-A (xL) Multiplier [1:0]		01	R/W
04	RX LPF Tuning Update Disable	RX LPF Tuning Update in Progress	RX Path DC Offset Correction	RX Digital HPF Bypass	Fast ADC Sampling	Wideband RX LPF	Enable 1-Pole RX LPF	RX LPF Bypass	01	R/W
05	RX LPF Filter Tuning Target [7:0]								80	R/W
06	RXBOOST Active Low	RXBOOST	PGA Gain Setting through Register	RX PGA Gain [4:0]					00	R/W
07	TX Interpolation Filter Select						Sample TX on Falling TXCLKIN	TX Data Input Twos Complement	10	R/W
08	CLK-B Equal to OSC IN/4	CLK-A Equal to OSC IN	CLK-B Output Disable	CLK-A Output Disable	Three-State RX Port		ADC Output on Falling RXCLK	RX Data Output Twos Complement	00	R/W
0F					Version [3:0]				00	R

The serial port is operated by an internal state machine and is dependent on the number of SCLK cycles since the last time SENABLE went active. On every eighth rising edge of SCLK, a byte is transferred over the SPI. During a multibyte write cycle, this means the registers of the AD9975 are not simultaneously updated but occur sequentially. For this reason, it is recommended that single byte transfers be used when changing the SPI configuration or performing a software reset.

REGISTER PROGRAMMING DEFINITIONS

Register 0, RESET/SPI Configuration

Bit 5: Software Reset
Setting this bit high resets the chip. The PLLs will relock to the input clock and all registers (except Register 0x0, Bit 6) revert to their default values. Upon completion of the reset, Bit 5 is reset to 0.

The content of the interpolator stage is not cleared by software or hardware resets. It is recommended to "flush" the transmit path with zeros before transmitting data.

Bit 6: LSB/MSB First
Setting this bit high causes the serial port to send and receive data least significant bit (LSB) first. The default low state configures the serial port to send and receive data most significant bit (MSB) first.

Bit 7: Select 4-Wire SPORT
Setting this bit high puts the serial port into a four-line mode. The SCLK and SENABLE retain their normal functions, SDATA becomes an input only line, and the RXBOOST/SDO pin becomes the serial port output. When in 4-wire mode, the data on the RXBOOST/SDO pin will change on the falling edge of SCLK and should be sampled on the rising edge of SCLK.

Register 1, Power-Down

Bit 0: Power-Down Receive Filter and CPGA
Setting this bit high powers down and bypasses the RX LPF and continuous time programmable gain amplifier.

Bit 1: Power-Down ADC and SPGA
Setting this bit high powers down the ADC and the switched capacitor programmable gain amplifier (SPGA).

Bit 2: Power-Down RX Reference
Setting this bit high powers down the ADC reference. This bit should be set if an external reference is applied.

Bit 3: Power-Down Interpolators
Setting this bit high powers down the transmit digital interpolator. It does not clear the content of the data path.

Bit 4: Power-Down DAC
Setting this bit high powers down the transmit DAC.

Bit 5: Power-Down PLL-A
Setting this bit high powers down the on-chip phase-locked loop that generates the transmit path clocks and the auxiliary clock CLK-A. When powered down, the CLK-A output goes to a high impedance state.

Register 3, Clock Source Configuration

The AD9975 contains a programmable PLL referred to as PLL-A. The output of the PLL is used to generate the internal clocks for the TX path and the auxiliary clock, CLK-A.

Bit 1,0: PLL-A Multiplier
Bits 1 and 0 determine the multiplication factor (L) for PLL-A and the DAC sampling clock frequency, F_{DAC}. $F_{DAC} = L \times F_{CLKIN}$.
Bit 1,0
0,0: $L = 1$
0,1: $L = 2$
1,0: $L = 4$
1,1: $L = 8$

Bit 6: ADC Clock Source OSC IN/2
Setting Bit 6 high selects the the OSC IN clock signal divided by 2 as the ADC sampling clock source. Setting Bit 6 low selects the OSC IN clock to be used directly as the ADC sampling clock source. The best ADC performance is achieved by using an external crystal or by driving the OSC IN pin with a low jitter clock source.

Register 4, Receive Filter Selection

The AD9975 receive path has a continuous time 4-pole LPF and a 1-pole digital HPF. The 4-pole LPF has two selectable cutoff frequencies. Additionally, the filter can be tuned around those two cutoff frequencies. These filters can also be bypassed to different degrees as described below.

The continuous time 4-pole low-pass filter is automatically calibrated to one of two selectable cutoff frequencies. The cutoff frequency, F_{cutoff}, is described as a function of the ADC sampling frequency F_{ADC} and can be influenced ±15% by the RX filter tuning target word in Register 5.

$$F_{cutoff\_low} = F_{ADC} \times 64 / \left(64 + Target\right)$$

$$F_{cutoff\_high} = F_{ADC} \times 158 / \left(64 + Target\right)$$

Bit 0: RX LPF Bypass
Setting this bit high bypasses the 4-pole LPF. The filter is automatically powered down when this bit is set.

Bit 1: Enable 1-Pole RX LPF
The AD9975 can be configured with a 1-pole filter when the 4-pole receive low-pass filter is bypassed. The 1-pole filter is untrimmed and subject to cutoff frequency variations of ±20%.

Bit 2: Wideband RX LPF
This bit selects the nominal cutoff frequency of the 4-pole LPF. Setting this bit high selects a nominal cutoff frequency of 28.8 MHz. When the wideband filter is selected, the RX path gain is limited to 30 dB.

Bit 3: Fast ADC Sampling
Setting this bit increases the quiescent current in the SVGA block. This may provide some performance improvement when the ADC sampling frequency is greater than 40 MSPS.

Bit 4: RX Digital HPF Bypass
Setting this bit high bypasses the 1-pole digital HPF that follows the ADC. The digital filter must be bypassed for ADC sampling above 50 MSPS.

Bit 5: RX Path DC Offset Correction
Writing a 1 to this bit triggers an immediate receive path offset correction and reads back 0 after the completion of the offset correction.

Bit 6: RX LPF Tuning Update in Progress
This bit indicates when receive filter calibration is in progress. The duration of a receive filter calibration is about 500 µs. Writing to this bit has no effect.

Bit 7: RX LPF Tuning Update Disable
Setting this bit high disables the automatic background receive filter calibration. The AD9975 automatically calibrates the receive filter on reset and every few (~2) seconds thereafter to compensate for process and temperature variation, power supply, and long term drift. Programming a 1 to this bit disables this function. Programming a 0 triggers an immediate first calibration and enables the periodic update.

Register 5, Receive Filter Tuning Target
This register sets the filter tuning target as a function of F_{OSCIN}. See Register 4 description.

Register 6, RX Path Gain Adjust
The AD9975 uses a combination of a continuous time PGA (CPGA) and a switched capacitor PGA (SPGA) for a gain range of –6 dB to +36 dB with a resolution of 2 dB. The RX path gain can be programmed over the serial interface by writing to the RX path Gain Adjust Register or directly using the GAIN and MSB aligned TX[5:1] Bits. The register default value is 0x00 for the lowest gain setting (–6 dB). The register always reads back the actual gain setting irrespective of which of the two programming modes was used.

Bits [4:0]: RX PGA Gain
Table VI describes the gains and how they are achieved as a function of the RX path adjust bits. It should be noted that the value of these bits will read back the actual gain value to which the PGA is set. If Bit 5 of this register is low, then the value read back will be that set by the AGC[2:0] Pins.

Bit 5: PGA Gain Set through Register
Setting this bit high will result in the RX path gain being set by writing to the PGA Gain Control Register. Default is zero, which selects writing the gain through the AGC[2:0] pins in conjunction with the RXBOOST pin.

Bit 6: RXBOOST
This bit is read-only. It reflects the level of the RXBOOST pin.

Bit 7: RXBOOST Active Low
Setting this bit high results in the value mapped to the RXBOOST pin by the AGC inputs being inverted.

Table VI. PGA Programming Map

RX Path Gain [4:0]	RX Path Gain	CPGA Gain	SPGA Gain
0x00	–6	0	–6
0x01	–4	0	–4
0x02	–2	0	–2
0x03	0	0	0
0x04	2	0	2
0x05	4	0	4
0x06	6	6	0
0x07	8	6	2
0x08	10	6	4
0x09	12	12	0
0x0A	14	12	2
0x0B	16	12	4
0x0C	18	18	0
0x0D	20	18	2
0x0E	22	18	4
0x0F	24	24	0
0x10	26	24	2
0x11	28	24	4
0x12*	30/30	24/30	6/0
0x13*	30/32	24/30	6/2
0x14*	30/34	24/30	6/4
0x15*	30/36	24/30	6/6

*When the wideband RX filter bit is set high, the RX path gain is limited to 30 dB. The first of the two values refers to the mode when the lower RX LPF cutoff frequency is chosen, or when the RX LPF filter is bypassed.

Register 7, Transmit Path Settings

Bit 0: TX Data Input Twos Complement
Setting this bit high changes the TX path input data format to twos complement. When this bit is low, the TX data format is straight binary.

Bit 1: Sample TX Data on Falling TXCLKIN
If Bit 1 is set high, the TX path data will be sampled on the falling edge of TXCLKIN. When this bit is low, the data will be sampled on the rising edge of TXCLKIN.

Bit 4 to Bit 7: Interpolation Filter Select

Bits 4 to 7 define the interpolation filter characteristic and interpolation rate.
Bits 7:4;
0x1; see TPC 1. 2× Interpolation, LPF.
0x2; Interpolation Bypass.
0x5; see TPC 2. 2× Interpolation, BPF, Adj image.

The interpolation factor has a direct influence on the rate at which the TX path will read the input data-words from the input buffer. When the interpolation filter has been bypassed, the data will be read out of the buffer at a rate of $F_{OSCIN} \times L$. When the interpolator is configured to run in either of the 2× interpolation modes, the data will be read out of the buffer at a rate of $0.5 \times F_{OSCIN} \times L$.

Register 8, Receiver and Clock Output Settings

Bit 0: Rx Data Output Twos Complement
Setting this bit high changes the RX path input data format to twos complement. When this bit is low, the RX data format is straight binary.

Bit 1: ADC Output on Falling RXCLK
If Bit 1 is set high, the TX path data will be sampled on the falling edge of RXCLK. When this bit is low, the data will be sampled on the rising edge of RXCLK.

Bit 3: Three-State RX Port
This bit sets the receive output RX[5:0] into a high impedance three-state mode. It allows for sharing the bus with other devices.

Bit 4: CLK-A Output Disable
Setting Bit 4 high fixes the CLK-A output to a Logic 0 output level.

Bit 5: CLK-B Output Disable
Setting Bit 5 high fixes the CLK-A output to a Logic 0 output level.

Bit 6: CLK-A Equal to OSC IN
Setting Bit 6 high sets the CLK-A output signal frequency equal to the OSC IN signal frequency. Otherwise, the CLK-A output frequency is equal to $F_{OSCIN} \times L$.

Bit 7: CLK-B Equal to OSC IN/4
Setting Bit 7 high sets the CLKB output signal frequency equal to the OSC IN/4 signal frequency. Otherwise, the CLKB output frequency is equal to OSC IN/2.

Register F, Die Revision
This register stores the die revision of the chip. It is a read-only register.

PCB DESIGN CONSIDERATIONS

Although the AD9975 is a mixed signal device, the part should be treated as an analog component. The digital circuitry on-chip has been specially designed to minimize the impact that the digital switching noise will have on the operation of the analog circuits. Following the power, grounding, and layout recommendations in this section will help you get the best performance from the MxFE.

Component Placement
If the three following guidelines of component placement are followed, chances for getting the best performance from the MxFE are greatly increased. First, manage the path of return currents flowing in the ground plane so that high frequency switching currents from the digital circuits do not flow on the ground plane under the MxFE or analog circuits. Second, keep noisy digital signal paths and sensitive receive signal paths as short as possible. Third, keep digital (noise generating) and analog (noise susceptible) circuits as far away from each other as possible.

In order to best manage the return currents, pure digital circuits that generate high switching currents should be closest to the power supply entry. This will keep the highest frequency return current paths short and prevent them from traveling over the sensitive MxFE and analog portions of the ground plane. Also, these circuits should be generously bypassed at each device that will further reduce the high frequency ground currents. The MxFE should be placed adjacent to the digital circuits such that the ground return currents from the digital sections will not flow in the ground plane under the MxFE. The analog circuits should be placed furthest from the power supply.

The AD9975 has several pins that are used to decouple sensitive internal nodes. These pins are REFIO, REFB, and REFT. The decoupling capacitors connected to these points should have low ESR and ESL. These capacitors should be placed as close to the MxFE as possible and be connected directly to the analog ground plane.

The resistor connected to the FS ADJ pin should also be placed close to the device and connected directly to the analog ground plane.

Power Planes and Decoupling
The AD9975 evaluation board demonstrates a good power supply distribution and decoupling strategy. The board has four layers; two signal layers, one ground plane, and one power plane. The power plane is split into a 3VDD section, which is used for the 3 V digital logic circuits; a DVDD section, which is used to supply the digital supply pins of the AD9975; an AVDD section, which is used to supply the analog supply pins of the AD9975; and a VANLG section, which supplies the higher voltage analog components on the board. The 3VDD section will typically have the highest frequency currents on the power plane and should be kept the furthest from the MxFE and analog sections of the board. The DVDD portion of the plane brings the current used to power the digital portion of the MxFE to the device. This should be treated similar to the 3VDD power plane and be kept from going underneath the MxFE or analog components. The MxFE should largely sit on the AVDD portion of the power plane.

The AVDD and DVDD power planes may be fed from the same low noise voltage source; however, they should be decoupled from each other to prevent the noise generated in the DVDD portion of the MxFE from corrupting the AVDD supply. This can be done by using ferrite beads between the voltage source and DVDD and between the source and AVDD. Both DVDD and AVDD should have a low ESR, bulk decoupling capacitor on the MxFE side of the ferrite as well as a low ESR, ESL decoupling capacitors on each supply pin (i.e., the AD9975 requires five power supply decoupling caps, one each on Pins 5, 38, 47, 14, and 35). The decoupling caps should be placed as close to the MxFE supply pins as possible. An example of the proper decoupling is shown in the AD9975 evaluation board schematic.

Ground Planes
In general, if the component placing guidelines discussed earlier can be implemented, it is best to have at least one continuous ground plane for the entire board. All ground connections should be made as short as possible. This will result in the lowest impedance return paths and the quietest ground connections.

If the components cannot be placed in a manner that would keep the high frequency ground currents from traversing under the MxFE and analog components, it may be necessary to put current steering channels into the ground plane to route the high frequency currents around these sensitive areas. These current steering channels should be made only when and where necessary.

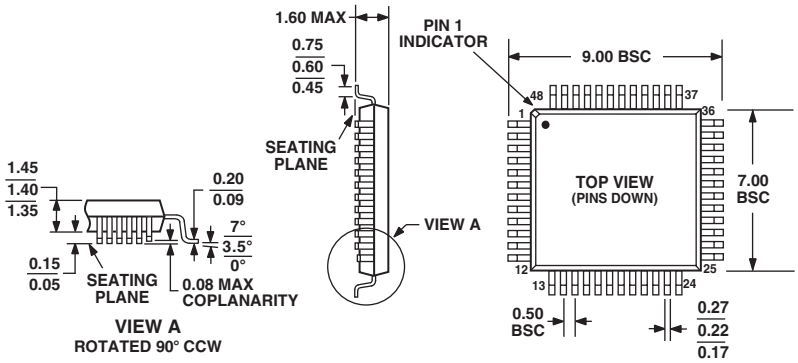
Signal Routing
The digital RX and TX signal paths should be kept as short as possible. Also, the impedance of these traces should have a controlled impedance of about 50 Ω. This will prevent poor signal integrity and the high currents that can occur during undershoot or overshoot caused by ringing. If the signal traces cannot be kept shorter than about 1.5 inches, then series termination resistors (33 Ω to 47 Ω) should be placed close to all signal sources. It is a good idea to series terminate all clock signals at their source regardless of trace length.

The receive RX+/RX– signals are the most sensitive signals on the entire board. Careful routing of these signals is essential for good receive path performance. The RX+/RX– signals form a differential pair and should be routed together as a pair. By keeping the traces adjacent to each other, noise coupled onto the signals will appear as common mode and will be largely rejected by the MxFE receive input. Keeping the driving point impedance of the receive signal low and placing any low-pass filtering of the signals close to the MxFE will further reduce the possibility of noise corrupting these signals.

OUTLINE DIMENSIONS

48-Lead Plastic Quad Flatpack [LQFP]
1.4 mm Thick
(ST-48)

Dimensions shown in millimeters



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