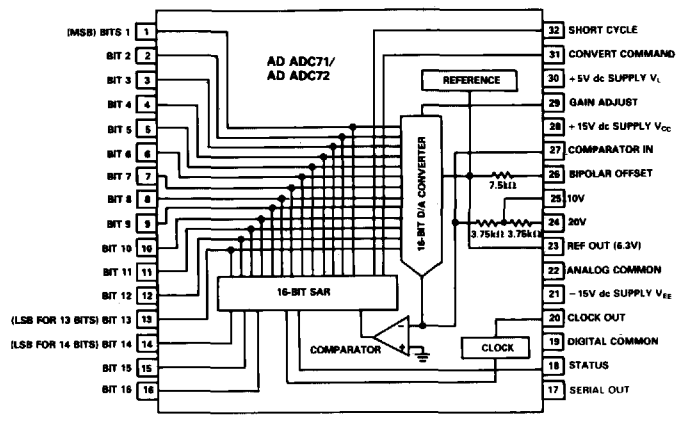
Complete, High Resolution 16-Bit A/D Converters

AD ADC71/AD ADC72

FEATURES

Complete 16-Bit Converter With Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits
Fast Conversion – 35μs (14 Bit)
Short Cycle Capability
Parallel and Serial Logic Outputs
Low Power: 645mW Typical
Industry Standard Pin Out

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC71 and AD ADC72 are high resolution 16-bit hybrid IC analog-to-digital converters including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin hermetic ceramic DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR (AD ADC71K, AD ADC72K and B), and maximum conversion time of 50μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD ADC71 and AD ADC72 provide data in parallel form with corresponding clock and status outputs. The AD ADC71 also provides data in serial form. All digital inputs and outputs are TTL compatible.

APPLICATIONS

The AD ADC71 and AD ADC72 are excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multichannel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required.

PRODUCT HIGHLIGHTS

1. The AD ADC71 and AD ADC72 provide 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J and A grades) at 25°C.
2. Conversion time is 35μs typical to 14 bits with short cycle capability.
3. Two binary codes are available on the AD ADC71 and AD ADC72 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary two's complement (CTC) coding may be obtained by inverting Pin 1 (MSB).
4. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.

This is an abridged version of the data sheet. To obtain a complete data sheet, contact your nearest sales office.

REV. A

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AD ADC71/AD ADC72—SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 volts unless otherwise noted)

Model	AD ADC71JD/KD	AD ADC72JD/KD	AD ADC72AD/BD	Units
RESOLUTION	16 (max)	*	*	Bits
ANALOG INPUTS				
Voltage Ranges				
Bipolar	±2.5, ±5, ±10	*	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	*	Volts
Impedance (Direct Input)				
0 to +5V, ±2.5V	1.88	*	*	kΩ
0 to +10V, ±5.0V	3.75	*	*	kΩ
0 to +20V, ±10V	7.50	*	*	kΩ
DIGITAL INPUTS[1]				
Convert Command	Positive Pulse 50ns Wide (min) Trailing Edge Initiates Conversion			
Logic Loading	1 (max)	*	*	LSTTL Load
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error	±0.1[2] (±0.2 max)	*	*	%
Offset Error				
Unipolar	±0.05[2] (±0.1 max)	*	*	% of FSR[3]
Bipolar	±0.1[2] (±0.2 max)*	*	*	% of FSR
Linearity Error (max)	±0.006 (J)	±0.006 (J)	±0.006 (A)	% of FSR
	±0.003 (K)	±0.003 (K)	±0.003 (B)	% of FSR
Inherent Quantization Error	±1/2	*	*	LSB
Differential Linearity Error	±0.003	*	*	% of FSR
No Missing Codes @ 25°C[4]	To 14 Bits (K Grade)	*	To 14 Bits (B Grade)	Guaranteed
POWER SUPPLY SENSITIVITY				
±15V dc	0.003	*	*	% of FSR/% ΔV_S
+5V dc	0.001	*	*	% of FSR/% ΔV_S
CONVERSION TIME[5] (14 BITS)	35 (50 max)	*	*	µs
WARM-UP TIME	5 (min)	*	*	Minutes
DRIFT				
Gain	±15 (max)	±10 (±20 max)	+7 (±15 max)	ppm/°C
Offset				
Unipolar	±2 (±4 max)	±2 (±4 max)	±2 (±4 max)	ppm of FSR/°C
Bipolar	±10 (max)	±8 (±10 max)	±5 (±10 max)	ppm of FSR/°C
Linearity	±2 (3 max)	±1.5 (2 max)	±1.0 (2 max)	ppm of FSR/°C
Guaranteed No Missing Code				
Temperature Range[4]				
71JD, 72JD, 72AD (13 Bits)	0 to 70	*	*	°C
71KD, 72KD, 72BD (14 Bits)				
DIGITAL OUTPUT[1]				
(All Codes Complementary)				
Parallel and Serial				
Output Codes[6]				
Unipolar	CSB	*	*	
Bipolar	COB, CTC[7]	*	*	
Output Drive	5	*	*	LSTTL Loads
Status	Logic "1" During Conversion			
Status Output Drive	5 (max)	*	*	LSTTL Loads
Internal Clock				
Clock Output Drive	5 (max)	*	*	LSTTL Loads
Frequency	400	*	*	kHz
INTERNAL REFERENCE VOLTAGE	6.3	*	*	V dc
Error	±5 max	*	*	%
Max External Current Drain				
With no Degradation of Specs	±200 max	*	*	µA
Temperature Coefficient	±10 max	*	±5 max	ppm/°C
POWER SUPPLY REQUIREMENTS				
Power Consumption	645 (850 max)	*	*	mW
Rated Voltage, Analog	±15 ±0.5 max	*	*	V dc
Rated Voltage, Digital	+5 ±0.25 max	*	*	V dc
Supply Drain +15V dc	+16	*	*	mA
Supply Drain −15V dc	−21	*	*	mA
Supply Drain +5V dc	+18	*	*	mA
TEMPERATURE RANGE				
Specification	0 to +70	*	−25 to +85	°C
Operating (Derated Specs)	−25 to +85	*	−25 to +125	°C
Storage	−55 to +125	*	*	°C

NOTES

[1] Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.

[2] Adjustable to zero.

[3] Full Scale Range.

[4] For definition of "No Missing Codes," refer to Theory of Operation (full data sheet.)

[5] Conversion time may be shortened with "Short Cycle" set for lower resolution.

[6] CSB – Complementary Straight Binary. COB – Complementary Offset Binary. CTC – Complementary Twos Complement.

[7] CTC coding obtained by inverting MSB (Pin 1).

*Specifications same as AD ADC71JD, KD.

Specifications subject to change without notice.

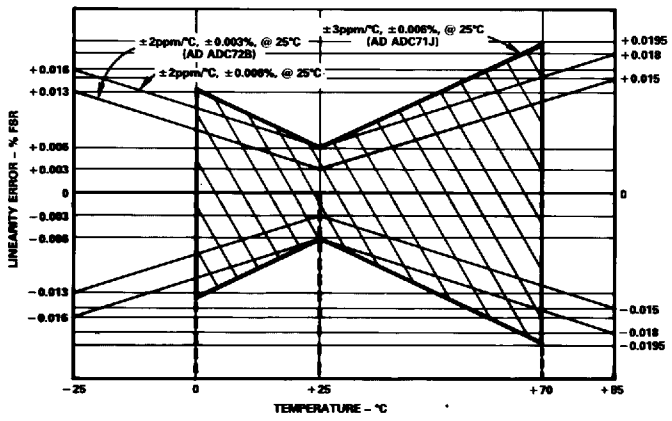

Figure 1. Linearity Error vs. Temperature

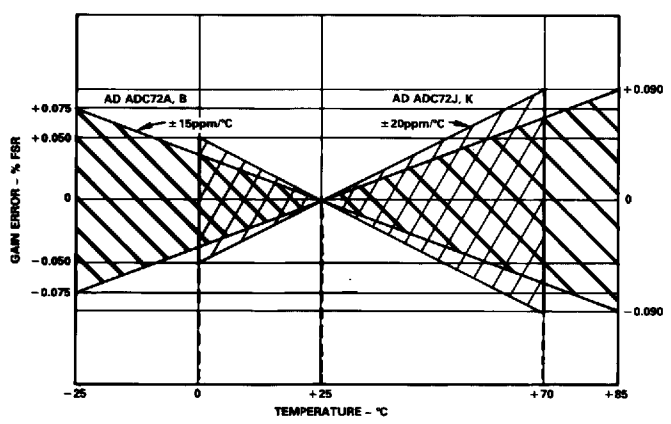

Figure 2. AD ADC72 Gain Drift Error vs. Temperature

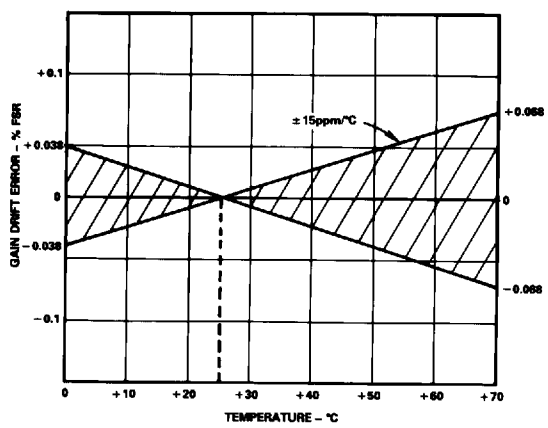

Figure 3. AD ADC71 Gain Drift Error vs. Temperature

THEORY OF OPERATION

The analog continuum is partitioned into 2^{16} discrete ranges for 16-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at ±0.2% FSR for gain and ±0.1% FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 5 and 6. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

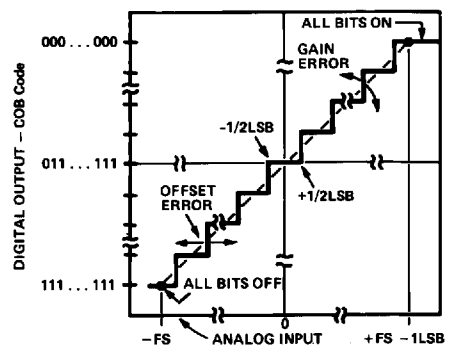

Figure 4. Transfer Characteristics for an Ideal Bipolar A/D

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD ADC71/AD ADC72 are specified as having no missing codes over temperature ranges as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD ADC71/AD ADC72 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each

bit comparison period, depending on the state of the comparator at that time.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 510kΩ resistor to the gain adjust pin 29 as shown in Figure 5.

If no external trim adjustment is desired, pins 27 (offset adj) and pin 29 (gain adj) may be left open.

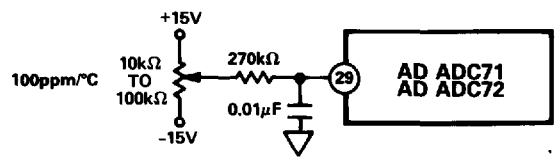

Figure 5. Gain Adjustment Circuit

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 27 for all ranges. As shown in Figure 6, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $32LSB_{14} \times 61ppm/LSB_{14} \times 1200ppm/°C = 2.3ppm/°C$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than $\pm 16LSB_{14}$, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

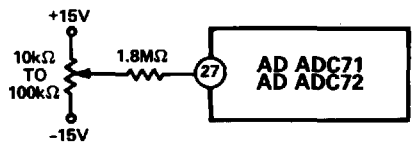

Figure 6. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100ppm/°C) are used, is shown in Figure 7.

In either adjust circuit, the fixed resistor connected to pin 27 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 27 is quite sensitive to external noise pick-up).

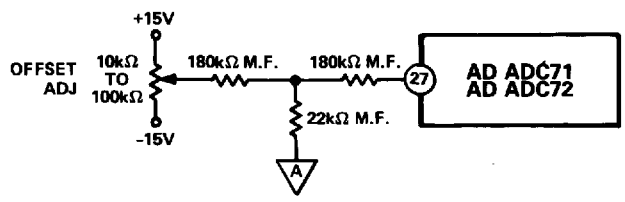

Figure 7. Low Tempco Zero Adjustment Circuit

TIMING

The timing diagram is shown in Figure 8. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 17 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{16}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. The STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the low Logic "0" state. Note that the clock remains low until the next conversion.

Corresponding parallel data bits become valid on the same positive-going clock edge.

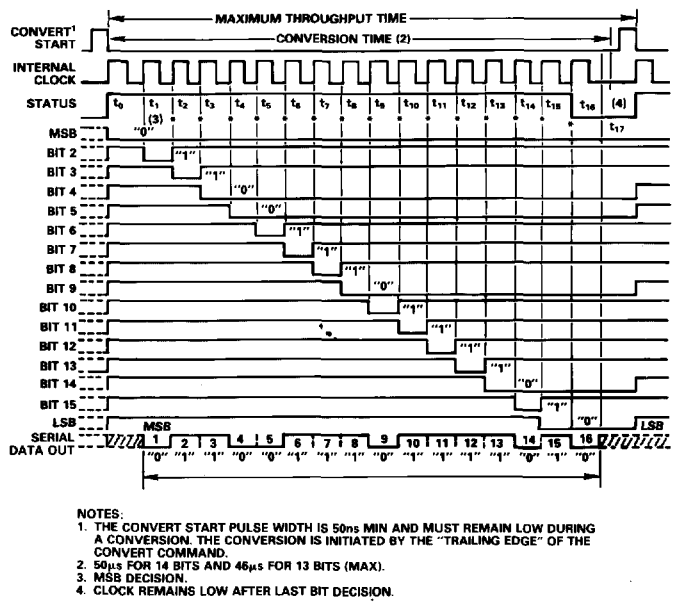

Figure 8. Timing Diagram (Binary Code 0110011101111010)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers is in negative true form (Logic "1" = 0V and Logic "0" = 2.4V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid at least 20ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag (see Figure 9).

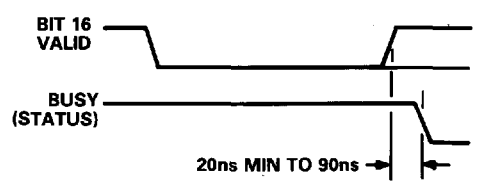

Figure 9. LSB Valid to Status Low

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 120ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 10. There are 17 negative-going clock

edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

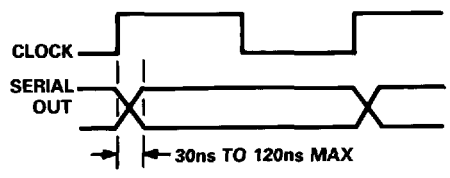

Figure 10. Clock High to Serial Out Valid

Short Cycle Input: A Short Cycle Input, pin 32, permits the timing cycle shown in Figure 8 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, pin 32 is connected to Bit 11 output pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (t_{10} + 40ns in timing diagram of Figure 6). Short cycle connections and associated maximum 8-, 10-, 12-, 13-, 14-, and 15-bit conversion times are summarized in Table I.

Connect Short Cycle Pin 32 to Pin:	Resolution Bits	Resolution (%FSR)	Maximum Conversion Time (μs)	Status Flag Reset
N/C (Open)	16	0.0015	57.0	t_{16} + 40ns
16	15	0.003	53.5	t_{15} + 40ns
15	14	0.006	50.0	t_{14} + 40ns
14	13	0.012	46.5	t_{13} + 40ns
13	12	0.024	42.8	t_{12} + 40ns
11	10	0.100	35.6	t_{10} + 40ns
9	8	0.390	28.5	t_8 + 40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC71 and AD ADC72 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 11 for circuit details.

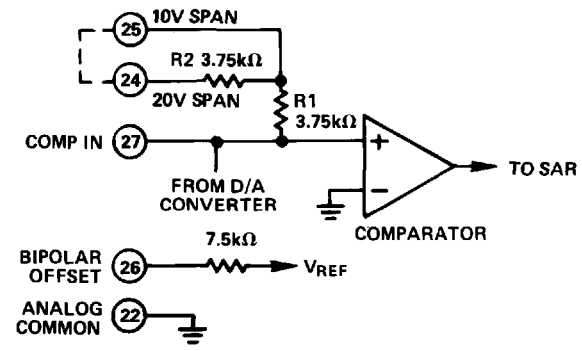

Figure 11. AD ADC71/AD ADC72 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	For Direct Input, Connect Input Signal to
±10V	COB	27	Input Signal	24
±5V	COB	27	Open	25
±2.5V	COB	27	Pin 27	25
0V to +5V	CSB	22	Pin 27	25
0V to +10V	CSB	22	Open	25
0V to +20V	CSB	22	Input Signal	24

Note: Pin 27 is extremely sensitive to noise and must be shielded/guarded by analog common.

Table II. AD ADC71/AD ADC72 Input Scaling Connections

Output Code MSB LSB	Range	±10V	±5V	±2.5V	0 to +10V	0 to +5V
000 . . . 000*	+ Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111	Mid Scale	0 −1/2LSB	0 −1/2LSB	0 −1/2LSB	+5V −1/2LSB	+2.5V −1/2LSB
111 . . . 110	− Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0V +1/2LSB	0V +1/2LSB

*Voltages given are the nominal value for transition to the code specified.
Note: For LSB value for range and resolution used, see Table IV.

Table III. Transition Values vs. Calibration Codes

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	FSR / 2^n	20V / 2^n	10V / 2^n	5V / 2^n	10V / 2^n	5V / 2^n
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
	n = 13	2.44mV	1.22mV	0.61mV	1.22mV	0.61mV
	n = 14	1.22mV	0.61mV	0.31mV	0.61mV	0.31mV
	n = 15	0.61mV	0.31mV	0.15mV	0.31mV	0.15mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Two's Complement – achieved by using an inverter to complement the most significant bit to produce ($\overline{MSB}$).
***CSB = Complementary Straight Binary.

Table IV. Input Voltage Range and LSB Values

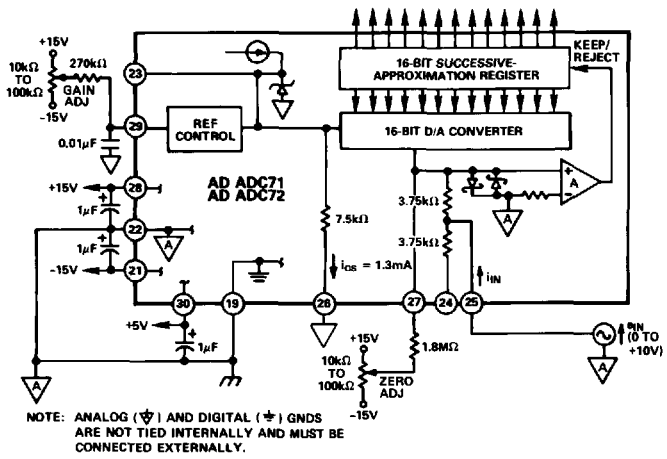

Figure 12. Analog and Power Connections for Unipolar 0 to + 10V Input Range

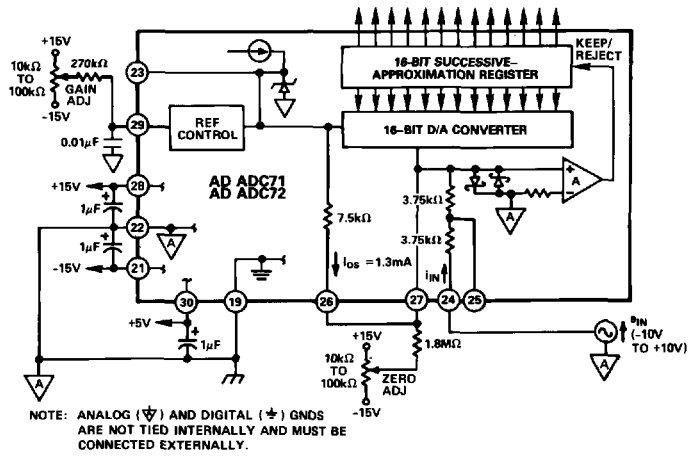

Figure 13. Analog and Power Connections for Bipolar – 10V to + 10V Input Range

CALIBRATION (14-Bit Resolution Examples)
External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 5 and 6, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and – FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to $+1LSB_{14} = 0.00061V$. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR – 2LSB = +9.9987V. Adjust Gain for 00000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000V; digital output code should be 01111111111111.

–10V to +10V Range: Set analog input to –9.99878V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000V; digital output (complementary offset binary) code should be 01111111111111.

Other Ranges: Representative digital coding for 0 to +10V and –10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, –2.5V to +2.5V and –5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and –10V to +10V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Handbook", D. Sheingold, Analog Devices, Inc., 1986, Part II, Chapter 4.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (pins 19 and 22) must be tied together at one point for the AD ADC71/AD ADC72 as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD ADC71/AD ADC72. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD ADC71/AD ADC72 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC71/AD ADC72's supply terminals should be capacitively decoupled as close to the AD ADC71/AD ADC72s as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

On the ceramic package the metal cover is internally grounded with respect to the power supplies, grounds and electrical signals. Do not externally ground the cover.

T/H REQUIREMENTS FOR HIGH RESOLUTION APPLICATIONS

The AD389 is a companion T/H designed for use with the AD ADC71/AD ADC72 family. The characteristics required for high resolution track-and-hold amplifiers are low feedthrough, low pedestal shifts with changes of input signal or temperature, high linearity, low temperature coefficients, and minimal droop rate.

The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The T/H amplifier slew rate determines the maximum frequency tracking rate and part of the settling time when sampling pulses and square waves. The feedthrough from input to output while in the hold mode should be less than 1LSB. The amplitude of 1LSB of the companion A/D converter for a given input range will vary from 610μV for a 14-bit A/D using a 0 to 10V input range to 4.88mV for a 12-bit A/D using a ±10V input range. The hold mode droop rate should produce less than 1LSB of droop in the output during the conversion time of the A/D converter. For 610μV/LSB, as noted in the example above, for a 50μs 14-bit A/D converter, the maximum droop rate will be 610μV/50μs or 12μV/μs during the 50μs conversion period.

Minimal thermal tail effects are another requirement of high resolution applications. The self-heating errors induced by the changing current levels in the output stages of T/H amps may cause more than 1LSB of error due to thermal tail effects.

The linearity error should be less than 1LSB over the transfer function, as set by the resolution of the A/D converter. The T/H acquisition time, T/H settling time along, with the conversion time of the A/D converter determines the highest sampling rate. This in turn will determine the highest input signal frequency that can be sampled at twice a cycle.

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in "under sampling" or aliasing errors of the input signal. In the following table the maximum input frequency is reported as half of the throughput rate, with an ideal brickwall low pass filter placed in the signal path prior to the AD389 and A/D converter to eliminate aliasing.

The pedestal shift due to input signal changes should either be linear, to be seen as a gain error, or negligible as with the feedthrough spec. The temperature coefficients for drift should be low enough such that full accuracy is maintained over some minimum temperature range. The droop rate and pedestal will shift more above +70°C (+158°F). For commercial and industrial users, these shifts will only appear above the highest temperatures their equipment will ever expect to experience. Most precision instrumentation is installed only in human inhabitable work spaces or in controlled enclosures if the area has a hostile environment. Thus, the AD ADC71 or AD ADC72 used with a companion AD389T/H offers high accuracy sampling in high precision applications.

Spec	14 Bit	AD389KD	Units
Aperture Jitter (max)	2.4	0.4	ns
Slew Rate (max w/20V pk-pk signal)	1.26	30	V/μs
Feedthrough (1LSB max)	−84.3	−86	dB
Droop Rate (1LSB max in 15μs)	40.7	0.1	μV/μs
Droop Rate (1LSB max in 50μs)	12.2	0.1	μV/μs
Acquisition Time (to ±1LSB max) for 20kHz Signal w/15μs ADC	10	3-5	μs
Pedestal Shift (max) with Input Signal	−84.3	−86	dB
Gain Temperature Coefficient (max) for ±10°C Ambient Operation	6.1	2.0	ppm/°C
Thermal Tail (max) within 50μs after Hold	1.2	0.1	mV
Linearity Error (max)	±0.0061	0.003	%FSR

Table V. T/H Amplifier Requirements vs. AD389 Specs

AD389 in Combination With an	Maximum Throughput Rate	Maximum Nyquist Input Frequency Range
AD ADC71 (13 bit)	22.2kHz	dc to 11.1kHz
AD ADC72 (14 bit)	16.7kHz	dc to 8.3kHz

Table VI. T/H & ADC Combinations and Maximum Throughput Rate

Using the AD ADC71/AD ADC72 at Slower Conversion Times

The user may wish to run the AD ADC71/AD ADC72 at slower conversion times in order to synchronize the A/D with an external clock. This is accomplished by running a slower clock than the internal clock into the START CONVERT input. This clock

must consist of narrow negative-going clock pulses, as seen in Figure 14. The pulse must be a minimum of 100ns wide but not greater than 700ns. Having a raising edge immediately after a falling edge inhibits the internal clock pulse. This enables the AD ADC71/AD ADC72 to function normally and complete a conversion after 16 clock pulses and serial out in 17 clock pulses. The STATUS command will function normally and switch high after the first clock pulse and will fall low after the 17th clock pulse. In this way an external clock can be used to control the AD ADC71/AD ADC72 at slower conversion times.

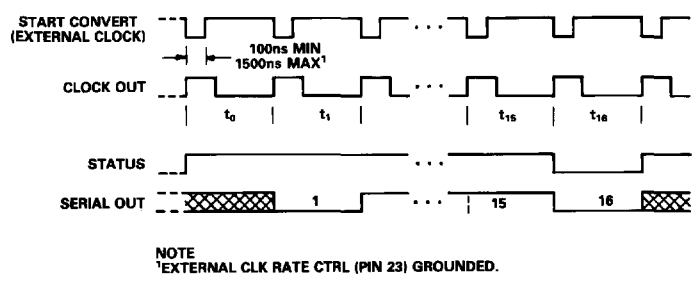

Figure 14. Timing Diagram for Use with an External Clock

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Model	Linearity Error (Max)	Specification Temp Range	Package Option*
AD ADC71JD	±0.006% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC71KD	±0.003% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72JD	±0.006% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72KD	±0.003% of FSR	0 to +70°C	Ceramic (DH-32E)
AD ADC72AD	±0.006% of FSR	−25°C to +85°C	Ceramic (DH-32E)
AD ADC72BD	±0.003% of FSR	−25°C to +85°C	Ceramic (DH-32E)

*DH-32E = Bottom Brazed Ceramic DIP. See outline information see Package Information section.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

32-PIN HERMETIC CERAMIC (AD ADC71/AD ADC72)