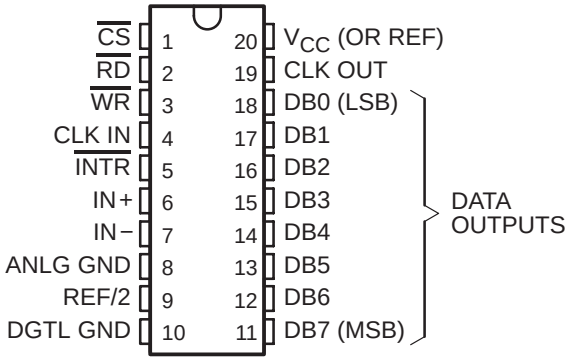
- **8-Bit Resolution**
- **Ratiometric Conversion**
- **100-μs Conversion Time**
- **135-ns Access Time**
- **Guaranteed Monotonicity**
- **High Reference Ladder Impedance 8 kΩ Typical**
- **No Zero Adjust Requirement**
- **On-Chip Clock Generator**
- **Single 5-V Power Supply**
- **Operates With Microprocessor or as Stand-Alone**
- **Designed to Be interchangeable With National Semiconductor and Signetics ADC0803 and ADC0805**

N PACKAGE
(TOP VIEW)



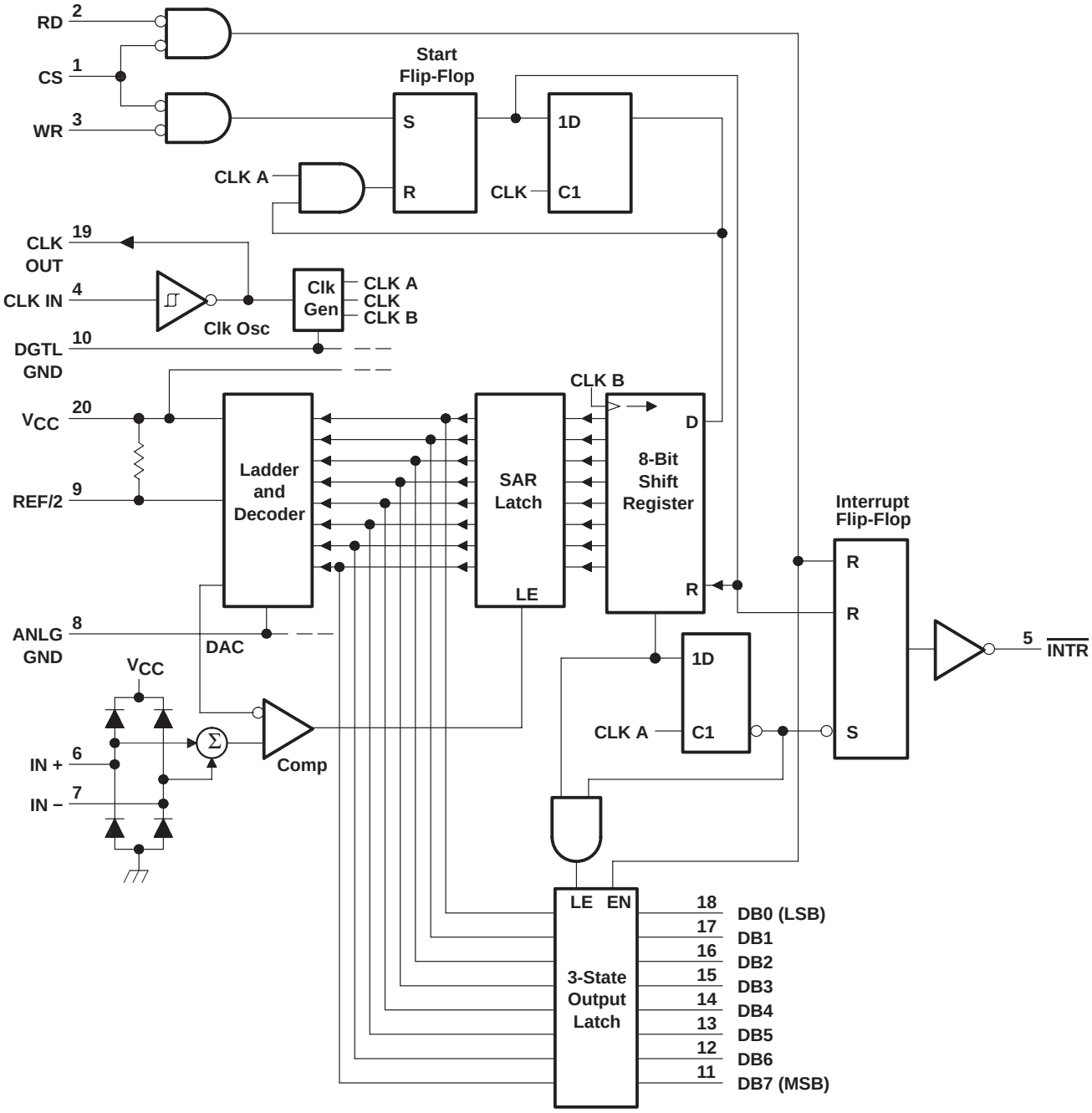
description

The ADC0803 and ADC0805 are CMOS 8-bit, successive-approximation, analog-to-digital converters that use a modified potentiometric (256R) ladder. These devices are designed to operate from common microprocessor control buses with the 3-state output latches driving the data bus. The devices can be made to appear to the microprocessor as a memory location or an I/O port. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

A differential analog voltage input allows increased common-mode rejection and offset of the zero-input analog voltage value. Although a reference input (REF/2) is available to allow 8-bit conversion over smaller analog voltage spans or to make use of an external reference, ratiometric conversion is possible with the REF/2 input open. Without an external reference, the conversion takes place over a span from V_{CC} to ANLG GND. The devices can operate with an external clock signal or with an additional resistor and capacitor, using an on-chip clock generator.

The ADC0803C and ADC0805C are characterized for operation from 0°C to 70°C. The ADC0803I and ADC0805I are characterized for operation from −40°C to 85°C.

functional block diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6.5 V
Input voltage range: $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ . . . . . −0.3 V to 18 V
Other inputs . . . . . −0.3 V to V_{CC} 0.3 V
Output voltage range . . . . . −0.3 V to V_{CC} 0.3 V
Operating free-air temperature range: ADC080_C . . . . . 0°C to 70°C
ADC080_I . . . . . −40°C to 85°C
Storage temperature range . . . . . − 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to digital ground (DGTL GND) with DGTL GND and ANLG GND connected together unless otherwise noted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	6.3	V
Analog input voltage (see Note 2)		−0.05		V_{CC} = 0.05	V
Voltage at REF/2 (see Note 3), $V_{REF/2}$		0.25	2.5		V
High-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$, V_{IH}		2		15	V
Low-level input voltage at $\overline{CS}$, $\overline{RD}$, or $\overline{WR}$, V_{IL}				0.8	V
Analog ground voltage (see Note 4)		−0.05	0	1	V
Clock iput frequency (see Note 5), f_{clock}		100	640	1460	kHz
Duty cycle for f_{clock} above 640 kHz (see Note 5)		40%		60%	
Pulse durartion, clock input (high or low) for f_{clock} below 640 kHz, t_W(CLK)		275	781		ns
Pulse durartion, $\overline{WR}$ input low, t_W(WR)		100			ns
Operating free−air temperature, T_A	ADC080_C	0		70	°C
	ADC080_I	−40		85	

NOTES: 2. When the differential input voltage ($V_{I+} - V_{I-}$) is less than or equal to 0 V, the output code is 0000 0000.
3. The internal reference voltage is equal to the voltage applied to REF/2 or approximately equal to one-half of the V_{CC} when REF/2 is left open. The voltage at REF/2 should be one-half the full-scale differential input voltage between the analog inputs. Thus, the differential input voltage range when REF/2 is open and V_{CC} = 5 V is 0 V to 5 V. $V_{REF/2}$ for an input voltage range from 0.5 V to 3.5 V (full-scale differential voltage of 3 V) is 1.5 V.
4. These values are with respect to DGTL GND.
5. Total unadjusted error is specified only at an f_{clock} of 640 kHz with a duty cycle of 40% to 60% (pulse duration 625 ns to 937 ns). For frequencies above this limit or pulse duration below 625 ns, error may increase. The duty cycle limits should be observed for an f_{clock} greater than 640 kHz. Below 640 kHz, this duty cycle limit can be exceeded provided $t_{w(CLK)}$ remains within limits.

electrical characteristics over recommended range of operating free-air temperature, V_{CC} = 5 V, f_{clock} = 640 kHz, $V_{REF/2}$ = 2.5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = 4.75 V,	I_{OH} = −360 µA		2.4			V
		DB and $\overline{INTR}$	V_{CC} = 4.75 V,	I_{OH} = −10 µA		4.5			
V_{OL}	Low-level output voltage	Data outputs	V_{CC} = 4.75 V,	I_{OL} = 1.6 mA				0.4	V
		$\overline{INTR}$ output	V_{CC} = 4.75 V,	I_{OL} = 1 mA				0.4	
		CLK OUT	V_{CC} = 4.75 V,	I_{OL} = 360 µA				0.4	
V_{T+}	Clock positive-going threshold voltage					2.7	3.1	3.5	V
V_{T-}	Clock negative-going threshold voltage					1.5	1.8	2.1	V
$V_{T+}-V_{T-}$	Clock input hysteresis					0.6	1.3	2	V
I_{IH}	High-level input current						0.005	1	µA
I_{IL}	Low-level input current						−0.005	−1	µA
I_{OZ}	Off-state output current		V_O = 0					−3	µA
			V_O = 5 V					3	
I_{OHS}	Short-current output current	Output high	V_O = 0,	T_A = 25°C		−4.5	−6		mA
I_{OLS}	Short-circuit output current	Output low	V_O = 5 V,	T_A = 25°C		9	16		mA
I_{CC}	Supply current plus reference current		$V_{REF/2}$ = open,	T_A = 25°C,	$\overline{CS}$ = 5 V		1.1	1.8	mA
$R_{REF/2}$	Input resistance to reference ladder		See Note 6			2.5	8		kΩ
C_i	Input capacitance (control)						5	7.5	pF
C_o	Output capacitance (DB)						5	7.5	pF

NOTE 6: Resistance is calculated from the current drawn from a 5-V supply applied to ANLG GND and REF/2.

operating characteristics over recommended operating free-air temperature, V_{CC} = 5 V, $V_{REF/2}$ = 2.5 V, f_{clock} = 640 kHz (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Supply-voltage-variation error		V_{CC} = 4.5 to 5.5 V,	See Note 7		+1/16	±1/8	LSB
	Total adusted error	ADC0803	With full-scale adjust,	See Notes 7 and 8			±1/4	LSB
							±1/2	
	Total unadjusted error	ADC0805	$V_{REF/2}$ = 2.5 V,	See Notes 7 and 8			±1/2	LSB
			$V_{REF/2}$ open,	See Notes 7 and 8			±1	
	DC common-mode error		See Notes 7 and 8			±1/16	±1/8	LSB
t_{en}	Output enable time		T_A = 25°C,	C_L = 100 pF		135	200	ns
t_{dis}	Output disable time		T_A = 25°C, CL = 10 pF,	R_L = 10 kΩ		125	200	ns
$t_{d(INTR)}$	Delay time to reset $\overline{INTR}$		T_A = 25°C			300	450	nx
t_{conv}	Conversion cycle time		f_{clock} = 100 kHz to 1.46 MHz, T_A = 25°C,	See Note 9			73	clock cycles
CR	Free-running conversion rate		$\overline{INTR}$ connected to $\overline{WR}$,	$\overline{CS}$ at 0 V	66		8770	conv/s

† All typical values are at T_A = 25°C.

NOTES: 7. These parameters are specified over the recommended analog input voltage range.
8. All errors are measured with reference to an ideal straight line through the end-points of the analog-to-digital transfer characteristics.
9. Although internal conversion is completed in 64 clock periods, a $\overline{CS}$ or $\overline{WR}$ low-to-high transition is followed by 1 to 8 clock periods before conversion starts. After conversion is complete, part of another clock period is required before a high-to-low transition of $\overline{INTR}$ completes the cycle.

PARAMETER MEASUREMENT INFORMATION

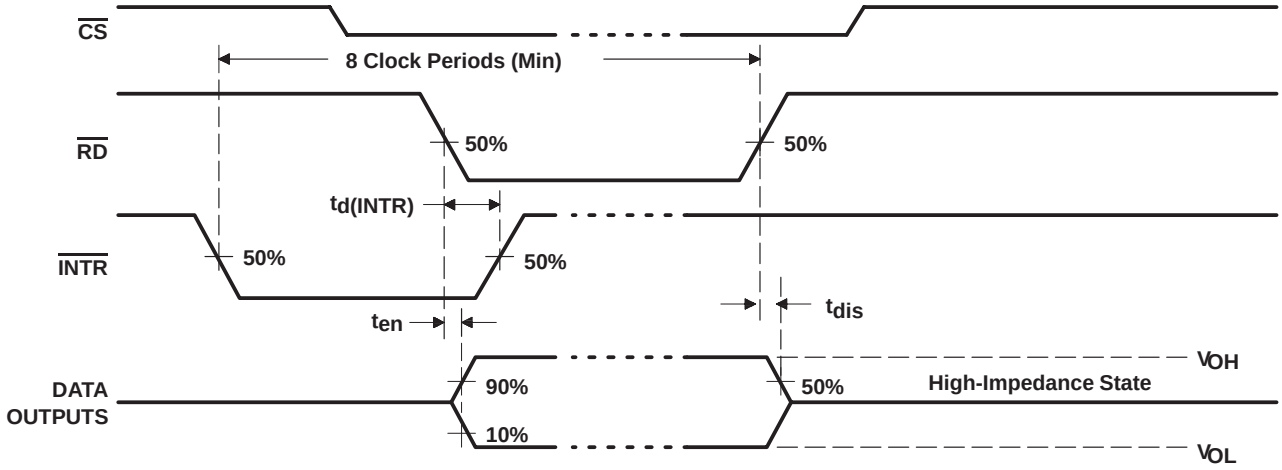

Figure 1. Read Operation Timing Diagram

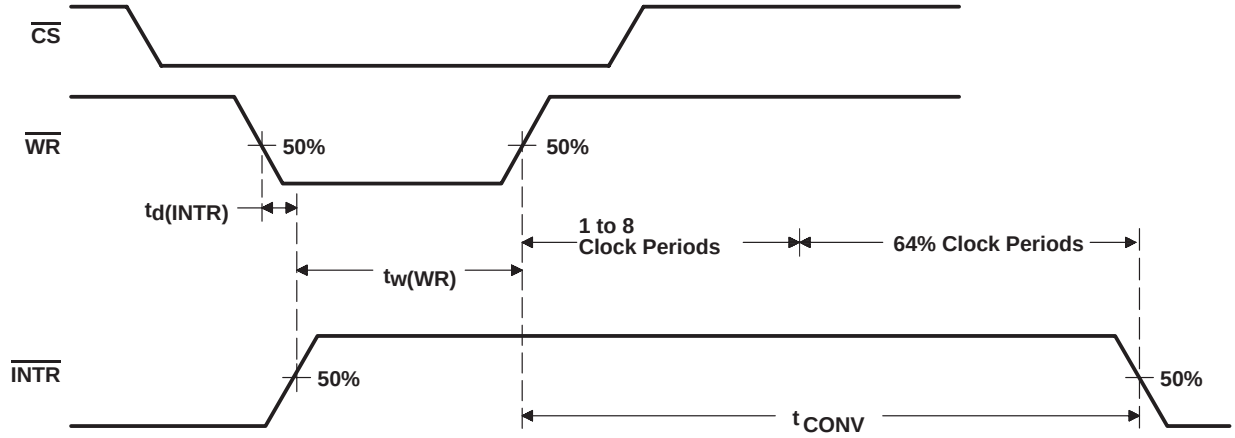

Figure 2. Write Operation Timing Diagram

PRINCIPLES OF OPERATION

The ADC0803 and ADC0805 each contain a circuit equivalent to 256-resistor network. Analog switches are sequenced by successive-approximation logic to match an analog differential input voltage ($V_{I+} - V_{I-}$) to a corresponding tap on the 256R network. The most significant bit (MSB) is tested first. After eight spelled out comparisons (64 clock periods), an eight-bit binary code (1111 1111 = full scale) is transferred to an output latch and the interrupt ($\overline{INTR}$) output goes low. The device can be operated in a free-running mode by connecting the $\overline{INTR}$ output to the write ($\overline{WR}$) input and holding the conversion start ($\overline{CS}$) input at a low level. To ensure start up under all conditions, a low-level $\overline{WR}$ input is required during the power-up cycle. Taking $\overline{CS}$ low any time after that will interrupt a conversion in process.

When $\overline{WR}$ goes low, the internal successive-approximation register (SAR) and 8-bit shift register are reset. As long as both $\overline{CS}$ and $\overline{WR}$ remain low, the analog-to-digital converter remains in a reset state. One to eight clock periods after $\overline{CS}$ or $\overline{WR}$ makes a low-to-high transition, conversion starts.

When $\overline{CS}$ and $\overline{WR}$ are low, the start flip-flop is set and the interrupt flip-flop and 8-bit register are reset. The next clock pulse transfers a logic high to the output of the start flip-flop. The logic high is ANDed with the next clock pulse, placing a logic high on the reset input of the start flip-flop. If either $\overline{CS}$ or $\overline{WR}$ have gone high, the set signal to the start flip-flop is removed, causing it to be reset. A logic high is placed on the D input of the eight-bit shift register and the conversion process is started. If $\overline{CS}$ and $\overline{WR}$ are still low, the start flip-flop, the 8-bit shift register, and the SAR remain reset. This action allows for wide $\overline{CS}$ and $\overline{WR}$ inputs, with conversion starting from one to eight clock periods after one of the inputs goes high.

When the logic high input has been clocked through the 8-bit shift register, which completes the SAR search, it is applied to an AND gate controlling the output latches and to the D input of a flip-flop. On the next clock pulse, the digital word is transferred to the 3-state output latches and the interrupt flip-flop is set. The output of the interrupt flip-flop is inverted to provide an $\overline{INTR}$ output that is high during conversion and low when the conversion is complete.

When a low is at both $\overline{CS}$ and $\overline{RD}$, an output is applied to the DB0 through DB7 outputs and the interrupt flip-flop is reset. When either $\overline{CS}$ or $\overline{RD}$ return to a high state, the DB0 through DB7 outputs are disabled (returned to the high-impedance state). The interrupt flip-flop remains reset.

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