National Semiconductor

ADC0829 μP Compatible 8-Bit A/D with 11-Channel MUX/Digital Input

General Description

The ADC0829 is an 8-bit successive approximation A/D converter with an 11-channel multiplexer of which six can be used as digital inputs, as well as, analog inputs.

This A/D is designed to operate from the μP data bus using a single 5V supply.

Channel selection, conversion control, software configuration and bus interface logic are all contained on this monolithic CMOS device.

This device contains three 16-bit registers which are accessed via double byte instructions. The control register is a write only register which controls the start of a new conversion, selects the channel to be converted, configures the 8-bit I/O port as input or output, and provides information for the 8-bit output register.

The conversion results register is a read only register which contains the current status and most recent conversion results. The discrete input register is also a read only register which contains the four address bits of the selected channel, and the six discrete inputs which are connected to the analog multiplexer.

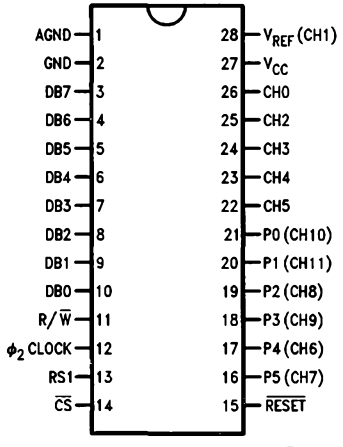
Features

- Easy interface to all microprocessors or operates "stand alone"
- Operates ratiometrically or with analog span adjusted voltage reference
- 11-Channel multiplexer with latched control logic of which six can be used as digital inputs
- 0 to 5V analog input range with single 5V supply
- TTL/MOS input/output compatible
- No zero or full scale adjusts required
- Standard 28-pin DIP
- Temperature range −40°C to +85°C
- ADC0829 equivalent to MM74C934

Key Specification

Resolution	8 Bits
Total Unadjusted Error	±½ LSB and ±1 LSB
Conversion Time	256 μs
Single Supply	$5V_{DC}$
Low Power	50 mW

Connection and Block Diagrams



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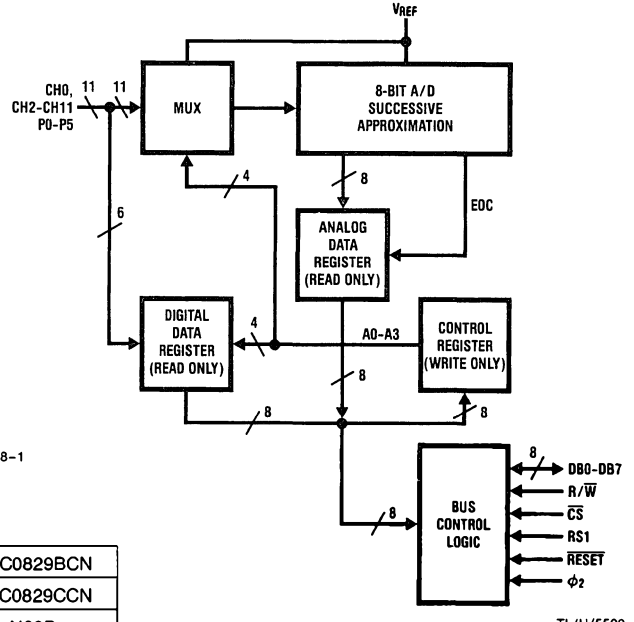
Top View



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Ordering Information

Error	± 1/2 Bit Unadjusted	ADC0829BCN
	± 1 Bit Unadjusted	ADC0829CCN
Package Outline		N28B

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to V_{CC} + 0.3V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Storage Temperature	−65°C to + 150°C
Package Dissipation at T_A = 25°C (Board Mount)	875 mW
Lead Temp. (Soldering, 10 seconds)	260°C
ESD Susceptability (Note 8)	2000V
Input Current Per Pin	±5 mA
Package	+20 mA

Operating Conditions (Notes 1 and 2)

Supply Voltage, V_{CC}	4.75 V_{DC} to 5.5 V_{DC}
Temperature Range	−40°C to + 85°C

Converter and Multiplexer Electrical Characteristics

$V_{CC}=5V_{DC}=V_{REF}(+)$, $V_{REF}(-)=GND$, SCLK $\phi_2=1.048$ MHz, $-40°C \le T_A + 85°C$ unless otherwise noted.

Parameter	Conditions		Min	Typ (Notes)	Max	Units
Total Unadjusted Error; (Note 3)						
ADC0829BCN	V_{REF} Forced to 5.000 V_{DC}				±½	LSB
ADC0829CCN	V_{REF} Forced to 5.000 V_{DC}				±1	LSB
Reference Input Resistance			1.0	4.5		kΩ
Analog Input Voltage Range	(Note 4) V(+) or V(−)		GND-0.10		V_{CC}+0.10	V
$V_{REF}(+)$ Voltage, Top of Ladder	Measured at REF(+)			V_{CC}	V_{CC}+0.01	V
$\frac{V_{REF}(+)+V_{REF}(-)}{2}$ Voltage, Center of Ladder			$V_{CC/2}-0.1$	$V_{CC/2}$	$V_{CC/2}+0.01$	V
$V_{REF}(-)$ Voltage, Bottom of Ladder	Measured at REF(−)		−0.1	0		V
I_{OFF}, Off Channel	ON Channel = 5V	ADC0829BCN			±400	nA
Leakage Current (Note 6)	OFF Channel = 0V	ADC0829CCN			±1	μA
I_{ON}, On Channel	ON Channel = 0V	ADC0829BCN			±400	nA
Leakage Current (Note 6)	OFF Channel = 5V	ADC0829CCN			±1	μA

AC Characteristics

$V_{CC}=V_{REF}(+)=5V$, $t_r=t_f=20$ ns and $T_A=25°C$ (Note 7) unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
$t_{CYC}(\phi_2)$, ϕ_2 Clock Cycle Time ($1/f_{\phi 2}$)		0.943		10.0	μs
$PW_H(\phi_2)$, ϕ_2 Clock Pulse Width, High		440			ns
$PW_L(\phi_2)$, ϕ_2 Clock Pulse Width, Low		410			ns
$t_r(\phi_2)$, ϕ_2 Rise Time				25	ns
$t_f(\phi_2)$, ϕ_2 Fall Time				30	ns
t_{AS}, Address Set Up Time	RS1, R/$\overline{W}$, $\overline{CS}$	145			ns
t_{DDR}, Data Delay (Read)	DB0-DB7			335	ns
t_{DSW}, Data Delay Setup (Write)	DB0-DB7	185			ns
t_{AH}, Address Hold Time	RS1, R/$\overline{W}$, $\overline{CE}$	20			ns
t_{DHW}, Input Data Hold Time	DB0-DB7	20			ns
t_{DHR}, Output Data Hold Time	DB0-DB7	10			ns
Analog Channel Settling Time		32			Clocks
t_c, Conversion Time		256			Clocks

Digital and DC Characteristics V_{CC} = 4.5V to 5.5V and $-40°C \leq T_A \leq 85°C$ unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Bus Control Inputs (R/$\overline{W}$, ENABLE $\overline{RESET}$, RS1, $\overline{CS}$) and Peripheral Inputs (P0-P5)					
$V_{IN}(1)$, Logical "1" Input Voltage		2.0			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.8	V
I_{IN}, Input Leakage Current				±1	μA
ϕ_2 CLOCK INPUT					
$V_{IN}(1)$, Logical "1" Input Voltage		$V_{CC}-0.8$			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.4	V
Data Bus (DB0-DB7)					
$V_{IN}(1)$, Logical "1" Input Voltage		2.0			V
$V_{IN}(0)$, Logical "0" Input Voltage				0.8	V
I_{OUT}, TRI-STATE® Output Current	$V_{OUT}=0V$			−10	μA
	$V_{OUT}=5V$			10	μA
$V_{OUT}(1)$, Logical "1" Output Voltage	$I_{OUT}=-1.6$ mA	2.4			V
$V_{OUT}(0)$, Logical "0" Output Voltage	$I_{OUT}=1.6$ mA			0.4	V
Power Supply Requirements					
I_{CC}, Supply Current				10	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to ground.

Note 3: Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than V_{CC} supply. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.90 V_{DC} over temperature variations, initial tolerance and loading.

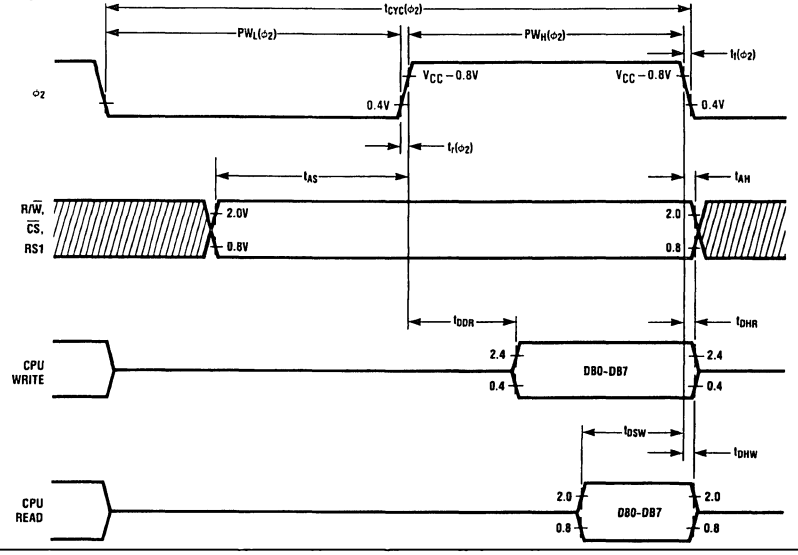
Note 5: Typicals are at 25°C and represent most likely parametric norm.

Note 6: Off channel leakage current is measured after the channel selection.

Note 7: The temperature coefficient is 0.3%/°C.

Note 8: Human Body Model, 100 pF discharged through a 1.5 kΩ resistor.

Timing Diagram



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Pin Descriptions

ANALOG AND DIGITAL INPUTS

CH0, CH2-CH5—These are dedicated analog inputs. They are fed directly to the internal 12 to 1 multiplexer which feeds the A/D converter.

P0-P5/CH6-CH11—These 6 pins are dual purpose and may be used as either TTL compatible digital inputs, or analog inputs. When used as digital inputs they may be read via the discrete input register. When they are used as analog inputs they function like CH-0, CH2-5.

MICROPROCESSOR INTERFACE SIGNALS

DB0-DB7—The bi-directional data lines for the data bus connect to the μP's main data bus to enable data transfer to and from the μP. DB0-DB7 remain in a high impedance state unless the ADC0829 is read.

ϕ_2 Clock—This signal is used for two purposes. First it synchronizes data transfer in and out of the ADC. Second, it is the master clock for the A/D converter logic and all other timing signals are derived from it.

R/$\overline{W}$—The read/write pin controls the direction of data transfer on D0-D7.

$\overline{RESET}$—A low on this pin forces the ADC0829 into a known state. The start bit is cleared, Channel CH0 is selected and the internal byte counter is reset to the MS Byte. The A/D data register is not reset. Reset must be held low for at least 3 clocks.

$\overline{CS}$—Chip Select must be low in order for data transfer between the ADC0829 and the μP to occur.

RS1—The Register Select pin is used to address the internal registers.

POWER SUPPLY PINS

V_{CC}—This is the positive 5V supply pin. It powers the digital load and the sample data comparator. Care should be exercised to ensure that supply noise on this pin is adequately filtered, by using a bypass capacitor from V_{CC} to D_{GND}.

D_{GND}—Digital ground should be connected to the systems digital ground.

V_{REF} and A_{GND}—The positive reference pin attaches to the top of the 256R resistor ladder and sets the full scale conversion voltage value. The A_{GND} connects to the bottom of the ladder. The conversion result is ratiometric to V_{REF} - A_{GND} and hence both V_{REF} and A_{GND} should be noise free. Ideally the V_{REF} and A_{GND} should be single point connected to the analog transducer's supply. The V_{REF} and A_{GND} voltages typically are 5V and Ground but they may be varied so long as $(V_{REF}-A_{GND})/2 = V_{CC}/2 \pm 0.1V$.

Functional Description

1.0 CONTROL LOGIC

The Control Logic interprets the microprocessor control signals and decodes these signals to perform the actual functions of selecting, reading, writing, enabling the outputs, etc.

2.0 STATE DESCRIPTIONS

There are three internal states within the A/D converter: the NO OP state; the sample state; and the converting state.

The NO OP state is a stable state since the external stimulus (e.g. start conversion signal) is needed for a state transition.

The first transient state is sampling the input. The first 32 clocks of the conversion are used for acquiring the channel; this settling time allows any transients to decay before conversion begins. The second transient state is the actual conversion. The conversion is completed in 256 clocks and the conversion results register is updated. The converter then returns to the stable NO OP state awaiting further instructions.

The device has no comparator bias current and draws minimal power during the NO OP state.

3.0 INITIALIZATION

The device is initialized by an active low on $\overline{RESET}$. All outputs are initialized to the inactive state and the converter placed in its NO OP state. The data register is not affected by $\overline{RESET}$. System TRI-STATE outputs are initialized to the high impedance state.

4.0 CONVERSION CONTROL

The program normally initiates a conversion cycle with a double write command. (See control word format.) The control word selects a channel, configures the peripheral I/O, and provides peripheral data information. The conversion is initiated by setting the SC bit in the control word high.

The converter then resets the start conversion bit and begins the conversion cycle.

When the conversion is complete and the new conversion results transferred to the data register, the status bit is set. The status bit is not reset when the conversion status is read. A full double byte write into the control word will reset the status bit, or a low level at master $\overline{RESET}$.

If a new conversion command occurs during a conversion, the conversion is aborted and a new channel acquisition phase will immediately begin.

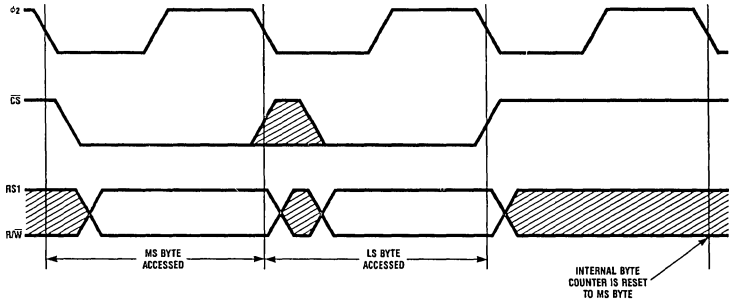
5.0 CONTROL STRUCTURE

The control logic continually monitors the control bus waiting for $\overline{CS}$ to go low and ϕ_2 to go high. When this condition occurs, the internal decoder, which has already selected the proper function, activitates.

The byte counter will always select the most significant (MS) half first, and the least significant (LS) half second. Single byte instructions will always access the MSB portion of any word. After a single byte instruction the byte counter will return to the MSB portion of a word when $\overline{CS}$ is high for a full clock cycle. A 16-bit read or write is accomplished by using a 16-bit load or store instruction which transfers each byte on consecutive clock cycles. This timing is shown in *Figure 1*. A single byte instruction is especially useful for reading the status bit during a polled interrupt. *Figure 2* shows the basic A/D conversion timing sequence and flow.

Functional Description (Continued)

Timing for a Typical μP 16 Byte Access



Timing for a Typical μP 8 Byte Access

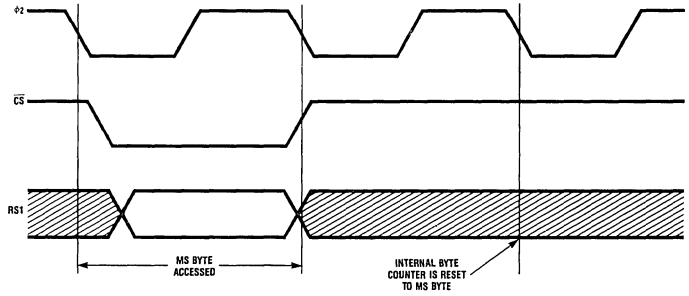


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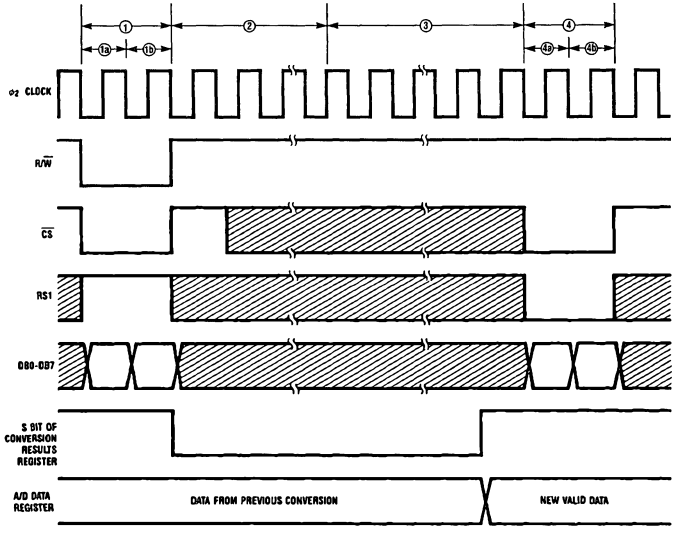
FIGURE 1



(1) START CONVERSION
  (a) SET SC BIT TO A 1
  (b) LOAD ADDRESS
(2) ANALOG INPUT SETTLING TIME ALLOWS INTERNAL MULTIPLEXER TO SELECT A CHANNEL AND STABILIZE (~ 32 CLOCKS).
(3) A/D CONVERSION TIME (~ 256 CLOCKS)
(4) READ END OF CONVERSION DATA
  (a) EOC BIT READ IF A 1 CONVERSION COMPLETE.
  (b) A/D DATA REGISTER READ. IF EOC = 1, THEN NEW VALID DATA.

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FIGURE 2. A/D Conversion Timing Sequence

Functional Description (Continued)

6.0 WORD FORMAT

6.1 Control Register Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
X	X	X	X	X	X	X	(LSB) SC	X	X	X	X	A3 CH3	A2 CH2	A1 CH1	A0 CH0

X: Don't Care

SC: Start Conversion
1 = Start new conversion
0 = Do not start new conversion

CH3-CH0: Channel Address

Hex Value	Definition
0	Select CH0
1	Select $V_{ref}(+)$
2-5	Select Channels CH2-CH5
6-9	Undefined
A	CH10
B	CH11
C	CH8
D	CH9
E	CH6
F	CH7

6.2 Conversion Results Register Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
S	0	0	0	0	0	0	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0

S: Status
1 = Data is valid (conversion complete)
0 = Data is not valid

C_7-C_0: 8 bit converted result

6.3 Discrete Input Word Format

← MSB Word →								← LSB WORD →							
DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
P5	P4	P3	P2	P1	P0	CH3	CH2	CH1	CH0	0	0	0	0	0	0

CH3-CH0: Status of channel address

P5-P0: Status of P5-P0 interpreted as discrete digital inputs

ADU ADDRESS SELECTION

CSO*	R/W	RSI	Description
1	X	X	Do not respond
0	0	0	Write NO OP
0	0	1	Write Control Word
0	1	0	Read Conversion Results
0	1	1	Read Discrete Inputs

Note: All words are transferred as two 8-bit bytes, MSB transferred first LSB transferred second.

7.0 ANALOG TO DIGITAL CONVERTER

The ADC0829 A/D Converter is composed of three major sections: the successive approximation register (SAR); the 256R ladder and analog decoder; and the sample-data comparator.

7.1 Successive Approximation

The analog signal at the A/D input is compared eight times to various ladder voltages to determine which of the 256 voltages in the ladder most closely approximates the input voltage. This stochastic technique is accomplished by converging on the proper tap in the ladder by simple iterative convergence. There are nine posting registers in the SAR which contain the position of the bit being tested and eight latching registers which remember if the comparison was high or low. Starting with the MSB and continuing downward each bit is set high by the posting register. The analog tree decoder selects the corresponding tap in the ladder and the A/D input is compared to that voltage. If the comparison is positive the latch remains set, so higher voltages in the ladder are checked next. If the comparison is negative the bit is reset so lower ladder voltages are sought.

After all eight comparisons are made, the contents of the latching register are transferred to a data register, thus the A/D can perform a new conversion while the previous results remain available.

7.2 256R Ladder

The ladder is a very accurate voltage divider which divides the reference voltage into 256 equal steps. Special consideration was given to the ladder terminations at each end, and also the center, to ensure consistent and accurate voltage steps. The use of a 256R ladder guarantees monotonicity since only a single voltage gradient across the ladder exists. Shorted or unequal resistors in the ladder may cause non-uniform steps but cannot cause a nonmonotonic response so often fatal in closed loop system applications. (See *Figure 3.*)

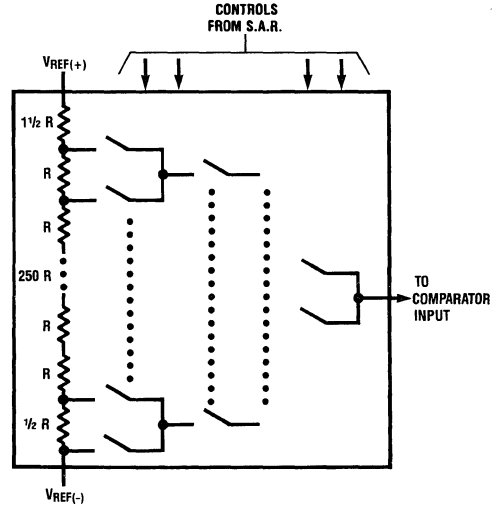

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FIGURE 3. Resistor Ladder and Switch Tree

Functional Description (Continued)

Actually of the 256 resistors in the ladder, 254 have the same value while the end point resistors are equal to 1-1/2R and 1/2R. This ensures the system output characteristic is symmetrical with the zero and full scale points of its input to output, or transfer curve.

The tree decoder routes the 256 voltages from the ladder to a single point at the comparator input. This allows comparisons between the A/D input and any voltage the SAR directs the decoder to route to the comparator.

Since the ladder is dependent upon only the matching of resistors, the voltages it generates are very stable with temperature and have excellent repeatability and long term drift.

8.0 MULTIPLEXER

8.1 Analog Inputs

The analog multiplexer selects one of 11 channels and directs them to the input of the A/D converter. The multiplexer was designed to minimize the effects of leakage currents and multiplexer output capacitance.

Special input protection is used to prevent damage from static voltages or voltages exceeding the specified range from $-0.3V$ to $V_{CC}+0.3V$. However, normal precautions are recommended to avoid such situations whenever possible.

8.2 Digital Inputs

Six of the analog inputs can also be used as digital inputs to sense TTL voltage levels. Care must be taken when these inputs are interpreted since TTL levels may not always be present.

8.3 A/D Comparator

Probably the most important section of the A/D converter is the comparator since the comparator's offset voltage and stability determine the converter's ultimate accuracy. The low voltage offset of the chopper-stabilized comparator of this converter optimizes performance by minimizing temperature dependent input offset errors as well as drift.

The dc signal appearing at the amplifier input is converted to an ac signal, amplified by an ac amplifier and restored to a dc signal. The drift of the comparator is minimized since the drift signal is a dc component blocked by the ac amplifier.

The comparator has very high input impedance to dc voltages since it looks like a capacitor. Because the comparator is chopping the dc voltages at the input, the difference between the A/D input voltage and ladder voltage appears on the comparator's input capacitor. The input voltage difference, chopping frequency, and comparator input capacitor causes a CVF current. The CVF current is a small bias current which will not produce any error when the A/D input is connected to a low impedance voltage source. If the voltage source has an output impedance of less than 10k, the error is still insignificant since the bias current exponentially decays.

Adding a capacitor to the input of the comparator integrates the exponential charging current converting it into dc bias current. (See Figure 1.) Two main considerations on the integration capacitor are charge sharing with a filter capacitor and settling time.

9.0 BUS INTERFACE

The ADC0829 communicates to the microprocessor through an 8-bit I/O port. The I/O port is composed of a TTL to CMOS buffer and a TRI-STATE® output driver.

The TTL to CMOS Buffer translates the TTL voltage levels into CMOS levels very rapidly and is quite stable with supply and temperature. The buffer has a small amount of hysteresis (about 100 mV) to improve both noise immunity and internal rise and fall times.

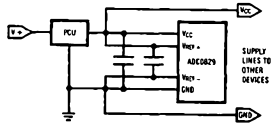
The TRI-STATE bus driver is a bipolar and N-channel pair that easily drive the bus capacitance. Since the bus drivers collectively can sink or source a quarter of an amp total, a non-overlap circuit is used which guarantees that only one of the two drive transistors is on at a time.

Since this output drives the bus capacitance, even the non-overlapping circuit cannot prevent noise on V_{CC}. The amount of noise depends on the V_{CC} current used to charge the bus capacitance.

The external filter capacitor on V_{CC} provides some of the transient current while the bus is being driven. A capacitor with good ac characteristics and low series resistance is a good choice to prevent V_{CC} transients from affecting accuracy.

Application Information

Recommended Supply



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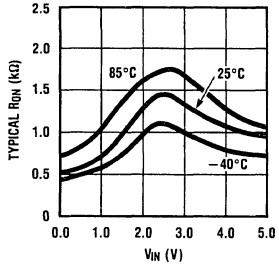
Multiplexer R_{ON} vs V_{IN}
($V_{CC}=V_{REF}=5V$)



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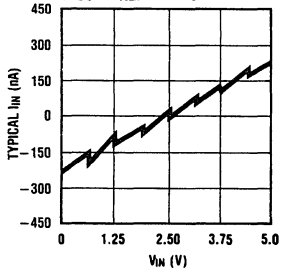
Comparator I_{IN} vs V_{IN}
($V_{CC}=V_{REF}=5V$, $f_C=1.048$ MHz)



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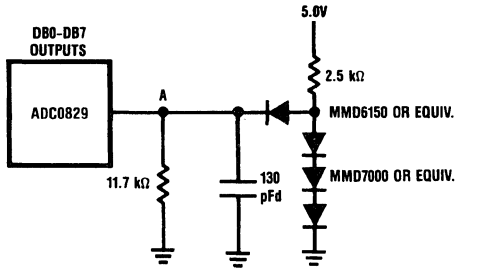
Data Bus Test Circuit



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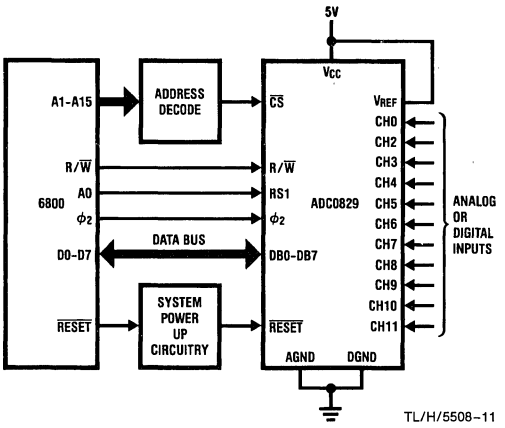
Typical Application



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