National Semiconductor

ADC0831/ADC0832/ADC0834 and ADC0838 8-Bit Serial I/O A/D Converters with Multiplexer Options

General Description

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or μPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

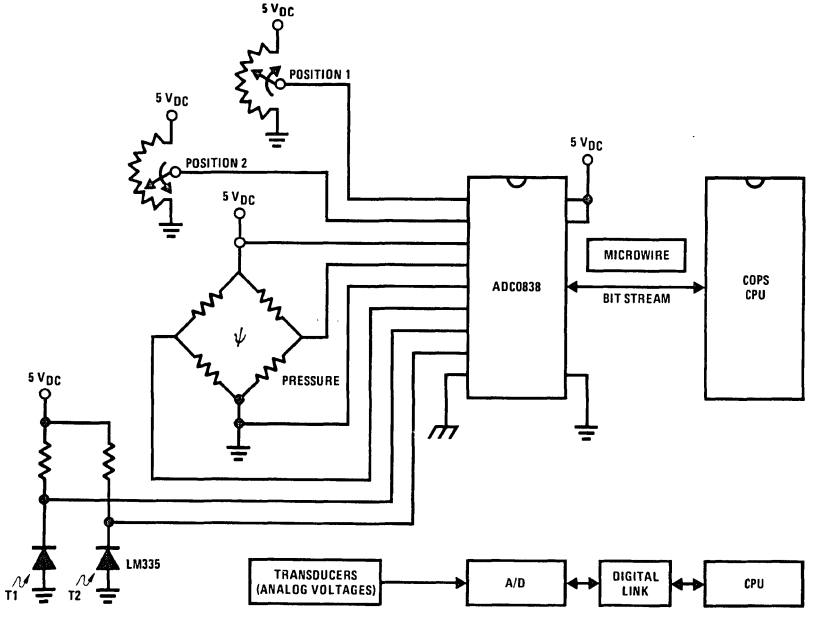
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand-alone"
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 2-, 4- or 8-channel multiplexer options with address logic
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- TTL/MOS input/output compatible
- 0.3" standard width, 8-, 14- or 20-pin DIP package
- 20 Pin Molded Chip Carrier Package (ADC0838 only)

Key Specifications

Resolution	8 Bits
Total Unadjusted Error	±½ LSB and ±1 LSB
Single Supply	5 V_{DC}
Low Power	15 mW
Conversion Time	32 μs

Typical Application



TL/H/5583–1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to V_{CC} + 0.3V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 4)	±5 mA
Package	±20 mA
Storage Temperature	−65°C to +150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temperature (Soldering 10 sec.)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Susceptibility (Note 5)	2000V

Operating Ratings (Notes 1 & 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0831/2/4/8BJ	−55°C to +125°C
ADC0831/2/4/8CJ	
ADC0831/2/4/8BCJ	−40°C to +85°C
ADC0831/2/4/8CCJ	
ADC0831/2/4/8BCN	−0°C to +70°C
ADC0838BCV	
ADC0831/2/4/8CCN	
ADC0838CCV	

Converter and Multiplexer Electrical Characteristics

The following specifications apply for V_{CC} = V+ = V_{REF} = 5V, $V_{REF} \le V_{CC}$ +0.1V, $T_A = T_j$ = 25°C, and f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	BJ, CJ, BCJ and CCJ Devices			BCV, CCV, BCN and CCN Devices			Units
		Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS								
Total Unadjusted Error	V_{REF} = 5.00 V							
ADC0838BCV	(Note 6)					±½	±½	
ADC0831/2/4/8BCN							±½	LSB
ADC0831/2/4/8BJ			±½			±½		
ADC0831/2/4/8BCJ			±½					
ADC0838CCV						±1	±1	
ADC0831/2/4/8CCN						±1	**±1**	
ADC0831/2/4/8CJ			**±1**					
ADC0831/2/4/8CCJ			**±1**					
Minimum Reference Input Resistance (Note 7)		3.5	**1.3**		3.5	1.3	**1.3**	kΩ
Maximum Reference Input Resistance (Note 7)		3.5	**5.9**		3.5	5.4	**5.9**	kΩ
Maximum Common-Mode Input Range (Note 8)			**V_{CC} +0.05**			V_{CC} +0.05	**V_{CC} +0.05**	V
Minimum Common-Mode Input Range (Note 8)			**GND −0.05**			GND −0.05	**GND −0.05**	V
DC Common-Mode Error		±1/16	±¼		±1/16	±¼	±¼	LSB
Change in zero error from V_{CC} = 5V to internal zener operation (Note 3)	15 mA into V+ V_{CC} = N.C. V_{REF} = 5V		**1**			1	**1**	LSB
V_Z, internal diode breakdown (at V+) (Note 3) MIN	15 mA into V+		**6.3**			6.3	**6.3**	
MAX			**8.5**			8.5	**8.5**	V
Power Supply Sensitivity	V_{CC} = 5V ±5%	±1/16	±¼	±¼	±1/16	±¼	±¼	LSB

Converter and Multiplexer Electrical Characteristics (Continued)

The following specifications apply for V_{CC} = V+ = 5V, T_A = T_j = 25°C, and f_{CLK} = 250 kHz unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}.**

Parameter	Conditions	BJ, CJ, BCJ and CCJ Devices			BCV, CCV, BCN and CCN Devices			Units
		Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)								
I_{OFF}, Off Channel Leakage Current (Note 9)	On Channel = 5V, Off Channel = 0V		−0.2 **−1**			−0.2	**−1**	μA
	On Channel = 0V, Off Channel = 5V		+0.2 **+1**			+0.2	**+1**	μA
I_{ON}, On Channel Leakage Current (Note 9)	On Channel = 0V, Off Channel = 5V		−0.2 **−1**			−0.2	**−1**	μA
	On Channel = 5V, Off Channel = 0V		+0.2 **+1**			+0.2	**+1**	μA
DIGITAL AND DC CHARACTERISTICS								
$V_{IN(1)}$, Logical "1" Input Voltage (Min)	V_{CC} = 5.25V		**2.0**			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage (Max)	V_{CC} = 4.75V		**0.8**			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current (Max)	V_{IN} = 5.0V	0.005	**1**		0.005	1	**1**	μA
$I_{IN(0)}$, Logical "0" Input Current (Max)	V_{IN} = 0V	−0.005	**−1**		−0.005	−1	**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage (Min)	V_{CC} = 4.75V I_{OUT} = −360 μA I_{OUT} = −10 μA		 **2.4** **4.5**			 2.4 4.5	 **2.4** **4.5**	 V V
$V_{OUT(0)}$, Logical "0" Output Voltage (Max)	V_{CC} = 4.75V I_{OUT} = 1.6 mA		**0.4**			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (Max)	V_{OUT} = 0V V_{OUT} = 5V	−0.1 0.1	**−3** **3**		−0.1 0.1	−3 +3	**−3** **+3**	μA μA
I_{SOURCE}, Output Source Current (Min)	V_{OUT} = 0V	−14	**−6.5**		−14	−7.5	**−6.5**	mA
I_{SINK}, Output Sink Current (Min)	V_{OUT} = V_{CC}	16	**8.0**		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Max) ADC0831, ADC0834, ADC0838		0.9	**2.5**		0.9	2.5	**2.5**	mA
ADC0832	Includes Ladder Current	2.3	**6.5**		2.3	6.5	**6.5**	mA

AC Characteristics

The following specifications apply for V_{CC} = 5V, t_r = t_f = 20 ns and 25°C unless otherwise specified.

Parameter		Conditions	Typ (Note 12)	Tested Limit (Note 13)	Design Limit (Note 14)	Limit Units
f_{CLK}, Clock Frequency	Min			10		kHz
	Max				400	kHz
t_C, Conversion Time		Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle (Note 10)	Min				40	%
	Max				60	%
t_{SET-UP}, $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge					250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge					90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 11)		C_L = 100 pF				
		Data MSB First	650		1500	ns
		Data LSB First	250		600	ns
t_{1H}, t_{0H},—Rising Edge of CS to Data Output and SARS Hi-Z		C_L = 10 pF, R_L = 10k (see TRI-STATE® Test Circuits)	125		250	ns
		C_L = 100 pf, R_L = 2k		500		ns
C_{IN}, Capacitance of Logic Input			5			pF
C_{OUT}, Capacitance of Logic Outputs			5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground plugs.

Note 3: Internal zener diodes (6.3 to 8.5V) are connected from V+ to GND and V_{CC} to GND. The zener at V+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V+. Functionality is therefore guaranteed for V+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max of 6.5V. It is recommended that a resistor be used to limit the max current into V+. (See *Figure 3* in Functional Description Section 6.0)

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

Note 7: Cannot be tested for ADC0832.

Note 8: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater then the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 9: Leakage current is measured with the clock not switching.

Note 10: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum, time the clock is high or the minimum time the clock is low must be at least 1 μs. The maximum time the clock can be high is 60 μs. The clock can be stopped when low so long as the analog input voltage remains stable.

Note 11: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

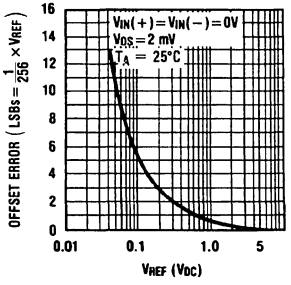
Note 12: Typicals are at 25°C and represent most likely parametric norm.

Note 13: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

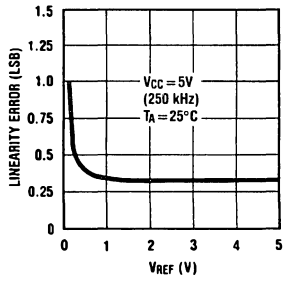
Note 14: Guaranteed but not 100% production tested. These limits are not used to calculate outgoing quality levels.

Typical Performance Characteristics

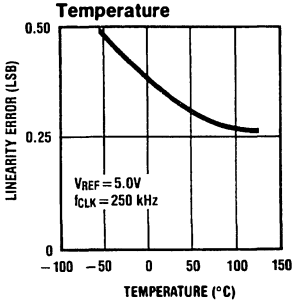
Unadjusted Offset Error vs V_{REF} Voltage



Linearity Error vs V_{REF} Voltage

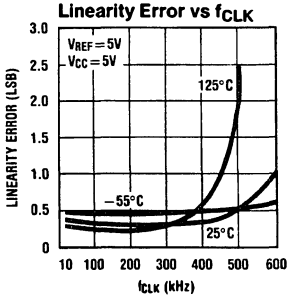


Linearity Error vs Temperature

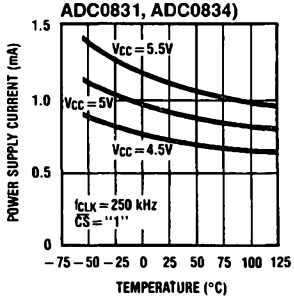


TL/H/5583–2

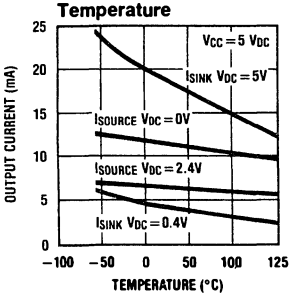
Linearity Error vs f_{CLK}



Power Supply Current vs Temperature (ADC0838, ADC0831, ADC0834)



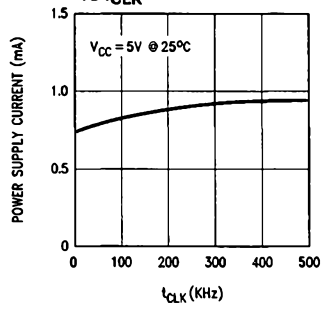
Output Current vs Temperature



Note: For ADC0832 add I_{REF}.

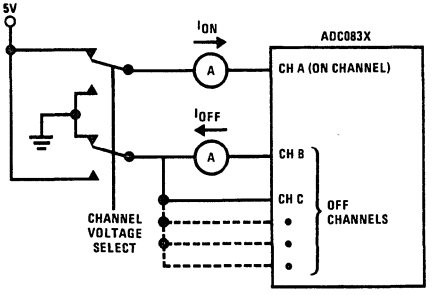
TL/H/5583–40

Power Supply Current vs f_{CLK}



TL/H/5583–29

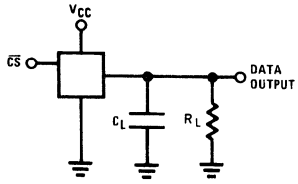
Leakage Current Test Circuit



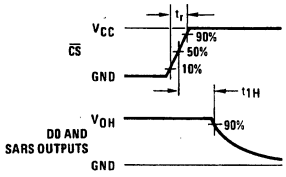
TL/H/5583–3

TRI-STATE Test Circuits and Waveforms

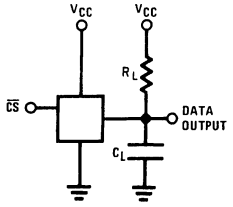
t_{1H}



t_{1H}

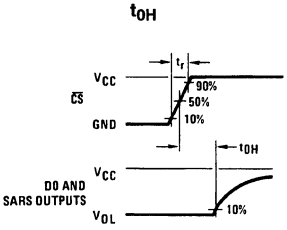


t_{0H}



TL/H/5583–4

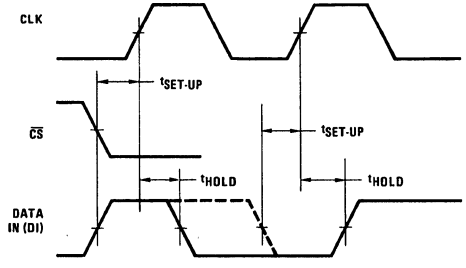
t_{0H}



TL/H/5583–23

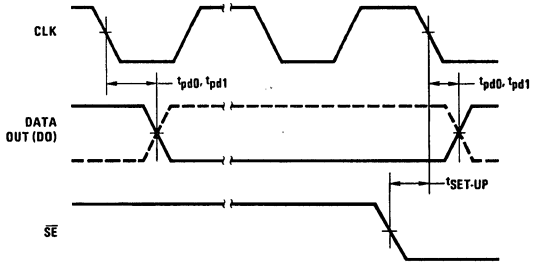
Timing Diagrams

Data Input Timing



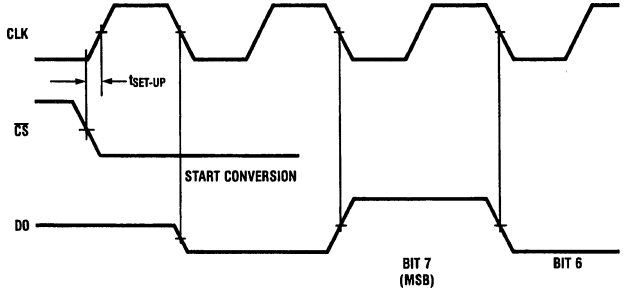
TL/H/5583–24

Data Output Timing



TL/H/5583–25

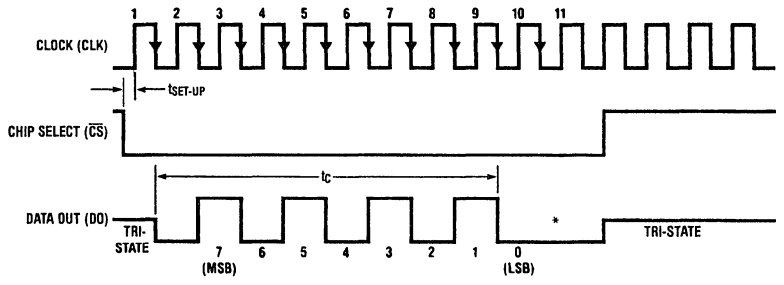
ADC0831 Start Conversion Timing



TL/H/5583–26

Timing Diagrams (Continued)

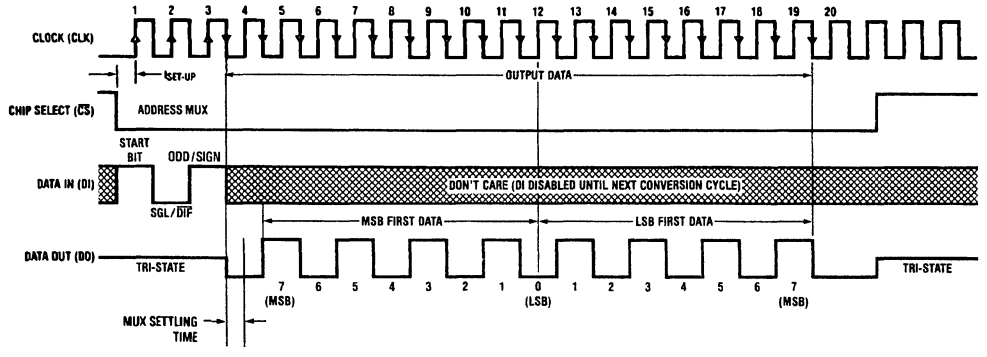
ADC0831 Timing



TL/H/5583–27

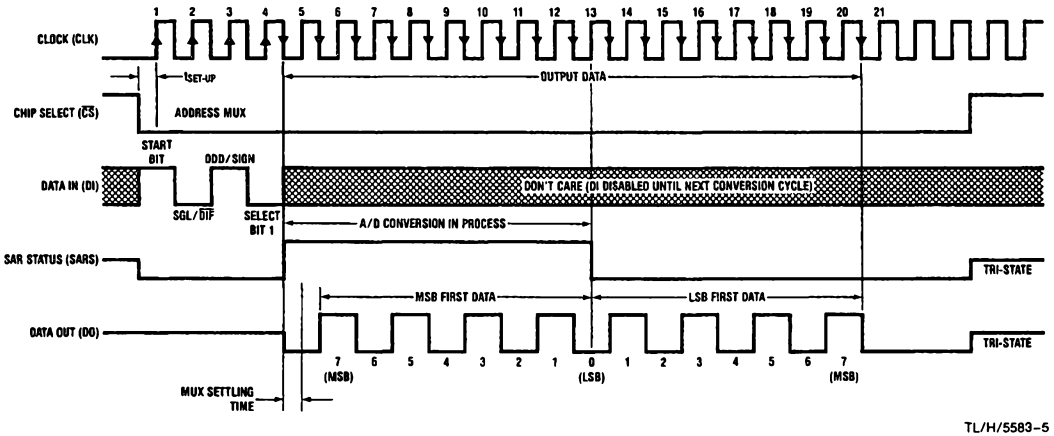
*LSB first output not available on ADC0831.

ADC0832 Timing



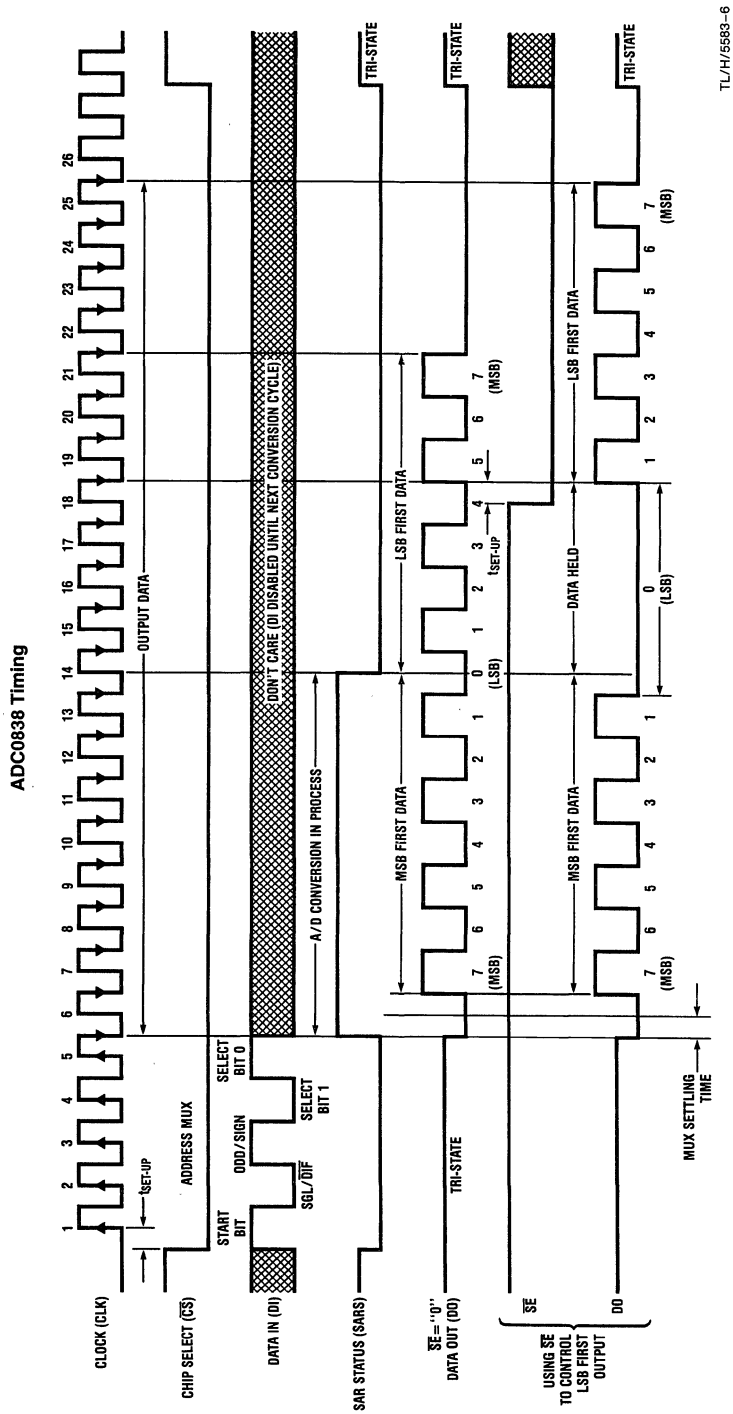
TL/H/5583–28

ADC0834 Timing



TL/H/5583–5

Timing Diagrams (Continued)

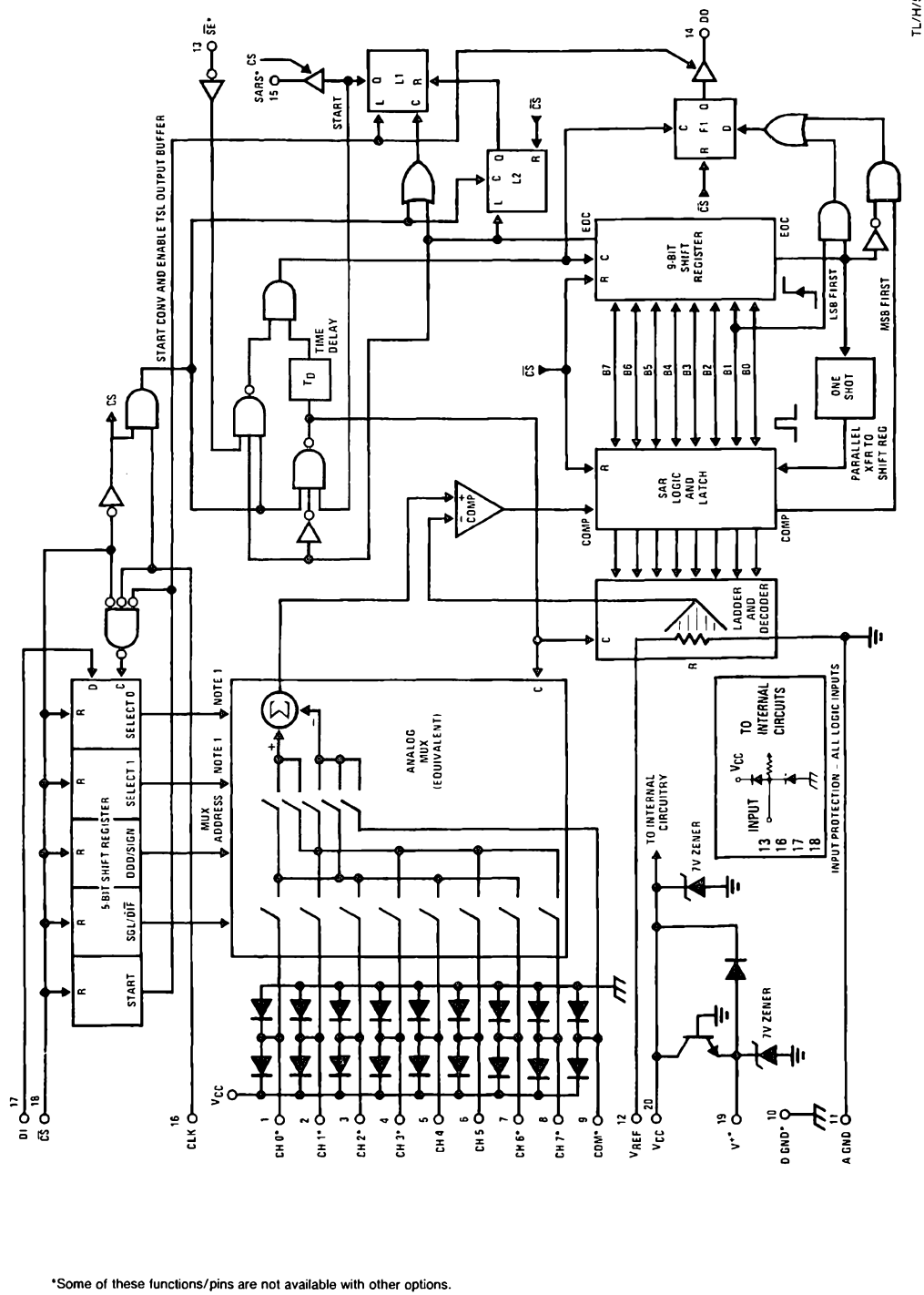


TL/H/5583–6

* Make sure clock edge #18 clocks in the LSB before $\overline{SE}$ is taken low

ADC0838 Functional Block Diagram

TL/H/5583–7



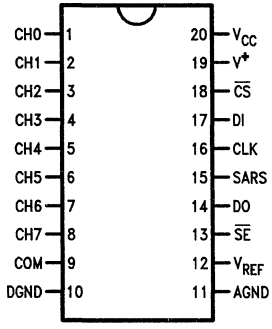
*Some of these functions/pins are not available with other options.

Note 1: For the ADC0834, DI is input directly to the D input of SELECT 1. SELECT 0 is forced to a "1". For the ADC0832, DI is input directly to the DI input of ODD/SIGN. SELECT 0 is forced to a "0" and SELECT 1 is forced to a "1".

Connection Diagrams

ADC0838 8-Channel MUX

Dual-In-Line Package

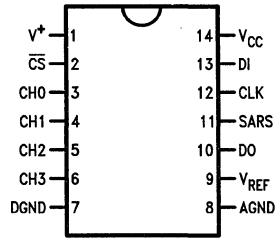


TL/H/5583–8

Top View

ADC0834 4-Channel MUX

Dual-In-Line Package



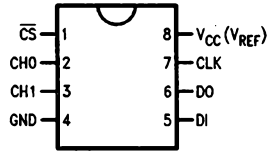
TL/H/5583–30

Top View

COM internally connected to A GND

ADC0832 2-Channel MUX

Dual-In-Line Package



TL/H/5583–31

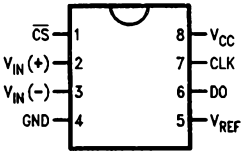
Top View

COM internally connected to GND.

V_{REF} internally connected to V_{CC}.

ADC0831 Single Differential Input

Dual-In-Line Package

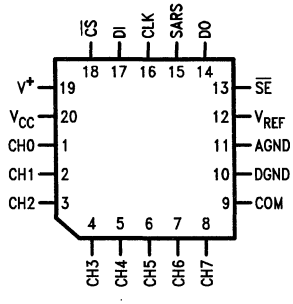


TL/H/5583–32

Top View

ADC0838 8-Channel MUX

Molded Chip Carrier (PCC) Package



TL/H/5583–33

Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of these converters utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended, differential, or a new pseudo-differential option which will convert the difference between the voltage at any analog input and a common terminal. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a different pair but channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following tables for the various product options.

The MUX address is shifted into the converter via the DI line. Because the ADC0831 contains only one differential input channel with a fixed polarity assignment, it does not require addressing.

The common input line on the ADC0838 can be used as a pseudo-differential input. In this mode, the voltage on this pin is treated as the "−" input for any of the other input channels. This voltage does not have to be analog ground; it can be any reference potential which is common to all of the inputs. This feature is most useful in single-supply application where the analog circuitry may be biased up to a potential other than ground and the output signals are all referred to this potential.

TABLE I. Multiplexer/Package Options

Part Number	Number of Analog Channels		Number of Package Pins
	Single-Ended	Differential	
ADC0831	1	1	8
ADC0832	2	1	8
ADC0834	4	2	14
ADC0838	8	4	20

Functional Description (Continued)

TABLE II. MUX Addressing: ADC0838

Single-Ended MUX Mode

MUX Address				Analog Single-Ended Channel #								
SGL/DIF	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								−
1	0	0	1			+						−
1	0	1	0					+				−
1	0	1	1							+		−
1	1	0	0		+							−
1	1	0	1				+					−
1	1	1	0						+			−
1	1	1	1								+	−

Differential MUX Mode

MUX Address				Analog Differential Channel-Pair #							
SGL/DIF	ODD/SIGN	SELECT 1	SELECT 0	0	1	2	3	4	5	6	7
0	0	0	0	+	−						
0	0	0	1			+	−				
0	0	1	0					+	−		
0	0	1	1							+	−
0	1	0	0	−	+						
0	1	0	1			−	+				
0	1	1	0					−	+		
0	1	1	1							−	+

TABLE III. MUX Addressing: ADC0834

Single-Ended MUX Mode

MUX Address			Channel #			
SGL/DIF	ODD/SIGN	SELECT 1	0	1	2	3
1	0	0	+			
1	0	1			+	
1	1	0		+		
1	1	1				+

COM is internally tied to A GND

Differential MUX Mode

MUX Address			Channel #			
SGL/DIF	ODD/SIGN	SELECT 1	0	1	2	3
0	0	0	+	−		
0	0	1			+	−
0	1	0	−	+		
0	1	1			−	+

TABLE IV. MUX Addressing: ADC0832

Single-Ended MUX Mode

MUX Address		Channel #	
SGL/DIF	ODD/SIGN	0	1
1	0	+	
1	1		+

COM is internally tied to A GND

Differential MUX Mode

MUX Address		Channel #	
SGL/DIF	ODD/SIGN	0	1
0	0	+	−
0	1	−	+

Functional Description (Continued)

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above V_{CC} (typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

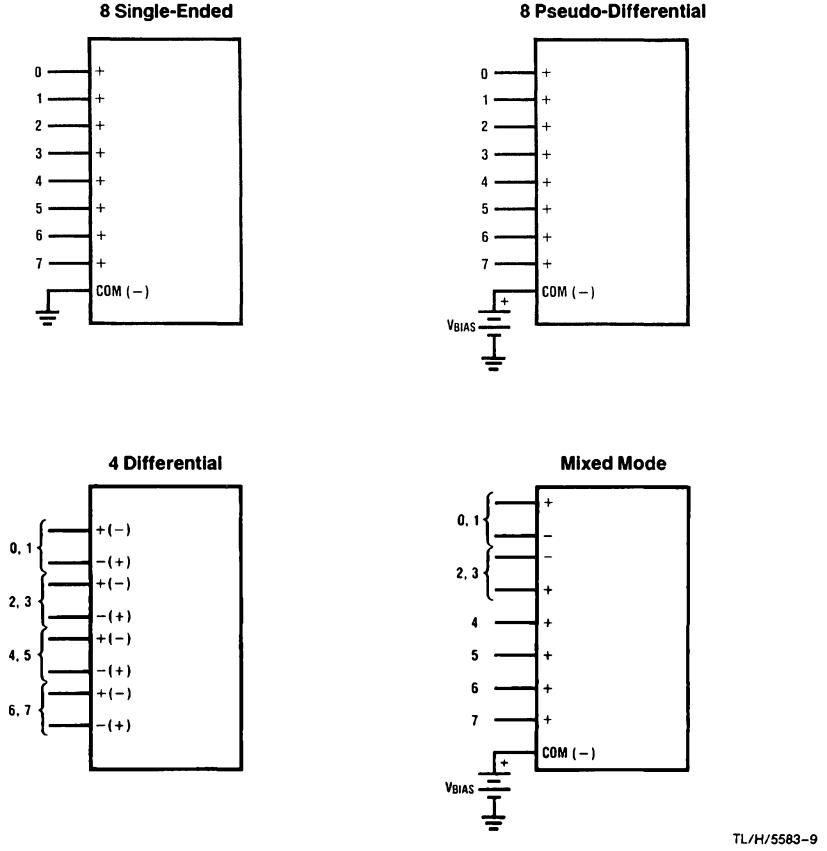
A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagrams and Functional Block Diagram and to follow a complete conversion sequence. For clarity a separate diagram is shown of each device.

1. A conversion is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic "1" that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 2 to 4 bits to be the MUX assignment word.



TL/H/5583–9

FIGURE 1. Analog Input Multiplexer Options for the ADC0838

Functional Description (Continued)

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

7. After 8 clock periods the conversion is completed. The SAR status line returns low to indicate this ½ clock cycle later.

8. If the programmer prefers, the data can be provided in an LSB first format [this makes use of the shift enable ($\overline{SE}$) control line]. All 8 bits of the result are stored in an output shift register. On devices which do not include the $\overline{SE}$ control line, the data, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high. On the ADC0838 the $\overline{SE}$ line is brought out and if held high, the value of the LSB remains valid on the DO line. When $\overline{SE}$ is forced low, the data is then clocked out LSB first. The ADC0831 is an exception in that its data is only output in MSB first format.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only "looked-at" during the MUX addressing interval while the DO line is still in a high impedance state.

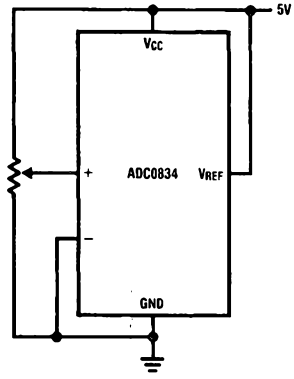
3.0 REFERENCE CONSIDERATIONS

The voltage applied to the reference input to these converters defines the voltage span of the analog input (the difference between $V_{IN(MAX)}$ and $V_{IN(MIN)}$) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the reference input resistance of typically 3.5 kΩ. This pin is the top of a resistor divider string used for the successive approximation conversion.

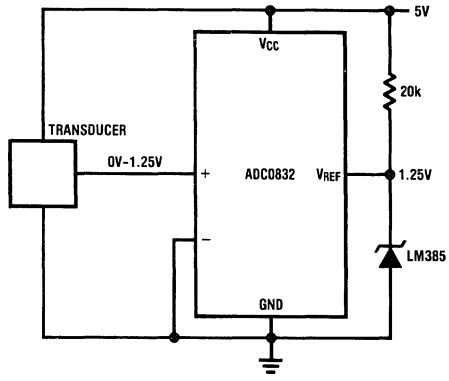
In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the V_{REF} pin can be tied to V_{CC} (done internally on the ADC0832). This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition.

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the V_{CC} supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals V_{REF}/256).



a) Ratiometric



b) Absolute with a Reduced Span

TL/H/5583–10

FIGURE 2. Reference Examples

Functional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the input be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM}) \left(\frac{0.5}{f_{CLK}} \right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK}, is the A/D clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ±1 μA over temperature will create a 1 mV input error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for V_{REF} = 5.000 V_{DC}).

5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input (or V_{CC} for the ADC0832) for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A V_{IN} (+) voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper $V_{IN}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+) \text{ fs adj} = V_{MAX} - 1.5 \left[\frac{(V_{MAX} - V_{MIN})}{256} \right]$$

where:

V_{MAX} = the high end of the analog input range

and

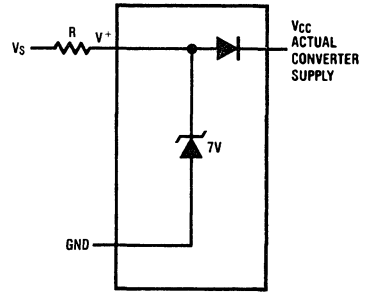
V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The V_{REF} (or V_{CC}) voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

6.0 POWER SUPPLY

A unique feature of the ADC0838 and ADC0834 is the inclusion of a zener diode connected from the V^+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in *Figure 3.* (See Note 3)



TL/H/5583–11

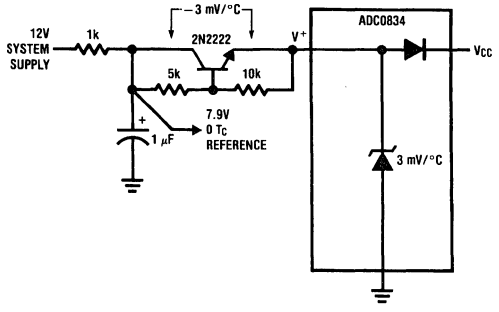
FIGURE 3. An On-Chip Shunt Regulator Diode

Functional Description (Continued)

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. *Figures 4 and 5* illustrate two useful applications of this on-board zener when an external transistor can be afforded.

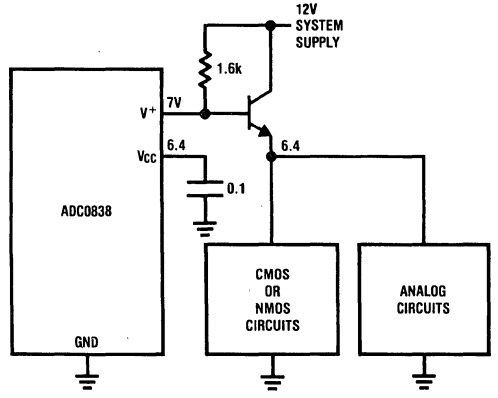
An important use of the interconnecting diode between V^+ and V_{CC} is shown in *Figures 6 and 7*. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The low current requirements of the A/D and the relatively high clock frequencies used (typically in the range of 10k–400 kHz) allows using the small value filter capacitor shown to keep the ripple on the V_{CC} line to well under 1/4 of an LSB. The shunt zener regulator can also be used in this mode. This requires a clock voltage swing which is in excess of V_Z. A current limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V^+ pin.

Applications



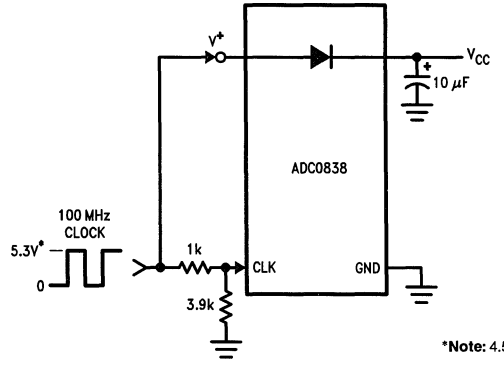
TL/H/5583–12

FIGURE 4. Operating with a Temperature Compensated Reference



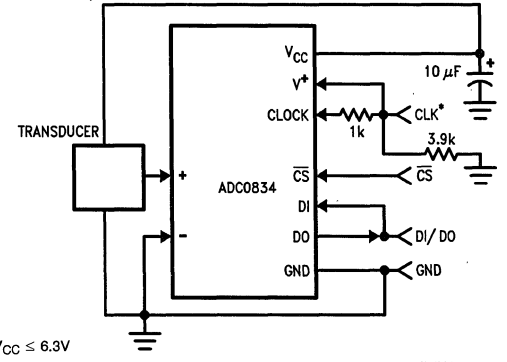
TL/H/5583–34

FIGURE 5. Using the A/D as the System Supply Regulator



TL/H/5583–35

FIGURE 6. Generating V_{CC} from the Converter Clock



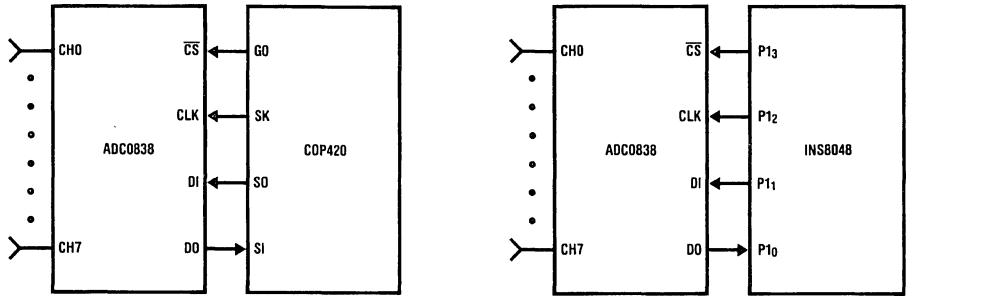
*Note: $4.5V \leq V_{CC} \leq 6.3V$

TL/H/5583–36

FIGURE 7. Remote Sensing—Clock and Power on 1 Wire

Applications (Continued)

Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048



TL/H/5583–13

COP CODING EXAMPLE

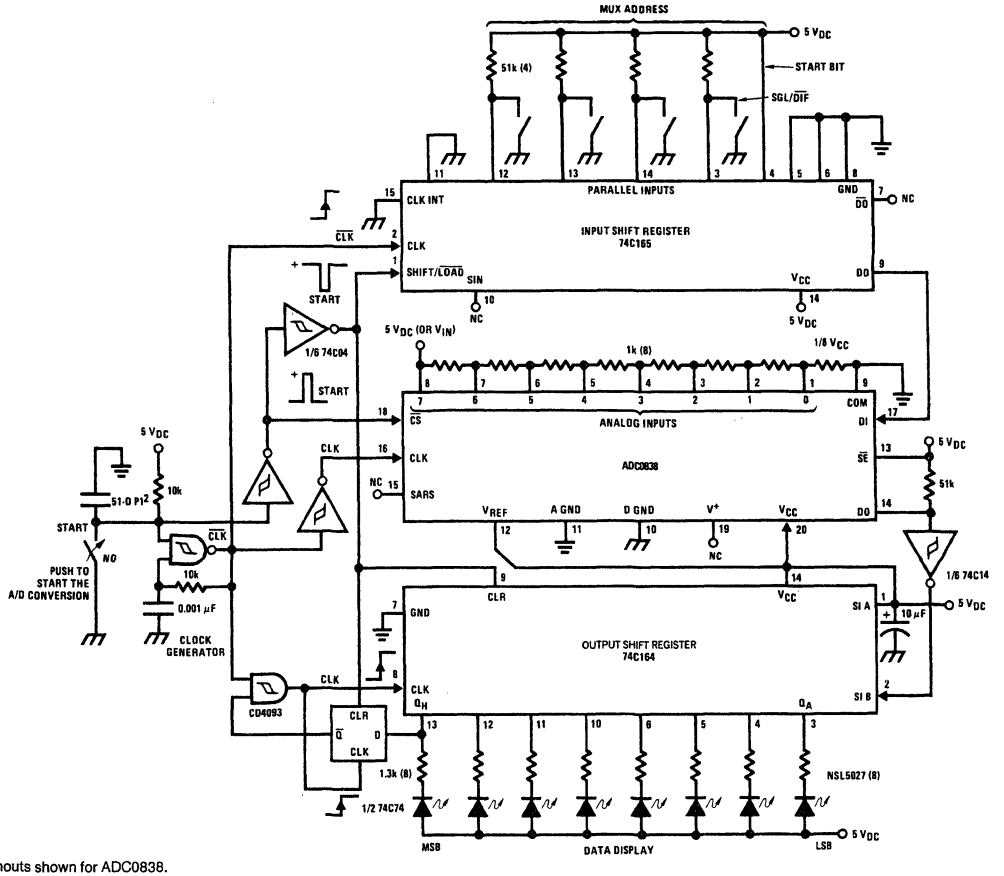
Mnemonic	Instruction
LEI	ENABLES SIO's INPUT AND OUTPUT
SC	C = 1
OGI	G0 = 0 ($\overline{CS}$ = 0)
CLR A	CLEARS ACCUMULATOR
AISC 1	LOADS ACCUMULATOR WITH 1
XAS	EXCHANGES SIO WITH ACCUMULATOR AND STARTS SK CLOCK
LDD	LOADS MUX ADDRESS FROM RAM INTO ACCUMULATOR
NOP	—
XAS	LOADS MUX ADDRESS FROM ACCUMULATOR TO SIO REGISTER
↑	
8 INSTRUCTIONS	
↓	
XAS	READS HIGH ORDER NIBBLE (4 BITS) INTO ACCUMULATOR
XIS	PUTS HIGH ORDER NIBBLE INTO RAM
CLR A	CLEARS ACCUMULATOR
RC	C = 0
XAS	READS LOW ORDER NIBBLE INTO ACCUMULATOR AND STOPS SK
XIS	PUTS LOW ORDER NIBBLE INTO RAM
OGI	G0 = 1 ($\overline{CS}$ = 1)
LEI	DISABLES SIO's INPUT AND OUTPUT

8048 CODING EXAMPLE

Mnemonic			Instruction
START:	ANL	P1, #0F7H	;SELECT A/D ($\overline{CS}$ = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX ADDRESS
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT
			;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	JMP	CONT	;CONTINUE
			;BIT = 1
ONE:	ORL	P1, #1	;DI ← 1
CONT:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	CALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	IN	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETR			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

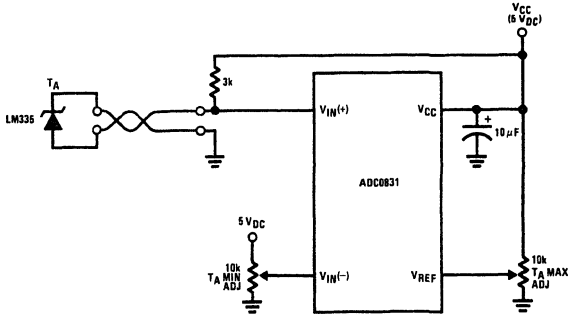
Applications (Continued)

A "Stand-Alone" Hook-Up for ADC0838 Evaluation



*Pinouts shown for ADC0838.
For all other products tie to pin functions as shown.

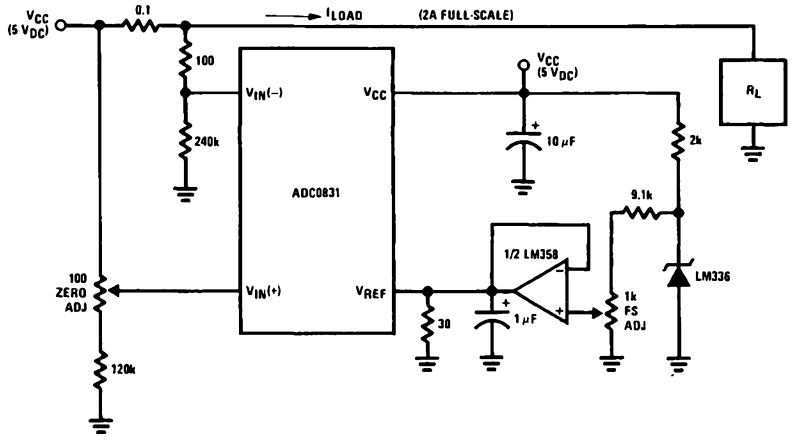
Low-Cost Remote Temperature Sensor



TL/H/5583–14

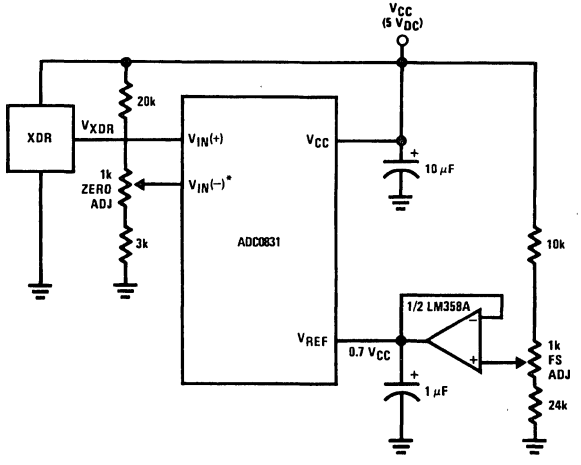
Applications (Continued)

Digitizing a Current Flow



TL/H/5583–15

Operating with Ratiometric Transducers

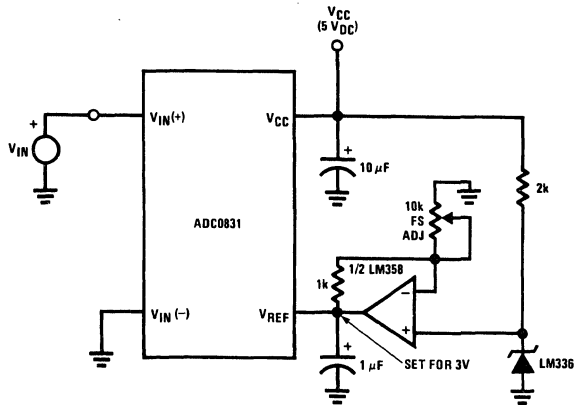


TL/H/5583–37

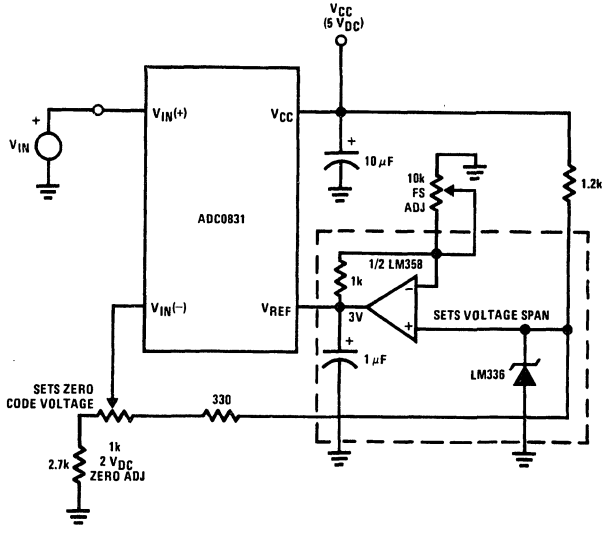
*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

Applications (Continued)

Span Adjust: $0V \leq V_{IN} \leq 3V$



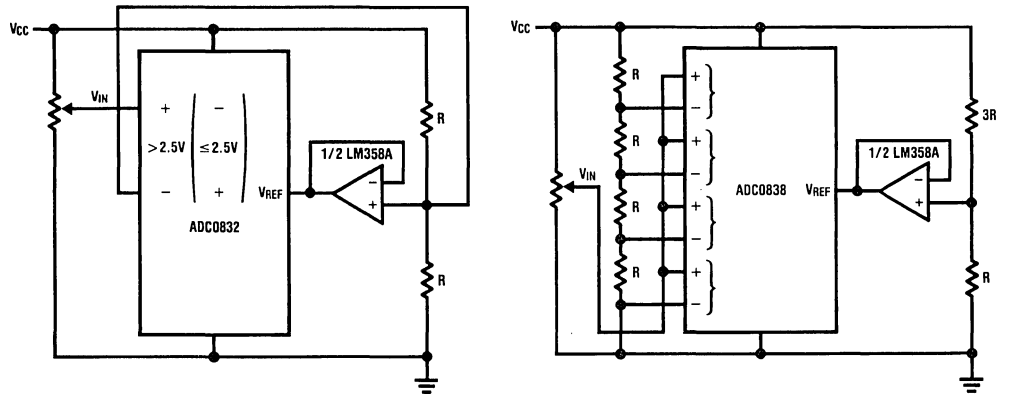
Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



TL/H/5583–16

Applications (Continued)

Obtaining Higher Resolution

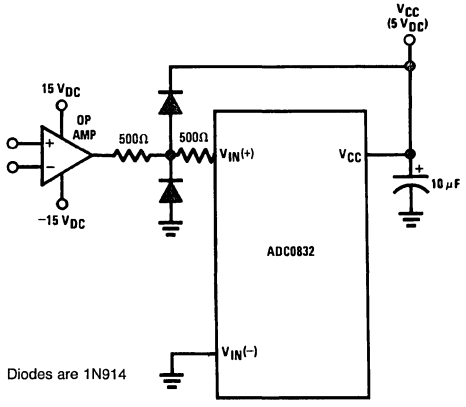


TL/H/5583–17

Controller performs a routine to determine which input polarity (9-bit example) or which channel pair (10-bit example) provides a non-zero output code. This information provides the extra bits.

a) 9-Bit A/D **b)10-Bit A/D**

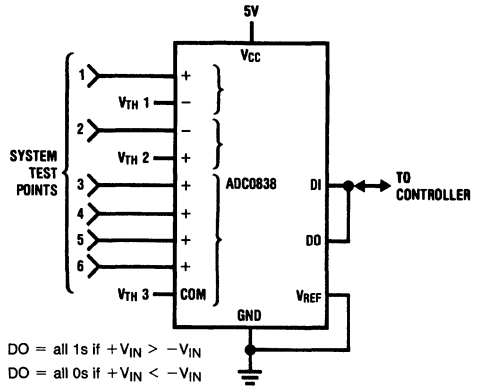
Protecting the Input



TL/H/5583–18

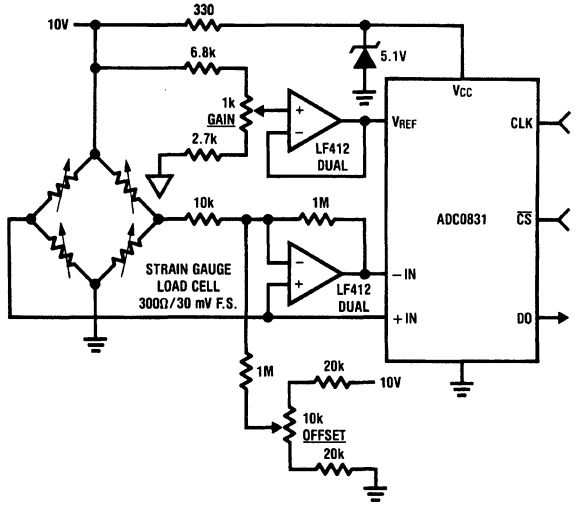
Applications (Continued)

High Accuracy Comparators



TL/H/5583–38

Digital Load Cell

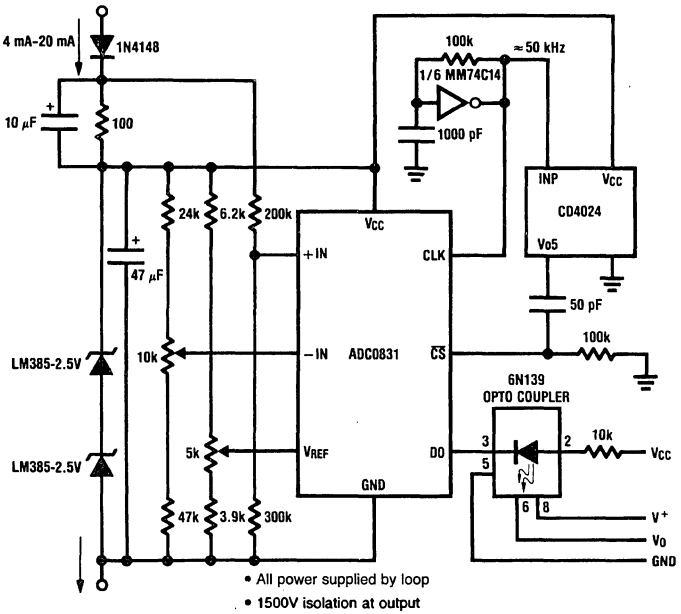


TL/H/5583–19

- Uses one more wire than load cell itself
- Two mini-DIPs could be mounted inside load cell for digital output transducer
- Electronic offset and gain trims relax mechanical specs for gauge factor and offset
- Low level cell output is converted immediately for high noise immunity

Applications (Continued)

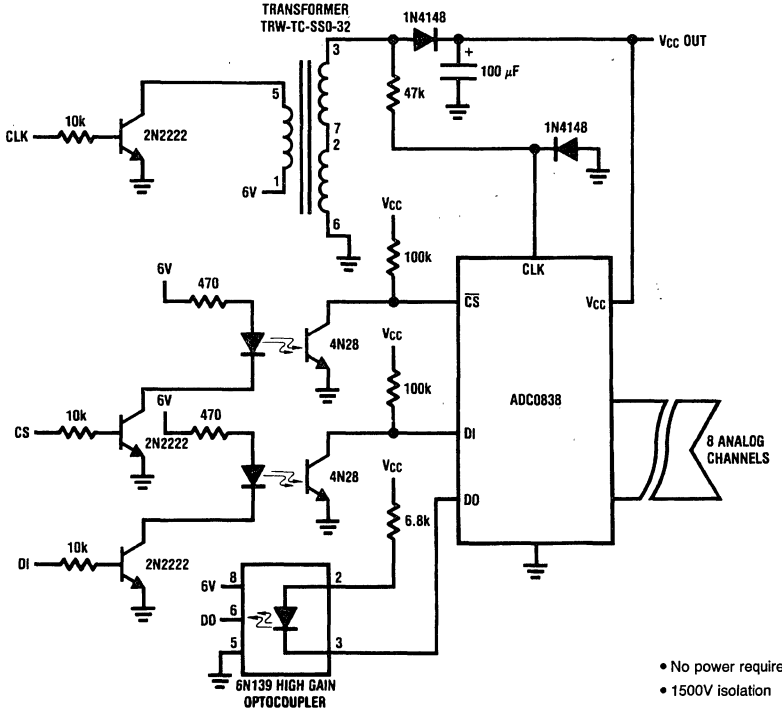
4 mA–20 mA Current Loop Converter



- All power supplied by loop
- 1500V isolation at output

TL/H/5583–20

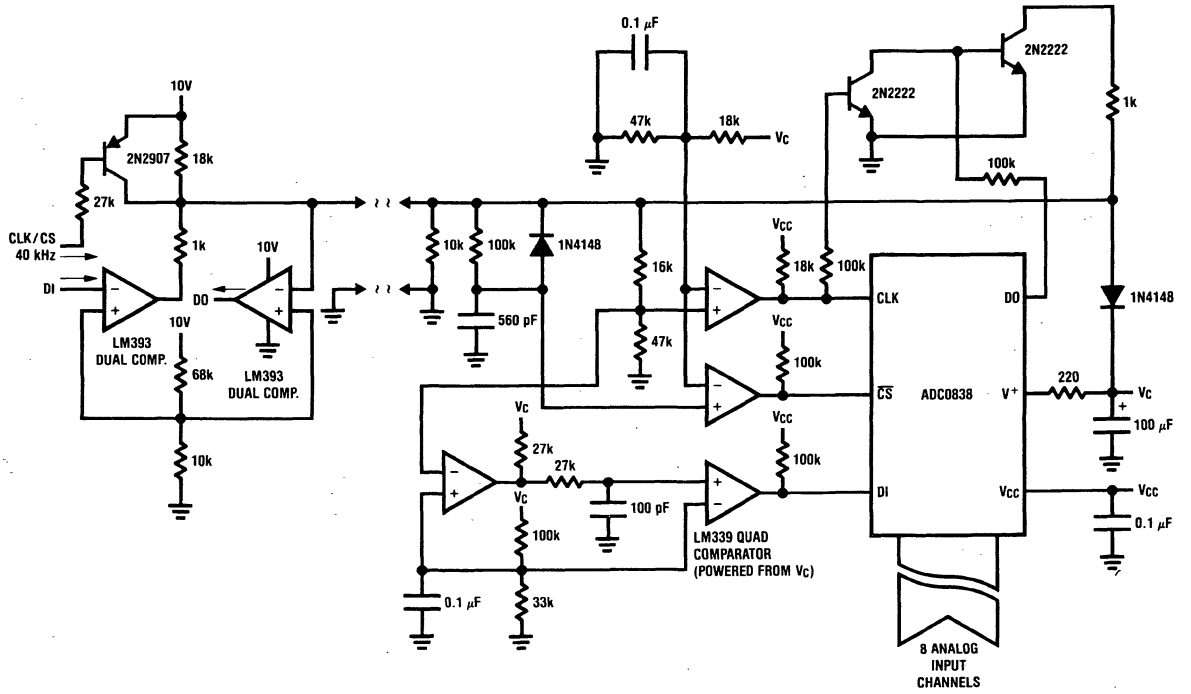
Isolated Data Converter



- No power required remotely
- 1500V isolation

TL/H/5583–39

Two Wire Interface for 8 Channels

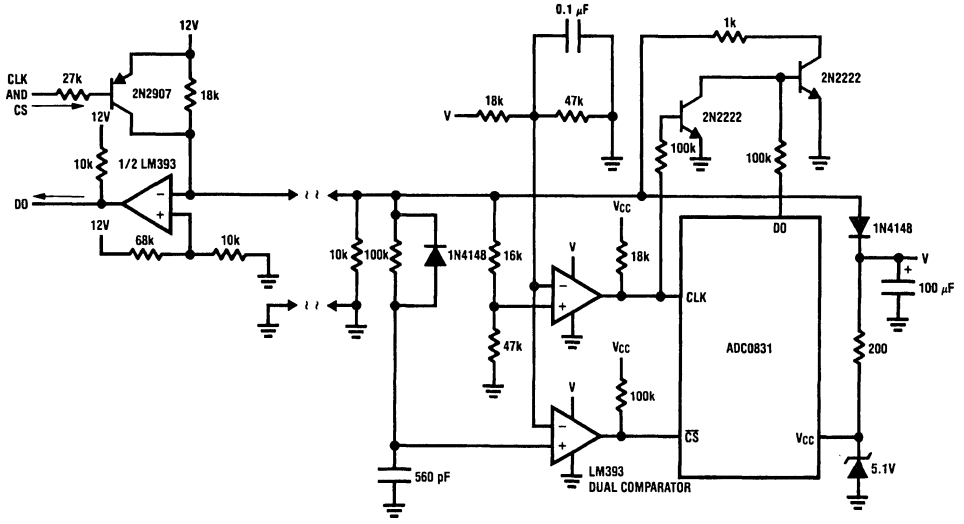


- No additional connections
- $\overline{CS}$ derived from extended high on CLK line > 100 μs
- Timing arranged for 40 kHz, could be changed up or down by component change
- 10% CLK frequency change without component change OK

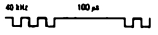
TL/H/5583–21

Applications (Continued)

Two Wire 1-Channel Interface



- Simpler version of 8-channel
- $\overline{CS}$ derived from long CLK pulse



TL/H/5583–22

Ordering Information

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0831BJ	1	±½	Hermetic (J)	−55°C to +125°C
ADC0831BCJ			Hermetic (J)	−40°C to +85°C
ADC0831BCN			Molded (N)	0°C to +70°C
ADC0831CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0831CCN			Molded (N)	0°C to +70°C
ADC0832BJ	2	±½	Hermetic (J)	−55°C to +125°C
ADC0832BCJ			Hermetic (J)	−40°C to +85°C
ADC0832BCN			Molded (N)	0°C to +70°C
ADC0832CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0832CCN			Molded (N)	0°C to +70°C
ADC0834BJ	4	±½	Hermetic (J)	−55°C to +125°C
ADC0834BCJ			Hermetic (J)	−40°C to +85°C
ADC0834BCN			Molded (N)	0°C to +70°C
ADC0834CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0834CCN			Molded (N)	0°C to +70°C
ADC0838BJ	8	±½	Hermetic (J)	−55°C to +125°C
ADC0838BCJ			Hermetic (J)	−40°C to +85°C
ADC0838BCV			PCC (V)	0°C to +70°C
ADC0838BCN			Molded (N)	0°C to +70°C
ADC0838CCJ		±1	Hermetic (J)	−40°C to +85°C
ADC0838CCV			PCC (V)	0°C to +70°C
ADC0838CCN			Molded (N)	0°C to +70°C

See NS Package Number J08A, J14A, J20A, N08E, N14A, N20A or V20A