ADC0833

ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer

Literature Number: SNAS533A

National Semiconductor

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ADC0833 8-Bit Serial I/O A/D Converter with 4-Channel Multiplexer

General Description

The ADC0833 series is an 8-bit successive approximation A/D converter with a serial I/O and configurable input multiplexer with 4 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, as well as with standard shift registers or μPs.

The 4-channel multiplexer is software configured for single-ended or differential inputs when channel assigned by a 4-bit serial word.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Key Specifications

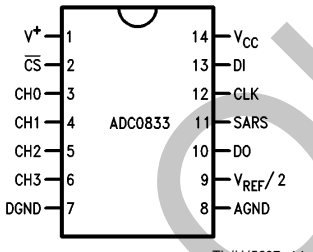
- Resolution — 8 Bits
- Total Unadjusted Error — ± ½ LSB and ± 1 LSB
- Single Supply — 5 V_{DC}
- Low Power — 23 mW
- Conversion Time — 32 μs

Features

- NSC MICROWIRE compatible–direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand alone"
- Works with 2.5V (LM336) voltage reference
- No full-scale or zero adjust required
- Differential analog voltage inputs
- 4-channel analog multiplexer
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- TTL/MOS input/output compatible
- 0.3″ standard width 14-pin DIP package

Connection and Functional Diagrams

Dual-In-Line Package (J and N)



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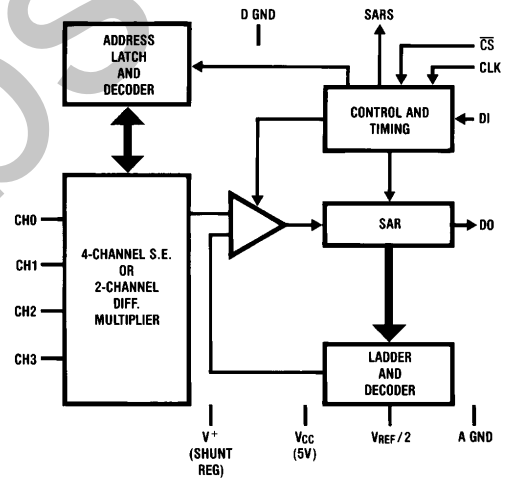
Top View

Order Number ADC0833CCJ, ADC0833BCN or ADC0833CCN
See NS Package Number J14A or N14A



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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Current into V+ (Note 3)	15 mA
Supply Voltage, V_{CC} (Note 3)	6.5V
Voltage	
Logic Inputs	−0.3V to V_{CC} + 0.3V
Analog Inputs	−0.3V to V_{CC} + 0.3V
Input Current per Pin (Note 4)	±5 mA
Package Input Current (Note 4)	±20 mA
Storage Temperature	−65°C to + 150°C
Package Dissipation at T_A = 25°C (Board Mount)	0.8W
Lead Temperature (Soldering, 10 sec.)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
ESD Susceptibility (Note 5)	2000V

Operating Conditions (Notes 1 & 2)

Supply Voltage, V_{CC}	4.5 V_{DC} to 6.3 V_{DC}
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0833CCJ	$-40°C \le T_A \le 85°C$
ADC0833BCN, ADC0833CCN	$0°C \le T_A \le 70°C$

Electrical Characteristics

The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz and $V_{REF}/2 \le (V_{CC} + 0.1V)$ unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_j = 25°C$.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS					
Total Unadjusted Error	$V_{REF}/2$ Forced to 2.500 V_{DC}				
ADC0833BCN			±½	**±½**	LSB
ADC0833CCN			±1	**±1**	LSB
ADC0833CCJ			**±1**		LSB
Minimum Total Ladder Resistance (Note 9)					
ADC0833CCJ		7.0	**2.6**		kΩ
ADC0833BCN/CCN		7.0	2.6	**2.6**	kΩ
Maximum Total Ladder Resistance (Note 9)					
ADC0833CCJ		7.0	**11.8**		kΩ
ADC0833BCN/CCN		7.0	10.8	**11.8**	kΩ
Minimum Common-Mode Input Range (Note 10)	All MUX Inputs and COM Input				
ADC0833CCJ			**GND−0.05**		V
ADC0833BCN/CCN			GND−0.05	**GND−0.05**	V
Maximum Common-Mode Input Range (Note 10)	All MUX Inputs and COM Input				
ADC0833CCJ			**V_{CC}+0.05**		V
ADC0833BCN/CCN			V_{CC}+0.05	**V_{CC}+0.05**	V
DC Common-Mode Error					
ADC0833CCJ		±1/16	**±¼**		LSB
ADC0833BCN/CCN		±1/16	±¼	**±¼**	LSB
Change In Zero Error From V_{CC} = 5V To Internal Zener Operation (Note 3)	15mA Into V+ V_{CC} = N.C. $V_{REF}/2$ = 2.500V				
ADC0833CCJ			**1**		LSB
ADC0833BCN/CCN			1	**1**	LSB

Electrical Characteristics The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz and $V_{REF}/2 \leq (V_{CC} + 0.1V)$ unless otherwise specified. **Boldface limits apply from t_{MIN} to t_{MAX};** all other limits $T_A = T_j = 25°C$. (Continued)

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
CONVERTER AND MULTIPLEXER CHARACTERISTICS (Continued)					
V_Z, Minimum Internal Diode Breakdown (At V+) (Note 3)	15mA Into V+				
ADC0833CCJ			**6.3**		V
ADC0833BCN/CCN			6.3	**6.3**	V
V_Z, Maximum Internal Diode Breakdown (At V+) (Note 3)	15mA Into V+				
ADC0833CCJ			**8.5**		V
ADC0833BCN/CCN			8.5	**8.5**	V
Power Supply Sensitivity	$V_{CC} = 5V \pm 5\%$				
ADC0833CCJ		$\pm 1/16$	$\pm$ **¼**		LSB
ADC0833BCN/CCN		$\pm 1/16$	$\pm ¼$	$\pm$ **¼**	LSB
I_{OFF}, Off Channel Leakage Current (Note 11)	On Channel = 5V, Off Channel = 0V				
ADC0833CCJ			**−1**		μA
			−200		nA
ADC0833BCN/CCN				**−1**	μA
			−200		nA
	On Channel = 0V, Off Channel = 5V				
ADC0833CCJ			**1**		μA
			200		nA
ADC0833BCN/CCN				**1**	μA
			200		nA
I_{ON}, On Channel Leakage Current (Note 11)	On Channel = 5V, Off Channel = 0V				
ADC083CCJ			**1**		μA
			200		nA
ADC0833BCN/CCN				**1**	μA
			200		nA
	On Channel = 0V, Off Channel = 5V				
ADC083CCJ			**−1**		μA
			−200		nA
ADC0833BCN/CCN				**−1**	μA
			−200		nA
DIGITAL AND DC CHARACTERISTICS					
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC} = 5.25V$				
ADC0833CCJ			**2.0**		V
ADC0833BCN/CCN			2.0	**2.0**	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC} = 4.75V$				
ADC0833CCJ			**0.8**		V
ADC0833BCN/CCN			0.8	**0.8**	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN} = V_{CC}$				
ADC0833CCJ		0.005	**1**		μA
ADC0833BCN/CCN		0.005	1	**1**	μA

Electrical Characteristics The following specifications apply for $V_{CC} = V^+ = 5V$, $f_{CLK} = 250$ kHz and $V_{REF}/2 \leq (V_{CC} + 0.1V)$ unless otherwise specified. **Boldface limits apply from t_{MIN} to t_{MAX};** all other limits $T_A = T_j = 25°C$. (Continued)

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
DIGITAL AND DC CHARACTERISTICS (Continued)					
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN} = 0V$				
ADC0833CCJ		−0.005	**−1**		μA
ADC0833BCN/CCN		−0.005	−1	**−1**	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC} = 4.75V$				
ADC0833CCJ	$I_{OUT} = -360\mu A$		**2.4**		V
ADC0833BCN/CCN			2.4	**2.4**	V
ADC0833CCJ	$I_{OUT} = -10\mu A$		**4.5**		V
ADC0833BCN/CCN			4.5	**4.5**	V
$V_{OUT(0)}$, Logical "0" Output Voltage	$I_{OUT} = 1.6mA$, $V_{CC} = 4.75V$				
ADC0833CCJ			**0.4**		V
ADC0833BCN/CCN			0.4	**0.4**	V
I_{OUT}, TRI-STATE Output Current (DO, SARS)					
ADC0833CCJ	$V_{OUT} = 0.4V$	−0.1	**−3**		μA
ADC0833BCN/CCN		−0.1	−3	**−3**	μA
ADC0833CCJ	$V_{OUT} = 5V$	0.1	**3**		μA
ADC0833BCN/CCN		0.1	3	**3**	μA
I_{SOURCE}	V_{OUT} Short to GND				
ADC0833CCJ		−14	**−6.5**		mA
ADC0833BCN/CCN		−14	−7.5	**−6.5**	mA
I_{SINK}	V_{OUT} Short to V_{CC}				
ADC0833CCJ		16	**8.0**		mA
ADC0833BCN/CCN		16	9.0	**8.0**	mA
I_{CC}, Supply Current (Note 3)	$V_{REF}/2$ Open Circuit				
ADC0833CCJ		0.9	**4.5**		mA
ADC0833BCN/CCN		0.9	4.5	**4.5**	mA

AC Electrical Characteristics

The following specifications apply for $V_{CC} = V^+ = 5V$ and $t_r = t_f = 20$ ns unless otherwise specified. These limits apply for $T_A = T_j = 25°C$.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
f_{CLK}, Clock Frequency Min Max			10	 400	kHz kHz
T_C, Conversion Time	Not including MUX Addressing Time		8		$1/f_{CLK}$
Clock Duty Cycle (Note 12) Min Max				40 60	% %
t_{SET-UP}, $\overline{CS}$ Falling Edge or Data Input Valid to CLK Rising Edge				250	ns
t_{HOLD}, Data Input Valid after CLK Rising Edge				90	ns
t_{pd1}, t_{pd0}—CLK Falling Edge to Output Data Valid (Note 13)	$C_L = 100$ pF Data MSB First Data LSB First	 650 250		 1500 600	 ns ns
t_{1H}, t_{OH}—Rising Edge of $\overline{CS}$ to Data Output and SARS Hi-Z	$C_L = 10$ pF, $R_L = 10k$ $C_L = 100$ pF, $R_L = 2k$ (see TRI-STATE Test Circuits)	125	 500	250	ns ns
C_{IN}, Capacitance of Logic Input		5			pF
C_{OUT}, Capacitance of Logic Outputs		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the ground pins.

Note 3: Internal zener diodes (approx. 7V) are connected from V^+ to GND and V_{CC} to GND. The zener at V^+ can operate as a shunt regulator and is connected to V_{CC} via a conventional diode. Since the zener voltage equals the A/D's breakdown voltage, the diode insures that V_{CC} will be below breakdown when the device is powered from V^+. Functionality is therefore guaranteed for V^+ operation even though the resultant voltage at V_{CC} may exceed the specified Absolute Max. of 6.5V. It is recommended that a resistor be used to limit the max. current into V^+.

Note 4: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 9: See Applications, section 3.0.

Note 10: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} or V_{REF} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

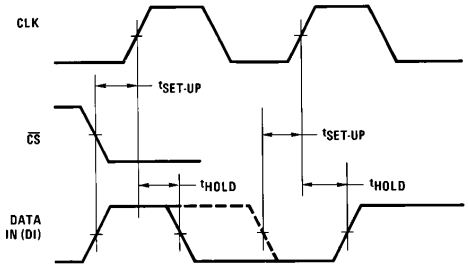
Note 11: Leakage current is measured with the clock not switching.

Note 12: A 40% to 60% clock duty cycle range insures proper operation at all clock frequencies. In the case that an available clock has a duty cycle outside of these limits, the minimum time the clock is high or the minimum time the clock is low must be at least 1 μs. The maximum time the clock can be high is 60 μs. The clocked can be stopped when low so long as the analog input voltage remains stable.

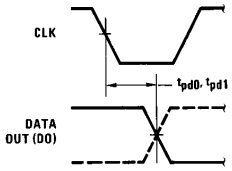
Note 13: Since data, MSB first, is the output of the comparator used in the successive approximation loop, an additional delay is built in (see Block Diagram) to allow for comparator response time.

Timing Diagrams

Data Input Timing

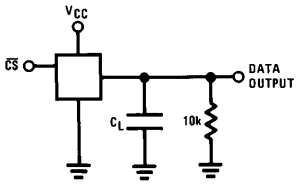


Data Output Timing

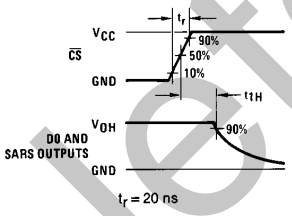


TRI-STATE Test Circuits and Waveforms

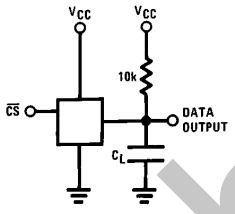
t_{1H}



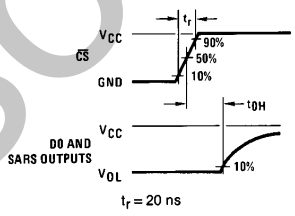
t_{1H}, C_L = 10 pF



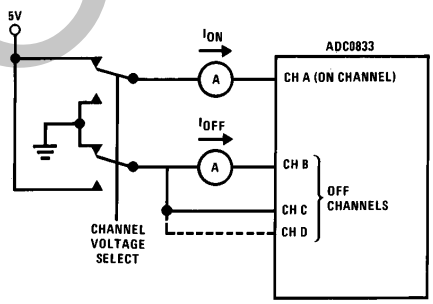
t_{0H}



t_{0H}, C_L = 10 pF



Leakage Current Test Circuit



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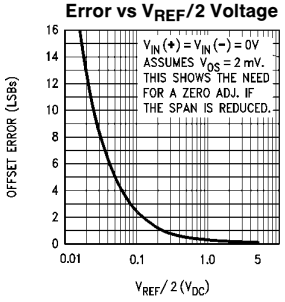
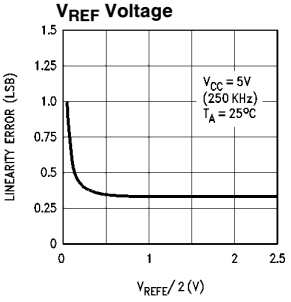
Typical Performance Characteristics

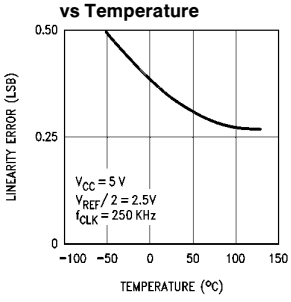
Effect of Unadjusted Offset Error vs $V_{REF}/2$ Voltage



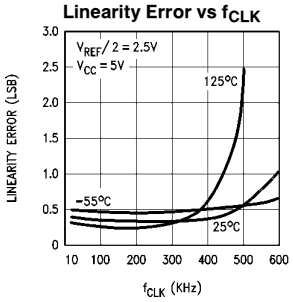
Linearity Error vs V_{REF} Voltage



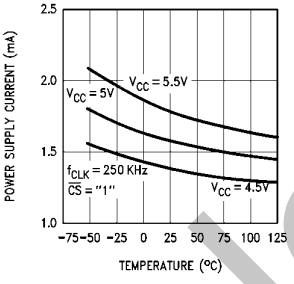
Linearity Error vs Temperature



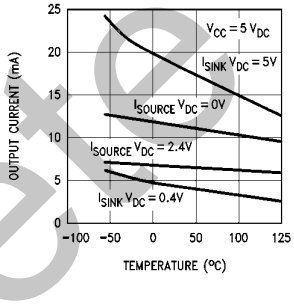
Linearity Error vs f_{CLK}



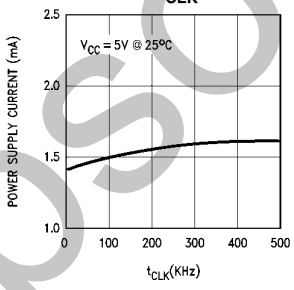
Power Supply Current vs Temperature



Output Current vs Temperature



Power Supply Current vs f_{CLK}



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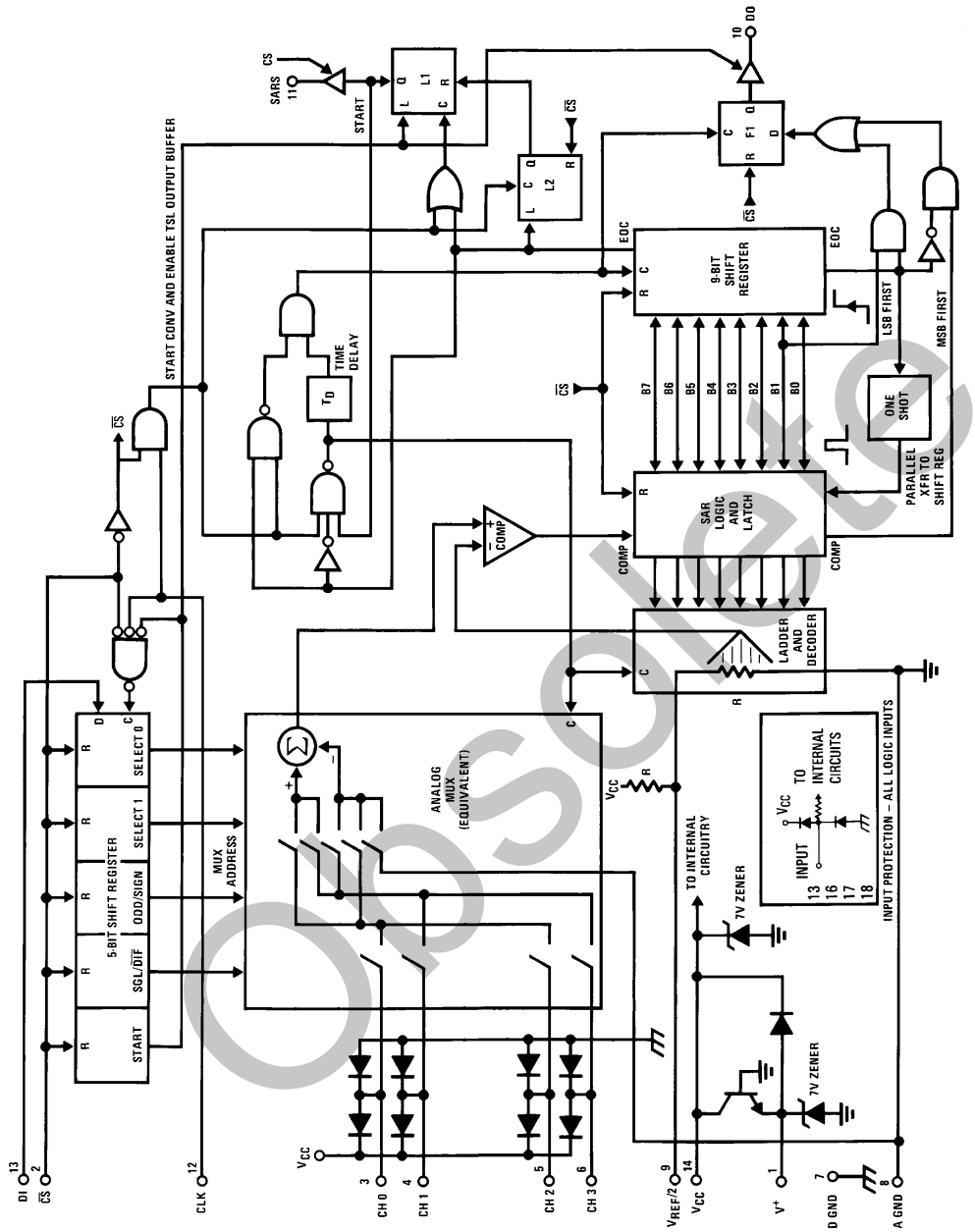
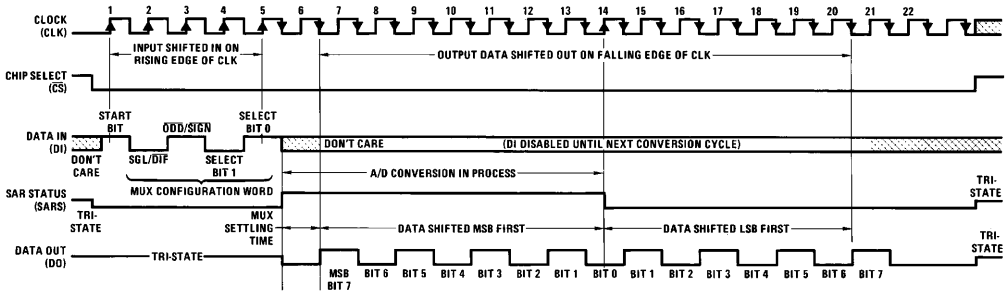
ADC0833 Functional Block Diagram



Timing Diagram



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Functional Description

1.0 MULTIPLEXER ADDRESSING

The design of the ADC0833 utilizes a sample-data comparator structure which provides for a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned "+" input terminal and a "−" input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned "+" input is less than the "−" input the converter responds with an all zeros output code.

A unique input multiplexing scheme has been utilized to provide multiple analog channels with software-configurable single-ended (ground referred) or differential inputs. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs.

A particular input configuration is assigned during the MUX addressing sequence, prior to the start of a conversion. The MUX address selects which of the analog inputs are to be enabled and whether this input is single-ended or differential. In the differential case, it also assigns the polarity of the channels. Differential inputs are restricted to adjacent channel pairs. For example channel 0 and channel 1 may be selected as a differential pair. Channel 0 or 1 cannot act differentially with any other channel. In addition to selecting differential mode the sign may also be selected. Channel 0 may be selected as the positive input and channel 1 as the negative input or vice versa. This programmability is best illustrated by the MUX addressing codes shown in the following table. The MUX address is shifted into the converter through the DI line.

TABLE I. MUX Addressing

Single-Ended MUX Mode

Address				Channel #			
SGL/ $\overline{\text{DIF}}$	$\overline{\text{ODD}}$/ $\overline{\text{SIGN}}$	SELECT		0	1	2	3
		1	0				
1	0	0	1	+			
1	0	1	1			+	
1	1	0	1		+		
1	1	1	1				+

COM is internally ties to a GND

Differential MUX Mode

Address				Channel #			
SGL/ $\overline{\text{DIF}}$	$\overline{\text{ODD}}$/ $\overline{\text{SIGN}}$	SELECT		0	1	2	3
		1	0				
0	0	0	1	+	−		
0	0	1	1			+	−
0	1	0	1	−	+		
0	1	1	1			−	+

Functional Description (Continued)

Since the input configuration is under software control, it can be modified, as required, at each conversion. A channel can be treated as a single-ended, ground referenced input for one conversion; then it can be reconfigured as part of a differential channel for another conversion. *Figure 1* illustrates the input flexibility which can be achieved.

The analog input voltages for each channel can range from 50 mV below ground to 50mV above V_{CC}(typically 5V) without degrading conversion accuracy.

2.0 THE DIGITAL INTERFACE

A most important characteristic of these converters is their serial data link with the controlling processor. Using a serial communication format offers two very significant system improvements; it allows more function to be included in the converter package with no increase in package size and it can eliminate the transmission of low level analog signals by locating the converter right at the analog sensor; transmitting highly noise immune digital data back to the host processor.

To understand the operation of these converters it is best to refer to the Timing Diagram and Functional Block Diagram and to follow a complete conversion sequence.

1. A conversion is initiated by first pulling the $\overline{CS}$ (chip select) line low. This line must be held low for the entire conversion. The converter is now waiting for a start bit and its MUX assignment word.

2. A clock is then generated by the processor (if not provided continuously) and output to the A/D clock input.

3. On each rising edge of the clock the status of the data in (DI) line is clocked into the MUX address shift register. The start bit is the first logic ''1'' that appears on this line (all leading zeros are ignored). Following the start bit the converter expects the next 4 bits to be the MUX assignment word.

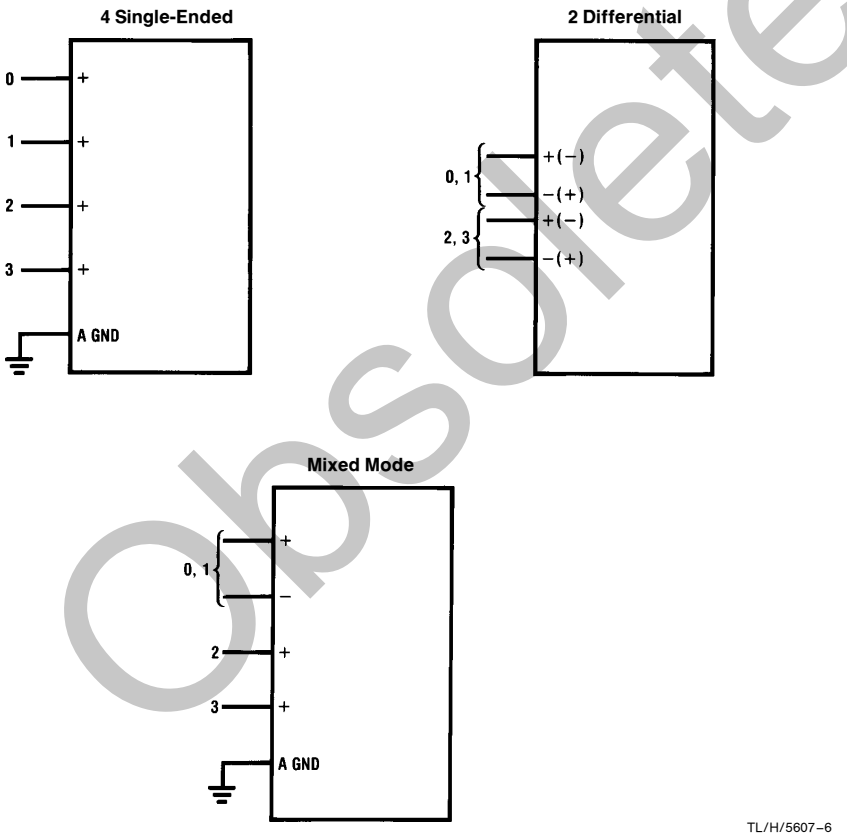


FIGURE 1. Analog Input Multiplexer Options for the ADC0833

Functional Description (Continued)

4. When the start bit has been shifted into the start location of the MUX register, the input channel has been assigned and a conversion is about to begin. An interval of ½ clock period (where nothing happens) is automatically inserted to allow the selected MUX channel to settle. The SAR status line goes high at this time to signal that a conversion is now in progress and the DI line is disabled (it no longer accepts data).

5. The data out (DO) line now comes out of TRI-STATE and provides a leading zero for this one clock period of MUX settling time.

6. When the conversion begins, the output of the SAR comparator, which indicates whether the analog input is greater than (high) or less than (low) each successive voltage from the internal resistor ladder, appears at the DO line on each falling edge of the clock. This data is the result of the conversion being shifted out (with the MSB coming first) and can be read by the processor immediately.

7. After 8 clock periods the conversion is completed. The SAR status line returns low to indicate this ½ clock cycle later.

8. If the programmer prefers, the data can be read in an LSB first format. All 8 bits of the result are stored in an output shift register. The conversion result, LSB first, is automatically shifted out the DO line, after the MSB first data stream. The DO line then goes low and stays low until $\overline{CS}$ is returned high.

9. All internal registers are cleared when the $\overline{CS}$ line is high. If another conversion is desired, $\overline{CS}$ must make a high to low transition followed by address information.

The DI and DO lines can be tied together and controlled through a bidirectional processor I/O bit with one wire. This is possible because the DI input is only ''looked-at'' during the MUX addressing interval while the DO line is still in a high impedance state.

3.0 REFERENCE CONSIDERATIONS

The ADC0833 is intended primarily for use in circuits requiring absolute accuracy. In this type of system, the analog inputs vary between very specific voltage limits and the reference voltage for the A/D converter must remain stable with time and temperature. For ratiometric applications, an ADC0834 is a pin-for-pin compatible alternative since it has a V_{REF} input (note the ADC0834 needs one less bit of mux addressing information).

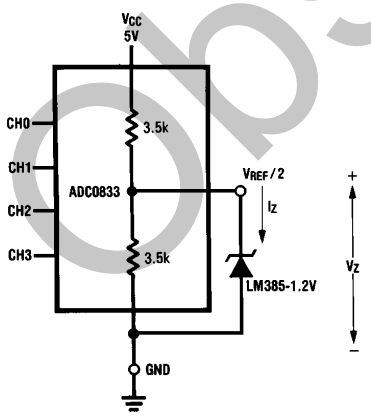
The voltage applied to the $V_{REF}/2$ pin defines the voltage span of the analog input [the difference between $V_{IN}(+)$ and $V_{IN}(-)$] over which the 256 possible output codes apply. A full-scale conversion (an all 1s output code) will result when the voltage difference between a selected ''+'' input and ''−'' input is approximately *twice* the voltage at the $V_{REF}/2$ pin. This internal gain of 2 from the applied reference to the full-scale input voltage allows biasing a low voltage reference diode from the $5V_{DC}$ converter supply. To accommodate a 5V input span, only a 2.5V reference is required. The LM385 and LM336 reference diodes are good low current devices to use with these converters. The output code changes in accordance with the following equation:

$$\text{Output Code} = 256 \left(\frac{V_{IN}(+) - V_{IN}(-)}{2(V_{REF}/2)} \right)$$

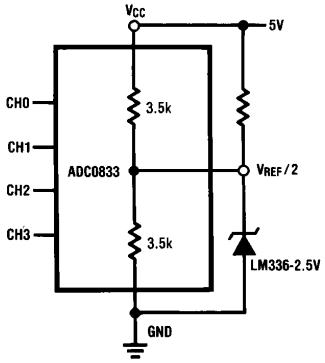
where the output code is the decimal equivalent of the 8-bit binary output (ranging from 0 to 255) and the term $V_{REF}/2$ is the voltage from pin 9 to ground.

The $V_{REF}/2$ pin is the center point of a two resistor divider (each resistor is 3.5 kΩ) connected from V_{CC} to ground. Total ladder input resistance is the sum of these two equal resistors. As shown in *Figure 2,* a reference diode with a voltage less than $V_{CC}/2$ can be connected without requiring an external biasing resistor if its current requirements meet the indicated level.

The minimum value of $V_{REF}/2$ can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals $V_{REF}/256$).



$V_{FULL\text{-}SCALE} \cong 2.4V$



$V_{FULL\text{-}SCALE} \cong 5.0V$

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Note: No external biasing resistor needed if $V_Z < \frac{V_{CC}}{2}$ and I_Z min $< \frac{V_{CC}/2 - V_Z}{1.75\ k\Omega}$

FIGURE 2. Reference Biasing Examples

Functional Description (Continued)

4.0 THE ANALOG INPUTS

The most important feature of these converters is that they can be located right at the analog signal source and through just a few wires can communicate with a controlling processor with a highly noise immune serial bit stream. This in itself greatly minimizes circuitry to maintain analog signal accuracy which otherwise is most susceptible to noise pickup. However, a few words are in order with regard to the analog inputs should the inputs be noisy to begin with or possibly riding on a large common-mode voltage.

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected "+" and "−" inputs for a conversion (60 Hz is most typical). The time interval between sampling the "+" input and then the "−" input is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{error}(max) = V_{PEAK}(2\pi f_{CM})\left(\frac{0.5}{f_{CLK}}\right)$$

where f_{CM} is the frequency of the common-mode signal,

V_{PEAK} is its peak voltage value

and f_{CLK} is the A/D clock frequency.

For a 60 Hz common-mode signal to generate a ¼ LSB error (≈5 mV) with the converter running at 250 kHz, its peak value would have to be 6.63V which would be larger than allowed as it exceeds the maximum analog input limits.

Due to the sampling nature of the analog inputs short spikes of current enter the "+" input and exit the "−" input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 kΩ.

This source resistance limitation is important with regard to the DC leakage currents of input multiplexer as well. The worst-case leakage current of ± 1 μA over temperature will create a 1 mV inut error with a 1 kΩ source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

5.0 OPTIONAL ADJUSTMENTS

5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any V_{IN} (−) input at this $V_{IN(MIN)}$ value. This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage which is 1 ½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the V_{REF} input or V_{CC} for a digital output code which is just changing from 1111 1110 to 1111 1111.

5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage which equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, using 1 LSB = analog span/256) is applied to selected "+" input and the zero reference voltage at the corresponding "−" input should then be adjusted to just obtain the 00_{HEX} to 01_{HEX} code transition.

The full-scale adjustment should be made [with the proper $V_{In}(-)$ voltage applied] by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ fs\ adj = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right]$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range.

(Both are ground referenced.)

The $V_{REF}/2$ voltage is then adjusted to provide a code change from FE_{HEX} to FF_{HEX}. This completes the adjustment procedure.

6.0 POWER SUPPLY

A unique feature of the ADC0833 is the inclusion of a 7V zener diode connected from the V^+ terminal to ground which also connects to the V_{CC} terminal (which is the actual converter supply) through a silicon diode, as shown in *Figure 3.*

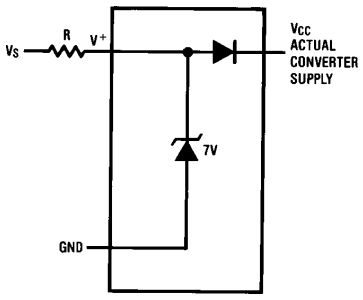

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FIGURE 3. An On-Chip Shunt Regulator Diode

Functional Description (Continued)

This zener is intended for use as a shunt voltage regulator to eliminate the need for any additional regulating components. This is most desirable if the converter is to be remotely located from the system power source. *Figures 4* and *5* illustrate two useful applications of this on-board zener when an external transistor can be afforded.

An important use of the interconnecting diode between V^+ and V_{CC} is shown in *Figures 6* and *7*. Here, this diode is used as a rectifier to allow the V_{CC} supply for the converter to be derived from the clock. The low current requirements of the A/D (~3 mA) and the relatively high clock frequencies used (typically in the range of 10k-400 kHz) allows using the small value filter capacitor shown to keep the ripple on the V_{CC} line to well under ¼ of an LSB. The shunt zener regulator can also be used in this mode. This requires a clock voltage swing which is in excess of V_Z. A current limit for the zener is needed, either built into the clock generator or a resistor can be used from the CLK pin to the V^+ pin.

Applications

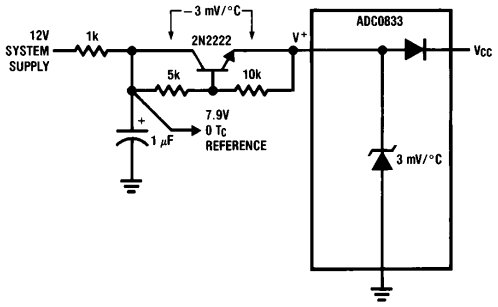

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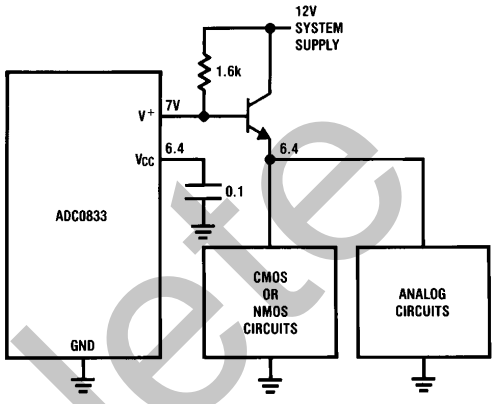
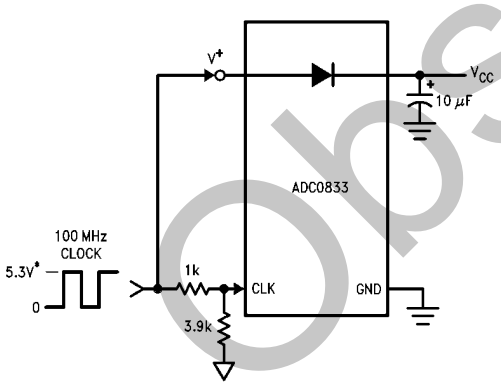
FIGURE 4. Operating with a Temperature Compensated Reference



TL/H/5607–16

FIGURE 5. Using the A/D as the System Supply Regulator



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*Note 4.5V ≤ V_{CC} ≤ 6.3V

FIGURE 6. Generally V_{CC} from the Converter Clock

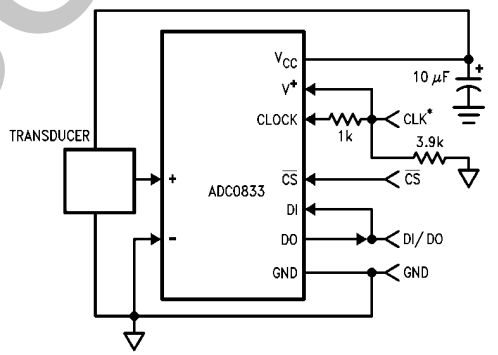

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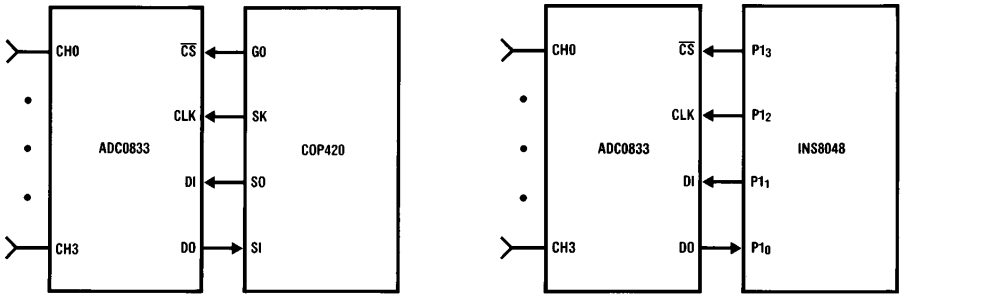
FIGURE 7. Remote Sensing—Clock and Power on 1 Wire

Applications (Continued)

Digital Link and Sample Controlling Software for the Serially Oriented COP420 and the Bit Programmable I/O INS8048



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COP CODING EXAMPLE

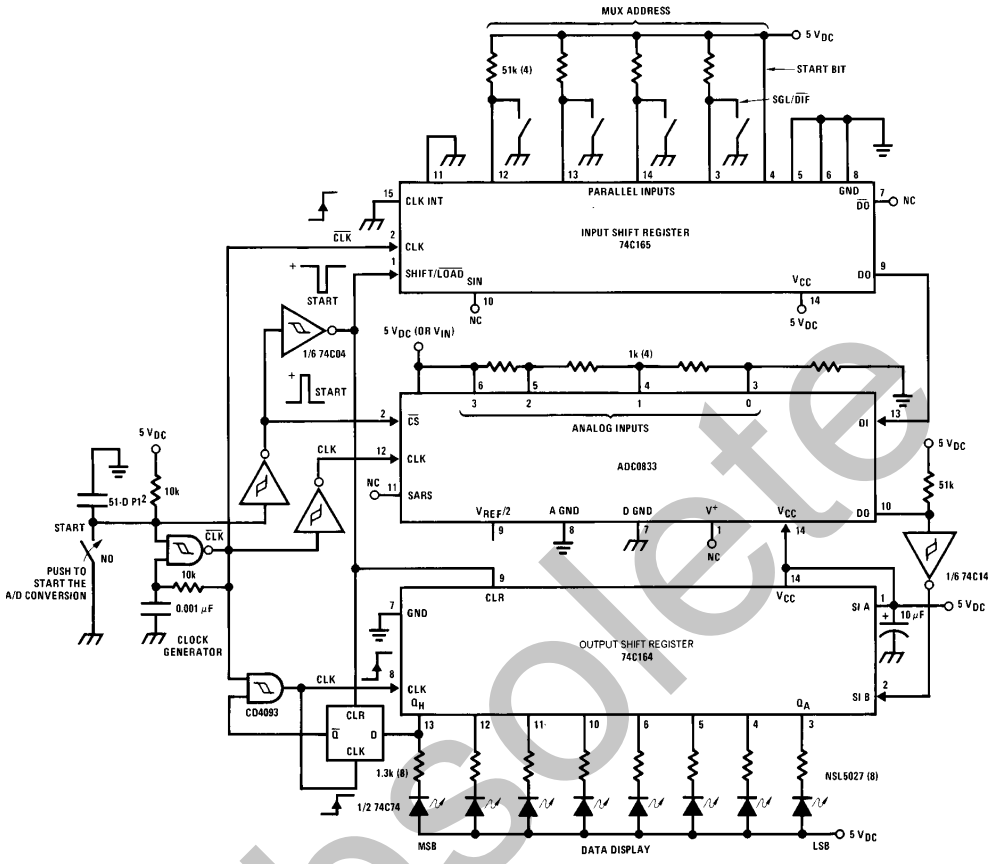
Mnemonic	Instruction
LEI	ENABLES SIO's INPUT AND OUTPUT
SC	C = 1
OGI	G0 = 0 ($\overline{CS}$ = 0)
CLR A	CLEARS ACCUMULATOR
AISC 1	LOADS ACCUMULATOR WITH 1
XAS	EXCHANGES SIO WITH ACCUMULATOR AND STARTS SK CLOCK
LDD	LOADS MUX ADDRESS FROM RAM INTO ACCUMULATOR
NOP	—
XAS	LOADS MUX ADDRESS FROM ACCUMULATOR TO SIO REGISTER
↑ 8 INSTRUCTIONS ↓	
XAS	READS HIGH ORDER NIBBLE (4 BITS) INTO ACCUMULATOR
XIS	PUTS HIGH ORDER NIBBLE INTO RAM
CLR A	CLEARS ACCUMULATOR
RC	C = 0
XAS	READS LOW ORDER NIBBLE INTO ACCUMULATOR AND STOPS SK
XIS	PUTS LOW ORDER NIBBLE INTO RAM
OGI	G0 = 1 ($\overline{CS}$ = 1)
LEI	DISABLES SIO's INPUT AND OUTPUT

8048 CODING EXAMPLE

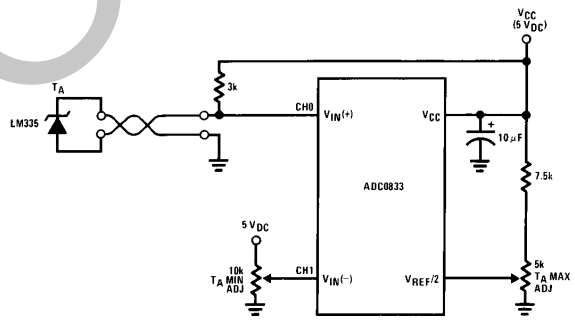
Mnemonic			Instruction
START:	ANL	P1, #0F7H	;SELECT A/D ($\overline{CS}$ = 0)
	MOV	B, #5	;BIT COUNTER ← 5
	MOV	A, #ADDR	;A ← MUX ADDRESS
LOOP 1:	RRC	A	;CY ← ADDRESS BIT
	JC	ONE	;TEST BIT
			;BIT = 0
ZERO:	ANL	P1, #0FEH	;DI ← 0
	JMP	CONT	;CONTINUE
			;BIT = 1
ONE:	ORL	P1, #1	;DI ← 1
CONT:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	DJNZ	B, LOOP 1	;CONTINUE UNTIL DONE
	CALL	PULSE	;EXTRA CLOCK FOR SYNC
	MOV	B, #8	;BIT COUNTER ← 8
LOOP 2:	CALL	PULSE	;PULSE SK 0 → 1 → 0
	IN	A, P1	;CY ← DO
	RRC	A	
	RRC	A	
	MOV	A, C	;A ← RESULT
	RLC	A	;A(0) ← BIT AND SHIFT
	MOV	C, A	;C ← RESULT
	DJNZ	B, LOOP 2	;CONTINUE UNTIL DONE
RETR			
			;PULSE SUBROUTINE
PULSE:	ORL	P1, #04	;SK ← 1
	NOP		;DELAY
	ANL	P1, #0FBH	;SK ← 0
	RET		

Applications (Continued)

A "Stand-Alone" Hook-Up for ADC0833 Evaluation



Low Cost Remote Temperature Sensor



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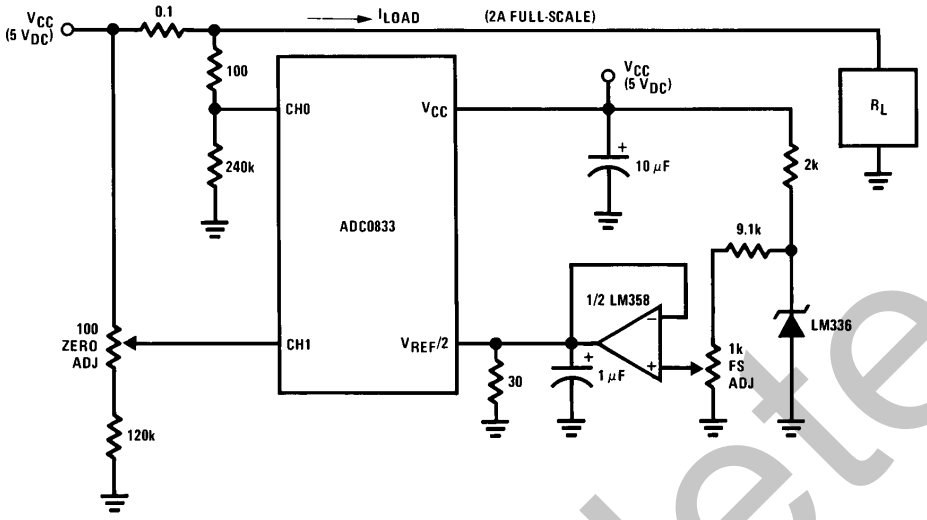
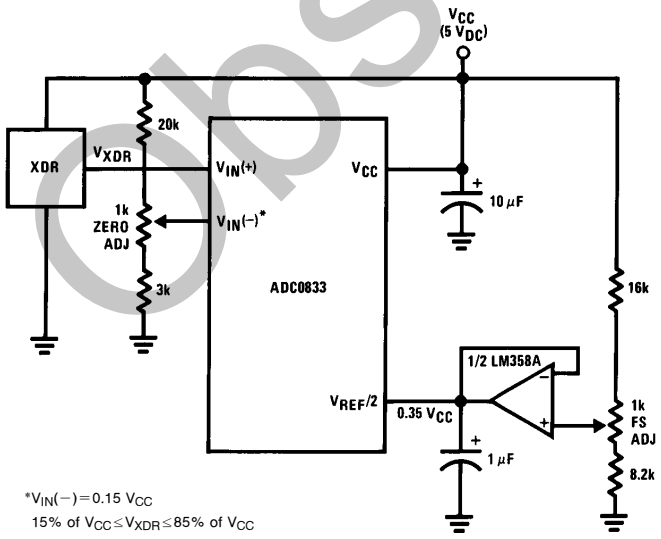
Applications (Continued)

Digitizing a Current Flow



Operating with Automotive Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

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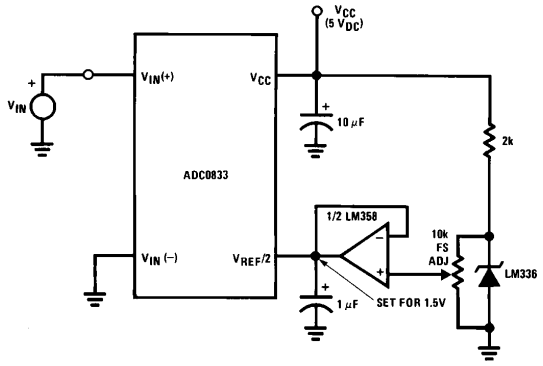
Applications (Continued)

Span Adjust: $0V \leq V_{IN} \leq 3V$



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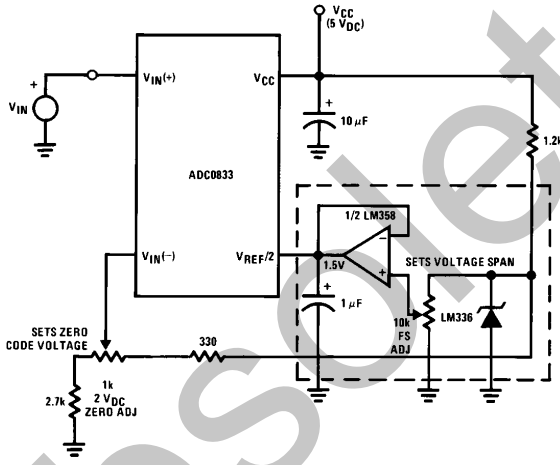
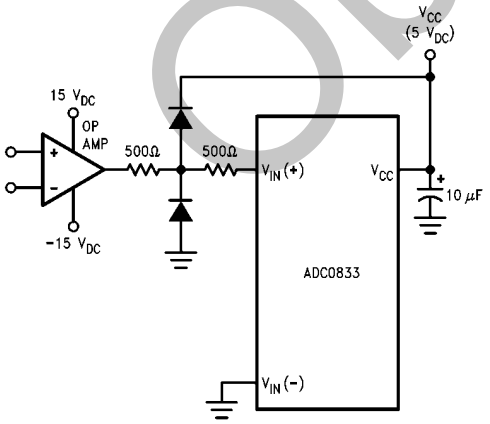
Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



TL/H/5607–19

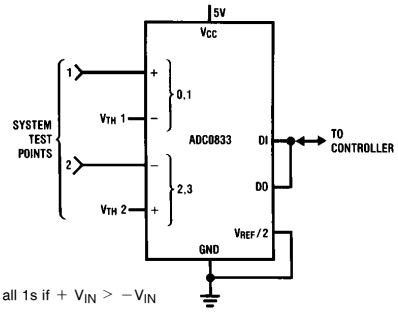
Protecting the Input



Diodes are 1N914

TL/H/5607–20

High Accuracy Comparators



DO = all 1s if $+V_{IN} > -V_{IN}$
DO = all 0s if $+V_{IN} < -V_{IN}$

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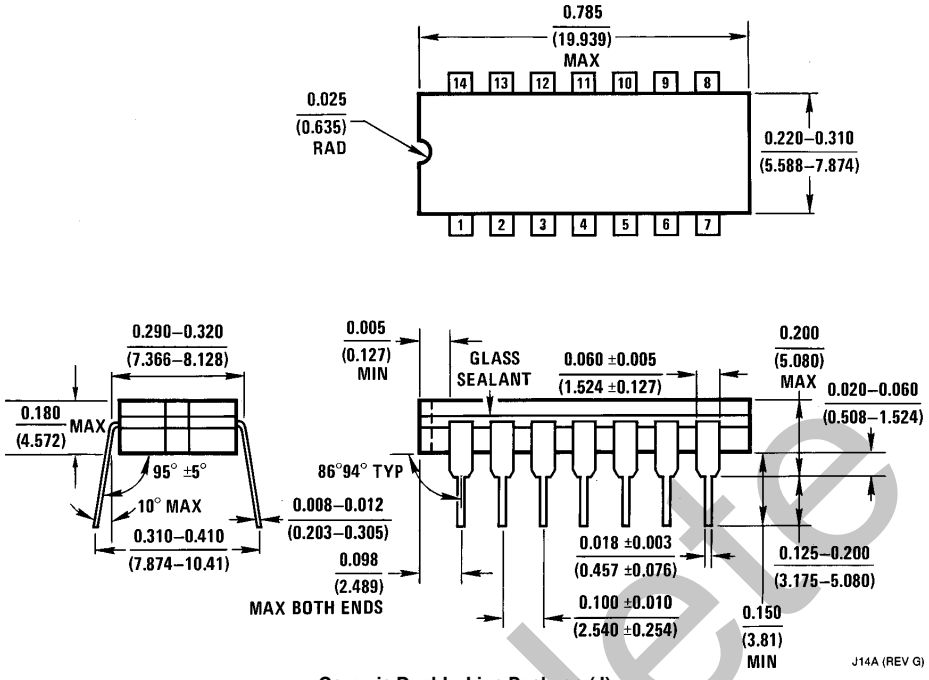
For additional application ideas, refer to the data sheet for the ADC0831 family of serial data converters.

Ordering Information

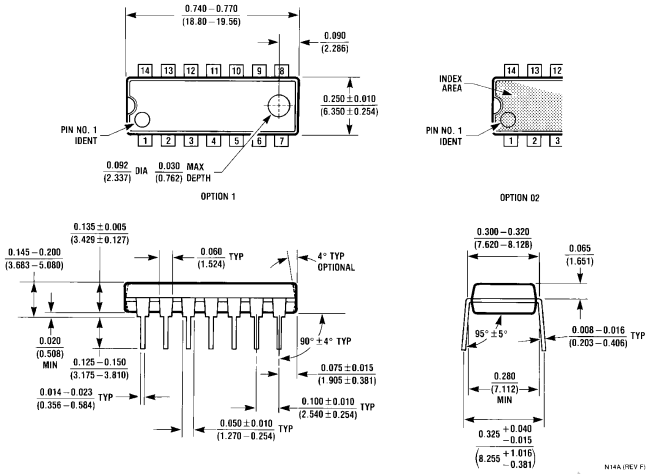
Part Number	Temperature Range	Total Unadjusted Error
ADC0833BCN	0°C to +70°C	±1/2 LSB
ADC0833CCJ	−40°C to +85°C	±1 LSB
ADC0833CCN	0°C to +70°C	

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number ADC0833CCJ
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number ADC0833BCN or ADC0833CCN
NS Package Number N14A

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1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

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