ADC12L030/ADC12L032/ADC12L034/ADC12L038 3.3V Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converters with MUX and Sample/Hold

Check for Samples: ADC12L030, ADC12L032, ADC12L034, ADC12L038

FEATURES

- **0V to 3.3V analog input range with single 3.3V supply**
- **Serial I/O (MICROWIRE and SPI Compatible)**
- **2 or 8 channel differential or single-ended multiplexer**
- **Power down mode**
- **Programmable acquisition time**
- **Variable digital output word length and format**
- **No zero or full scale adjustment required**

APPLICATIONS

- **Portable Medical instruments**
- **Portable computing**
- **Portable Test equipment**

DESCRIPTION

NOTE: These products are now *obsolete*.

The ADC12L030 family is 12-bit plus sign successive approximation A/D converters with serial I/O and configurable input multiplexers. These devices are fully tested with a single 3.3V power supply. The ADC12L032, ADC12L034 and ADC12L038 have 2, 4 and 8 channel multiplexers, respectively. Differential multiplexer outputs and A/D inputs are available at the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 pins. The ADC12L030 has a two channel multiplexer with the multiplexer outputs and A/D inputs internally connected. On request, these A/Ds go through a self calibration process that adjusts linearity, zero and full-scale errors to less than ±½ LSB each.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. A fully differential unipolar analog input range (0V to +3.3V) can be accommodated with a single +3.3V supply. In the differential modes, valid outputs are obtained even when the negative inputs are greater than the positive because of the 12-bit plus sign two's compliment output data format.

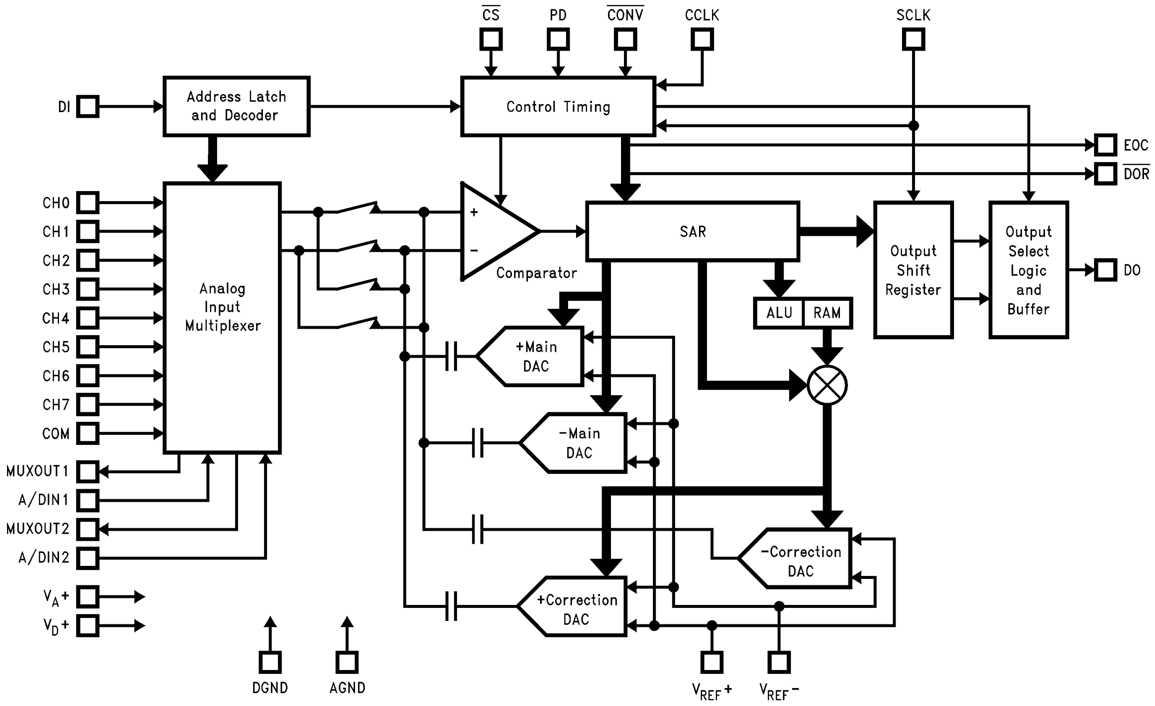
The serial I/O is configured to comply with NSC's MICROWIRE and Motorola's SPI standards. For voltage references, see the LM4040, LM4050 or LM4041 data sheets.

The ADC12L032 and the ADC12L034 are not recommended for new designs and are presented for reference only.

Table 1. Key Specifications

	VALUE	UNIT
Resolution		12-bit plus sign
12-bit plus sign conversion time	8.8	µs (min)
12-bit plus sign sampling rate	73	kHz (max)
Integral linearity error	±1	LSB (max)
Single supply	3.3V ±10%	
Power consumption, active	15	mW (max)
Power consumption, pwr down	40	µW (typ)

ADC12L038 SIMPLIFIED BLOCK DIAGRAM



Connection Diagram

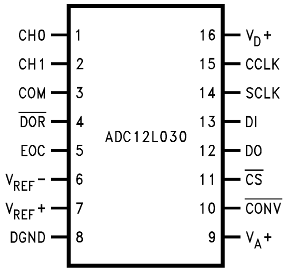
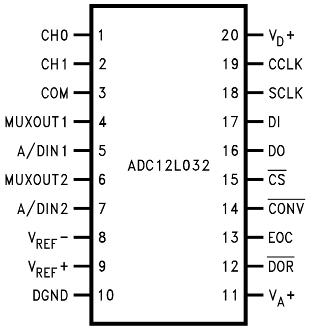


Figure 1. 16-Pin Wide Body (Top View)



* This product is on lifetime buy or obsolete. Shown for reference only.

Figure 2. 20-Pin Wide Body (Top View)

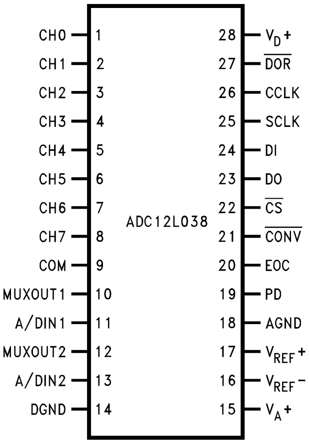
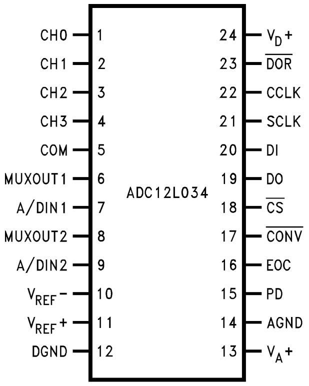


Figure 3. 28-Pin Wide Body (Top View)



* This product is on lifetime buy or obsolete. Shown for reference only.

Figure 4. 24-Pin Wide Body (Top View)

Pin Functions

Pin Descriptions

CCLK The clock applied to this input controls the successive approximation conversion and the acquisition time. The rise and fall times of the clock edges should not be longer than 1 µs.

SCLK This serial data clock input clocks out the serial data. The rising edge at this pin loads the information at the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the A/D. With $\overline{\text{CS}}$ low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out at DO, with the exception of the first bit of data. When $\overline{\text{CS}}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{\text{CS}}$ is toggled, the falling edge of $\overline{\text{CS}}$ always clocks out the first bit of data. $\overline{\text{CS}}$ should be brought low while SCLK is low. The rise and fall times of the clock edges should not be longer than 1 µs.

DI The data applied to this serial data input pin is shifted into the multiplexer address and mode select register on the rising edge of SCLK. Table 3, Table 4, Table 5, and Table 6 show the assignment of the multiplexer address and the mode select data.

DO This pin is the active push/pull output pin when $\overline{\text{CS}}$ is Low. When $\overline{\text{CS}}$ is High this output is off (high impedance). The A/D conversion result (DB0–DB12) and converter status data are clocked out on this pin at the falling edge of SCLK. The word length and format of this result can vary (see Table 2). The word length and format are controlled by the data shifted into the multiplexer address and mode select register (see Table 6).

EOC This active push/pull output indicates the status of the ADC. When low the A/D is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles.

$\overline{\text{CS}}$ When a logic low is applied to this chip select pin, the rising edge of SCLK shifts the data at DI into the address register and brings DO out of the high impedance state. With $\overline{\text{CS}}$ low, the falling edge of SCLK shifts the data resulting from the previous ADC conversion out at DO, with the exception of the first bit of data. When $\overline{\text{CS}}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{\text{CS}}$ is toggled the falling edge of $\overline{\text{CS}}$ always clocks out the first bit of data. $\overline{\text{CS}}$ should be brought low while SCLK is low. The falling edge of $\overline{\text{CS}}$ halts a conversion in progress (the data in the output latches may be corrupted) and starts the sequence for a new conversion. Therefore, when $\overline{\text{CS}}$ is brought low during a conversion in progress the data output at that time should be ignored. $\overline{\text{CS}}$ may also be left continuously low, in which case it is imperative that the correct number of SCLK cycles be applied to the ADC in order to remain synchronous. After the ADC supply power is applied, the ADC expects to see 13 clock cycles for each I/O sequence. After that, the number of clock cycles the ADC expects is the same as the digital output word length, which can be modified by the user. See Table 6.

$\overline{\text{DOR}}$ This data output ready pin is an active push/pull output. It is low when the conversion result is being shifted out and goes high to signal that all the data has been shifted out.

$\overline{\text{CONV}}$ A logic low is required on this pin to program any mode or change the ADC's configuration. (See the Table 6, *Mode Programming*). When this pin is high, the ADC is placed into the read data only mode. While in this mode, bringing $\overline{\text{CS}}$ low and pulsing SCLK will only clock out any data stored in the ADCs output shift register. The data at DI will be neglected, a new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto-Cal or Auto-Zero is in progress.

PD When this power down pin is high, the A/D is powered down; when PD is low the A/D is powered up. The A/D takes a maximum of 700 µs to power up after the command is given.

CH0–CH7 These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin (see Table 3, Table 4, and Table 5).
The voltage applied to these inputs should not exceed V_A+ or go below GND. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM This analog input pin is used as a pseudo ground when the analog multiplexer is single-ended.

MUXOUT1, MUXOUT2 These are the multiplexer output pins.

Pin Descriptions (continued)

A/DIN1, A/DIN2 These are the converter input pins. MUXOUT1 is usually tied to A/DIN1. MUXOUT2 is usually tied to A/DIN2. If external circuitry is placed between MUXOUT1 and A/DIN1, or MUXOUT2 and A/DIN2 it may be necessary to protect these pins. The voltage at these pins should not exceed V_A^+ or go below AGND (see Figure 27).

V_{REF}+ This is the positive analog voltage reference input. In order to maintain accuracy the voltage range of V_{REF} = (V_{REF}+) − (V_{REF}−) is 1 V_{DC} to 3.3 V_{DC} and V_{REF}+ cannot exceed V_A+.

V_{REF}− The negative voltage reference input. To maintain accuracy, this voltage must not go below GND or exceed (V_{REF}+) − 1V. (See Figure 26).

V_A+, V_D+ These analog and digital power supply pins are not connected together on the chip and should be tied to the same power supply but bypassed separately (see Figure 26). The operating voltage range of V_A+ and V_D+ is 3.0 V_{DC} to 5.5 V_{DC}.

DGND Digital ground pin (see Figure 26).

AGND Analog ground pin (see Figure 26).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2)

Positive Supply Voltage	
(V^+ = V_A+ = V_D+)	6.5V
Voltage at Inputs and Outputs except CH0–CH7 and COM	−0.3V to V^+ +0.3V
Voltage at Analog Inputs CH0–CH7 and COM	GND −5V to V^+ +5V
|V_A+ − V_D+|	300 mV
Input Current at Any Pin (3)	±30 mA
Package Input Current (3)	±120 mA
Package Dissipation at T_A = 25°C (4)	500 mW
ESD Susceptibility (5)	
Human Body Model	1500V
Soldering Information	
SO Package (6):	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Storage Temperature	−65°C to +150°C

(1) All voltages are measured with respect to GND, unless otherwise specified.

(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(3) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A+ or V_D+), the current at that pin should be limited to 20 mA. The 120 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 20 mA to four.

(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is P_D = ($T_J$max − T_A)/θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_J max = 150°C.

(5) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

(6) See AN450 “Surface Mounting Methods and Their Effect on Product Reliability” or the section titled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Operating Ratings (1) (2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$ $-40°C \le T_A \le +85°C$
Supply Voltage $(V^+ = V_A+ = V_D+)$	+3.0V to +5.5V
$\lvert V_A+ - V_D+ \rvert$	≤ 100 mV
$V_{REF}+$	0V to V_A+
$V_{REF}-$	0V to $(V_{REF}+ -1V)$
V_{REF} $(V_{REF}+ - V_{REF}-)$	1V to V_A+
V_{REF} Common Mode Voltage Range $[(V_{REF}+) - (V_{REF}-)] / 2$	0.1 V_A+ to 0.6 V_A+
A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 Voltage Range	0V to V_A+
A/D IN Common Mode Voltage Range $[(V_{IN}+) - (V_{IN}-)] / 2$	0V to V_A+

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) All voltages are measured with respect to GND, unless otherwise specified.

Package Thermal Resistance

Part Number	**Thermal Resistance (θ_{JA})**
ADC12L030CIWM	70°C/W
ADC12L032CIWM (1)	64°C/W
ADC12L034CIWM (1)	57°C/W
ADC12L038CIWM	50°C/W

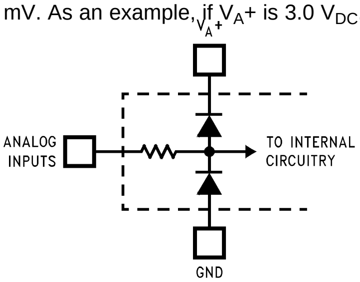
(1) This product is on lifetime buy or obsolete. Shown for reference only.

Converter Electrical Characteristics

The following specifications apply for $V^+ = V_A+ = V_D+ = +3.3\ V_{DC}$, $V_{REF}+ = +2.500\ V_{DC}$, $V_{REF}- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and 10(t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (1) (2) (3)

Symbol	Parameter	Conditions	Typical (4)	Limits (5)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
	Resolution with No Missing Codes			**12 + sign**	Bits (min)
ILE	Integral Linearity Error	After Auto-Cal (6) (7)	±1/2	**±1**	LSB (max)
DNL	Differential Non-Linearity	After Auto-Cal		**±1**	LSB (max)
	Positive Full-Scale Error	After Auto-Cal (6) (7)	±1/2	**±2**	LSB (max)
	Negative Full-Scale Error	After Auto-Cal (6) (7)	±1/2	**±2**	LSB (max)
	Offset Error	After Auto-Cal (8) (7) $V_{IN}(+) = V_{IN}(-) = 1.250V$	±1/2	**±2**	LSB (max)
	DC Common Mode Error	After Auto-Cal (9)	±2	**±3.5**	LSB (max)
TUE	Total Unadjusted Error	After Auto-Cal (6) (10) (11)	±1		LSB
	Resolution with No Missing Codes	8-bit + sign mode		**8 + sign**	Bits (min)
INL	Integral Linearity Error	8-bit + sign mode (6)		**±1/2**	LSB (max)
DNL	Differential Non-Linearity	8-bit + sign mode		**±3/4**	LSB (max)
	Positive Full-Scale Error	8-bit + sign mode (6)		**±1/2**	LSB (max)
	Negative Full-Scale Error	8-bit + sign mode (6)		**±1/2**	LSB (max)
	Offset Error	8-bit + sign mode after Auto-Zero $V_{IN}(+) = V_{IN}(-) = +1.250V$ (10)		**±1/2**	LSB (max)
TUE	Total Unadjusted Error	8-bit + sign mode after Auto-Zero (6) (10) (11)		**±3/4**	LSB (max)
	Multiplexer Chan-to-Chan Matching		±0.05		LSB
	Power Supply Sensitivity	$V^+ = +3.3V \pm 10\%$			
	Offset Error		±0.5	**±1**	LSB (max)
	+ Full-Scale Error		±0.5	**±1.5**	LSB (max)

(1) Two on-chip diodes are tied to each analog input through a series resistor as shown below. Input voltage magnitude up to 5V above V_A+ or 5V below GND will not damage this device. However, errors in the A/D conversion can occur (if these diodes are forward biased by more than 50 mV) if the input voltage magnitude of selected or unselected analog input go above V_A+ or below GND by more than 50 mV. As an example, if V_A+ is 3.0 V_{DC}, full-scale input voltage must be ≤3.05 V_{DC} to ensure accurate conversions.



(2) To guarantee accuracy, it is required that the V_A+ and V_D+ be connected together to the same power supply with separate bypass capacitors at each V^+ pin.
(3) With the test condition for V_{REF} ($V_{REF}+ - V_{REF}-$) given as +2.500V the 12-bit LSB is 610 µV and the 8-bit LSB is 9.8 mV.
(4) Typical figures are at $T_J = T_A = 25°C$ and represent most likely parametric norm.
(5) Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).
(6) Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error, the straight line passes through negative full-scale and zero (see Figure 6 and Figure 7).
(7) The ADC12L030 family's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a maximum repeatability uncertainty of 0.2 LSB.
(8) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.
(9) The DC common-mode error is measured in the differential multiplexer mode with the assigned positive and negative input channels shorted together.
(10) Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the worst-case value of the code transitions between 1 to 0 and 0 to +1 (see Figure 8).
(11) Total unadjusted error includes offset, full-scale, linearity and multiplexer errors.

Converter Electrical Characteristics (continued)

The following specifications apply for $V^+ = V_A+ = V_D+ = +3.3\ V_{DC}$, $V_{REF}+ = +2.500\ V_{DC}$, $V_{REF}- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (1) (2) (3)

Symbol	Parameter	Conditions	Typical (4)	Limits (5)	Units (Limits)
	− Full-Scale Error		±0.5	**±1.5**	LSB (max)
	Integral Linearity Error		±0.5		LSB
	Output Data from “12-Bit Conversion of Offset” (see Table 6)	(12)		**+10** **−10**	LSB (max) LSB (min)
	Output Data from “12-Bit Conversion of Full-Scale” (see Table 6)	(12)		**4095** **4093**	LSB (max) LSB (min)
UNIPOLAR DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = 2.5\ V_{P-P}$	69.4		dB
		$f_{IN} = 20$ kHz, $V_{IN} = 2.5\ V_{P-P}$	68.3		dB
		$f_{IN} = 40$ kHz, $V_{IN} = 2.5\ V_{PP}$	65.7		dB
	−3 dB Full Power Bandwidth	$V_{IN} = 2.5\ V_{P-P}$, where S/(N+D) drops 3 dB	31		kHz
DIFFERENTIAL DYNAMIC CONVERTER CHARACTERISTICS					
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	$f_{IN} = 1$ kHz, $V_{IN} = \pm 2.5V$	77.0		dB
		$f_{IN} = 20$ kHz, $V_{IN} = \pm 2.5V$	73.9		dB
		$f_{IN} = 40$ kHz, $V_{IN} = \pm 2.5V$	67.0		dB
	−3 dB Full Power Bandwidth	$V_{IN} = \pm 2.5V$, where S/(N+D) drops 3 dB	40		kHz
REFERENCE INPUT, ANALOG INPUTS AND MULTIPLEXER CHARACTERISTICS					
C_{REF}	Reference Input Capacitance		85		pF
$C_{A/D}$	A/DIN1 and A/DIN2 Analog Input Capacitance		75		pF
	A/DIN1 and A/DIN2 Analog Input Leakage Current	$V_{IN} = +3.3V$ or $V_{IN} = 0V$	±0.1	**±1.0**	µA (max)
	CH0–CH7 and COM Input Voltage			**GND − 0.05** **V_A+ + 0.05**	V (min) V (max)
C_{CH}	CH0–CH7 and COM Input Capacitance		10		pF
C_{MUXOUT}	MUX Output Capacitance		20		pF
	Off Channel Leakage (13) CH0–CH7 and COM Pins	On Channel = 3.3V and Off Channel = 0V	−0.01	**−0.3**	µA (min)
		On Channel = 0V and Off Channel = 3.3V	0.01	**0.3**	µA (max)
	On Channel Leakage (13) CH0–CH7 and COM Pins	On Channel = 3.3V and Off Channel = 0V	0.01	**0.3**	µA (max)
		On Channel = 0V and Off Channel = 3.3V	−0.01	**−0.3**	µA (min)
	MUXOUT1 and MUXOUT2 Leakage Current	$V_{MUXOUT} = 3.3V$ or $V_{MUXOUT} = 0V$	0.01	**0.3**	µA (max)
R_{ON}	MUX On Resistance	$V_{IN} = 1.65V$ and $V_{MUXOUT} = 1.55V$	1300	**1900**	Ω (max)
	R_{ON} Matching Channel to Channel	$V_{IN} = 1.65V$ and $V_{MUXOUT} = 1.55V$	5		%
	Channel-to-Channel Crosstalk	$V_{IN} = 3.3\ V_{P-P}$, $f_{IN} = 40$ kHz	−72		dB
	MUX Bandwidth		90		kHz

(12) The “12-Bit Conversion of Offset” and “12-Bit Conversion of Full-Scale” modes are intended to test the functionality of the device. Therefore, the output data from these modes are not an indication of the accuracy of a conversion result.
(13) Channel leakage current is measured after the channel selection.

DC and Logic Electrical Characteristics

The following specifications apply for $V^+ = V_A+ = V_D+ = +3.3\ V_{DC}$, $V_{REF}+ = +2.500\ V_{DC}$, $V_{REF}- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J =$**

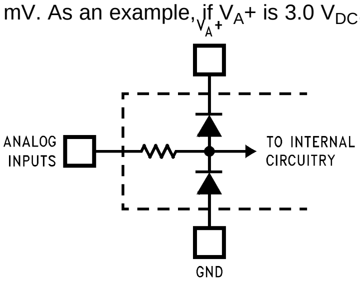
DC and Logic Electrical Characteristics (continued)

The following specifications apply for $V^+ = V_A+ = V_D+ = +3.3\ V_{DC}$, $V_{REF}+ = +2.500\ V_{DC}$, $V_{REF}- = 0\ V_{DC}$, 12-bit + sign conversion mode, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25°C$. (1) (2) (3)

T_{MIN} to T_{MAX}; all other limits $T_A = T_J = 25°C$. (1) (2) (3)

Symbol	Parameter	Conditions	Typical (4)	Limits (5)	Units (Limits)
CCLK, $\overline{CS}$, $\overline{CONV}$, DI, PD AND SCLK INPUT CHARACTERISTICS					
$V_{IN(1)}$	Logical “1” Input Voltage	$V^+ = 3.6V$		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	$V^+ = 3.0V$		**0.8**	V (max)
$I_{IN(1)}$	Logical “1” Input Current	$V_{IN} = 3.3V$	0.005	**1.0**	µA (max)
$I_{IN(0)}$	Logical “0” Input Current	$V_{IN} = 0V$	−0.005	**−1.0**	µA (min)
DO, EOC AND $\overline{DOR}$ DIGITAL OUTPUT CHARACTERISTICS					
$V_{OUT(1)}$	Logical “1” Output Voltage	$V^+ = 3.0V$, $I_{OUT} = −360$ µA		**2.4**	V (min)
		$V^+ = 3.0V$, $I_{OUT} = −10$ µA		**2.9**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	$V^+ = 3.0V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE Output Current	$V_{OUT} = 0V$	−0.1	**−3.0**	µA (max)
		$V_{OUT} = 3.3V$	0.1	**3.0**	µA (max)
$+I_{SC}$	Output Short Circuit Source Current	$V_{OUT} = 0V$	14	**6.5**	mA (min)
$−I_{SC}$	Output Short Circuit Sink Current	$V_{OUT} = V_D+$	16	**8.0**	mA (min)
POWER SUPPLY CHARACTERISTICS					
I_D+	Digital Supply Current	Awake	1.1	**1.5**	mA (max)
		$\overline{CS}$ = HIGH, Powered Down, CCLK on	600		µA
		$\overline{CS}$ = HIGH, Powered Down, CCLK off	12		µA
I_A+	Positive Analog Supply Current	Awake	2.2	**3.0**	mA (max)
		$\overline{CS}$ = HIGH, Powered Down, CCLK on	10		µA
		$\overline{CS}$ = HIGH, Powered Down, CCLK off	0.1		µA
I_{REF}	Reference Input Current	Awake	70		µA
		$\overline{CS}$ = HIGH, Powered Down	0.1		µA

(1) Two on-chip diodes are tied to each analog input through a series resistor as shown below. Input voltage magnitude up to 5V above V_A+ or 5V below GND will not damage this device. However, errors in the A/D conversion can occur (if these diodes are forward biased by more than 50 mV) if the input voltage magnitude of selected or unselected analog input go above V_A+ or below GND by more than 50 mV. As an example, if V_A+ is 3.0 V_{DC}, full-scale input voltage must be ≤3.05 V_{DC} to ensure accurate conversions.



(2) To guarantee accuracy, it is required that the V_A+ and V_D+ be connected together to the same power supply with separate bypass capacitors at each V^+ pin.

(3) With the test condition for V_{REF} ($V_{REF}+ − V_{REF}−$) given as +2.500V the 12-bit LSB is 610 µV and the 8-bit LSB is 9.8 mV.

(4) Typical figures are at $T_J = T_A = 25°C$ and represent most likely parametric norm.

(5) Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

AC Electrical Characteristics

The following specifications apply for $V^+ = V_A+ = V_D+ = +3.3\ V_{DC}$, $V_{REF}+ = +2.500\ V_{DC}$, $V_{REF}- = 0\ V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3$ ns, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply**

AC Electrical Characteristics (continued)

The following specifications apply for $V^+ = V_A+ = V_D+ = +3.3\ V_{DC}$, $V_{REF}+ = +2.500\ V_{DC}$, $V_{REF}- = 0\ V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3$ ns, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and 10(t_{CK}) acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (1)

for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$. (1)

Symbol	Parameter	Conditions	Typical (2)	Limits (3)	Units (Limits)
f_{CK}	Conversion Clock (CCLK) Frequency		10	**5**	MHz (max)
			1		MHz (min)
f_{SK}	Serial Data Clock SCLK Frequency		10	**5**	MHz (max)
			0		Hz (min)
	Conversion Clock Duty Cycle			**40**	% (min)
				60	% (max)
	Serial Data Clock Duty Cycle			**40**	% (min)
				60	% (max)
t_C	Conversion Time	12-Bit + Sign or 12-Bit	44(t_{CK})	**44(t_{CK})**	(max)
				8.8	µs (max)
		8-Bit + Sign or 8-Bit	21(t_{CK})	**21(t_{CK})**	(max)
				4.2	µs (max)
t_A	Acquisition Time (4)	6 Cycles Programmed	6(t_{CK})	**6(t_{CK})**	(min)
				7(t_{CK})	(max)
				1.2	µs (min)
				1.4	µs (max)
		10 Cycles Programmed	10(t_{CK})	**10(t_{CK})**	(min)
				11(t_{CK})	(max)
				2.0	µs (min)
				2.2	µs (max)
		18 Cycles Programmed	18(t_{CK})	**18(t_{CK})**	(min)
				19(t_{CK})	(max)
				3.6	µs (min)
				3.8	µs (max)
		34 Cycles Programmed	34(t_{CK})	**34(t_{CK})**	(min)
				35(t_{CK})	(max)
				6.8	µs (min)
				7.0	µs (max)
t_{CAL}	Self-Calibration Time		4944(t_{CK})	**4944(t_{CK})**	(max)
				988.8	µs (max)
t_{AZ}	Auto-Zero Time		76(t_{CK})	**76(t_{CK})**	(max)
				15.2	µs (max)
t_{SYNC}	Self-Calibration or Auto-Zero Synchronization Time from DOR		2(t_{CK})	**2(t_{CK})**	(min)
				3(t_{CK})	(max)
				0.40	µs (min)
				0.60	µs (max)
$t_{\overline{DOR}}$	DOR High Time when $\overline{CS}$ is Low Continuously for Read Data and Software Power Up/Down		9(t_{SK})	**9(t_{SK})**	(max)
				1.8	µs (max)

---

(1) Timing specifications are tested at the TTL logic levels, $V_{IL} = 0.4V$ for a falling edge and $V_{IH} = 2.4V$ for a rising edge. TRI-STATE output voltage is forced to 1.4V.

(2) Typical figures are at $T_J = T_A = 25°C$ and represent most likely parametric norm.

(3) Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

(4) If SCLK and CCLK are driven from the same clock source, then t_A is 6, 10, 18 or 34 clock periods minimum and maximum.

AC Electrical Characteristics (continued)

The following specifications apply for $V^+ = V_A+ = V_D+ = +3.3\ V_{DC}$, $V_{REF}+ = +2.500\ V_{DC}$, $V_{REF}- = 0\ V_{DC}$, 12-bit + sign conversion mode, $t_r = t_f = 3$ ns, $f_{CK} = f_{SK} = 5$ MHz, $R_S = 25\Omega$, source impedance for $V_{REF}+$ and $V_{REF}- \leq 25\Omega$, fully-differential input with fixed 1.250V common-mode voltage, and $10(t_{CK})$ acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (1)

Symbol	Parameter	Conditions	Typical (2)	Limits (3)	Units (Limits)
$t_{\overline{CONV}}$	$\overline{\text{CONV}}$ Valid Data Time		$8(t_{SK})$	**$8(t_{SK})$**	(max)
				1.6	µs (max)
t_{HPU}	Hardware Power-Up Time, Time from PD Falling Edge to EOC Rising Edge		250	**700**	µs (max)
t_{SPU}	Software Power-Up Time, Time from Serial Data Clock Falling Edge to EOC Rising Edge		500	**700**	µs (max)
t_{ACC}	Access Time Delay from $\overline{\text{CS}}$ Falling Edge to DO Data Valid		25	**60**	ns (max)
t_{SET-UP}	Set-Up Time of $\overline{\text{CS}}$ Falling Edge to Serial Data Clock Rising Edge			**50**	ns (min)
t_{DELAY}	Delay from SCLK Falling Edge to $\overline{\text{CS}}$ Falling Edge		0	**5**	ns (min)
t_{1H}, t_{0H}	Delay from $\overline{\text{CS}}$ Rising Edge to DO TRI-STATE	$R_L = 3k$, $C_L = 100$ pF	70	**100**	ns (max)
t_{HDI}	DI Hold Time from Serial Data Clock Rising Edge		5	**15**	ns (min)
t_{SDI}	DI Set-Up Time from Serial Data Clock Rising Edge		5	**10**	ns (min)
t_{HDO}	DO Hold Time from Serial Data Clock Falling Edge	$R_L = 3k$, $C_L = 100$ pF	35	**65** **5**	ns (max) ns (min)
t_{DDO}	Delay from Serial Data Clock Falling Edge to DO Data Valid		50	**90**	ns (max)
t_{RDO}	DO Rise Time, TRI-STATE to High DO Rise Time, Low to High	$R_L = 3k$, $C_L = 100$ pF	10	**40**	ns (max)
t_{FDO}	DO Fall Time, TRI-STATE to Low DO Fall Time, High to Low	$R_L = 3k$, $C_L = 100$ pF	15 15	**40** **40**	ns (max) ns (max)
t_{CD}	Delay from $\overline{\text{CS}}$ Falling Edge to $\overline{\text{DOR}}$ Falling Edge		50	**80**	ns (max)
t_{SD}	Delay from Serial Data Clock Falling Edge to $\overline{\text{DOR}}$ Rising Edge		45	**80**	ns (max)
C_{IN}	Capacitance of Logic Inputs		10		pF
C_{OUT}	Capacitance of Logic Outputs		20		pF

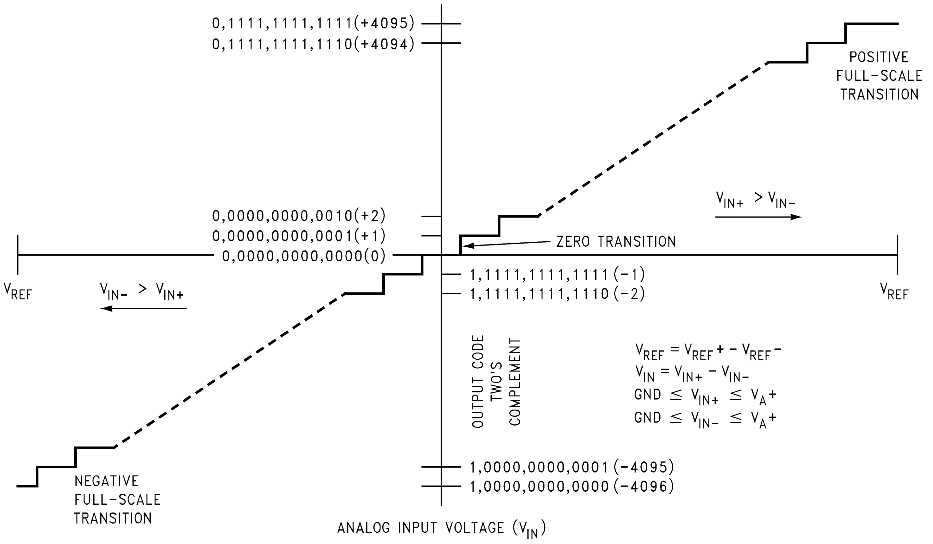


Figure 5. Transfer Characteristic

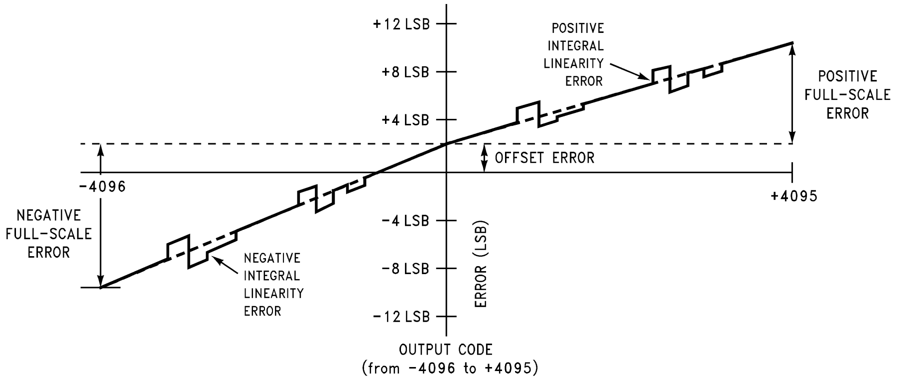


Figure 6. Simplified Error Curve vs. Output Code without Auto-Calibration or Auto-Zero Cycles

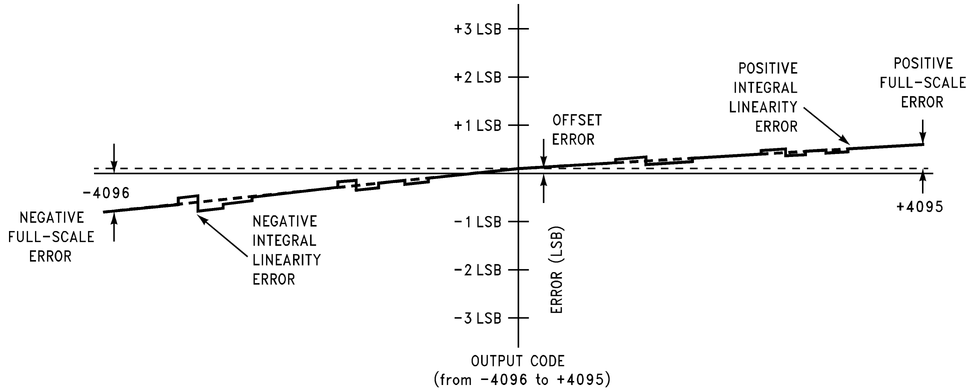


Figure 7. Simplified Error Curve vs. Output Code after Auto-Calibration Cycle

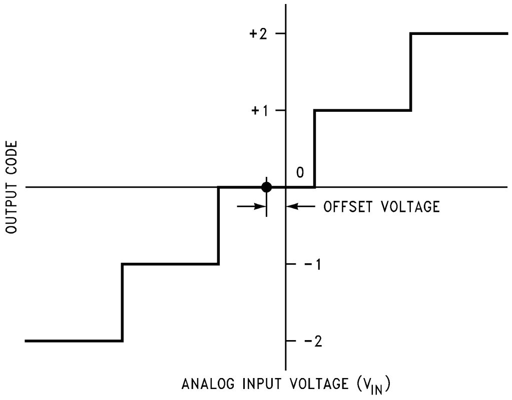
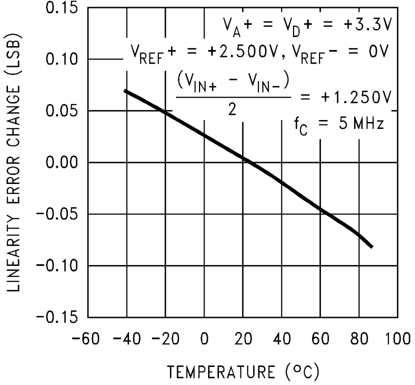


Figure 8. Offset or Zero Error Voltage

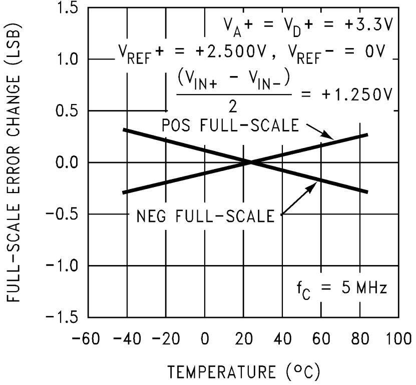
Typical Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign mode is equal to or better than shown.

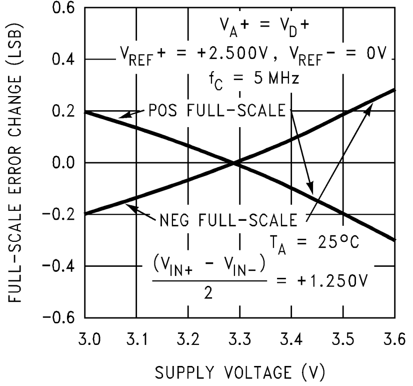
Linearity Error Change vs. Temperature



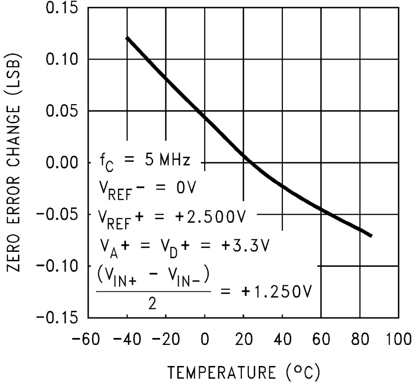
Full-Scale Error Change vs. Temperature



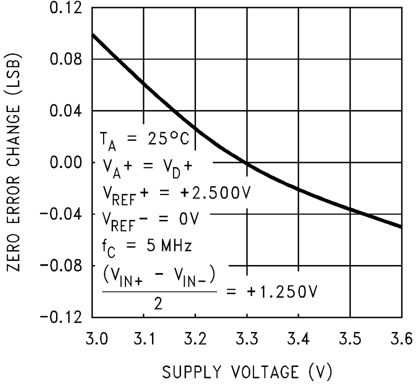
Full-Scale Error Change vs. Supply Voltage



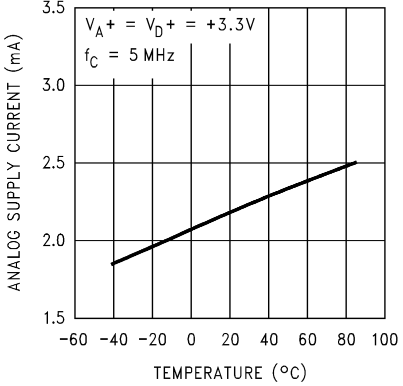
Zero Error Change vs. Temperature



Zero Error Change vs. Supply Voltage



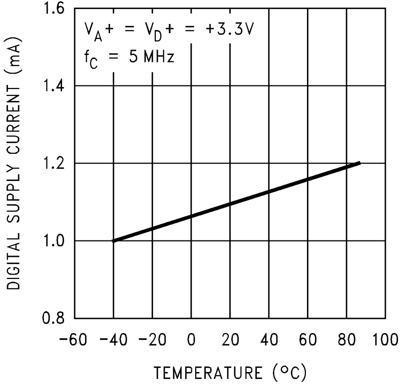
Analog Supply Current vs. Temperature



Typical Performance Characteristics (continued)

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign mode is equal to or better than shown.

Digital Supply Current vs. Temperature



TEST CIRCUITS

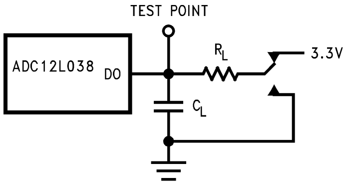


Figure 9. DO “TRI-STATE” (t_{1H}, t_{0H})

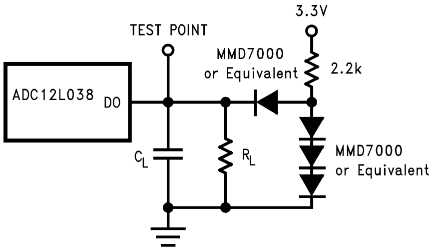
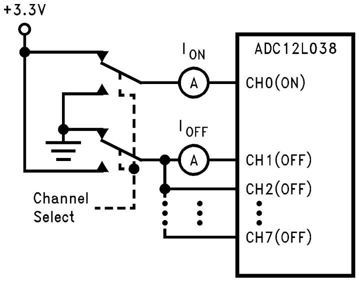


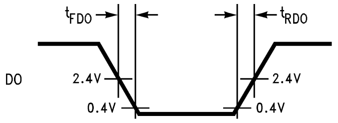
Figure 10. DO except “TRI-STATE”

Figure 11. Leakage Current



TIMING DIAGRAMS

DO Falling and Rising Edge



DO "TRI-STATE" Falling and Rising Edge

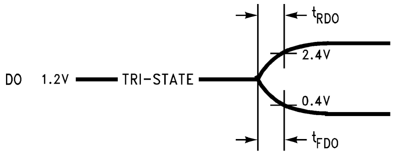


Figure 12. DI Data Input Timing

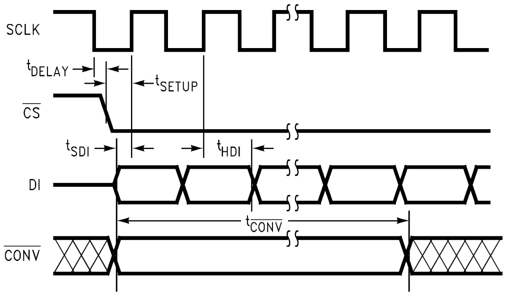


Figure 13. DO Data Output Timing Using $\overline{\text{CS}}$

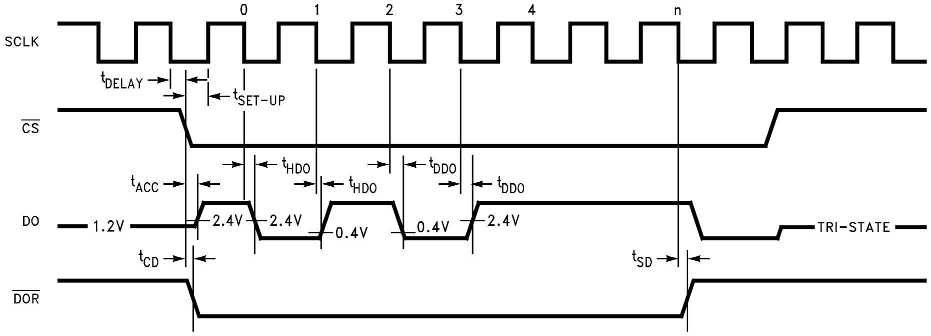


Figure 14. DO Data Output Timing with $\overline{\text{CS}}$ Continuously Low

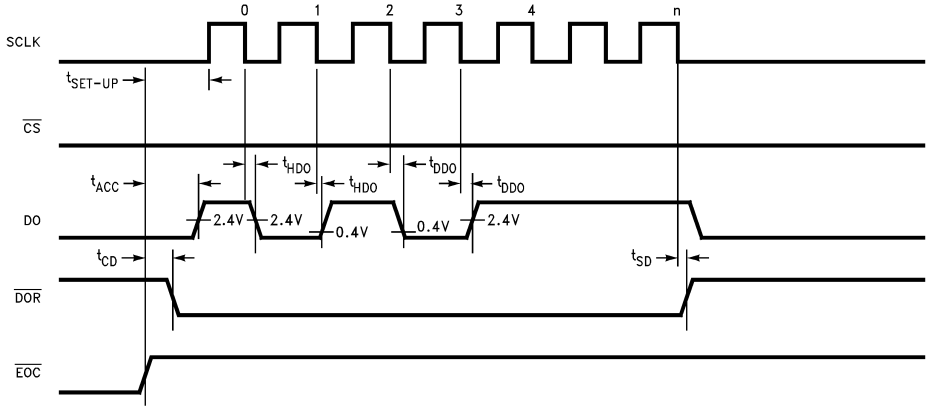
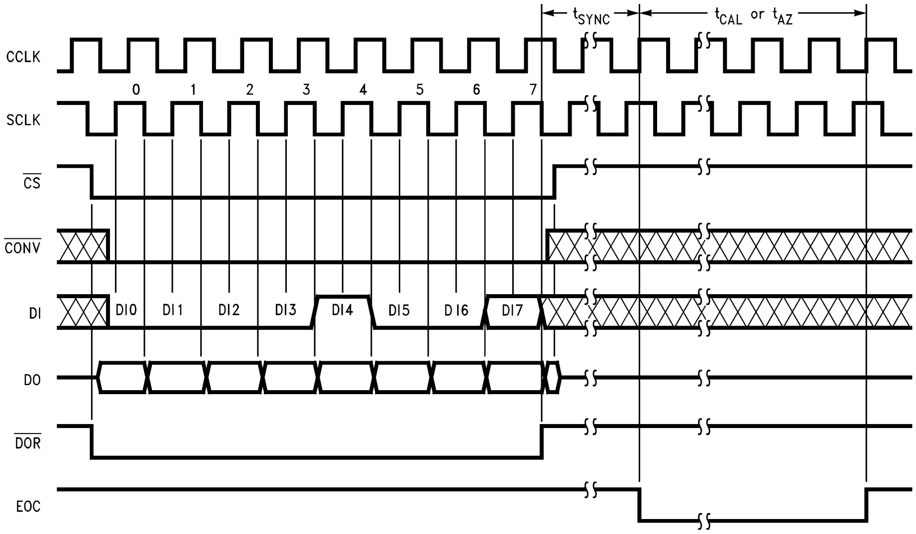


Figure 15.
ADC12L038 Auto-Cal or Auto-Zero



Note: DO output data is not valid during this cycle.

Figure 16.
ADC12L038 Read Data without Starting a Conversion Using $\overline{\text{CS}}$

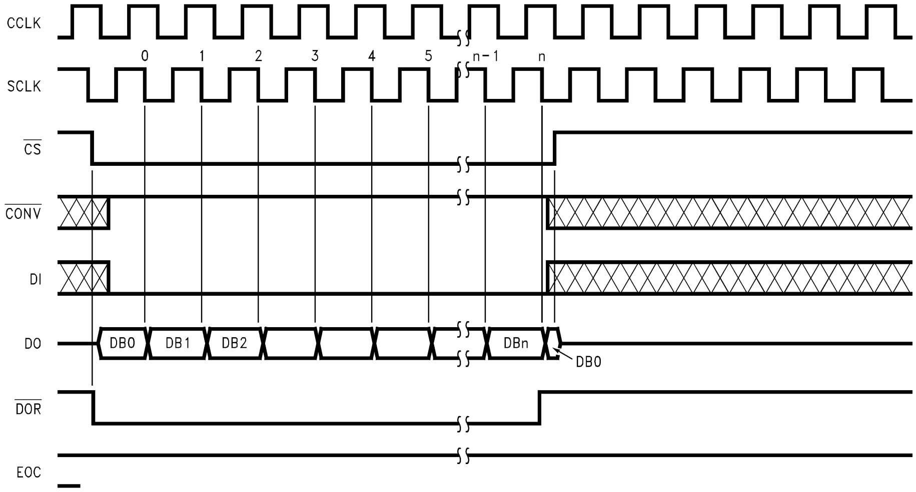


Figure 17.
ADC12L038 Read Data without Starting a Conversion with $\overline{CS}$ Continuously Low

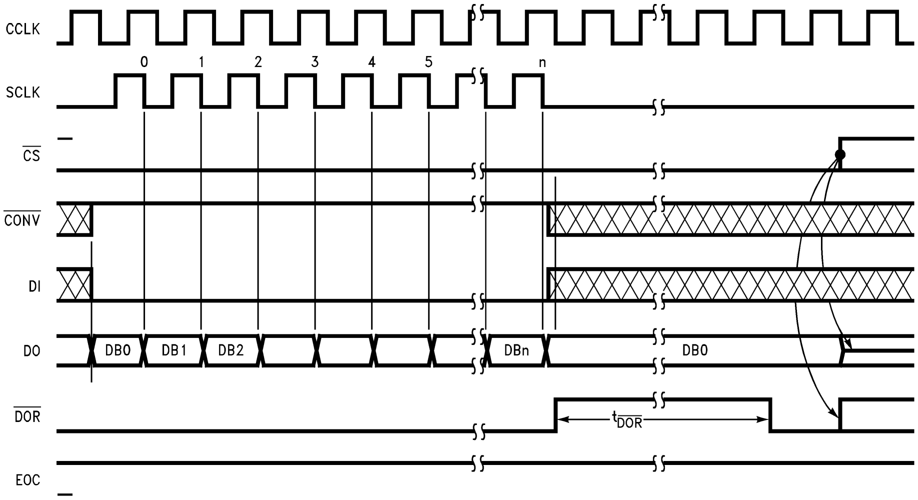


Figure 18.
ADC12L038 Conversion Using $\overline{CS}$ with 8-Bit Digital Output Format

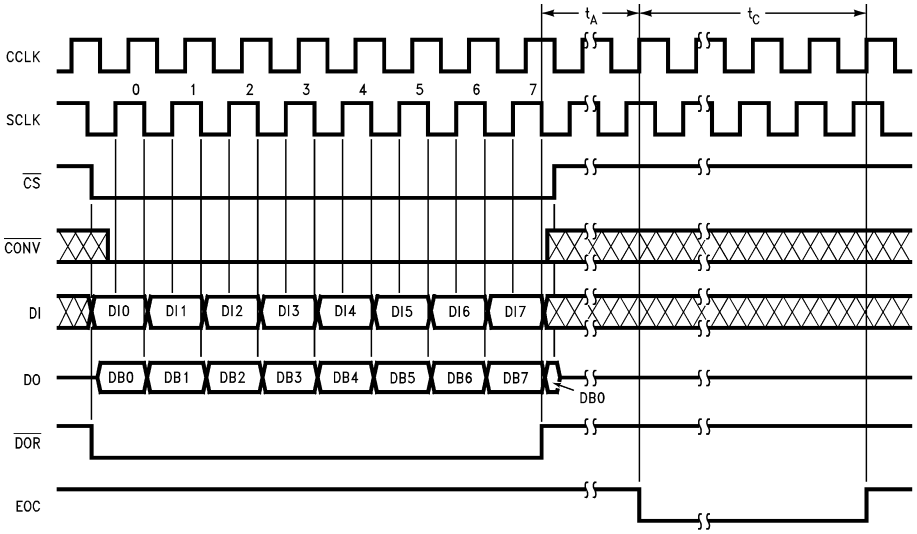


Figure 19.
ADC12L038 Conversion Using $\overline{CS}$ with 16-Bit Digital Output Format

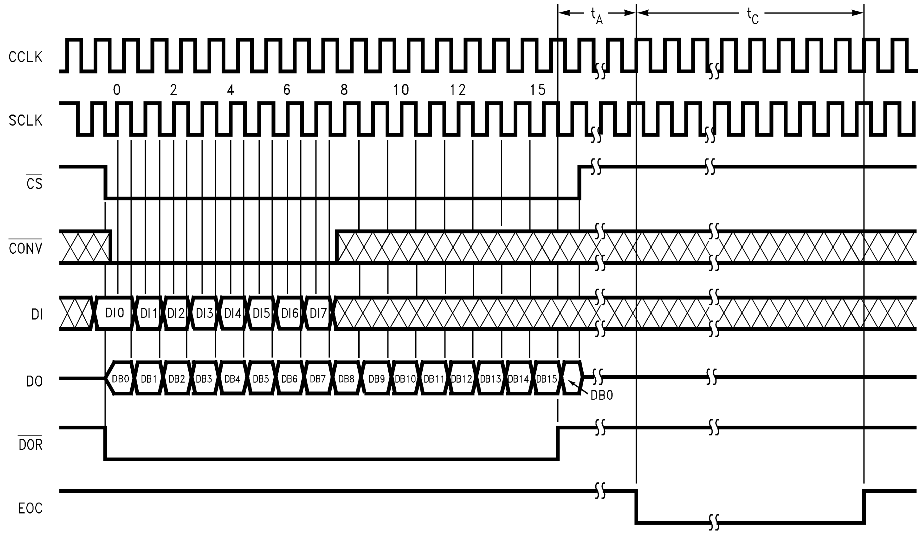


Figure 20.
ADC12L038 Conversion with $\overline{CS}$ Continuously Low and 8-Bit Digital Output Format

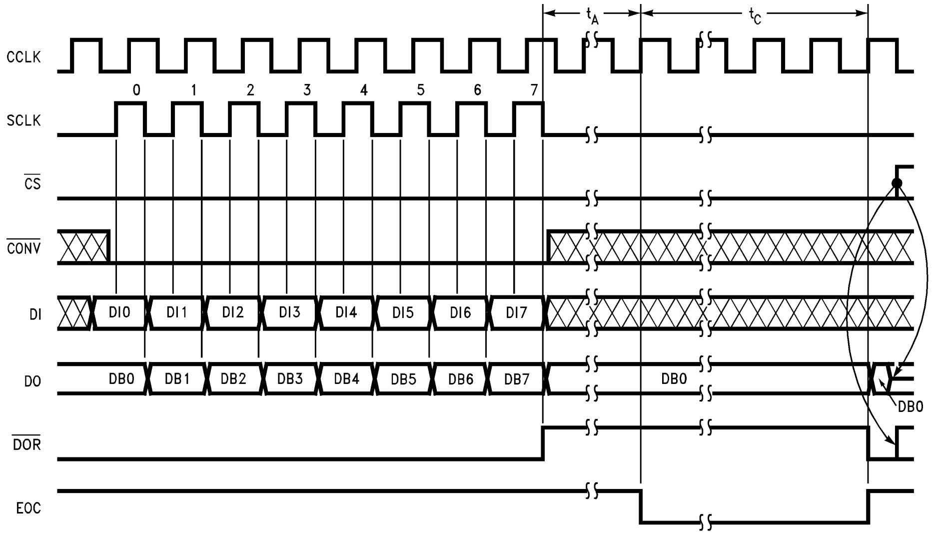


Figure 21.
ADC12L038 Conversion with $\overline{CS}$ Continuously Low and 16-Bit Digital Output Format

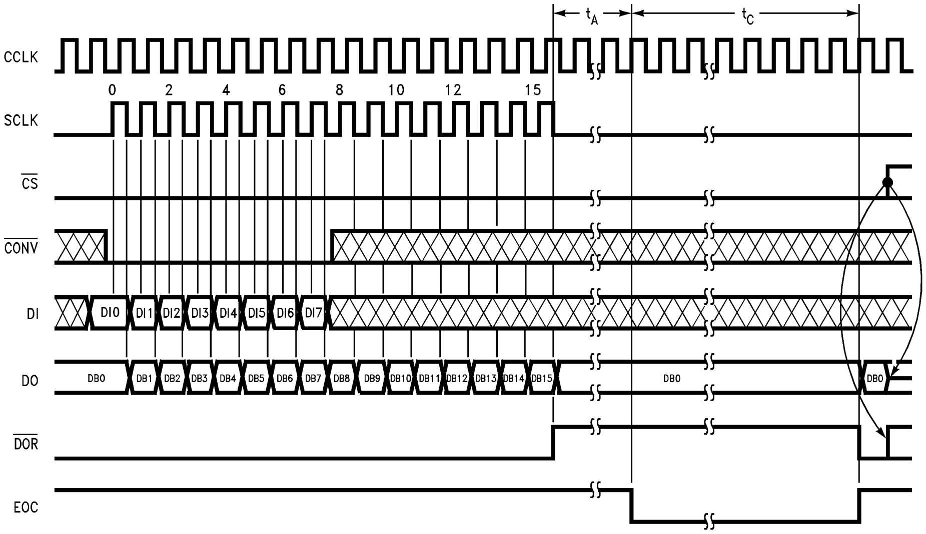


Figure 22.
ADC12L038 Software Power Up/Down Using $\overline{CS}$ with 16-Bit Digital Output Format

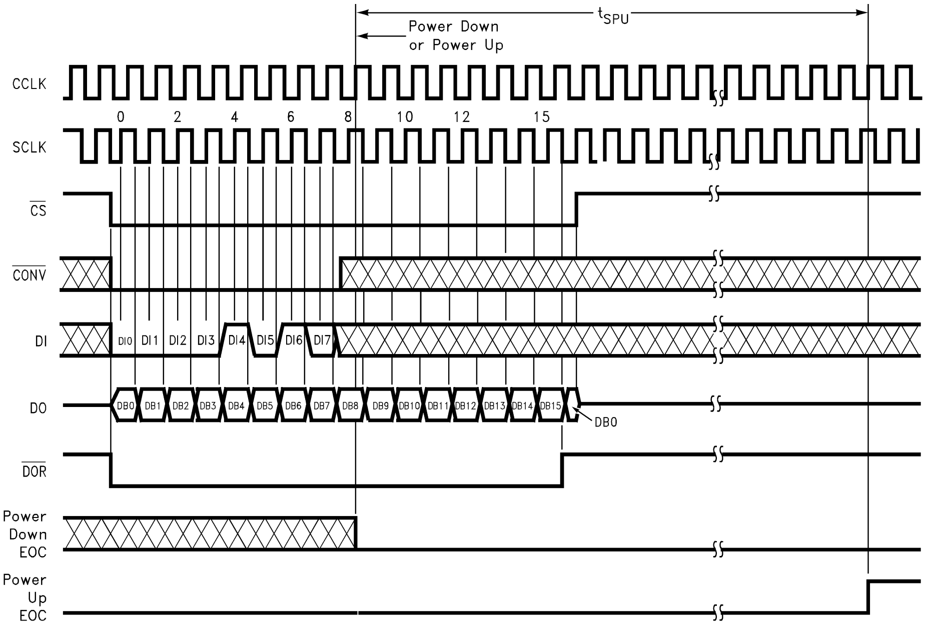


Figure 23.
ADC12L038 Software Power Up/Down with $\overline{CS}$ Continuously Low and 16-Bit Digital Output Format

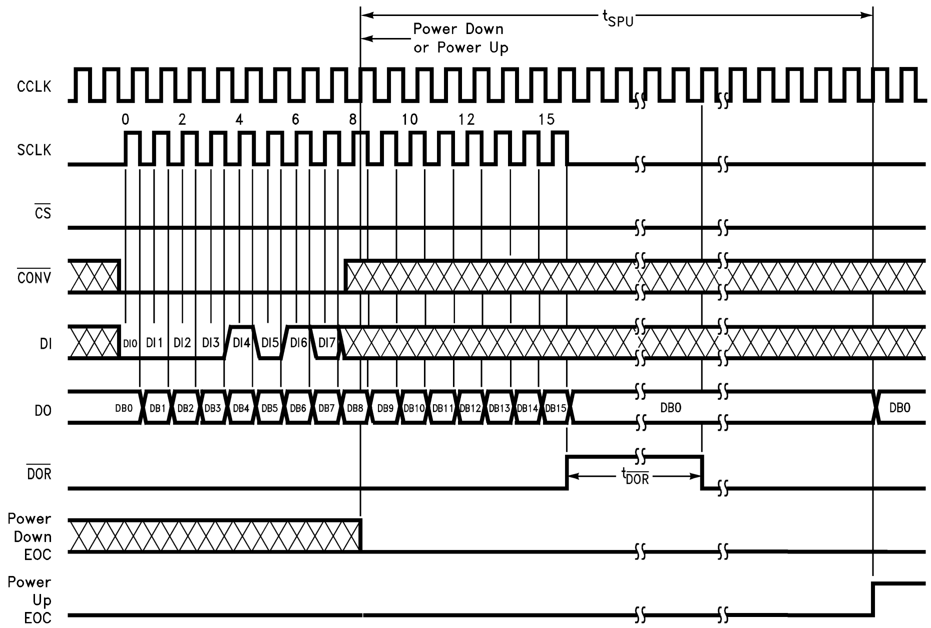
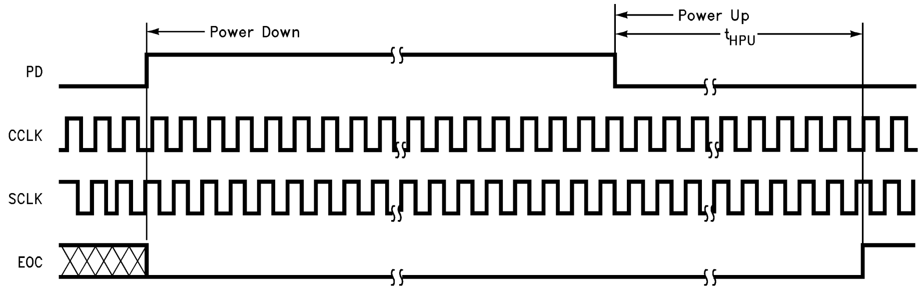
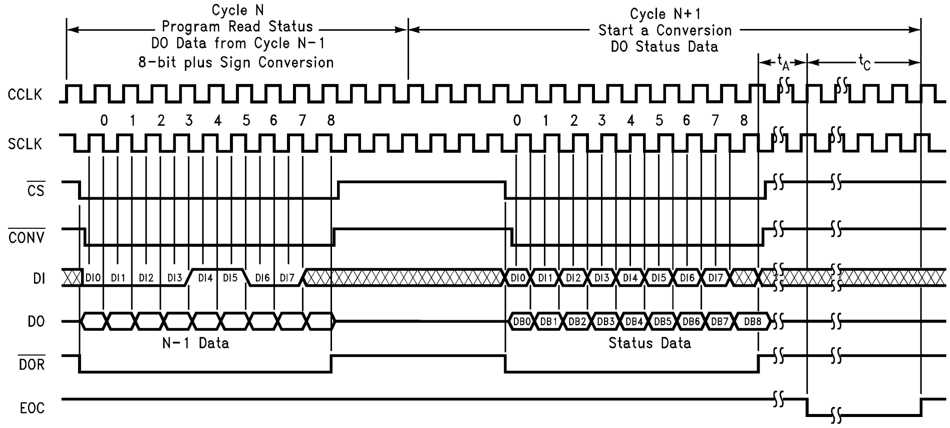


Figure 24.
ADC12L038 Hardware Power Up/Down

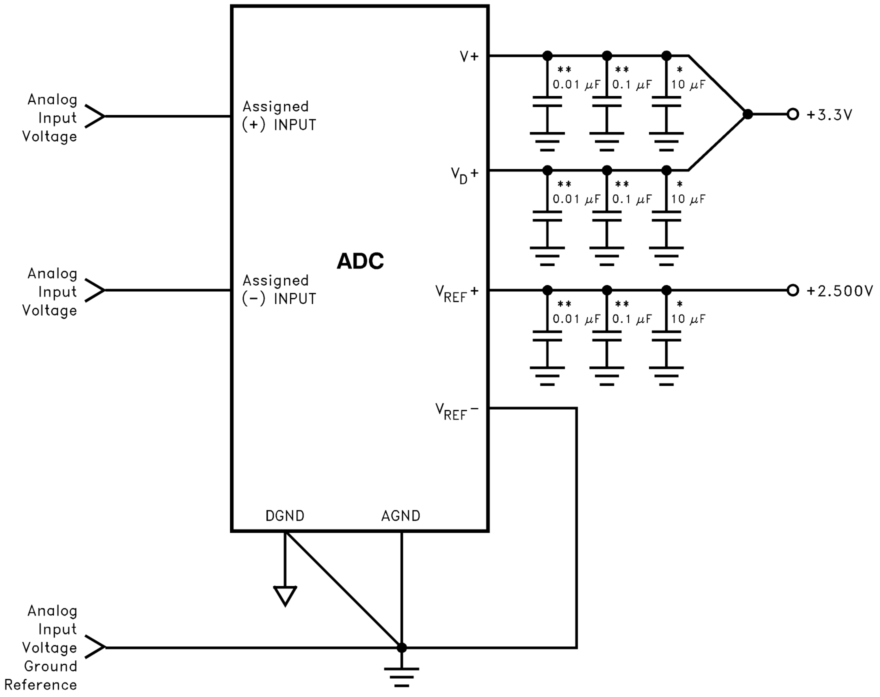


Note: Hardware power up/down may occur at any time. If PD is high while a conversion is in progress that conversion will be corrupted and erroneous data will be stored in the output shift register.

Figure 25.
ADC12L038 Configuration Modification—Example of a Status Read



Note: In order for all 9 bits of status information to be accessible the last conversion programmed before Cycle N needs to have a resolution of 8 bits plus sign, 12 bits, 12 bits plus sign, or greater.



*Tantalum

**Monolithic Ceramic or better

Figure 26. Recommended Power Supply Bypassing and Grounding

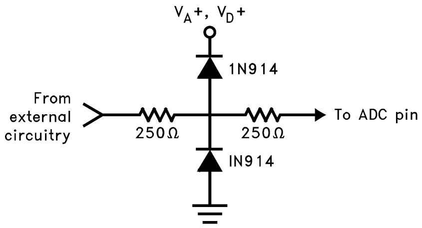


Figure 27. Protecting the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 Analog Pins

Format and Set-Up Tables

Table 2. Data Out Formats[1]

DO Formats			DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	DB16
with Sign	MSB First	17 Bits	X	X	X	X	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB
		13 Bits	Sign	MSB	10	9	8	7	6	5	4	3	2	1	LSB				
		9 Bits	Sign	MSB	6	5	4	3	2	1	LSB								
	LSB First	17 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign	X	X	X	X
		13 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	Sign				
		9 Bits	LSB	1	2	3	4	5	6	MSB	Sign								

---

(1) X = High or Low state.

Table 2. Data Out Formats[(1)] (continued)

DO Formats			DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	DB16
without Sign	MSB First	16 Bits	0	0	0	0	MSB	10	9	8	7	6	5	4	3	2	1	LSB	
		12 Bits	MSB	10	9	8	7	6	5	4	3	2	1	LSB					
		8 Bits	MSB	6	5	4	3	2	1	LSB									
	LSB First	16 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB	0	0	0	0	
		12 Bits	LSB	1	2	3	4	5	6	7	8	9	10	MSB					
		8 Bits	LSB	1	2	3	4	5	6	MSB									

Table 3. ADC12L038 Multiplexer Addressing

MUX Address				Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2									A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	**DI1**	**DI2**	**DI3**	**CH 0**	**CH 1**	**CH 2**	**CH 3**	**CH 4**	**CH 5**	**CH 6**	**CH 7**	**COM**	**A/DIN1**	**A/DIN2**	**MUXOUT1**	**MUXOUT2**	
L	L	L	L	+	−								+	−	CH0	CH1	Differential
L	L	L	H			+	−						+	−	CH2	CH3	
L	L	H	L					+	−				+	−	CH4	CH5	
L	L	H	H							+	−		+	−	CH6	CH7	
L	H	L	L	−	+								−	+	CH0	CH1	
L	H	L	H			−	+						−	+	CH2	CH3	
L	H	H	L					−	+				−	+	CH4	CH5	
L	H	H	H							−	+		−	+	CH6	CH7	
H	L	L	L	+								−	+	−	CH0	COM	Single-Ended
H	L	L	H			+						−	+	−	CH2	COM	
H	L	H	L					+				−	+	−	CH4	COM	
H	L	H	H							+		−	+	−	CH6	COM	
H	H	L	L		+							−	+	−	CH1	COM	
H	H	L	H				+					−	+	−	CH3	COM	
H	H	H	L						+			−	+	−	CH5	COM	
H	H	H	H								+	−	+	−	CH7	COM	

Table 4. ADC12L034 Multiplexer Addressing

MUX Address			Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2					A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	**DI1**	**DI2**	**CH0**	**CH1**	**CH2**	**CH3**	**COM**	**A/DIN1**	**A/DIN2**	**MUXOUT1**	**MUXOUT2**	
L	L	L	+	−				+	−	CH0	CH1	Differential
L	L	H			+	−		+	−	CH2	CH3	
L	H	L	−	+				−	+	CH0	CH1	
L	H	H			−	+		−	+	CH2	CH3	
H	L	L	+				−	+	−	CH0	COM	Single-Ended
H	L	H			+		−	+	−	CH2	COM	
H	H	L		+			−	+	−	CH1	COM	
H	H	H				+	−	+	−	CH3	COM	

Table 5. ADC12L032 and ADC12L030 Multiplexer Addressing

MUX Address		Analog Channel Addressed and Assignment with A/DIN1 tied to MUXOUT1 and A/DIN2 tied to MUXOUT2			A/D Input Polarity Assignment		Multiplexer Output Channel Assignment		Mode
DI0	**DI1**	**CH0**	**CH1**	**COM**	**A/DIN1**	**A/DIN2**	**MUXOUT1**	**MUXOUT2**	
L	L	+	−		+	−	CH0	CH1	Differential
L	H	−	+		−	+	CH0	CH1	
H	L	+		−	+	−	CH0	COM	Single-Ended
H	H		+	−	+	−	CH1	COM	

The ADC12L030 does not have A/DIN1, A/DIN2, MUXOUT1 and MUXOUT2 pins.

Table 6. Mode Programming[1]

ADC12L038	**DI0**	**DI1**	**DI2**	**DI3**	**DI4**	**DI5**	**DI6**	**DI7**	**Mode Selected (Current)**	**DO Format (next Conversion Cycle)**
ADC12L034	**DI0**	**DI1**	**DI2**		**DI3**	**DI4**	**DI5**	**DI6**		
ADC12L030 and ADC12L032	**DI0**	**DI1**			**DI2**	**DI3**	**DI4**	**DI5**		
	See Table 3, Table 4, and Table 5				L	L	L	L	12 Bit Conversion	12 or 13 Bit MSB First
	See Table 3, Table 4, and Table 5				L	L	L	H	12 Bit Conversion	16 or 17 Bit MSB First
	See Table 3, Table 4, and Table 5				L	L	H	L	8 Bit Conversion	8 or 9 Bit MSB First
	L	L	L	L	L	L	H	H	12 Bit Conversion of Full-Scale	12 or 13 Bit MSB First
	See Table 3, Table 4, and Table 5				L	H	L	L	12 Bit Conversion	12 or 13 Bit LSB First
	See Table 3, Table 4, and Table 5				L	H	L	H	12 Bit Conversion	16 or 17 Bit LSB First
	See Table 3, Table 4, and Table 5				L	H	H	L	8 Bit Conversion	8 or 9 Bit LSB First
	L	L	L	L	L	H	H	H	12 Bit Conversion of Offset	12 or 13 Bit LSB First
	L	L	L	L	H	L	L	L	Auto-Cal	No Change
	L	L	L	L	H	L	L	H	Auto-Zero	No Change
	L	L	L	L	H	L	H	L	Power Up	No Change
	L	L	L	L	H	L	H	H	Power Down	No Change
	L	L	L	L	H	H	L	L	Read Status Register	No Change
	L	L	L	L	H	H	L	H	Data Out without Sign	No Change
	H	L	L	L	H	H	L	H	Data Out with Sign	No Change
	L	L	L	L	H	H	H	L	Acquisition Time—6 CCLK Cycles	No Change
	L	H	L	L	H	H	H	L	Acquisition Time—10 CCLK Cycles	No Change
	H	L	L	L	H	H	H	L	Acquisition Time—18 CCLK Cycles	No Change
	H	H	L	L	H	H	H	L	Acquisition Time—34 CCLK Cycles	No Change
	L	L	L	L	H	H	H	H	User Mode	No Change
	H	X	X	X	H	H	H	H	Test Mode (CH1–CH7 become Active Outputs)	No Change

(1) X = Don't Care

The A/D powers up with no Auto-Cal, no Auto-Zero, 10 CCLK acquisition time, 12-bit + sign conversion, power up, 12- or 13-bit MSB first and user mode.

Table 7. Conversion/Read Data Only Mode Programming(1)

$\overline{\text{CS}}$	$\overline{\text{CONV}}$	PD	Mode
L	L	L	See Table 6 for Mode
L	H	L	Read Only (Previous DO Format) No Conversion
H	X	L	Idle
X	X	H	Power Down

(1) X = Don't Care

Table 8. Status Register

Status Bit Location	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
Status Bit	**PU**	**PD**	**Cal**	**8 or 9**	**12 or 13**	**16 or 17**	**Sign**	**Justification**	**Test Mode**
	Device Status			**DO Output Format Status**					
Function	“High” indicates a Power Up Sequence is in progress	“High” indicates a Power Down Sequence is in progress	“High” indicates an Auto-Cal Sequence is in progress	“High” indicates an 8 or 9 bit format	“High” indicates a 12 or 13 bit format	“High” indicates a 16 or 17 bit format	“High” indicates that the sign bit is included. When “Low” the sign bit is not included.	When “High” the conversion result will be output MSB first. When “Low” the result will be output LSB first.	When “High” the device is in test mode. When “Low” the device is in user mode.

APPLICATION INFORMATION

DIGITAL INTERFACE

Interface Concepts

The example in Figure 28 shows a typical sequence of events after the power is applied to the ADC12L030/2/4/8:

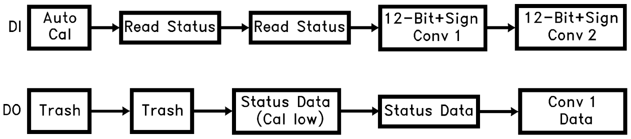


Figure 28. Typical Power Supply Power Up Sequence

The first instruction input to the A/D via DI initiates Auto-Cal. The data output on DO at that time is meaningless and is completely random. To determine whether the Auto-Cal has been completed, a read status instruction is issued to the A/D. Again the data output at that time has no significance since the Auto-Cal procedure modifies the data in the output shift register. To retrieve the status information, an additional read status instruction is issued to the A/D. At this time the status data is available on DO. If the Cal signal in the status word is low Auto-Cal has been completed. Therefore, the next instruction issued can start a conversion. The data output at this time is again status information. To keep noise from corrupting the A/D conversion, the status can not be read during a conversion. If $\overline{\text{CS}}$ is brought low during a conversion, that conversion is prematurely ended. EOC can be used to determine the end of a conversion or the A/D controller can keep track in software of when it would be appropriate to communicate to the A/D again. Once it has been determined that the A/D has completed a conversion another instruction can be transmitted to the A/D. The data from this conversion can be accessed when the next instruction is issued to the A/D.

Note, when $\overline{\text{CS}}$ is low continuously it is important to transmit the exact number of SCLK cycles, as shown in the timing diagrams. Not doing so will desynchronize the serial communication to the A/D (see $\overline{\text{CS}}$ Low Continuously Considerations).

Changing Configuration

The configuration of the ADC12L030/2/4/8 on power up defaults to 12-bit plus sign resolution, 12- or 13-bit MSB First, 10 CCLK acquisition time, user mode, no Auto-Cal, no Auto-Zero, and power up mode. Changing the acquisition time and turning the sign bit on and off requires an 8-bit instruction to be issued to the ADC. This instruction will not start a conversion. The instructions that select a multiplexer address and format the output data do start a conversion. Figure 29 describes an example of changing the configuration of the ADC12L030/2/4/8.

During I/O sequence 1, the instruction at DI configures the ADC12L030/2/4/8 to do a conversion with 12-bit +sign resolution. Notice that when the 6 CCLK Acquisition and Data Out without Sign instructions are issued to the ADC, I/O sequences 2 and 3, a new conversion is not started. The data output during these instructions is from conversion N which was started during I/O sequence 1. The Configuration Modification timing diagram describes in detail the sequence of events necessary for a Data Out without Sign, Data Out with Sign, or 6/10/18/34 CCLK Acquisition time mode selection. Table 6 describes the actual data necessary to be input to the ADC to accomplish this configuration modification. The next instruction, shown in Figure 29, issued to the A/D starts conversion N+1 with 8 bits of resolution formatted MSB first. Again the data output during this I/O cycle is the data from conversion N.

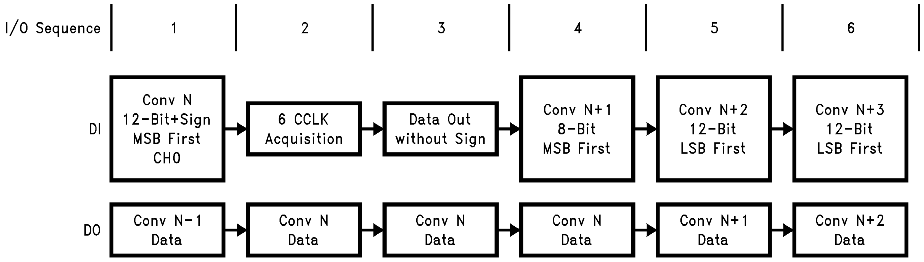


Figure 29. Changing the ADC's Conversion Configuration

The number of SCLKs applied to the A/D during any conversion I/O sequence should vary in accord with the data out word format chosen during the previous conversion I/O sequence. The various formats and resolutions available are shown in Table 2. In Figure 29, since 8-bit without sign MSB first format was chosen during I/O sequence 4, the number of SCLKs required during I/O sequence 5 is 8. In the following I/O sequence the format changes to 12-bit without sine MSB first; therefore the number of SCLKs required during I/O sequence 6 changes accordingly to 12.

$\overline{\text{CS}}$ Low Continuously Considerations

When $\overline{\text{CS}}$ is continuously low, it is important to transmit the exact number of SCLK pulses that the ADC expects. Not doing so will desynchronize the serial communications to the ADC. When the supply power is first applied to the ADC, it will expect to see 13 SCLK pulses for each I/O transmission. The number of SCLK pulses that the ADC expects to see is the same as the digital output word length. The digital output word length is controlled by the Data Out (DO) format. The DO format maybe changed any time a conversion is started or when the sign bit is turned on or off. The following table details out the number of clock periods required for different DO formats:

DO Format		Number of SCLKs Expected
8-Bit MSB or LSB First	SIGN OFF	8
	SIGN ON	9
12-Bit MSB or LSB First	SIGN OFF	12
	SIGN ON	13
16-Bit MSB or LSB first	SIGN OFF	16
	SIGN ON	17

If erroneous SCLK pulses desynchronize the communications, the simplest way to recover is by cycling the power supply to the device. Not being able to easily resynchronize the device is a shortcoming of leaving $\overline{\text{CS}}$ low continuously.

The number of clock pulses required for an I/O exchange may be different for the case when $\overline{\text{CS}}$ is left low continuously vs. the case when $\overline{\text{CS}}$ is cycled. Take the I/O sequence detailed in Figure 28 (Typical Power Supply Sequence) as an example. The following table lists the number of SCLK pulses required for each instruction:

Instruction	$\overline{\text{CS}}$ Low Continuously	$\overline{\text{CS}}$ Strobed
Auto-Cal	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
Read Status	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 1	13 SCLKs	8 SCLKs
12-Bit + Sign Conv 2	13 SCLKs	13 SCLKs

Analog Input Channel Selection

The data input on DI also selects the channel configuration for a particular A/D conversion (See Table 3, Table 4, Table 5, and Table 6). In Figure 29 the only times when the channel configuration could be modified would be during I/O sequences 1, 4, 5 and 6. Input channels are reselected before the start of each new conversion. Shown below is the data bit stream required on DI, during I/O sequence number 4 in Figure 29, to set CH1 as the positive input and CH0 as the negative input for the different versions of ADCs:

Part Number	**DI Data**[1]							
	DI0	**DI1**	**DI2**	**DI3**	**DI4**	**DI5**	**DI6**	**DI7**
ADC12L030	L	H	L	L	H	L	X	X
ADC12L032	L	H	L	L	H	L	X	X
ADC12L034	L	H	L	L	L	H	L	X
ADC12L038	L	H	L	L	L	L	H	L

(1) Where X can be a logic high (H) or low (L).

Power Up/Down

The ADC may be powered down by taking the PD pin HIGH or by the instruction input on DI (see Table 6 and Table 7, and the Power Up/Down Timing Diagrams). When the ADC is powered down in this way, the A/D conversion circuitry is deactivated, but the digital I/O circuitry is kept active. Hardware power up/down is controlled by the state of the PD pin. Software power up/down is controlled by the instruction issued to the ADC. If a software power up instruction is issued to the ADC while a hardware power down is in effect (PD pin high) the device will remain in the power-down state. If a software power down instruction is issued to the ADC while a hardware power up is in effect (PD pin low), the device will power down. When the device is powered down by software, it may be powered up by either issuing a software power up instruction or by taking PD pin high and then low. If the power down command is issued during an A/D conversion, that conversion is disrupted. Therefore, the data output after power up cannot be relied on.

User Mode and Test Mode

An instruction may be issued to the ADC to put it into test mode, which is used by the manufacturer to verify complete functionality of the device. During test mode CH0–CH7 become active outputs. If the device is inadvertently put into the test mode with $\overline{\text{CS}}$ low continuously, the serial communications may be desynchronized. Synchronization may be regained by cycling the power supply voltage to the device. Cycling the power supply voltage will also set the device into user mode. If $\overline{\text{CS}}$ is used in the serial interface, the ADC may be queried to see what mode it is in. This is done by issuing a “read STATUS register” instruction to the ADC. When bit 9 of the status register is high the ADC is in test mode; when bit 9 is low the ADC is in user mode. As an alternative to cycling the power supply, an instruction sequence may be used to return the device to user mode. This instruction sequence must be issued to the ADC using $\overline{\text{CS}}$. The following table lists the instructions required to return the device to user mode. Note that this **entire sequence**, including both Test Mode and User Mode values, should be sent to recover from the test mode.

Instruction	**DI Data**[1]							
	DI0	**DI1**	**DI2**	**DI3**	**DI4**	**DI5**	**DI6**	**DI7**
TEST MODE	H	X	X	X	H	H	H	H
Reset Test Mode Instructions	L	L	L	L	H	H	H	L
	L	L	L	L	H	L	H	L
	L	L	L	L	H	L	H	H
USER MODE	L	L	L	L	H	H	H	H
Power Up	L	L	L	L	H	L	H	L
Set DO with or without Sign	H or L	L	L	L	H	H	L	H
Set Acquisition Time	H or L	H or L	L	L	H	H	H	L
Start a Conversion	H or L	H or L	H or L	H or L	L	H or L	H or L	H or L

(1) X = Don't Care

Reading the Data Without Starting a Conversion

The data from a particular conversion may be accessed without starting a new conversion by ensuring that the $\overline{\text{CONV}}$ line is taken high during the I/O sequence. See the Read Data Timing Diagrams. Table 7 describes the operation of the $\overline{\text{CONV}}$ pin.

DESCRIPTION OF THE ANALOG MULTIPLEXER

For the ADC12L038, the analog input multiplexer can be configured with 4 differential channels or 8 single ended channels with the COM input as the zero reference or any combination thereof (see Figure 30). The difference between the voltages on the V_{REF}^+ and V_{REF}^- pins determines the input voltage span (V_{REF}). The analog input voltage range is 0 to V_A^+. Negative digital output codes result when $V_{IN}^- > V_{IN}^+$. The actual voltage at V_{IN}^- or V_{IN}^+ cannot go below AGND.

CH0, CH2, CH4, and CH6 can be assigned to the MUXOUT1 pin in the differential configuration, while CH1, CH3, CH5, and CH7 can be assigned to the MUXOUT2 pin. In the differential configuration, the analog inputs are paired as follows: CH0 with CH1, CH2 with CH3, CH4 with CH5 and CH6 with CH7. The A/DIN1 and A/DIN2 pins can be assigned positive or negative polarity.

With the single-ended multiplexer configuration CH0 through CH7 can be assigned to the MUXOUT1 pin. The COM pin is always assigned to the MUXOUT2 pin. A/DIN1 is assigned as the positive input; A/DIN2 is assigned as the negative input. (See Figure 31)

The Multiplexer assignment tables for the ADC12L030,2,4,8 (Table 3, Table 4, and Table 5) summarize the aforementioned functions for the different versions of A/Ds.

Figure 30.

A/DIN1 and A/DIN2 can be assigned as the + or − input

A/DIN1 is + input

A/DIN2 is − input

Figure 31.

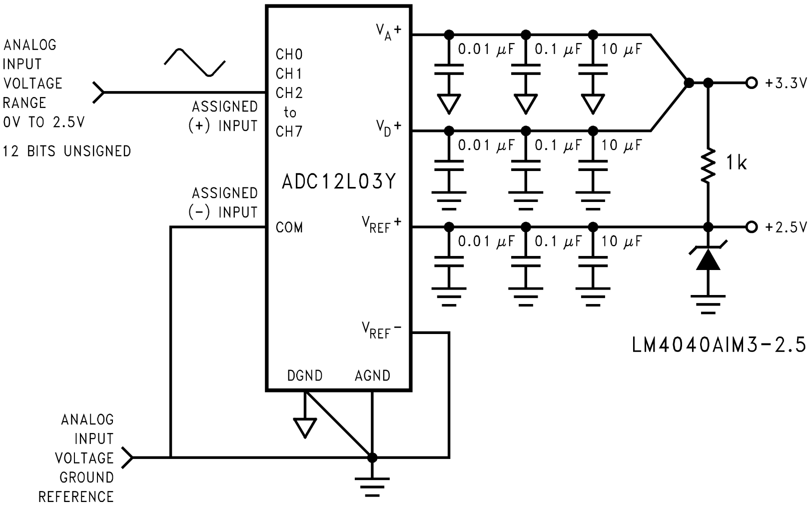


Figure 32. Single-Ended Biasing

Biasing for Various Multiplexer Configurations

Figure 32 is an example of biasing the device for single-ended operation. The sign bit is always low. The digital output range is 0 0000 0000 0000 to 0 1111 1111 1111. One LSB is equal to 610 µV (2.5V/4096 LSBs).

For pseudo-differential signed operation the biasing circuit shown in Figure 34 shows a signal AC coupled to the ADC. This gives a digital output range of −4096 to +4095. With a 1.25V reference, 1 LSB is equal to 305 µV. Although the ADC is not production tested with a 1.25V reference, linearity error typically will not change more than 0.3 LSB. With the ADC set to an acquisition time of 10 clock periods the input biasing resistor needs to be 600Ω or less. Notice though that the input coupling capacitor needs to be made fairly large to bring down the high pass corner. Increasing the acquisition time to 34 clock periods (with a 5 MHz CCLK frequency) would allow the 600Ω to increase to 6k, which with a 1 µF coupling capacitor would set the high pass corner at 26 Hz. The value of R1 will depend on the value of R2.

An alternative method for biasing pseudo-differential operation is to use the +1.25V from the LM4040 to bias any amplifier circuits driving the ADC as shown in Figure 33. The value of the resistor pull-up biasing the LM4040-2.5 will depend upon the current required by the op amp biasing circuitry.

Fully differential operation is shown in Figure 35. One LSB for this case is equal to (2.5V/4096) = 610 mV.

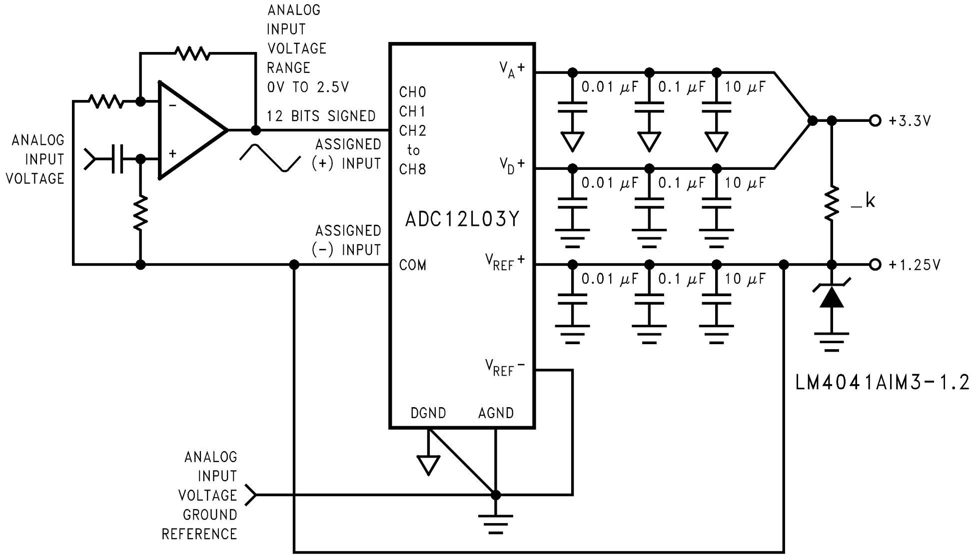


Figure 33. Alternative Pseudo-Differential Biasing

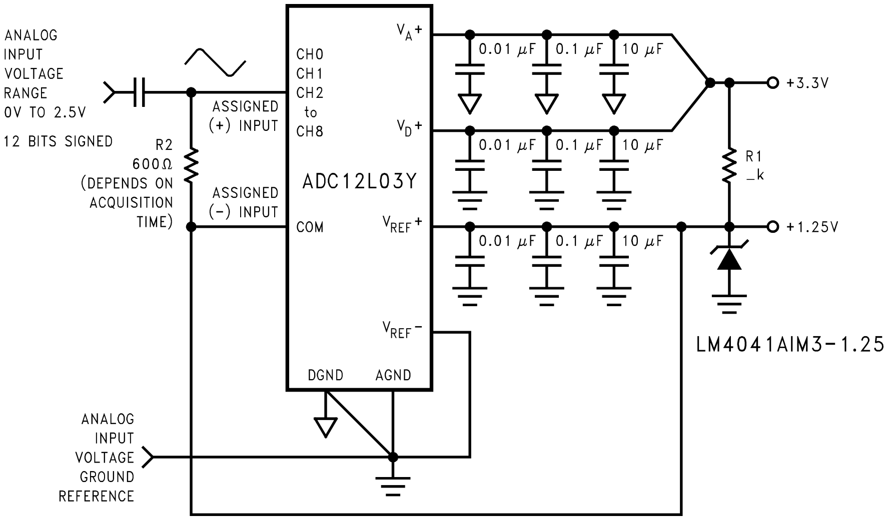


Figure 34. Pseudo-Differential Biasing with the Signal Source AC Coupled Directly into the ADC

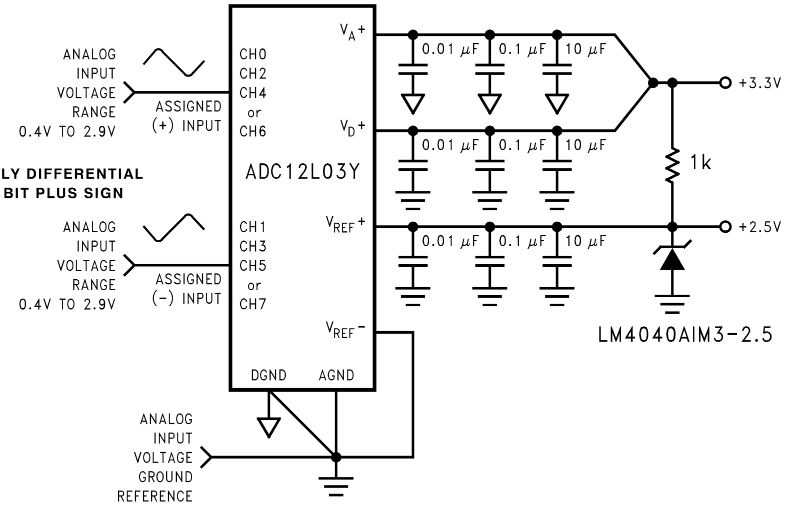


Figure 35. Fully Differential Biasing

REFERENCE VOLTAGE

The difference in the voltages applied to the V_{REF}^+ and V_{REF}^- defines the analog input span (the difference between the voltage applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground), over which 4095 positive and 4096 negative codes exist. The voltage sources driving V_{REF}^+ or V_{REF}^- must have very low output impedance and noise.

The ADC12L030/2/4/8 can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the V_{REF}^+ pin is connected to V_A^+ and V_{REF}^- is connected to ground. This technique relaxes the system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions. For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

Below are recommended references along with some key specifications.

Part Number	Output Voltage Tolerance	Temperature Coefficient (max)
LM4041CIM3-Adj	±0.5%	±100ppm/°C
LM4040AIM3-2.5	±0.1%	±100ppm/°C
LM4050AIM3-2.5	±0.1%	±50ppm/°C

The reference voltage inputs are not fully differential. The ADC12L030/2/4/8 will not generate correct conversions or comparisons if V_{REF}^+ is taken below V_{REF}^-. Correct conversions result when V_{REF}^+ and V_{REF}^- differ by 1V and remain, at all times, between ground and V_A^+. The V_{REF} common mode range, $(V_{REF}^+ + V_{REF}^-)/2$, is restricted to $(0.1 \times V_A^+)$ to $(0.6 \times V_A^+)$. Therefore, with $V_A^+ = 3.3V$ the center of the reference ladder should not go below 0.33V or above 1.98V. Figure 36 is a graphic representation of the voltage restrictions on V_{REF}^+ and V_{REF}^-.

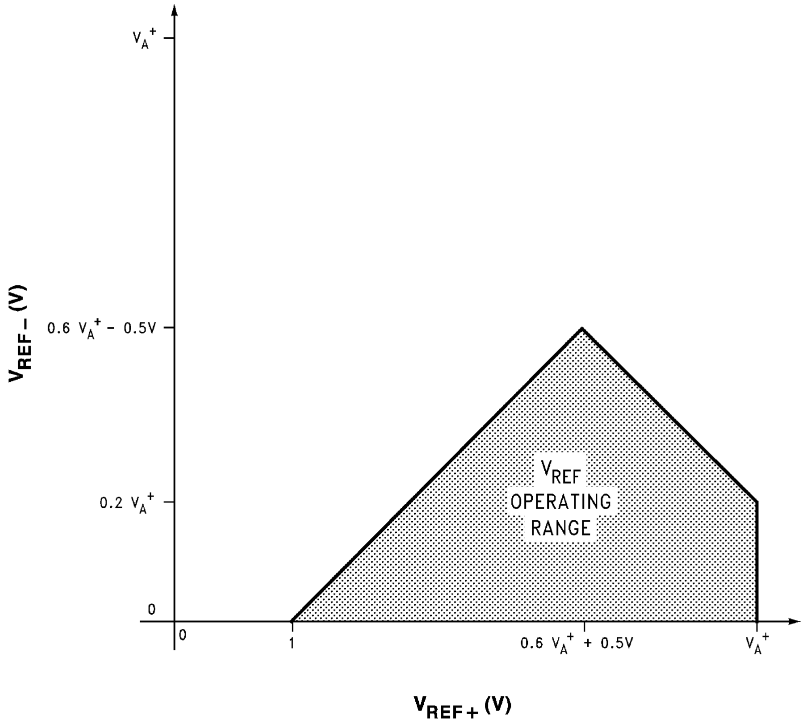


Figure 36. V_{REF} Operating Range

ANALOG INPUT VOLTAGE RANGE

The ADC12L030/2/4/8's fully differential ADC generate a two's complement output that is found by using the equations shown below:

for (12-bit) resolution the Output Code =

$$\frac{(V_{IN}{}^{+} - V_{IN}{}^{-})\ (4096)}{(V_{REF}{}^{+} - V_{REF}{}^{-})} \quad (1)$$

for (8-bit) resolution the Output Code =

$$\frac{(V_{IN}{}^{+} - V_{IN}{}^{-})\ (256)}{(V_{REF}{}^{+} - V_{REF}{}^{-})} \quad (2)$$

Round off to the nearest integer value between −4096 to 4095 for 12-bit resolution and between −256 to 255 for 8-bit resolution if the result of the above equation is not a whole number.

Examples are shown in the table below:

V_{REF}^+	V_{REF}^-	V_{IN}^+	V_{IN}^-	Digital Output Code
+2.5V	+1V	+1.5V	0V	0,1111,1111,1111
+2.500V	0V	+2V	0V	0,1100,1100,1101
+2.500V	0V	+2.499V	+2.500V	1,1111,1111,1111
+2.500V	0V	0V	+2.500V	1,0000,0000,0000

INPUT CURRENT

At the start of the acquisition window (t_A) a charging current flows into or out of the analog input pins (A/DIN1 and A/DIN2) depending on the input voltage polarity. The analog input pins are CH0–CH7 and COM when A/DIN1 is tied to MUXOUT1 and A/DIN2 is tied to MUXOUT2. The peak value of this input current will depend on the actual input voltage applied, the source impedance and the internal multiplexer switch on resistance. With MUXOUT1 tied to A/DIN1 and MUXOUT2 tied to A/DIN2 the internal multiplexer switch on resistance is typically 1.6 kΩ. The A/DIN1 and A/DIN2 mux on resistance is typically 750Ω.

INPUT SOURCE RESISTANCE

For low impedance voltage sources (<600Ω), the input charging current will decay, before the end of the S/H's acquisition time of 2 µs (10 CCLK periods with f_C = 5 MHz), to a value that will not introduce any conversion errors. For high source impedances, the S/H's acquisition time can be increased to 18 or 34 CCLK periods. For less ADC resolution and/or slower CCLK frequencies the S/H's acquisition time may be decreased to 6 CCLK periods. To determine the number of clock periods (N_c) required for the acquisition time with a specific source impedance for the various resolutions the following equations can be used:

12 Bit + Sign $N_C = [R_S + 2.3] \times f_C \times 0.824$

8 Bit + Sign $N_C = [R_S + 2.3] \times f_C \times 0.57$

Where f_C is the conversion clock (CCLK) frequency in MHz and R_S is the external source resistance in kΩ. As an example, operating with a resolution of 12 Bits+sign, a 5 MHz clock frequency and maximum acquisition time of 34 conversion clock periods the ADC's analog inputs can handle a source impedance as high as 6 kΩ. The acquisition time may also be extended to compensate for the settling or response time of external circuitry connected between the MUXOUT and A/DIN pins.

An acquisition is started by a falling edge of SCLK and ends with a rising edge of CCLK (see Timing Diagrams). If SCLK and CCLK are asynchronous one extra CCLK clock period may be inserted into the programmed acquisition time for synchronization. Therefore, with asynchronous SCLK and CCLK, the acquisition time will change from conversion to conversion.

INPUT BYPASS CAPACITANCE

External capacitors (0.01 µF–0.1 µF) can be connected between the analog input pins, CH0–CH7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. These capacitors will not degrade the conversion accuracy.

NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

POWER SUPPLIES

Noise spikes on the V_A^+ and V_D^+ supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any power supply spikes that occur during the auto-zero or linearity correction. The minimum power supply bypassing capacitors recommended are low inductance tantalum capacitors of 10 µF or greater paralleled with 0.1 µF monolithic ceramic capacitors. More or different bypassing may be necessary depending on the overall system requirements. Separate bypass capacitors should be used for the V_A^+ and V_D^+ supplies and placed as close as possible to these pins.

GROUNDING

The ADC12L030/2/4/8's performance can be maximized through proper grounding techniques. These include the use of separate analog and digital areas of the board with analog and digital components and traces located only in their respective areas. Bypass capacitors of 0.01 µF and 0.1 µF surface mount capacitors and a 10 µF are recommended at each of the power supply pins for best performance. These capacitors should be located as close to the bypassed pin as practical, especially the smaller value capacitors.

CLOCK SIGNAL LINE ISOLATION

The ADC12L030/2/4/8's performance is optimized by routing the analog input/output and reference signal conductors as far as possible from the conductors that carry the clock signals to the CCLK and SCLK pins. Maintaining a separation of at least 7 to 10 times the height of the clock trace above its reference plane is recommended.

THE CALIBRATION CYCLE

A calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize after initial turn on. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full-scale, offset, and linearity errors down to the specified limits. Full-scale error typically changes ±0.4 LSB over temperature and linearity error changes even less; therefore it should be necessary to go through the calibration cycle only once after power up if the Power Supply Voltage and the ambient temperature do not change significantly (see the curves in Typical Performance Characteristics).

THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the auto-zero cycle can be used. It may be necessary to do an auto-zero cycle whenever the ambient temperature or the power supply voltage change significantly. (See the curves titled “Zero Error Change vs. Temperature” and “Zero Error Change vs. Supply Voltage” in Typical Performance Characteristics.)

DYNAMIC PERFORMANCE

Many applications require the A/D converter to digitize AC signals, but the standard DC integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with AC input signals. The important specifications for AC applications reflect the converter's ability to digitize AC signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise (S/N), signal-to-noise + distortion ratio (S/(N + D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's AC performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N + D) and S/N are calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/N are shown in the table of Electrical Characteristics, and spectral plots of S/(N + D) are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N + D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N + D) or S/N drops 3 dB).

Effective number of bits can also be useful in describing the A/D's noise and distortion performance. An ideal A/D converter will have some amount of quantization noise, determined by its resolution, and no distortion, which will yield an optimum S/(N + D) ratio given by the following equation:

$$S/(N + D) = (6.02 \times n + 1.76)\ \text{dB} \quad (3)$$

where "n" is the A/D's resolution in bits.

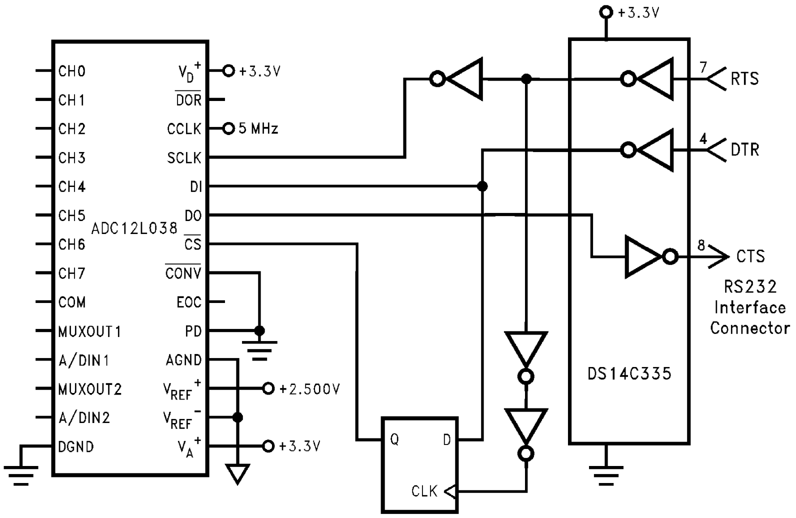
Since the ideal A/D converter has no distortion, the effective bits of a real A/D converter, therefore, can be found by::

$$n(\text{effective}) = \text{ENOB} = (S/(N + D) - 1.76 / 6.02 \quad (4)$$

As an example, this device with a ±2.5V, 10 kHz sine wave input signal will typically have a S/N of 78 dB, which is equivalent to 12.6 effective bits.

AN RS232 SERIAL INTERFACE

Shown below is a schematic for an RS232 interface to any IBM and compatible PCs. The DTR, RTS, and CTS RS232 signal lines are buffered via level translators and connected to the ADC12L038's DI, SCLK, and DO pins, respectively. The D flip flop drive the $\overline{\text{CS}}$ control line.



Note: V_A^+, V_D^+, and V_{REF}^+ on the ADC12L038 each have 0.01 µF and 0.1 µF chip caps, and 10 µF tantalum caps. All logic devices are bypassed with 0.1 µF caps. The DS14C335 has an internal DC-DC converter that generates the necessary TIA/EIA-232-E output levels from a 3.3V supply. There are four 0.47 µF capacitors required for the DC-DC converter that are not shown in the above schematic.

The assignment of the RS232 port is shown below

			B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
COM1	Input Address	3FE	X	X	X	CTS	X	X	X	X
	Output Address	3FC	X	X	X	0	X	X	RTS	DTR

A sample program, written in Microsoft™ QuickBasic, is shown on the next page. The program prompts for data mode select instruction to be sent to the A/D. This can be found from Table 6. The data should be entered in “1”s and “0”s as shown in the table with DI0 first. Next the program prompts for the number of SCLKs required for the programmed mode select instruction. For instance, to send all “0”s to the A/D, selects CH0 as the +input, CH1 as the −input, 12-bit conversion, and 13-bit MSB first data output format (if the sign bit was not turned off by a previous instruction). This would require 13 SCLK periods since the output data format is 13 bits. The device powers up with No Auto-Cal, No Auto-Zero, 10 CCLK Acquisition Time, 12-bit conversion, data out with sign, 12- or 13-bit MSB First, power up, and user mode. Auto-Cal, Auto-Zero, Power UP and Power Down instructions do not change these default settings. The following power up sequence should be followed:

1. Run the program
2. Prior to responding to the prompt apply the power to the ADC12L038
3. Respond to the program prompts

It is recommended that the first instruction issued to the ADC12L038 be Auto-Cal (see Interface Concepts).

```
'variables DOL=Data Out word length, DI=Data string for A/D DI input,
'          DO=A/D result string
'SET CS# HIGH
OUT &H3FC, (&H2 OR INP (&H3FC))            'set RTS HIGH
OUT &H3FC, (&HFE AND INP (&H3FC))          'SET DTR LOW
OUT &H3FC, (&HFD AND INP (&H3FC))          'SET RTS LOW

OUT &H3FC, (&HEF AND INP (&H3FC))          'set B4 low
10
LINE INPUT "DI data for ADC12038 (see Mode Table on data sheet)"; DI$
INPUT "ADC12038 output word length (8,9,12,13,16 or 17)"; DOL
20

'SET CS# HIGH
OUT &H3FC, (&H2 OR INP (&H3FC))            'set RTS HIGH
OUT &H3FC, (&HFE AND INP (&H3FC))          'SET DTR LOW
OUT &H3FC, (&HFD AND INP (&H3FC))          'SET RTS LOW

'SET CS# LOW
OUT &H3FC, (&H2 OR INP (&H3FC))            'set RTS HIGH
OUT &H3FC, (&H1 OR INP (&H3FC))            'SET DTR HIGH
OUT &H3FC, (&HFD AND INP (&H3FC))          'SET RTS LOW

DO$=""                                     'reset DO variable
  OUT &H3FC, (&H1 OR INP (&H3FC))          'SET DTR HIGH
  OUT &H3FC, (&HFD AND INP (&H3FC))        'SCLK low
FOR N=1 TO 8
  Temp$=MID$(DI$,N,1)
  IF Temp$="0"THEN
    OUT &H3FC,(&H1 OR INP(&H3FC))
  ELSE OUT &H3FC, (&HFE AND INP (&H3FC))
  END IF 'out DI
  OUT &H3FC,(&H2 OR INP (&H3FC))           'SCLK high
  IF (INP (&H3FE) AND 16)=16 THEN
    DO$=DO$+"0"
    ELSE
    DO$=DO$+"1"
  END IF                                   'Input DO
  OUT &H3FC, (&H1 OR INP (&H3FC))          'SET DTR HIGH
  OUT &H3FC, (&HFD AND INP (&H3FC))        'SCLK low
NEXT N
IF DOL>8 THEN
  FOR N=9 TO DOL
  OUT &H3FC,(&H1 OR INP (&H3FC))           'SET DTR HIGH
  OUT &H3FC,(&HFD AND INP (&H3FC))         'SCLK low
  OUT &H3FC,(&H2 OR INP (&H3FC))           'SCLK high

  IF (INP(&H3FE) AND &H16)=&H16 THEN
    DO$=DO$+"0"
  ELSE
    DO$=DO$+"1"
  END IF
  NEXT N
END IF
OUT &H3FC,(&HFA AND INP(&H3FC))            'SCLK low and DI high
FOR N=1 TO 500
NEXT N
PRINT DO$
INPUT "Enter "C" to convert else "RETURN" to alter DI data"; s$
IF s$="C" OR s$="c" THEN
  GOTO 20
ELSE
  GOTO 10
END IF
END
```

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