National Semiconductor

ADC16071/ADC16471
16-Bit Delta-Sigma 192 ks/s Analog-to-Digital Converters

General Description

The ADC16071/ADC16471 are 16-bit delta-sigma analog-to-digital converters using 64 × oversampling at 12.288 MHz. A 5th-order comb filter and a 246 tap FIR decimation filter are used to achieve an output data rate of up to 192 kHz. The combination of oversampling and internal digital filtering greatly reduces the external anti-alias filter requirements to a simple RC low pass filter. The FIR filters offer linear phase response, 0.005 dB passband ripple, and ≥90 dB stopband rejection. The ADC16071/ADC16471's analog fourth-order modulator uses switched capacitor technology. A built-in fully-differential bandgap voltage reference is also included in the ADC16471. The ADC16071 has no internal reference and requires externally applied reference voltages.

The ADC16071/ADC16471 use an advanced BiCMOS process for a low power consumption of 500 mW (max) while operating from a single 5V supply. A power-down mode reduces the power supply current from 100 mA (max) in the active mode to 1.3 mA (max).

The ADC16071/ADC16471 are ideal analog-to-digital front ends for signal processing applications. They provide a complete high resolution signal acquisition system that requires a minimal external anti-aliasing filter, reference, or interface logic.

The ADC16071/ADC16471's serial interface is compatible with the DSP56001, TMS320, and ADSP2100 digital signal processors.

Key Specifications

■ Resolution	16 bits
■ Total harmonic distortion	
48 kHz output data rate	−94 dB (typ)
192 kHz output data rate	−80 dB (typ)
■ Maximum output data rate	192 kHz (min)
■ Power dissipation	
— Active	
192 kHz output data rate	500 mW (max)
48 kHz output data rate	275 mW (max)
— Power-down	6.5 mW (max)

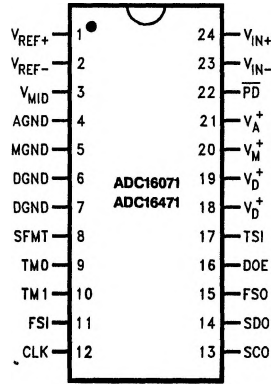
Key Features

- Voltage reference (ADC16471 only)
- Fourth-order modulator
- 64 × oversampling with a 12.288 MHz sample rate
- Adjustable output data rate from 7 kHz to 192 kHz
- Linear-phase digital anti-aliasing filter:
  - 0.005 dB passband ripple
  - 90 dB stopband rejection
- Single +5V supply
- Power-down mode
- Serial data interface compatible with popular DSP devices

Applications

- Medical instrumentation
- Process control systems
- Test equipment
- High sample-rate audio
- Digital Signal Processing (DSP) analog front-end
- Vibration and noise analysis

Connection Diagram



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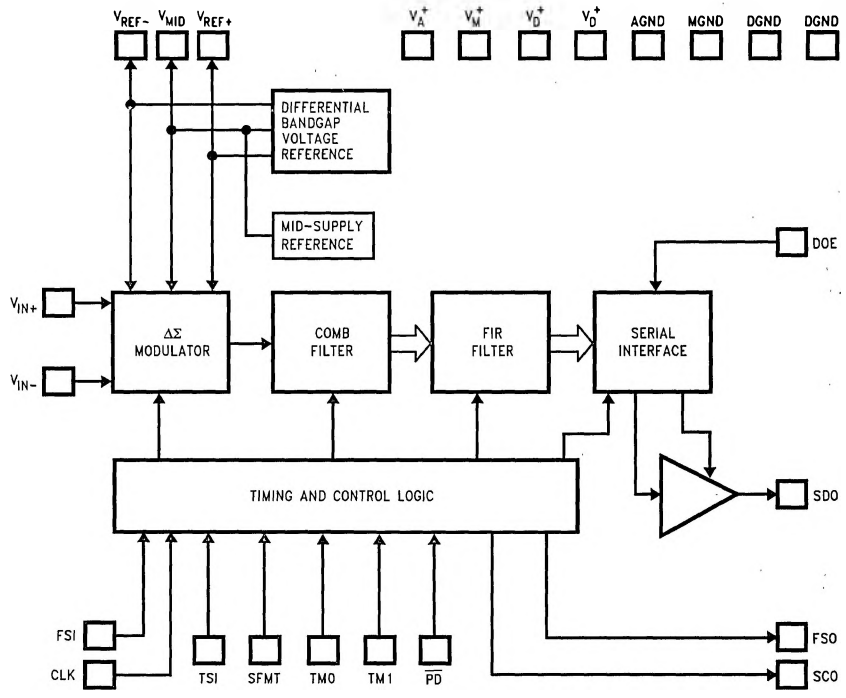
Ordering Information

Part No.	Package	NS Package No.
ADC16471CIN	24-Pin Molded DIP	N24C
ADC16471CIWM	24-Pin SOIC	M24B
ADC16071CIN	24-Pin Molded DIP	N24C
ADC16071CIWM	24-Pin SOIC	M24B

Block Diagram

ADC16471



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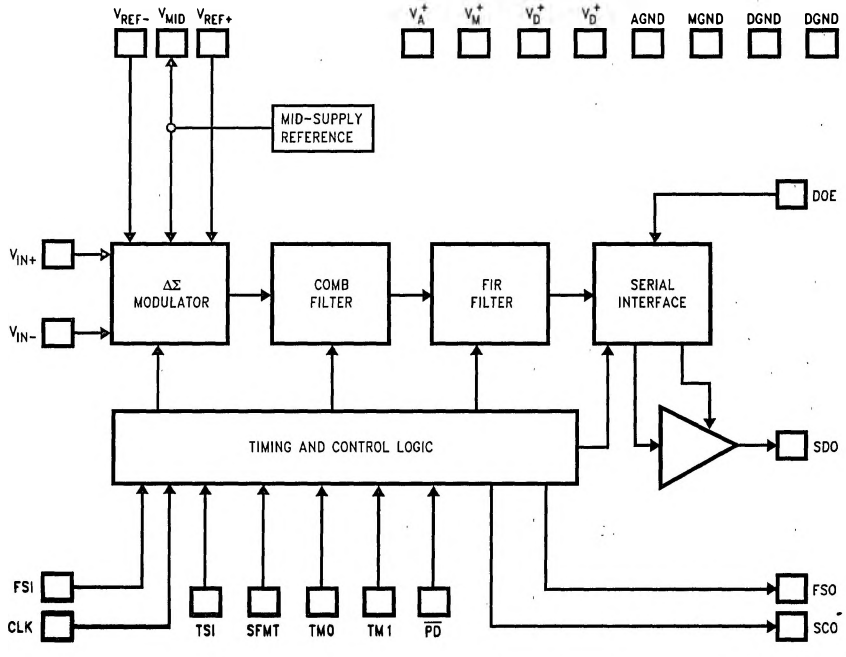
ADC16071



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Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_A^+, V_D^+, and V_M^+)	+6.5V
Logic Control Inputs	−0.3V to V_D^+ + 0.3V
Voltage at Other Inputs and Outputs	−0.3V to $V_A^+ = V_M^+$ + 0.3V
Input Current at Any Pin (Note 3)	±25 mA
Package Input Current (Note 3)	±100 mA
Maximum Junction Temperature (Note 4)	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature	
N Package (Soldering, 10 sec.)	300°C
WM Package (Infrared, 15 sec.)	220°C
WM Package (Vapor Phase, 60 sec.)	215°C
ESD Susceptibility (Note 5)	
Human Body Model	4000V
Machine Model	250V

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Ratings (Notes 1 and 2)

Temperature Range ($T_{min} \le T_A \le T_{max}$)	
ADC16471CIN, ADC16071CIN, ADC16471CIWM, ADC16071CIWM	$-40°C \le T_A \le +85°C$
Supply Voltage	
V_A^+, V_D^+, V_M^+	4.75V to 5.25V

Converter Electrical Characteristics

The following specifications apply for $V_M^+ = V_A^+ = V_D^+ = 5.0V_{DC}$, $V_{MID} = V_A^+/2 = 2.50V$, $V_{REF+} = V_{MID} + 1.25V$, $V_{REF-} = V_{MID} - 1.25V$, $f_{CLK} = 24.576$ MHz, and dynamic tests are performed with an input signal magnitude set at −6 dB with respect to a full-scale input unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{min}$ to T_{max}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
	Resolution			**16**	Bits
f_{CLK} = 24.576 MHz (f_s = 192 kHz)					
S/(N+D)	Signal-to-Noise + Distortion Ratio	Measurement bandwidth = $0.45f_s$ f_{IN} = 19 kHz	76	**72**	dB (min)
THD	Total Harmonic Distortion	f_{IN} = 19 kHz	0.010	**0.022**	% (max)
IMD	Intermodulation Distortion	f_1 = 18.5 kHz, f_2 = 19.5 kHz	0.010	**0.017**	% (max)
	Converter Noise Floor (Note 8)	Measurement Bandwidth = $0.45f_s$	−88	**−77**	dBFS (min)
f_{CLK} = 6.144 MHz (f_s = 48 kHz)					
S/(N+D)	Signal-to-Noise + Distortion Ratio	Measurement bandwidth = $0.45f_s$ f_{IN} = 5 kHz	85	80 **73**	dB (min) dB (min)
THD	Total Harmonic Distortion	f_{IN} = 5 kHz	0.002	0.0055 **0.008**	% (max) % (max)
IMD	Intermodulation Distortion	f_1 = 4 kHz, f_2 = 5.5 kHz	0.003	0.009 **0.01**	% (max) % (max)
	Converter Noise Floor (Note 8)	Measurement Bandwidth = $0.45f_s$	−99	−92 **−89**	dBFS (min) dBFS (min)
OTHER CONVERTER CHARACTERISTICS					
Z_{IN}	Input Impedance (Note 9)		34		kΩ
ΔA_V	Gain Error		±0.2	**±1.0**	%FS (max)
V_{OS}	Input Offset Voltage		15		mV
I_A	Analog Power Supply Current		23	**31**	mA (max)
I_M	Modulator Power Supply Current	f_{CLK} = 24.576 MHz f_{CLK} = 6.144 MHz	1.6 0.4	**2.4** **0.8**	mA (max)
I_D	Digital Power Supply Current	f_{CLK} = 24.576 MHz f_{CLK} = 6.144 MHz	50 13	**65** **23**	mA (max)
I_{SPD}	Power-Down Supply Current	$I_A + I_D + I_M$	0.25	**1.3**	mA
P_D	Power Dissipation		0.375	**0.5**	W
V_{MID}			$V_A^+/2$		V

Digital Filter Characteristics

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{min}$ to T_{max}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
	Stopband Rejection		−90.0		dB
	Passband Ripple		±0.005		dB
	3 dB Cutoff Frequency		0.45		fs
	Data Latency		3,968		Clock Cycles

Reference Characteristics (ADC16471 Only)

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{min}$ to T_{max}**; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
V_{REF}^+	Positive Internal Reference Output Voltage		V_{MID} + 1.25	**V_{MID} + 1.175** **V_{MID} + 1.325**	V (min) V (max)
V_{REF}^-	Negative Internal Reference Output Voltage		V_{MID} − 1.25	**V_{MID} − 1.325** **V_{MID} − 1.175**	V (min) V (max)
$\Delta(V_{REF+} - V_{REF-})/\Delta T$	Internal Reference Temperature Coefficient		30		ppm/°C
$\Delta V_{REF+}/\Delta I$	Positive Internal Reference Load Regulation	Sourcing (0 mA ≤ I ≤ +10 mA) Sinking (−1 mA ≤ I ≤ 0 mA)	3.4	**6.0**	mV (max)
$\Delta V_{REF-}/\Delta I$	Negative Internal Reference Load Regulation	Sinking (−1 mA ≤ I ≤ 0 mA) Sourcing (0 mA ≤ I ≤ 10 mA)	3.2	**6.0**	

Input Reference Characteristics (ADC16071 Only)

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units
V_{REF+}	Positive Reference Voltage		1 V_A+		V V
V_{REF-}	Negative Reference Voltage		0 $V_A+ - 1$		V V
$V_{REF+} - V_{REF-}$	Total Reference Voltage		1 V_A+		V V

DC Electrical Characteristics

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
V_{IH}	Logic High Input Voltage	$V_D^+ = 5.25V$		**V_D^+** **2.3**	V (max) V (min)
V_{IL}	Logic Low Input Voltage	$V_D^+ = 4.75V$		**0.8** **−0.3**	V (max) V (min)
V_{OH}	Logic High Output Voltage	Logic High Output Current = −400 μA, $V_D^+ = 4.75V$		**2.4**	V (min)
V_{OL}	Logic Low Output Voltage	Logic Low Output Current = 2 mA, $V_D^+ = 5.25V$		**0.5**	V (max)
$I_{IN(1)}$	Logical "1" Input Current		1.0	**5.0**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current		−1.0	**−5.0**	μA (max)
I_{TSI}	SDO TRI-STATE® Leakage Current	$V_{IN} = 0.4V$ to 2.4V	1.0	**5.0**	μA (max)
C_{IN}	Logic Input Capacitance	$V_{IN} = 0$ to V_D^+	5		pF

AC Electrical Characteristics for Clock In (CLK), Serial Clock Out (SCO), and Frame Sync In (FSI)

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
f_{CLK}	CLK Frequency Range ($f_{CLK} = 1/t_{CLK}$)			**25** **1**	MHz (max) MHz (min)
t_{CLK}	CLK Period ($t_{CLK} = 1/f_{CLK}$)			**1000** **40**	ns (max) ns (min)
t_{CLKL}	CLK Low Pulse Width			**16**	ns (min)
t_{CLKH}	CLK High Pulse Width			**14**	ns (min)
t_R	CLK Rise Time			**10** **3**	ns (max) ns (min)
t_F	CLK Fall Time			**10** **3**	ns (max) ns (min)
t_{FSILOW}	Minimum Frame Sync Input Low Time before Frame Sync Input Asserted High		2		t_{CLK} (min)
t_{FSISU}	Frame Sync Input Setup Time			**10**	ns (min)
t_{FSIH}	Frame Sync Input Hold Time			**10**	ns (min)
t_{SCOD}	Serial Clock Output Delay Time from Rising Edge of CLK		12	**20** **5**	ns (max) ns (min)
t_{SCO}	Serial Clock Output Period			**4**	t_{CLK}

AC Electrical Characteristics for Frame Sync Out (FSO), Serial Clock Out (SCO), and Serial Data Out (SDO)

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
$t_{SCOFSOH}$	Delay from Serial Clock Out to Frame Sync Output High		2	**5**	ns (max)
$t_{SCOFSOL}$	Delay from Serial Clock Out to Frame Sync Output Low		2	**5**	ns (max)
t_{SDOV}	Delay from Serial Clock Out to Serial Data Output Valid		3	**8**	ns (max)
$t_{FSIFSOL}$	Delay from Frame Sync Input to Frame Sync Output Low			**8**	t_{CLK} (max)

AC Electrical Characteristics for Data Output Enable (DOE)

The following specifications apply for $V_A^+ = V_D^+ = V_M^+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 6)	Limits (Note 7)	Units (Limit)
t_{DOEE}	Data Output Enable Delay Time		20	**25**	ns (max)
t_{DOED}	Data Output Disable Delay Time		16	**20**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} <$ GND or $V_{IN} > (V_A^+, V_M^+,$ or $V_D^+)$), the current at that pin should be limited to 25 mA. The 100 mA maximum package input current rating allows the voltage at any four pins, with an input current of 25 mA each, to simultaneously exceed the power supply voltages.

Note 4: The maximum power dissipation is a function of the maximum junction temperature ($T_{J(MAX)}$), total thermal resistance (θ_{JA}), and ambient temperature (T_A). The maximum allowable power dissipation at any ambient temperature is $P_{D(max)} = (T_{J(max)} - T_A)/\theta_{JA}$. When board mounted, the ADC16071/ADC16471's typical thermal resistance is:

Order Number	θ_{JA}
ADC16071CIN, ADC16471CIN	47°C/W
ADC16071CIWM, ADC16471CIWM	72°C/W

Note 5: Human body model, 100 pF discharge through a 1.5 kΩ resistor. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 6: Typicals are at $T_A = 25°C$ and represent most likely parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Output Quality Level).

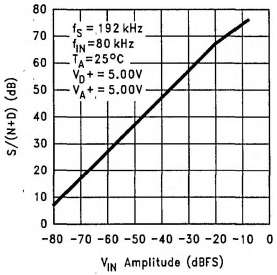
Note 8: The V_{IN}^+ pin is shorted to the V_{IN}^- pin.

Note 9: The input impedance between V_{IN+} and V_{IN-} due to the effective resistance of the switch capacitor input varies as follows:

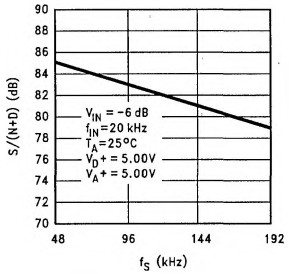
$$Z_{IN} = \frac{10^{12}}{2.35^* (\frac{f_{CLK}}{2})}$$

Typical Performance Characteristics

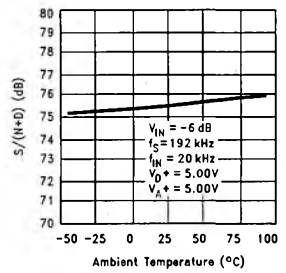
S/(N + D) vs V_{IN} Amplitude



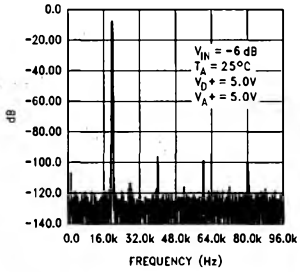
S/(N + D) vs Output Data Rate (fs)



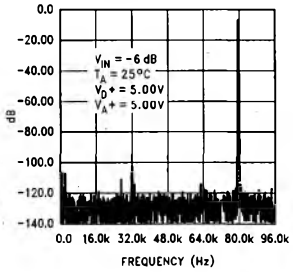
S/(N + D) vs Temperature



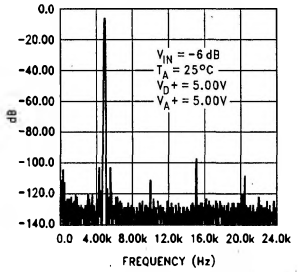
Spectral Response, f_S = 192 kHz, f_{IN} = 20 kHz



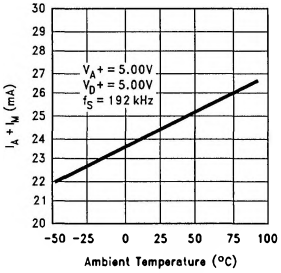
Spectral Response, f_S = 192 kHz, f_{IN} = 80 kHz



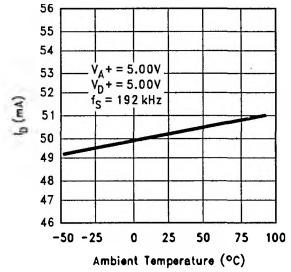
Spectral Response, f_S = 48 kHz, f_{IN} = 5 kHz



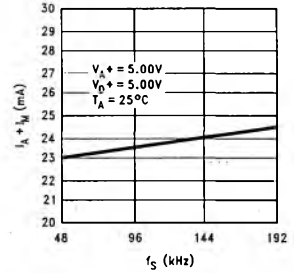
Analog Supply Current (I_A + I_M) vs Temperature



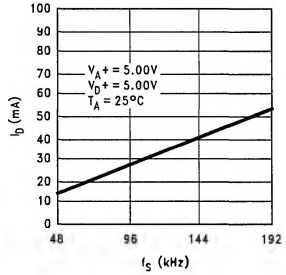
Digital Supply Current I_D vs Temperature



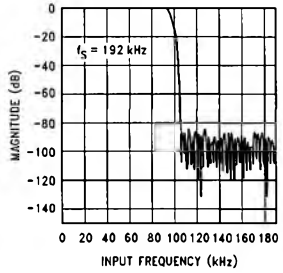
Analog Supply Current (I_A + I_M) vs Output Data Rate (fs)



Digital Supply Current (I_D) vs Output Data Rate (fs)



Frequency Response of Digital Filter



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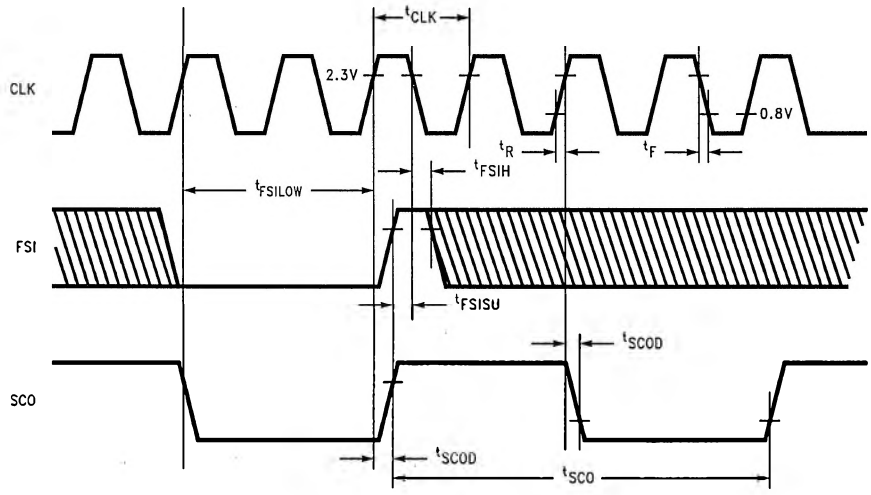

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FIGURE 1. Timing Diagrams for Clock Input (CLK), Frame Sync Input (FSI), and Serial Clock Output (SCO)

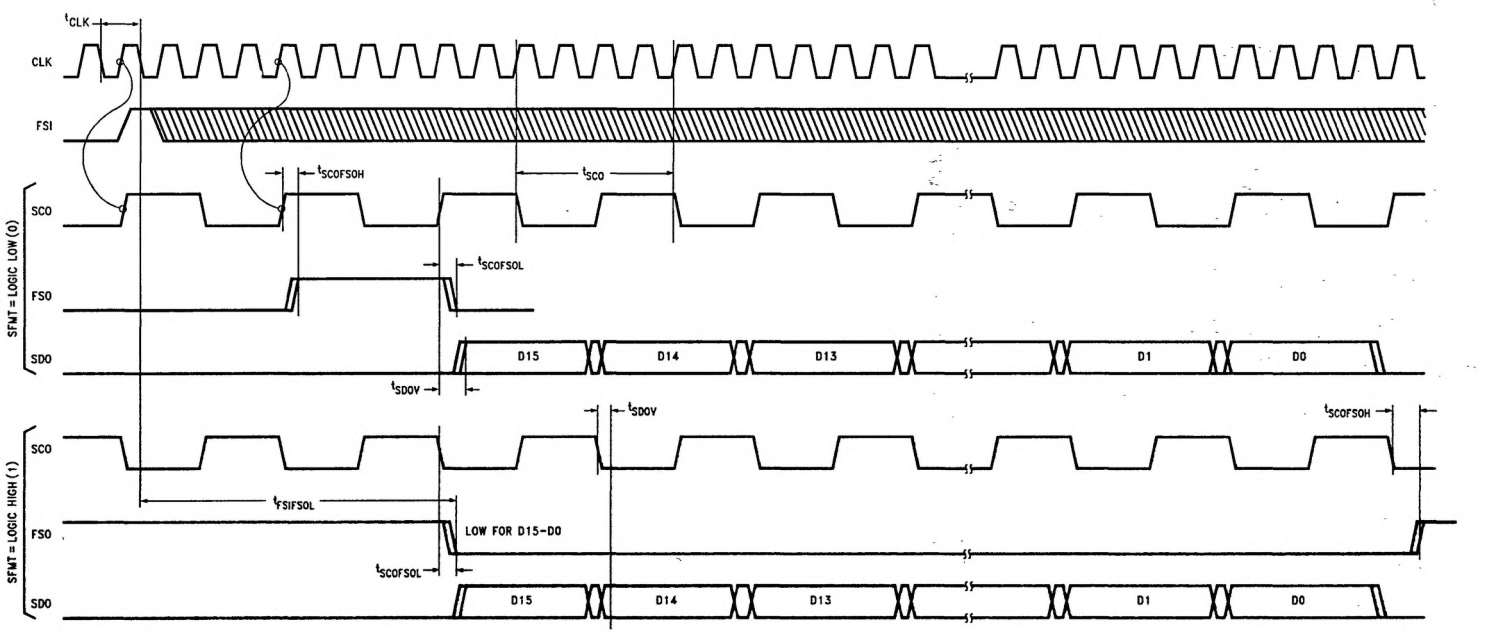

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FIGURE 2. Detailed Timing Diagrams for Frame Sync Input (FSI), Frame Sync Out (FSO), Serial Clock Out (SCO), and Serial Data Out (SDO)

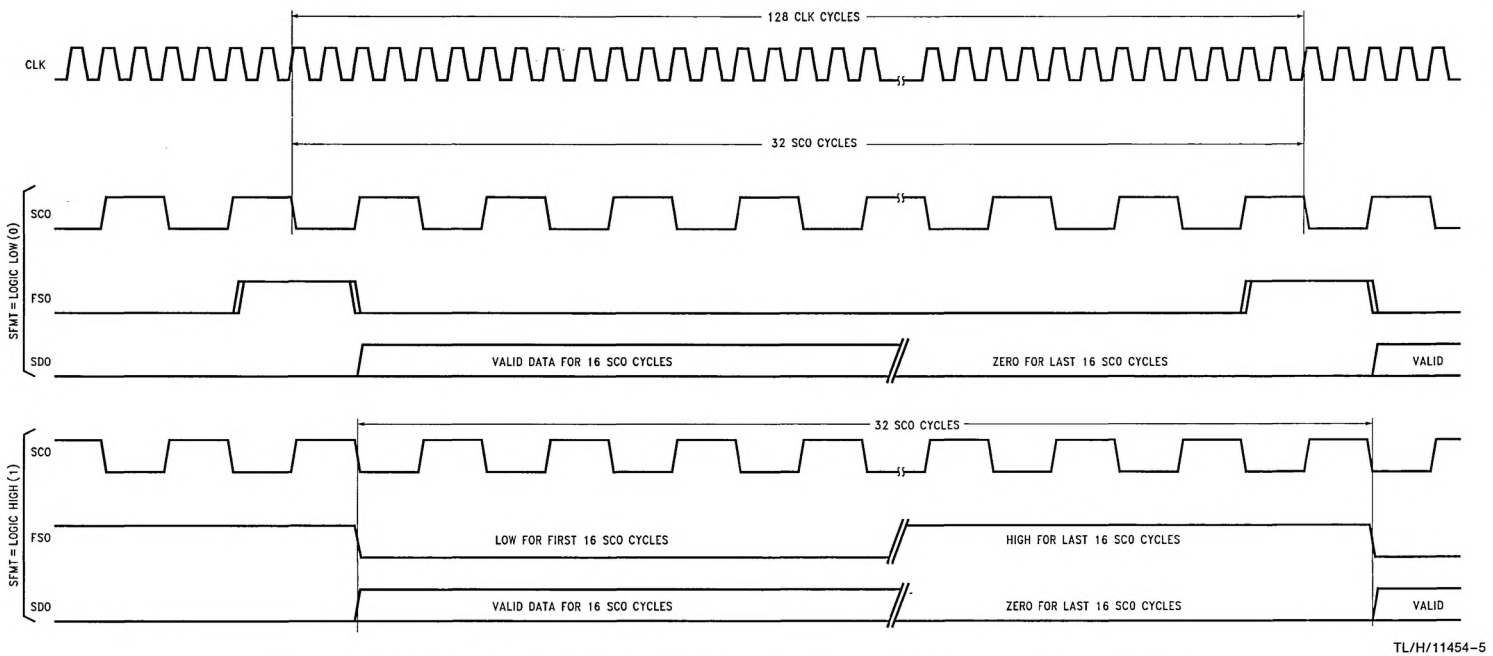

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FIGURE 3. Timing Diagrams for Frame Sync Out (FSO), Serial Clock Out (SCO), and Serial Data Out (SDO)

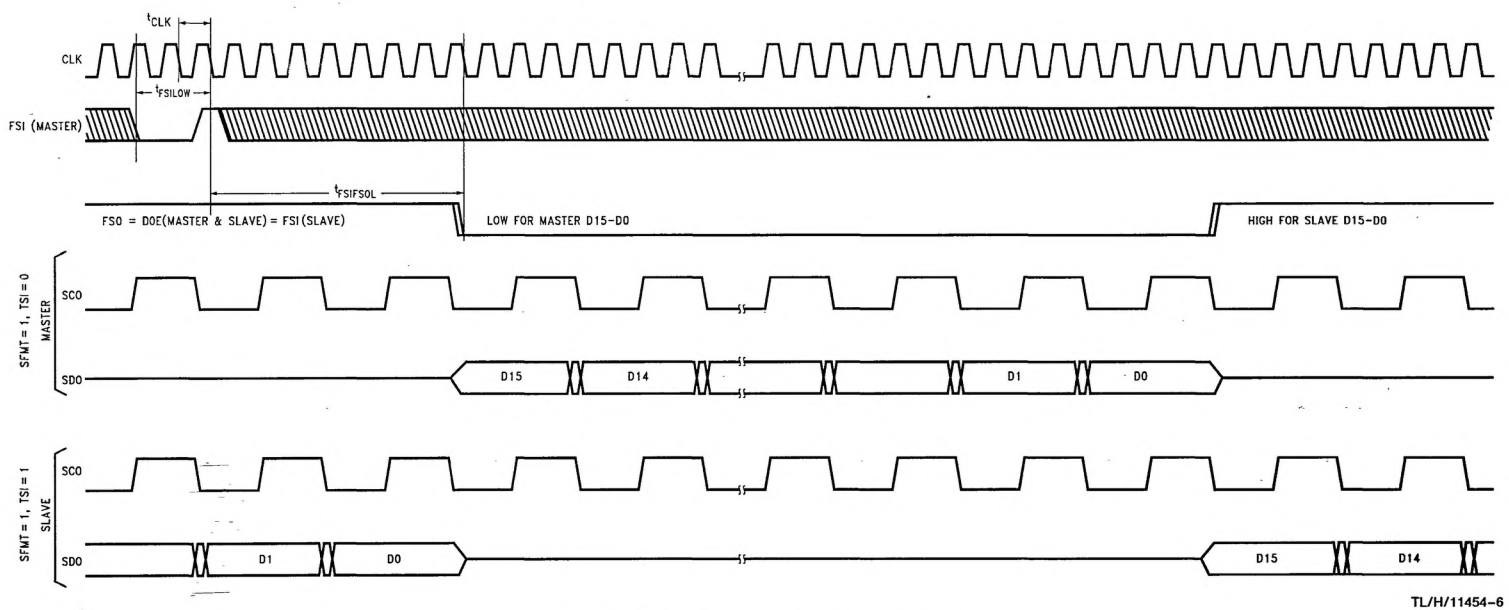

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FIGURE 4. Master/Slave Mode Timing Diagrams

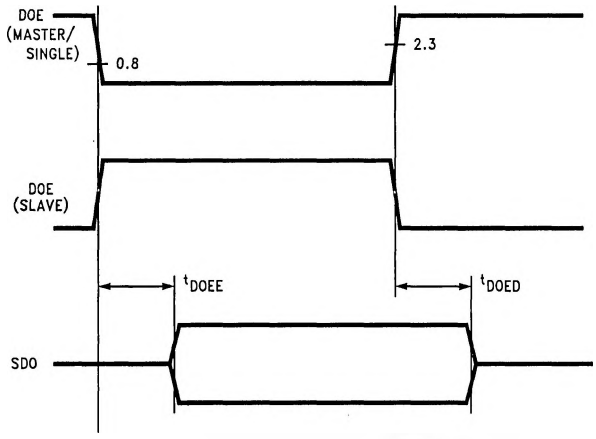

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FIGURE 5. Timing Diagrams for Data Output Enable (DOE) and Serial Data Out (SDO)

Pin Description

V_{REF}^+, V_{REF}^- These are the ADC16471's internal differential reference's bypass pins. Their nominal output voltage is ±1.25V centered around the voltage at the V_{MID} pin, typically $V_A^+/2$. V_{REF+}, V_{MID}, and V_{REF-} should be bypassed with a parallel combination of 10 μF and 0.1 μF capacitors. For the ADC16071, these are the reference voltage inputs. V_{REF+} and V_{MID} should be bypassed with a parallel combination of 10 μF and 0.1 μF capacitors.

V_{MID} This pin is the internal differential reference's $V_A^+/2$ output pin. V_{MID} should be bypassed with a parallel combination of 10 μF and 0.1 μF capacitors.

V_{IN}^+, V_{IN}^- These are the ADC's differential input pins. Signals applied to these pins can be single-ended or differential with respect to the V_{MID} voltage.

$\overline{PD}$ This is the input pin used to activate the power-down mode. When a logic LOW (0) is applied to this pin the supply current drops from 100 mA (max) to 1.3 mA (max).

AGND This is the connection to system analog ground. Internally, this ground is connected to the analog circuitry, including the fourth-order modulator.

DGND This is the connection to system digital ground. Internally, this ground is connected to all digital circuitry except the modulator's clock.

MGND This is the ground pin for the modulator's clock. It should be connected to analog ground through its own connection that is separate from that used by AGND.

V_A^+ This pin is the connection to the system analog voltage supply. Best performance is achieved when this pin is bypassed with a parallel combination of 10 μF and 0.1 μF capacitors.

V_M^+ This is the modulator's supply pin. V_M^+ should be connected to the system analog voltage supply with a circuit board trace or connection that is separate from that used to supply V_A^+. Best performance is achieved when this pin is bypassed with a parallel combination of 10 μF and 0.1 μF capacitors.

V_D^+ This pin is the connection to the system digital voltage supply. Best performance is achieved when this pin is bypassed with a parallel combination of 10 μF and 0.1 μF capacitors.

SFMT This is the Serial Format pin. The logic level applied to the **SFMT** pin determines whether conversion data shifted out of the **SDO** pin is valid on the rising or falling edge of **SCO**. It also controls the format of the Frame Sync Out **(FSO)** signal. See the **Serial Interface** section for details.

TM0, TM1 Used to enabled test mode during production. Connect both pins to DGND.

FSI This is the Frame Sync Input pin. **FSI** is an input used to synchronize the ADC16071/ADC16471's conversions to an external source. The state of **FSI** is sampled on the falling edge of **CLK**. See the **Serial Interface** section for details.

CLK This is the clock signal input pin. The signal applied to this pin sets the sample rate of the ADC16071/ADC16471's modulator to $f_{CLK}/2$. The frequency range can be 1 MHz ≤ f_{CLK} ≤ 25 MHz.

SCO This is the Serial Clock Output pin. The ADC16071/ADC16471's serial data transmission is synchronous with the **SCO** signal. **SCO** has a frequency of $f_{CLK}/4$. See the **Serial Interface** section for details.

SDO This is the Serial Data Output pin. The ADC16071/ADC16471's conversion data is shifted out from this pin synchronous to the **SCO** signal. See the **Serial Interface** section for details.

Pin Description (Continued)

FSO This is the Frame Sync Output pin. **FSO** is used to synchronize an external device to the ADC16071/ADC16471's 32 SCO cycle data transmission frame. The format of the signal on **FSO** depends on the logic level applied to the **SFMT** pin. See the **Serial Interface** section for details.

TSI This is the Time Slot Input pin. **TSI** can be used to allow two ADC16071/ADC16471's to share a single serial data line. The logic level applied to **TSI** controls the active state of the ADC16071/ADC16471's **DOE** pin. See the **Serial Interface** and the **Two Channel Multiplexed Operation** sections for details.

DOE This is the Data Output Enable pin. **DOE** is used to control **SDO**'s TRI-STATE output buffer. The active state of **DOE** is controlled by the logic level applied to the **TSI** pin. See the **Serial Interface** and the **Two Channel Multiplexed Operation** sections for details.

Applications Information

TYPICAL PERFORMANCE RESULTS

Figure 6 shows a 16k point FFT plot of the baseband output spectrum during conversion of a 24 kHz input signal.

CLOCK GENERATION

The ADC16071/ADC16471 requires a sampling-clock signal that is free of ringing (over/undershoot of no more than 100 mV_{p-p}) and has a rise and fall time in the range of 3 ns–10 ns. We have tested and recommended crystal clock oscillators from Ecliptek (EC1100 series) and SaRonix (NCH060 and NCH080 series). Both of these families use HCMOS logic circuitry for very fast rise and fall times.

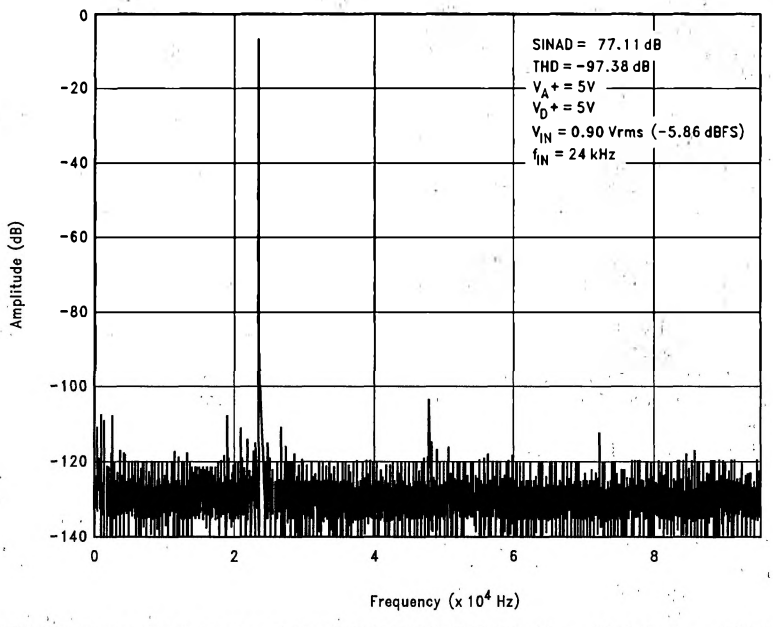

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FIGURE 6. Typical Performance of the ADC16071/ADC16471 at f_S = 192 kHz, f_{IN} = 24 kHz

Applications Information (Continued)

Overshoot and ringing can be reduced by adding a series damping resistor between the crystal oscillator's output (pin 8) and the ADC16071/ADC16471's CLK (pin 12), as shown in *Figure 7*. The actual resistor value is dependent on the board layout and trace length that connects the oscillator or CLK source to the ADC. A typical starting value is 50Ω with a range of 27Ω to 150Ω.

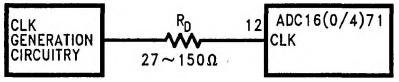

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FIGURE 7. Damping Resistor Reduces Clock Signal Overshoot

SERIAL INTERFACE

The ADC16071 and the ADC16471 have three serial interface output pins: Serial Data Output (**SDO**), Frame Sync Output (**FSO**), and Serial Clock Output (**SCO**). **SCO** has a frequency of $f_{CLK}/4$. Each of the ADC16071/ADC16471's 16-bit conversions is transmitted within the first half of the **data transmission frame.** A data transmission frame is 32 SCO cycles in duration. Two's complement data shifts out on the **SDO** pin beginning with bit 15 (MSB) and ending with bit 0 (LSB), taking 16 **SCO** cycles. **SDO** then shifts out zeroes for the next 16 **SCO** cycles to maintain compatibility with two channel multiplexed operation.

The serial data that is shifted out of the **SDO** pin is synchronous with **SCO**. Depending on the logic level applied to the Serial Format pin (**SFMT**), the data on the **SDO** pin is valid on either the falling or rising edge of **SCO**. If a logic Low is applied to **SFMT**, then the data on **SDO** is valid on the falling edge of **SCO**. If a logic High is applied to **SFMT**, then the data on **SDO** is valid on the rising edge of **SCO**. See *Figure 2*.

The **FSO** signal is used to synchronize other devices to the ADC16071/ADC16471's data transmission frame. Depending on the logic level applied to **SFMT**, the signal on **FSO** is either a short pulse (approximately one SCO cycle in duration) ending just before the transmission of bit 15 on **SDO**, or a square wave with a period of 32 SCO cycles going low just before the transmission of bit 15 and going high just after the transmission of bit 0. If a logic Low is applied to **SFMT**, **FSO** will be high for approximately one SCO cycle and fall low just before the transmission of bit 15 and stay low for the remainder of the transmission frame. If a logic High is applied to **SFMT**, **FSO** will be low during the transmission of bits 15–0 and high during the next 16 SCO cycles. See *Figure 3*.

The Frame Sync Input (**FSI**), is used to synchronize the ADC16071/ADC16471's conversions to an external source. The logic state of **FSI** is captured by the ADC16071/ADC16471 on the falling edge of **CLK**. If an **FSI** low to high transition is sensed between adjacent **CLK** falling edges, the ADC16071/ADC16471 will interrupt its current data transmission frame and begin a new one. See *Figure 4*.

Due to the data latency of the ADC16071/ADC16471's digital filters, the first 31 conversions following a frame sync input signal will represent inaccurate data, unless the frame syncs are applied at constant 32 SCO cycle intervals. If no **FSI** signal is applied (FSI is kept High or Low), the ADC16071/ADC16471 will internally create a frame sync every 32 SCO cycles.

The Data Output Enable pin (**DOE**), is used to enable and disable the output of data on **SDO**. When **DOE** is deactivated, **SDO** stops driving the serial data line by entering a high impedance TRI-STATE. **DOE**'s active state matches the logic level applied to the Time Slot Input pin (**TSI**). If a logic Low is applied to **TSI**, the ADC16071/ADC16471's **SDO** pin will shift out data when **DOE** is Low, and be in a high impedance TRI-STATE when **DOE** is High. If a logic High is applied to **TSI**, **SDO** will shift out data when **DOE** is High, and be in a high impedance TRI-STATE when **DOE** is Low.

TWO CHANNEL MULTIPLEXED OPERATION

Two ADC16071/ADC16471's can easily be configured to share a single serial data line and operate in a "stereo", or two channel multiplexed mode. They share the serial data bus by alternating transmission of conversion data on their respective **SDO** pins. One of the ADC16071/ADC16471's, the Master, shifts its conversion data out of **SDO** during the first 16 SCO cycles of the data transmission frame. The other ADC16071/ADC16471, the Slave, shifts its data out during the second 16 SCO cycles of the data transmission frame.

The Slave is selected by applying a logic High to its **TSI** pin and a logic High to its **SFMT** pin. The Master is chosen by applying a logic Low to its **TSI** pin and a logic High to its **SFMT** pin. As shown in *Figure 8*, the Master's **FSO** is used to control the **DOE** of both the Master and the Slave as well as to synchronize the two ADC16071/ADC16471's by driving the Slave's Frame Sync Input pin, **FSI**. As the Master finishes transmitting its 16 bits of conversion data, its **FSO** goes High. This triggers the Slave's **FSI**, causing the Slave to begin transmitting its 16 bits of conversion data.

The Master's **DOE** is active Low and the Slave's **DOE** is active High. Since the same signal, the Master's **FSO**, is connected to both of the converters' **DOE** pins, one converter will shift out data on its **SDO** pin while the other is in TRI-STATE, allowing the two ADC16071/ADC16471's to share the same serial data transmission line.

POWER SUPPLY AND GROUNDING

The ADC16071/ADC16471 has on-chip 50 pF bypass capacitors between the supply-pin bonding pads and their corresponding grounds. There are 24 of these capacitors, 6 for the analog section and 18 for the digital, resulting in a total value of 1200 pF. They help control ringing on the on-chip power supply busses, especially in the digital section. Further, they help enhance the baseband noise performance of the analog modulator.

Applications Information (Continued)

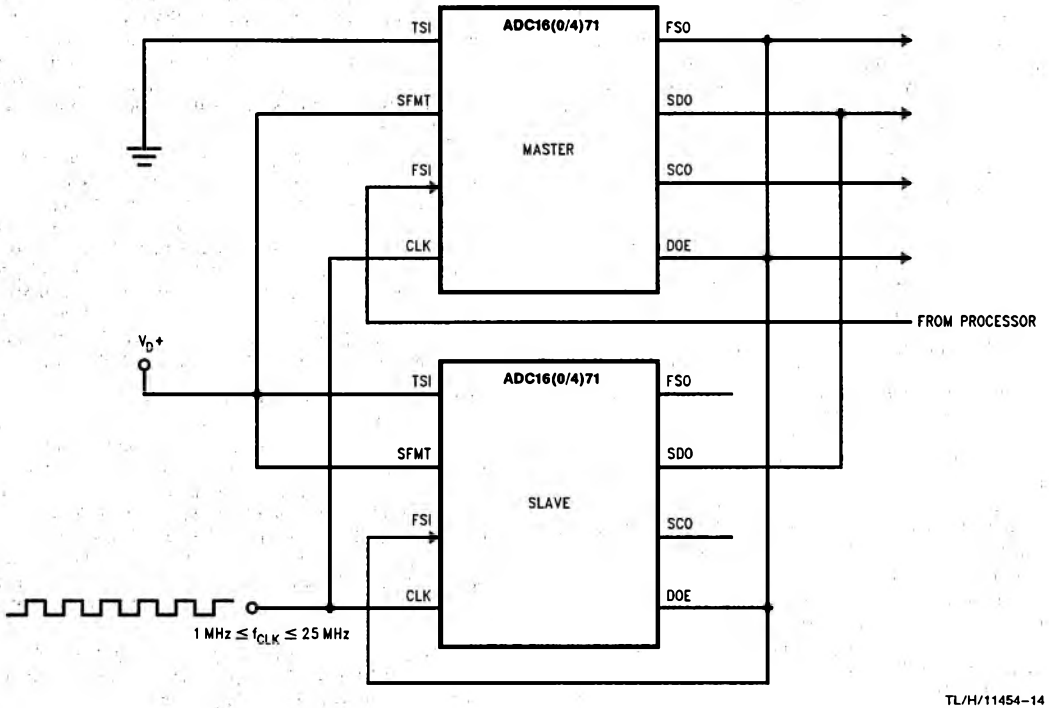


FIGURE 8. Two Channel Multiplexed Operation Connection Diagram

Best converter performance is achieved when these internal bypass capacitors are supplemented with additional external power-supply decoupling capacitors. This ensures the lowest ac-bypass impedance path for the ADC16071/ADC16471's dynamic current requirements. Each of the ADC16071/ADC16471's four supply pins should be individually bypassed, using a parallel combination of 10 μF (tantalum) and 0.1 μF (monolithic ceramic), to its corresponding ground pin:

V_A+ (Pin 21) → AGND (Pin 4)
V_M+ (Pin 20) → MGND (Pin 5)
V_D+ (Pin 19) → DGND (Pin 6)
V_D+ (Pin 18) → DGND (Pin 7)

Short lead lengths are mandatory. Therefore, surface mount capacitors are ***strongly*** recommended.

POWER SUPPLY VOLTAGES FOR BEST PERFORMANCE

While adequate performance will be achieved by operating the ADC16071/ADC16471 with +5V connected to V_A+, V_M+ and V_D+, dynamic performance, as measured by S/(N + D), can be further enhanced by slightly raising the analog supply voltage and lowering the digital supply voltage.

ANALOG INPUT

The ADC16071 and the ADC16471 generate a two's complement output determined by the following equation:

$$\text{Output Code} = \frac{(V_{IN}+ - V_{IN}-)\,(32768)}{(V_{REF}+ - V_{REF}-)}$$

Round off to the nearest integer value between −32768 and 32767.

The signals applied to V_{IN}^+ and V_{IN}^- must be between V_A^+ and analog ground. For accurate conversions, the absolute difference between V_{IN}^+ and V_{IN}^- should be less than the difference between V_{REF}^+ and V_{REF}^-. Best harmonic performance will result when a differential voltage is applied to V_{IN}^+ and V_{IN}^- that has a common mode voltage at or below V_{MID}.

Due to overloading in the ADC16071/ADC16471's ΔΣ modulator, performance degrades considerably as the input amplitude approaches full scale. With an input that peaks at −2 dB from full scale, S/(N + D) is about 2 dB worse than with a −6 dB input. With a −1 dB input, S/(N + D) can be 10 dB worse than with a −6 dB input.

Applications Information (Continued)

ANALOG SIGNAL CONDITIONING

The ADC16071/ADC16471's digital comb and FIR filter combine to create the band-limiting anti-aliasing filter, generating a steep cutoff at the upper range of the sampled baseband. Additional external filtering is needed to ensure that the best conversion performance is maintained. The external filtering uses a simple R-C lowpass filter. A suggested circuit is shown in *Figure 9.* The values of R_1, R_2, C_1, C_2, and C_3 are found using the following equation:

$$f_{c\,(-3\,dB)} = \frac{1}{6\pi RC}$$

where $R = R_1 = R_2$ and $C = C_1 = C_2 = C_3$.

The effects of the external filter are minimized by choosing a minimum cutoff frequency equal to $f_{CLK}/32$. As an example, for f_{CLK} equal to 6.144 MHz, set $R_1 = R_2 = 82.5\Omega$ and $C_1 = C_2 = C_3 = 3300$ pF. This sets the input network's cutoff frequency at 194 kHz. For f_{CLK} equal to 24.576 MHz, set $R_1 = R_2 = 20\Omega$ and $C_1 = C_2 = C_3 = 3300$ pF. This sets the input network's cutoff frequency at 803 kHz.

RELATION BETWEEN CAPACITOR DIELECTRIC AND SIGNAL DISTORTION

For any capacitors connected to the ADC16071/ADC16471's analog inputs, the dielectric plays an important role in determining the amount of distortion generated in the input signal. The capacitors used must have low dielectric absorption. This requirement is fulfilled using capacitors that have film dielectrics. Of these, polypropylene and polystyrene are the best. These are followed by polycarbonate and mylar. If ceramic capacitors are chosen, use only capacitors with NPO dielectrics.

INTERNAL DIFFERENTIAL BANDGAP REFERENCE

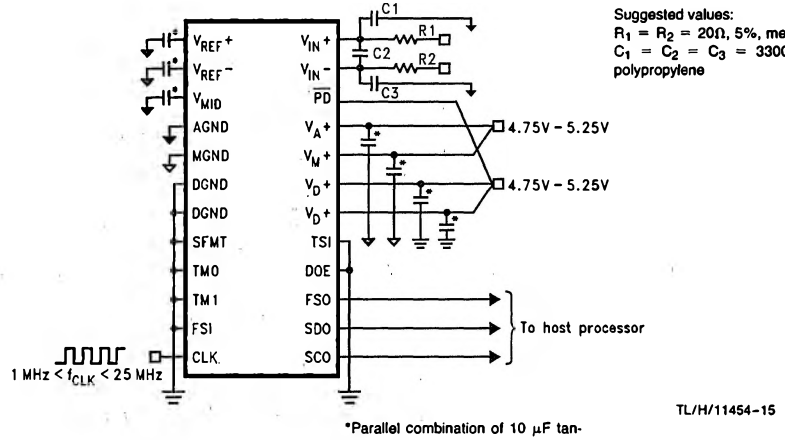
A fully differential bandgap reference generates local feedback voltages, $V_{REF}+$ and $V_{REF}-$, for the analog modulator. The outputs of this reference are trimmed to be equal to V_{MID} plus or minus 1.25V. This gives a differential reference voltage of 2.5V which results in a ±2.5V differential input range. The ADC16071 does not have the internal differential bandgap reference, allowing the user the flexibility to determine the full scale range by using an external voltage reference.

EXTERNAL VOLTAGE REFERENCE FOR THE ADC16071

Figure 10 shows the suggested connection diagram for the ADC16071. The LM4041-ADJ is set to 2.0V and is applied to the ADC16071's $V_{REF}+$ input.

The reference voltage must be free of noise. This is accomplished using the same capacitor combination used with the ADC16471's reference pins with the exception of $V_{REF}-$, which is connected to analog ground.

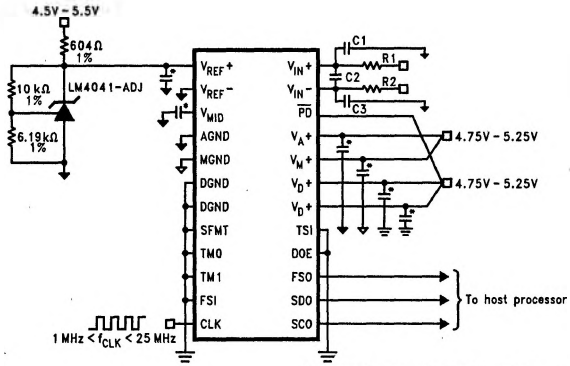
Figures 11 and *12* show the suggested circuits for ac-coupled applications.



*Parallel combination of 10 µF tantalum and a 0.1 µF monolithic ceramic capacitors.

FIGURE 9. Typical Connection Diagram for the ADC16471

Applications Information (Continued)



Suggested values:
$R_1 = R_2 = 20\Omega$, 5%, metal film
$C_1 = C_2 = C_3 = 3300$ pF, 5%, polypropylene

*Parallel combination of 10 μF tantalum and a 0.1 μF monolithic ceramic capacitors.

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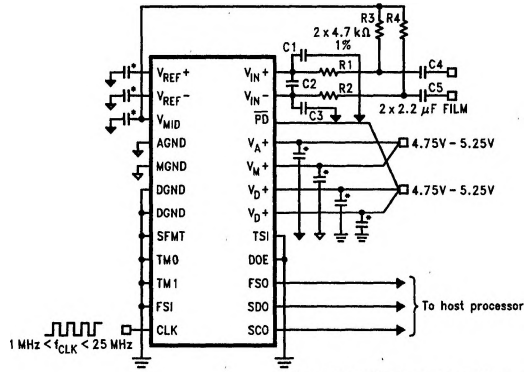
FIGURE 10. Typical Connection Diagram for the ADC16071



Suggested values:
$R_1 = R_2 = 20\Omega$, 5%, metal film
$C_1 = C_2 = C_3 = 3300$ pF, 5%, polypropylene

*Parallel combination of 10 μF tantalum and a 0.1 μF monolithic ceramic capacitors.

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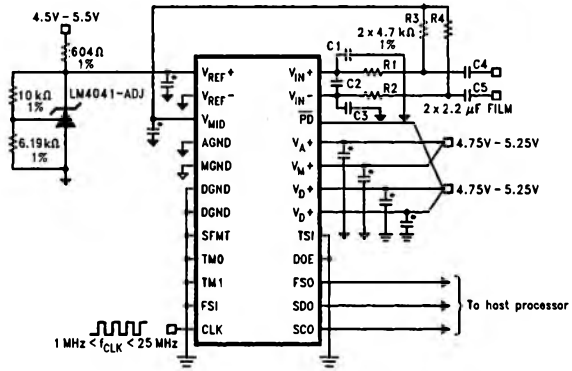
FIGURE 11. Typical Connection Diagram for the ADC16471 with AC-Coupled Inputs



Suggested values:
$R_1 = R_2 = 20\Omega$, 5%, metal film
$C_1 = C_2 = C_3 = 3300$ pF, 5%, polypropylene

*Parallel combination of 10 μF tantalum and a 0.1 μF monolithic ceramic capacitors.

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FIGURE 12. Typical Connection Diagram for the ADC16071 with AC-Coupled Inputs

Applications Information (Continued)

DSP INTERFACES

The ADC16071/ADC16471 was designed to connect to popular DSPs without intervening "glue logic". *Figures 13, 14,* and *15* show suggested connection schematics for the DSP56001, TMS320C3x, and the ADSP-2101 families.

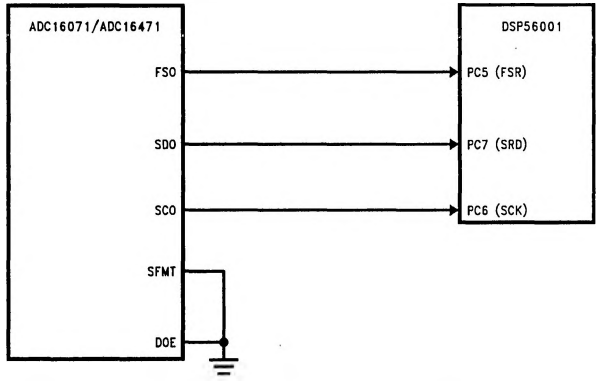

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FIGURE 13. Interface Connections between the ADC16071/ADC16471 and the Motorola DSP56001

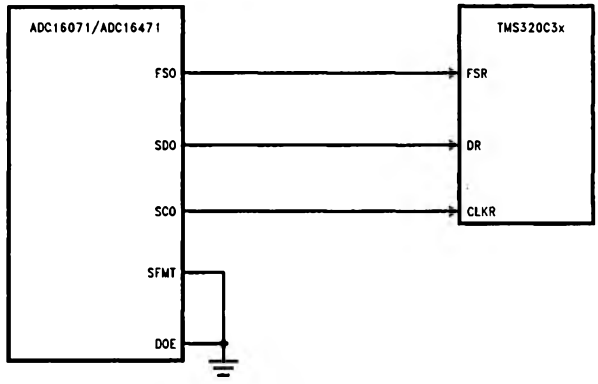

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FIGURE 14. Interface Connections between the ADC16071/ADC16471 and the Texas Instruments TMS320C3x

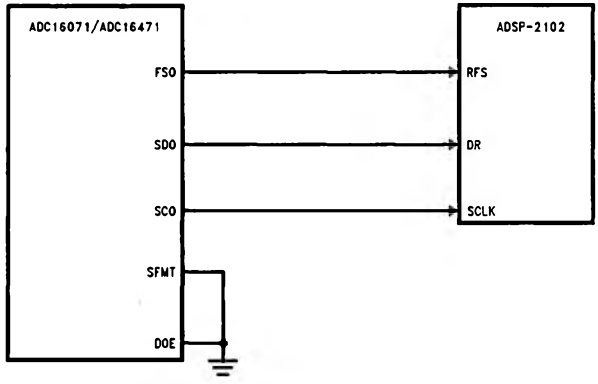

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FIGURE 15. Interface Connections between the ADC16071/ADC16471 and the Analog Devices ADSP-2101