BURR - BROWN®

ADC614

14-Bit 5.12MHz Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- HIGH SPURIOUS-FREE DYNAMIC RANGE: –90dB (L Grade)
- WIDEBAND SAMPLE/HOLD: 60MHz
- SAMPLE RATE: DC to 5.12MHz
- HIGH SIGNAL/NOISE RATIO: 78dB
- NO MISSING CODES
- SINGLE 46-PIN DIP PACKAGE
- COMPLETE SUBSYSTEM: Contains Sample/Hold and Reference

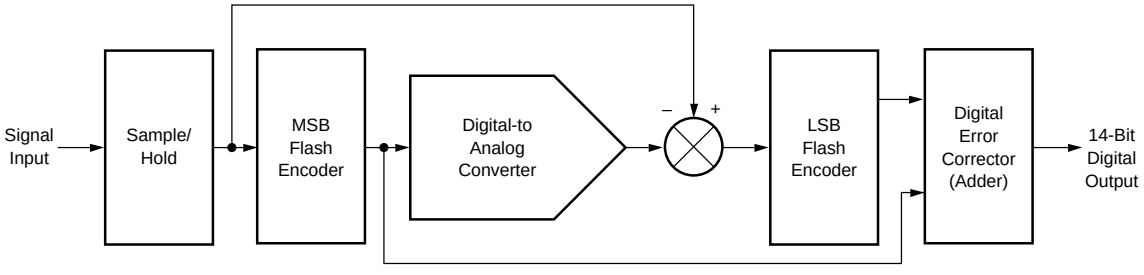
APPLICATIONS

- FFT SPECTRAL ANALYSIS
- MEDICAL IMAGING
- RADAR SIGNAL ANALYSIS
- CCD IMAGING SYSTEMS
- DIGITAL RECEIVERS
- TRANSIENT SIGNAL RECORDING
- HIGH-SPEED DATA ACQUISITION
- SIGINT, ECM, AND EW SYSTEMS

DESCRIPTION

The ADC614 is a high dynamic range analog-to-digital converter capable of digitizing signals at any rate from DC to 5.12 megasamples per second. Outstanding spurious-free dynamic range has been achieved by minimizing potential distortion sources.

The ADC614 is a two-step subranging ADC subsystem containing an ADC, sample/hold amplifier, voltage reference, timing, and error-correction circuitry in a 46-pin hybrid DIP package. The logic interface is TTL. An evaluation board (DEM-ADC614-E) is available for quick evaluation.



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PDS-1085F
Printed in U.S.A., November, 1996

SPECIFICATIONS

ELECTRICAL

At T_C = +25°C, 5.12MHz sampling rate, output data latched with the convert command, R_S = 50Ω, $\pm V_{CC}$ = +15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, and 15-minute warmup in convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC614JH			ADC614KH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				14			14	Bits
INPUTS								
Analog								
Input Range	Full Scale	–1.25		+1.25	✻		✻	V
Input Impedance			1.5			✻		MΩ
Input Capacitance			5			✻		pF
Digital								
Logic Family								
Convert Command	Start Conversion							
Pulse Width	t = Conversion Period	10		t-20	✻		✻	ns
TRANSFER CHARACTERISTICS								
Accuracy								
Gain Error	DC		±0.8	±2		±0.4	±1	%FSR[1]
Input Offset	DC		±0.4	±2		±0.2	±0.75	%FSR
Differential Linearity Error	f = 100kHz: 100% of All Codes		1.3	1.5		0.9	1.25	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta+V_{CC}$ = ±5%		±0.03	±0.1		✻	✻	%FSR/%
	$\Delta-V_{CC}$ = ±5%		±0.04	±0.1		✻	✻	%FSR/%
	$\Delta+V_{DD1}$ = ±5%		±0.004	±0.07		✻	✻	%FSR/%
	$\Delta-V_{DD2}$ = ±5%		±0.01	±0.07		✻	✻	%FSR/%
CONVERSION CHARACTERSITICS								
Sample Rate		DC		5.12M	✻		✻	Samples/s
Pipeline Delay	Logic Selectable		1, 2, or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS[1, 2]								
Differential Linearity Error	f = 2.3MHz: 100% of All Codes		1.3	2.0		0.8	1.25	LSB
Spurious-Free Dynamic Range (SFDR)								
f = 2.3MHz (–0.5dB)	f_S = 5.12MHz	77			80			dBFS[3]
f = 100kHz (–0.5dB)		79			82			dBFS[3]
Two-Tone Intermodulation Distortion[6]								
f = 2.2MHz (–6.5dB)	f_S = 5.12MHz		–80	–73		–85	–78	dBFS[3]
f = 2.3MHz (–6.5dB)								
Signal-to-Noise Ratio (SNR)[6]								
f = 2.3MHz (–0.5dB)	f_S = 5.12MHz	71	73		73	74		dB
f = 100kHz (–0.5dB)		73	75		74	76		dB
SINAD								
f = 2.3MHz (–0.5dB)	f_S = 5.12MHz		72			73		dB
f = 100kHz (–0.5dB)			74			75		dB
Aperature Delay Time		–20	–5	+20	✻	✻	✻	ns
Aperature Jitter			3	10		✻	✻	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input	40	60		✻	✻		MHz
Full Power	0dB Input		30		✻	✻		MHz
Overload Recovery Time	2x Full-Scale Input		205	400		✻	✻	ns
OUTPUTS								
Logic Family				TTL Compatible				
Logic Coding	Logic Selectable		Two's Complement or Inverted Two's Complement					
Logic Levels	Logic "LO" I_{OL} = –3.2mA	0	+0.3	+0.5	✻	✻	✻	V
	Logic "HI" I_{OH} = 160µA	+2.4	+3.5	+5.0	✻	✻	✻	V
EOC Delay Time	Data Out to DV		See Timing Diagram: Figure 13					
Tri-State Enable/Disable Time	I_{OL} = –6.4mA, 50% In to 50% Out		37	100		✻	✻	ns
Data Valid Pulse Width			See Timing Diagram: Figure 13					
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	✻	✻	✻	V
$-V_{CC}$		–14.25	–15	–15.75	✻	✻	✻	V
$+V_{DD1}$		+4.75	+5	+5.25	✻	✻	✻	V
$-V_{DD2}$		–4.95	–5.2	–5.46	✻	✻	✻	V
Supply Currents: $+I_{CC}$	Operating		+60			✻	+80	mA
$-I_{CC}$			–60			✻	–80	mA
$+I_{DD1}$[4]			+305			✻	+330	mA
$-I_{DD2}$[5]			–550			✻	–630	mA
Power Consumption	Operating		6.1	6.5		✻	✻	W

✻ Same specifications as next grade to the left.

SPECIFICATIONS (CONT)

ELECTRICAL (FULL TEMPERATURE RANGE SPECIFICATIONS)

At $\pm V_{CC}$ = +15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 5.12MHz sampling rate, output data latched with the convert command, 15-minute warmup, and T_C = T_{MIN} to T_{MAX}, unless otherwise noted.

PARAMETER	CONDITIONS	ADC614JH			ADC614KH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	T_{CASE}	0		+85	✻		✻	°C
TRANSFER CHARACTERISTICS								
Accuracy								
Gain Error	DC		±0.9	±2		±0.4	±1.5	%FSR(1)
Input Offset	DC		±0.5	±2		±0.2	±1.5	%FSR
Differential Linearity Error	f = 100kHz: 100% of all Codes		1.4	2.0		1.0	1.5	LSB
No Missing Codes			Guaranteed			Guaranteed		
Power Supply Rejection	$\Delta+V_{CC}$ = ±5%		±0.04	±0.2		✻	✻	%FSR/%
	$\Delta-V_{CC}$ = ±5%		±0.05	±0.2		✻	✻	%FSR/%
	$\Delta+V_{DD1}$ = ±5%		±0.004	±0.1		✻	✻	%FSR/%
	$\Delta-V_{DD2}$ = ±5%		±0.02	±0.1		✻	✻	%FSR/%
CONVERSION CHARACTERISTICS								
Sample Rate		DC		5.12M	✻		✻	Samples/s
Pipeline Delay			1, 2, or 3 Convert Command Periods					
DYNAMIC CHARACTERISTICS(2)								
Differential Linearity Error	f = 2.3MHz: 100% of all Codes		1.4	2.0		1.0	1.5	LSB
Spurious-Free Dynamic Range (SFDR)								
f = 2.3MHz (–0.5dB)	f_S = 5.12MHz	75			78			dBFS(3)
f = 100kHz (–0.5dB)		77			80			dBFS(3)
Two-Tone Intermodulation Distortion(6)								
f = 2.20MHz (–6.5dB)	f_S = 5.12MHz		–80	–71	–84	–76		dBFS(3)
f = 2.3MHz (–6.5dB)								
Signal-to-Noise Ratio (SNR)								
f = 2.3MHz (–0.5dB)	f_S = 5.12MHz		69			71		dB
f = 100kHz (–0.5dB)			72			74		dB
SINAD								
f = 2.3MHz (–0.5dB)	f_S = 5.12MHz		68			70		dB
f = 100kHz (–0.5dB)			71			73		dB
Aperature Delay Time		–25	–6	+25	✻	✻	✻	ns
Aperature Jitter			3	10		✻	✻	ps rms
Analog Input Bandwidth (–3dB)								
Small Signal	–20dB Input		60					MHz
Full Power	0dB Input		30					MHz
Overload Recovery Time	2x Full Scale Input		220					ns
OUTPUTS								
Logic Levels	Logic "LO" I_{OL} = –3.2mA	0	+0.3	+0.8	✻	✻	✻	V
	Logic "HI" I_{OH} = 160µA	+2.4	+3.5	+5.0	✻	✻	✻	V
EOC Delay Time	Data Out to DV	See Figure 13; Δ Timing Typically Within ±20% Over Temperature						
Tri-State Enable/Disable TIme	I_{OL} = –6.4mA, 50% In to 50% Out		42	100				ns
Data Valid Pulse Width		See Figure 13; Δ Timing Typically Within ±20% Over Temperature						
POWER SUPPLY REQUIREMENTS								
Supply Currents: $+I_{CC}$	Operating		+65	+80		✻	✻	mA
$-I_{CC}$			–61	–80		✻	✻	mA
$+I_{DD1}$(4)			+305	+333		✻	✻	mA
$-I_{DD2}$(5)			–550	–630		✻	✻	mA
Power Consumption	Operating		6.1	6.5		✻	✻	W

✻ Same specifications as next grade to the left.

NOTES: (1) FSR: Full-Scale Range = 2.5Vp-p. (2) Units with lower distortion are available on special order; inquire. (3) dBFS = level referred to full scale. The input signal is within 1 dB of full scale; f = input frequency; f_s = sampling frequency. (4) Pins 3 and 30 (analog typically draw 80% of the total +5V current. Pin 21 (digital) typically draws 20%. (5) Pin 6 (analog) typically draws 45% of the total –5.2V current. Pin 31 (digital) typically draws 55%. (6) SNR and two-tone intermodulation distortion are guaranteed but not 100% tested.

PIN ASSIGNMENTS

1	Common (Analog)	46	Common (Analog)
2	DNC	45	Analog Signal In
3	$+V_{DD1}$ (+5V) Analog	44	$+V_{CC}$ (+15V) Analog
4	S/H Out	43	$-V_{CC}$ (–15V) Analog
5	A/D In	42	NC
6	$-V_{DD2}$ (–5.2V) Analog	41	NC
7	Bit 13	40	NC
8	Bit 14 (LSB)	39	DNC
9	Bit 1 (MSB)	38	DNC
10	Bit 2	37	Gain Adjust
11	Bit 3	36	Offset Adjust
12	Bit 4	35	Common (Analog)
13	Bit 5	34	$+V_{CC}$ (+15V) Analog
14	Bit 6	33	$-V_{CC}$ (–15V) Analog
15	Bit 7	32	Common (Analog)
16	Bit 8	31	$-V_{DD2}$ (–5.2V) Digital
17	Bit 9	30	$+V_{DD1}$ (+5V) Analog
18	Bit 10	29	1 Pipeline Delay Select
19	Bit 11	28	0 Pipeline Delay Select
20	Bit 12	27	Output Logic Invert
21	$+V_{DD1}$ (+5V) Digital	26	Common (Digital)
22	Data Valid Output	25	3-State $\overline{\text{ENABLE}}$
23	Common (Digital-Case)	24	Convert Command In

NOTE: NC = no connection, DNC = do not connect.

ORDERING INFORMATION

ADC614 ( ) H

Basic Model Number

Performance Grade Code
J, K: 0°C to +85°C Case Temperature

Package Code
H: Metal and Ceramic

ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	±16.5V
$+V_{DD1}$	+7.0V
$\pm V_{DD2}$	–7.0V
Analog Input	±5.0V
Logic Input	–0.5V to $+V_{DD1}$
Case Temperature (Operating)	+85°C
Junction Temperature	+100°C
Storage Temperature	–65°C to +125°C

Stresses above these ratings may permanently damage the device.

PACKAGING INFORMATION

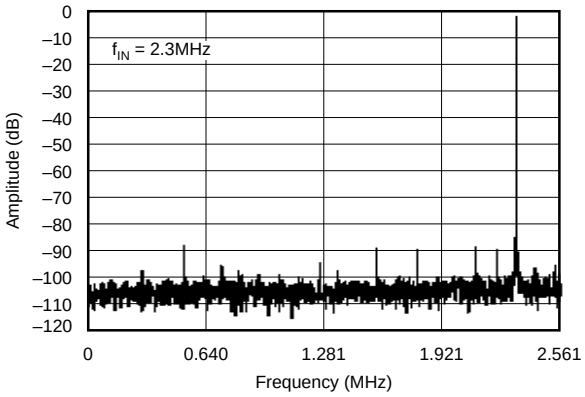
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC614JH	Metal and Ceramic	234
ADC614KH	Metal and Ceramic	234

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

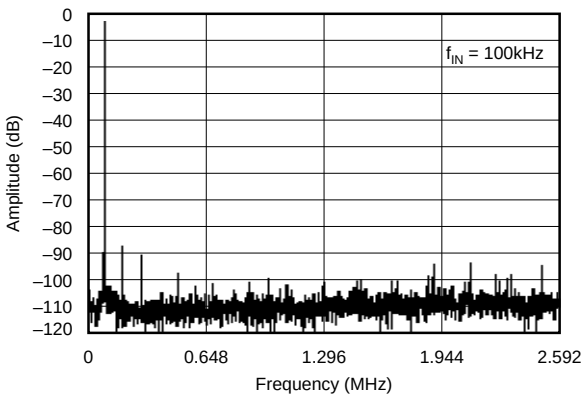
TYPICAL PERFORMANCE CURVES

At $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 5.12MHz sampling rate, 15-minute warmup, and T_C = +25°C, unless otherwise noted.

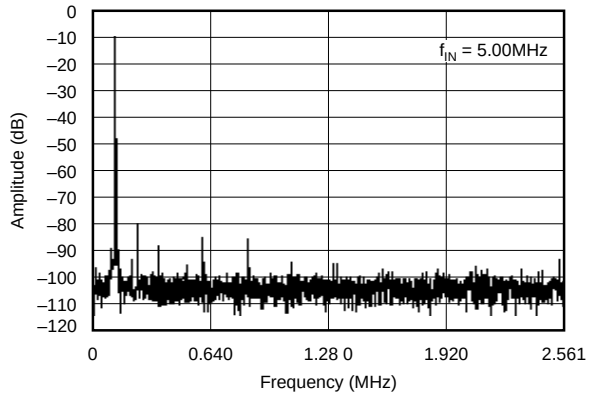
2.3MHz SPECTRAL PERFORMANCE



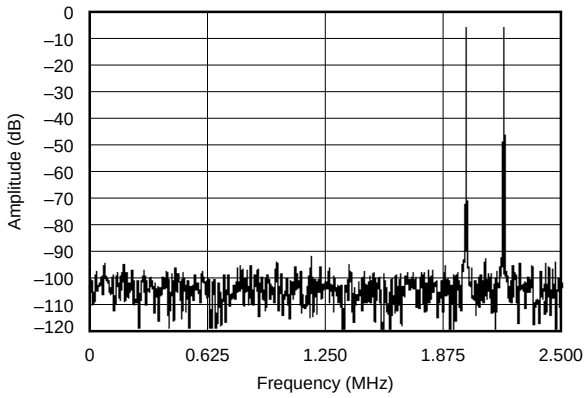
100kHz SPECTRAL PERFORMANCE



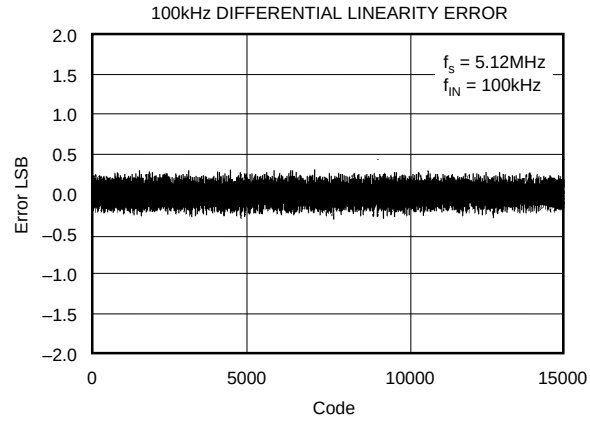
UNDERSAMPLING AT 5.0MHz



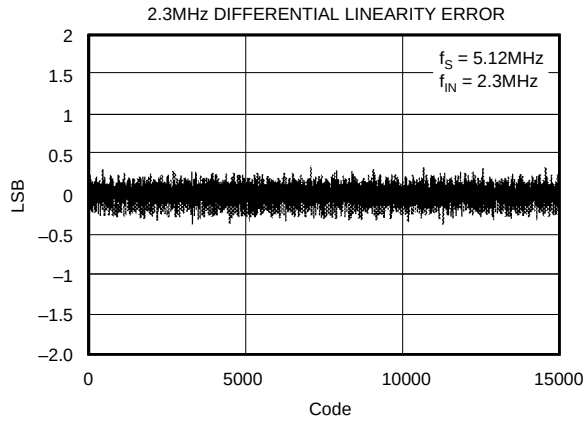
TWO-TONE INTERMODULATION DISTORTION



100kHz DIFFERENTIAL LINEARITY ERROR



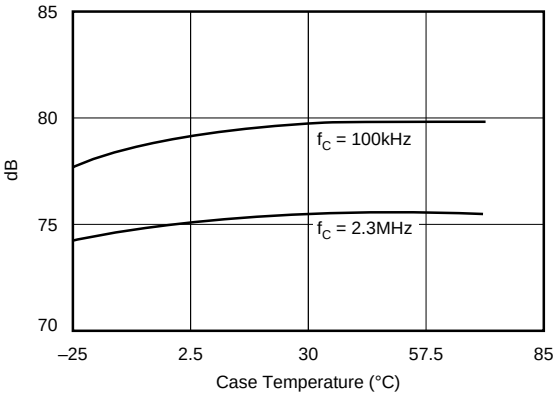
2.3MHz DIFFERENTIAL LINEARITY ERROR



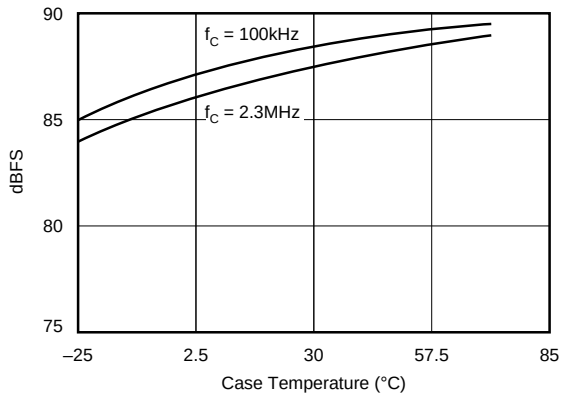
TYPICAL PERFORMANCE CURVES (CONT)

At $\pm V_{CC}$ = ±15V, $+V_{DD1}$ = +5V, $-V_{DD2}$ = –5.2V, R_S = 50Ω, 5.12MHz sampling rate, 15-minute warmup, and T_C = +25°C, unless otherwise noted.

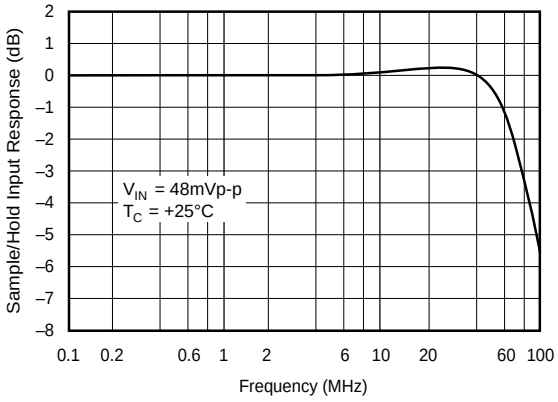
SIGNAL-TO-NOISE RATIO
vs TEMPERATURE



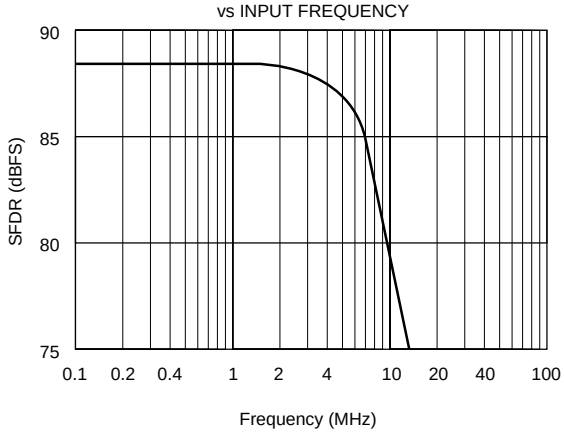
SPURIOUS FREE DYNAMIC RANGE
vs TEMPERATURE



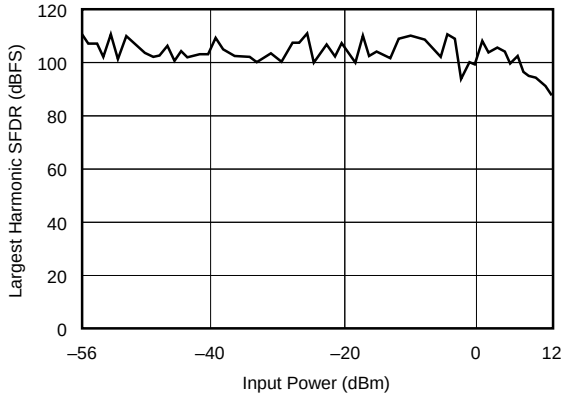
ANALOG INPUT BANDWIDTH



SPURIOUS FREE DYNAMIC RANGE
vs INPUT FREQUENCY



SWEPT POWER AT f_{IN} = 2MHz, f_S = 5MHz



THEORY OF OPERATION

The ADC614 is a two-step subranging analog-to-digital converter. This architecture is shown in Figure 1. The major system building blocks are: sample/hold amplifier, MSB flash encoder, DAC and error amplifier, LSB flash encoder, digital error corrector, and timing circuits. The ADC614 uses hybrid technology with laser-trimmed integrated circuits mounted in a multilayer ceramic package to integrate this complex circuit into a complete analog-to-digital converter subsystem with state-of-the-art performance.

Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high-accuracy) DAC, subtract this voltage from the S/H output, amplify this "remainder," convert to digital with a second coarse ADC, and combine the digital output from the first ADC (MSB) with the digital output from the second ADC (LSB). In practice, however, achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed sample/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter). A diode bridge sampling switch is used to achieve an acceptable compromise between speed and accuracy. The diode bridge switching transients are buffered from the analog input by a high input impedance buffer amplifier. Since the hold capacitor does not appear in the feedback of the diode bridge output buffer, the capacitor can acquire the signal in 65ns. The low-bias-current output buffer is then required to settle to only the resolution (8 bits) of the first (MSB) flash encoder in 65ns, while an additional 85ns is allowed for settling to the resolution (14 bits) of the second (LSB) flash encoder. Sample/Hold droop appears as only an offset error and does not effect linearity.

Both the MSB and the LSB flash encoder (ADC) functions are performed by one 8-bit flash encoder. The DAC voltage reference is also used to generate reference voltages for the MSB and LSB encoder to compensate drift errors. Buffering and scaling amplifiers are laser-trimmed to minimize voltage offset errors and optimize gain (input full-scale range) symmetry.

The subtraction DAC is an ECL 8-bit resolution monolithic DAC with 14-bit accuracy. Laser-trimmed thin-film nichrome resistors and high-speed bipolar circuitry allow the DAC output to settle to 14-bit accuracy in only 35ns.

A "remainder" or coarse conversion-error voltage is generated by resistively subtracting the DAC output from the output of the sample/hold amplifier. Before the second (LSB) conversion, the "remainder" is amplified by a wideband fast-settling two-input amplifier with a gain of 32V/V. To prevent overload on large amplitude transients, the active input is switched off to blank the amplifier input from the beginning of the S/H acquisition time to the end of the MSB encoder update time.

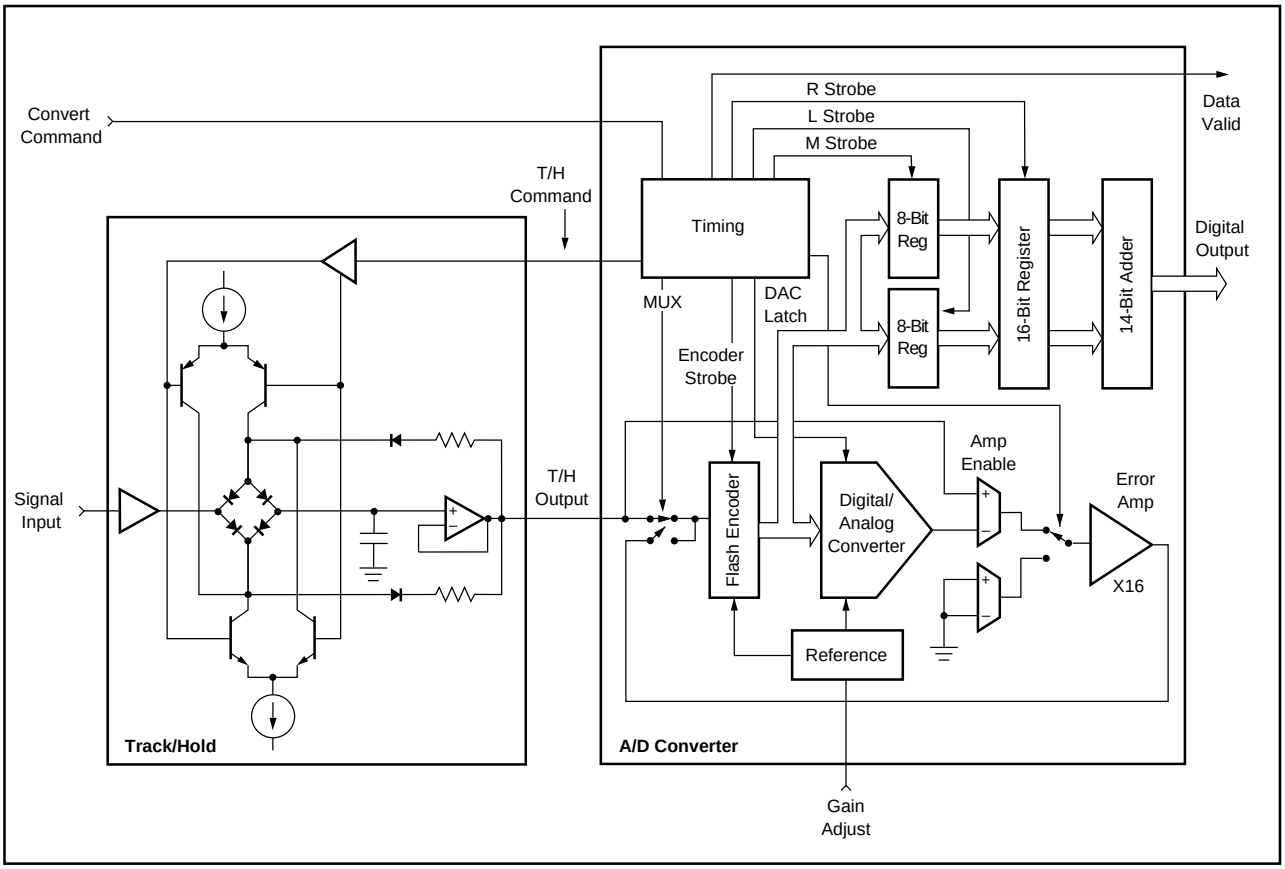


FIGURE 1. ADC614 Block Diagram—A Two-Step Subranging Architecture.

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADC614. Some noncritical timing signals are also generated in the digital error correction circuitry. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages. Basic timing is derived from the output of a three-stage shift register driven by a synchronized 20MHz oscillator.

The convert command pulse is differentiated to allow triggering by pulses from as narrow as 10ns to as wide as 80% duty cycle.

The ADC614 timing technique generates a variable width S/H gate pulse which is determined by the conversion command pulse period minus a fixed 135ns ADC conversion time. ADC614 conversion rates are therefore possible somewhat above the 5.12MHz specification but S/H acquisition time is sacrificed and accuracy is rapidly degraded.

The output of the MSB and LSB encoders are read into separate 8-bit latches. The latched MSB data, along with the latched LSB data, is then read into a 16-bit latch after the leading edge of the LSB strobe and before being applied to the adder, where the actual error correction takes place. These latches eliminate any critical timing problems that could result when the converter is operated at the maximum conversion rate.

The function of the digital error correction circuitry is to assemble the 8-bit words from the two flash encoders into a 14-bit output word.

The 16-bit register output is then sent to a 14-bit adder where the final data output word is created. The MSB data forms the most significant eight bits of a 14-bit word, with the last six bits being assigned zeros. In a similar fashion, the LSB data from the least significant bits forms the other input to the adder, with the first six bits being assigned zeros. As two 14-bit words are being added, the output of the adder could exceed 14 bits in range; however, the final data output is only a 14-bit word, so a means of detecting an overrange is included to prevent reading erroneous data. The converter data output is forced to all ones for a full-scale input or overrange. The data output does not "roll-over" if the converter input exceeds its specified full-scale range of ±l.25V.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADC614 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: spurious free dynamic range (SFDR), signal-to-noise ratio (SNR) or the more severe signal-to-noise-and-distortion ratio (SINAD), and intermodulation distortion (IMD).

A typical test setup for performing high-speed FFT testing of analog-to-digital converters is shown in Figure 2 and 3. Highly accurate phase-locked signal sources allow high resolution FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an integral number of signal frequency periods can be sampled. As no spectral leakage results, a "rectangular" window (no window function) can be used. This was used to generate the typical FFT performance curves shown on page 5.

If generators cannot be phase-locked and set to extreme accuracy, a very low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended.[1] To assure that the majority of codes are exercised in the ADC614 (14 bits), a 4096-point FFT is taken. If the data storage RAM is limited, a smaller FFT may be taken if a sufficient number of samples are averaged (e.g., a l0-sample average of 512-point FFTs).

DYNAMIC PERFORMANCE DEFINITIONS

1. Spurious Free Dynamic Range:

$$\frac{\text{Largest Harmonic Power (first 9 harmonics)}}{\text{Full Scale Power}}$$

2. Intermodulation Distortion (IMD):

$$\frac{\text{Highest IMD Product Power (to 5th-order)}}{\text{Sinewave Signal Power}}$$

3. Signal-to-Noise Ratio (SNR):

$$\frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

4. Signal-to-(Noise + Distortion)[2] Ratio (SINAD):

$$\frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (first 9 harmonics)}}$$

IMD is referenced[3] to the larger of the test signals f_1 or f_2. Five "bins" either side of peak are used for calculation of fundamental and harmonic power. The DC frequency bin is not included in these calculations as it is of little importance in dynamic signal processing applications.

APPLICATION TIPS

Attention to test set-up details can prevent errors that contribute to poor test results. Important points to remember when testing high performance converters are:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the ADC and "hard limit" on signal peaks.

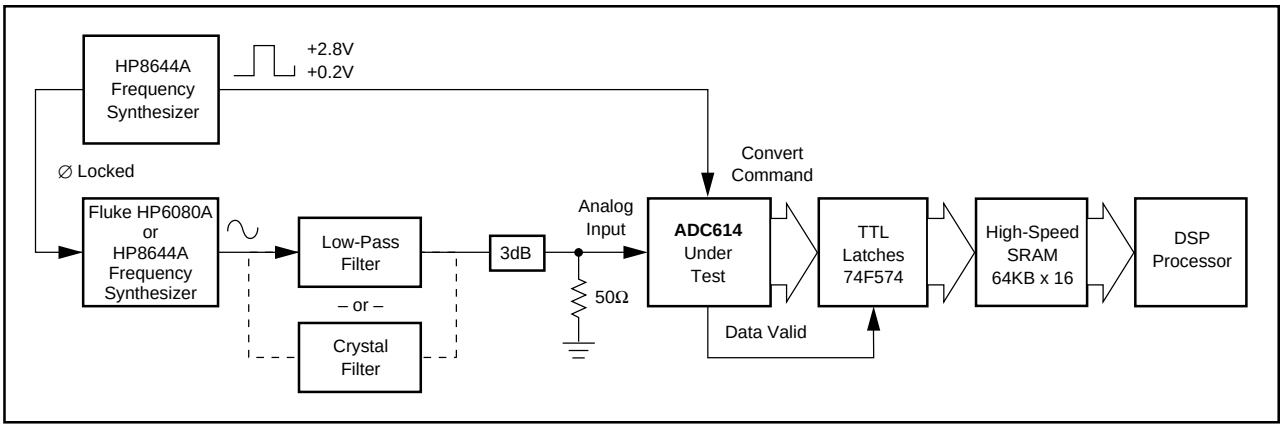


FIGURE 2. Block Diagram of FFT Test for SNR, SFDR and Swept-Power Test.

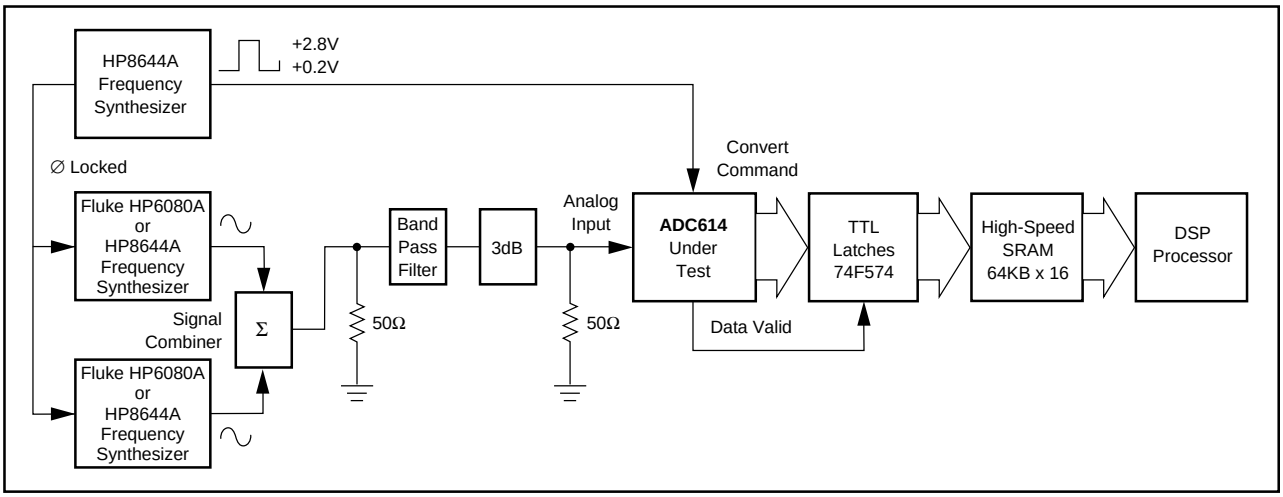
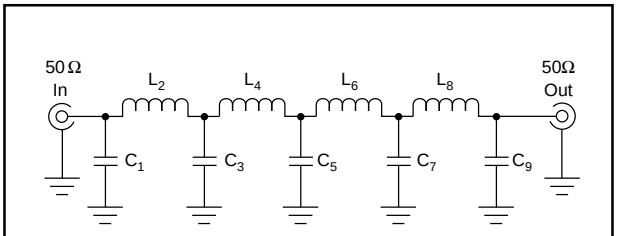


FIGURE 3. Block Diagram of FFT Test for Two-Tone IMD.



9th-Order 0.5dB Ripple
Tchebychev Low-Pass Filter

Attenuation at 2X cutoff frequency = 90dB.

Cutoff frequency = –3dB frequency; to convert cutoff frequency to –0.5dB frequency, multiply all LC values by 0.98997.

Cutoff Freq. (MHz)	C_1 (pF)	C_3 (pF)	C_5 (pF)	C_7 (pF)	C_9 (pF)	L_2 (µH)	L_4 (µH)	L_6 (µH)	L_8 (µH)
2.5	2269	3458	3531	3458	2269	4.11	4.43	4.43	4.11
1.25	4538	6917	7062	6917	4538	8.23	8.86	8.86	8.23
0.625	9077	13,833	14,125	13,833	9077	16.45	17.73	17.73	16.45

FIGURE 4. Ninth-Order Harmonic Filter.

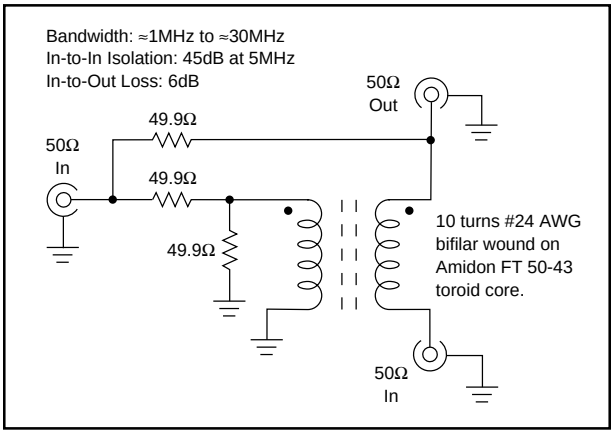


FIGURE 5. Passive Signal Combiner.

2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6B to prevent "hard limiting" on peaks.
3. Low-pass filtering (or bandpass filtering) of test signal generators is absolutely necessary for THD and IMD tests. An easily built LC low-pass filter (Figure 4) will eliminate harmonics from the test signal generator. Care must be taken not to saturate the filter. Saturation of these filters may cause odd order harmonics.
4. Test signal generators must have exceptional noise performance to achieve accurate SNR measurements. Good generators together with fifth-order elliptical bandpass filters are recommended for SNR tests. Recommended generators are the Fluke 6080A or HP8644A. Narrow-bandwidth crystal filters can also be used to filter generator broadband noise, but they should be carefully tested for operation at high levels.
5. The analog input of the ADC614 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω), or it should be driven by a low output impedance buffer such as an OPA642. Short leads are necessary to prevent digital noise pickup.
6. A low-noise (jitter) clock signal (convert command) generator is required for good ADC dynamic performance. A poor generator can seriously impair good SNR performance. A HP 8644A generator is a good clock source. Short leads are necessary to preserve fast TTL rise times.
7. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. A passive (hybrid transformer) signal combiner can also be used (Figure 5) over a range of about 0.lMHz to 30MHz. This combiner's port-to-port isolation will be ≈45dB between signal generators and its input-output insertion loss will be ≈6dB. Distortion will be better than –85dBc.
8. A very low side-lobe window must be used for FFT calculations if generators cannot be phase-locked and set to exact frequencies. A minimum four-sample Blackman-Harris window function is recommended.(l)
9. Floating inputs can eliminate ground-loop noise. A simple common-mode choke shown in Figures 6 and 7, or a single-ended amplifier (Figures 8 and 9) can be used for gain. Optimized harmonic performance can only be achieved with a very low distortion buffer. Burr-Brown OPA642 is an ideal op amp for driving the ADC614.
10. Digital data must be latched into an external TTL 14-bit register, preferably using the convert command pulse (Figures 10 and 11). Latches should be mounted on PC boards in very close proximity to the ADC614. Avoid long leads.
11. Do not overload the data output logic. These outputs are designed to drive two TTL loads. Do not connect ADC614 data output pins directly to a noisy digital bus; use external 3-state logic for noise immunity.
12. A well-designed, clean PC board layout will assure proper operation and clean spectral response.(4, 5) Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy (20 oz. foil) ground planes can give excellent results, if carefully designed.
13. Prototyping "plug-boards" or wire-wrap boards will not be satisfactory.
14. Connect analog and digital ground pins of the ADC614 directly to the ground plane. In our experience, connecting these pins to a common ground plane gives the best results. Analog and digital power supply commons should be tied together at the ground plane. Adding power supply and ground-return filtering(6) is optional and may improve noise rejection. The manual for the evaluation board (DEM-ADC614-E) gives a recommended layout.
15. If using a cable to drive the input of the ADC614, avoid reflections down the cable that could degrade dynamic performance by placing a 3dB attenuator at the end of the cable. Input amplitude should be doubled to maintain signal amplitude.

NOTES:
1. "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", Fredric J. Harris. *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
2. SINAD test includes harmonics whereas SNR does not include these important spurious products.
3. If IMD is referenced to peak envelope power, distortion will be 6dB better.
4. *MECL System Design Handbook*, 3rd Edition, Motorola Corp.
5. Motorola MECL, Motorola Corp.
6. Murata-Erie BNX002-01.

TIMING

The ADC614 generates all necessary timing signals internally. Only timing between Convert Command, Output Data, and Data Valid must be considered. Proper timing is shown in Figures 12 and 13. There are two methods for reading output data, offering three selectable levels of data pipeline delay as described below:

(1) Convert Command timing option (pin 29 = HIGH)— With this option, the Convert Command signal is used both for initiating a new conversion and for reading valid data from a previous conversion. This method is most useful in synchronous systems where data samples are taken continuously. See Figure 12 for timing relationships.

Pin 28 is used to control the amount of pipeling delay. If pin 28 is held LOW, then output data "N-2" will be valid on the rising edge of Convert Command "N". If pin 28 is held

HIGH, then output data "N-3" will be valid on the rising edge of Convert Command "N". These timing relationships are valid at any conversion rate up to 5.12MHz, the data setup time before the rising Convert Command edge is about 50ns.

(2) Data Valid timing option (pin 29 = LOW)—With this option, data from conversion "N" becomes valid after a fixed delay from the rising edge of Convert Command "N". The delay is about 165ns . At about t = 185ns, the Data Valid strobe signal will rise. This strobe signal may be connected directly to the clock input of the external data latches, providing a data setup time of approximately 20ns.

See Figure 13 for timing relationships. Pin 28 must be left HIGH at all times when using the Data Valid timing option.

This method does not require subsequent conversions in order to read the data (i.e., single-shot conversion capability). Therefore, the Data Valid option is useful in systems where the very first data latch output after power-up must represent a valid conversion.

	DATA LATCHED BY CONVERT COMMAND		DATA LATCHED BY DATA VALID STROBE
PIN NUMBER	N-2	N-1	N-1
28	HI	LO	HI
29	HI	HI	LO

TABLE I. Pipeline Delay Selection Logic.

	DIGITAL DATA OUTPUT LOGIC CODING	
INPUT VOLTAGE (EXACT CENTER OF CODE)	BINARY TWO'S COMPLEMENT (BTC) PIN 27 = LO	INVERTED BINARY TWO'S COMPLEMENT ($\overline{BTC}$) PIN 27 = HI
+FS (+1.25V)	01111111111111[1]	10000000000000[1]
+FS –1LSB (+1.24985V)	01111111111111	10000000000000
+FS –2LSB (+1.24969V)	01111111111110	10000000000001
+3/4 FS (+0.9375V)	01100000000000	10011111111111
+1/2 FS (+0.6250V)	01000000000000	10111111111111
+1/4 FS (+0.3125V)	00100000000000	11011111111111
+1LSB (+152µV)	00000000000001	11111111111110
Bipolar Zero (0V)	00000000000000	11111111111111
–1LSB (–152µV)	11111111111111	00000000000000
–1/4 FS (–0.3125V)	11100000000000	00011111111111
–1/2 FS (–0.625V)	11000000000000	00111111111111
–3/4 FS (–0.9375V)	10100000000000	01011111111111
–FS + 1LSB (–1.24985V)	10000000000001	01111111111110
–FS (–1.25V)	10000000000000	01111111111111
	MSB LSB	MSB LSB

NOTE: (1) Indicates overrange condition.

TABLE II. Coding Table for 14-bit ±1.25V ADC Function.

Data should be latched into external TTL latches that can operate reliably with a set-up time of 6ns minimum. Two 74F574 hex latches are recommended.

DATA OUTPUT

Output logic inversion can be accomplished by programming pin 27. Binary Two's Complement or Inverted Binary Two's Complement output data format is available (Table II).

The ADC614 output logic is TTL compatible. The 3-state output is controlled by ENABLE pin 25. For normal operation pin 25 will be tied LO. A logic HI on pin 25 will switch the output data register to a high-impedance state (Figure 14). Output OFF leakage current I_{OZL} and I_{OZH} will be less than 50µA over the converter's specified operating temperature range. The 3-state output should be isolated from noisy digital bus lines as the noise can couple back through the OFF data register and create noise in the ADC.

DIGITAL INPUTS

Logic inputs are TTL compatible. Open inputs will assume a HI logic state; unused inputs may be allowed to float or they may be tied to an appropriate TTL logic level.

OFFSET AND GAIN ADJUSTMENT

The ADC614 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed with external potentiometers (Figure 15). Trim range is typically only 0.1%; large offsets and gain changes should be made

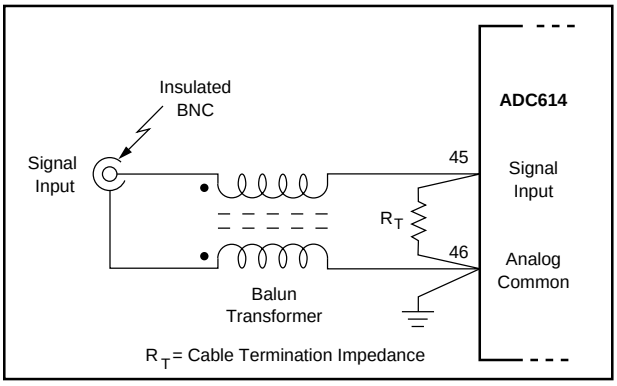


FIGURE 6. Floating-Input Balun Transformer.

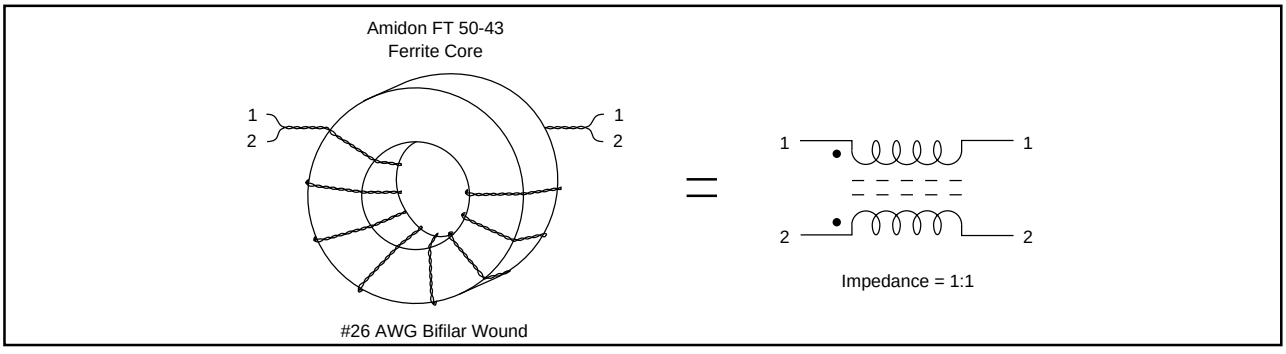


FIGURE 7. Common-Mode Choke Transformer Windings.

elsewhere in the system. Using an input buffer amplifier is the preferred way for injecting offset voltages and making wide gain adjustments.

THERMAL REQUIREMENTS

The ADC614 is tested and specified over a temperature range of 0°C to +85°C. The converters are tested in a forced-air environment with a 10 SCFM air flow. The ADC614 can be operated in a normal convection ambient air environment, provided the case temperature does not exceed the upper limit of its specification.

Proper heat transfer can be assured by placing a small heat sink (#0808HS) and an appropriately sized piece of 10mil. Berquist Sil-Pad 400 between the unit and PC board ground plane. Refer to Figure 16 for details.

High junction temperature can be avoided by using forced-air cooling, but it is not required at moderate ambient temperatures. Thermal resistance of the ADC614 package is: θ_{JC} = 4.8°C/W. measured to the underside of the case.

NOISE FIGURE

The noise figure is defined as the degradation of signal-to-noise ratio as an analog input is processed through the ADC614. An approximation of the noise figure of the ADC614 can be derived from the SNR specifications.

The signal-to-noise ratio of the ADC614 is measured typically at 78dB. The full-scale input signal of the ADC614 is +12dBm, so the noise level at the output of the ADC614 is –66dBm for the 2.56MHz band. The input noise is derived from the formula:

$$N = 10\log (4kTB/0.001) = -168dBm$$

The noise figure can be calculated using the following equation:

$$NF = \text{output noise} - (10\log BWo/BWi) - \text{input noise}$$

$$NF = -66dB - 64dB - (-168dB) = 38dB$$

An important consideration when using the Noise Figure for an analog-to-digital converter is the effect of input signal range on the noise figure. As the input range increases, the noise figure directly decreases. When the input is grounded, the RMS noise of the ADC614 is 72µV, and 99.7% of all codes will fall within a span of four codes. This figure represents the entire noise contribution of the ADC614.

CUSTOM SCREENING OPTIONS

Custom screened versions of the ADC614 are available. Screening may include extended temperature ranges, higher guaranteed dynamic specifications, additional environmental screens, higher sampling rates, etc. Inquire with your local sales representative or contact factory.

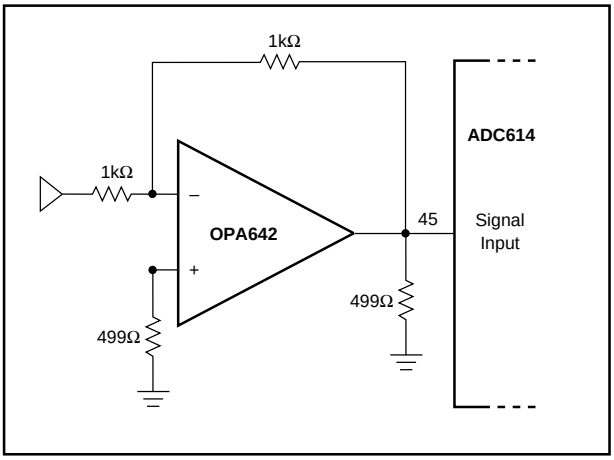


FIGURE 8. Single Ended Input Amplifier (Gain = –1V/V).

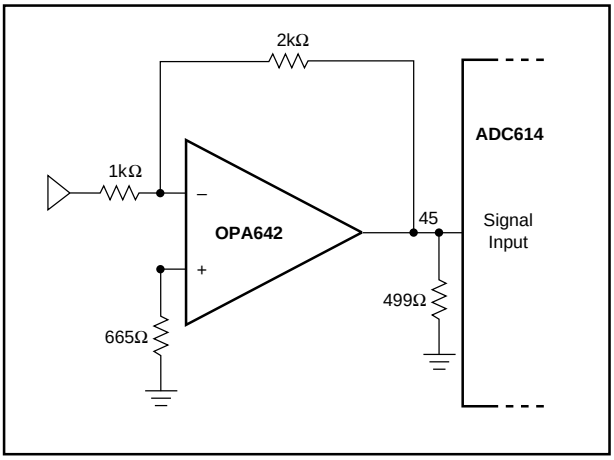


FIGURE 9. Single Ended Input Low Noise Amplifier (Gain = –2V/V).

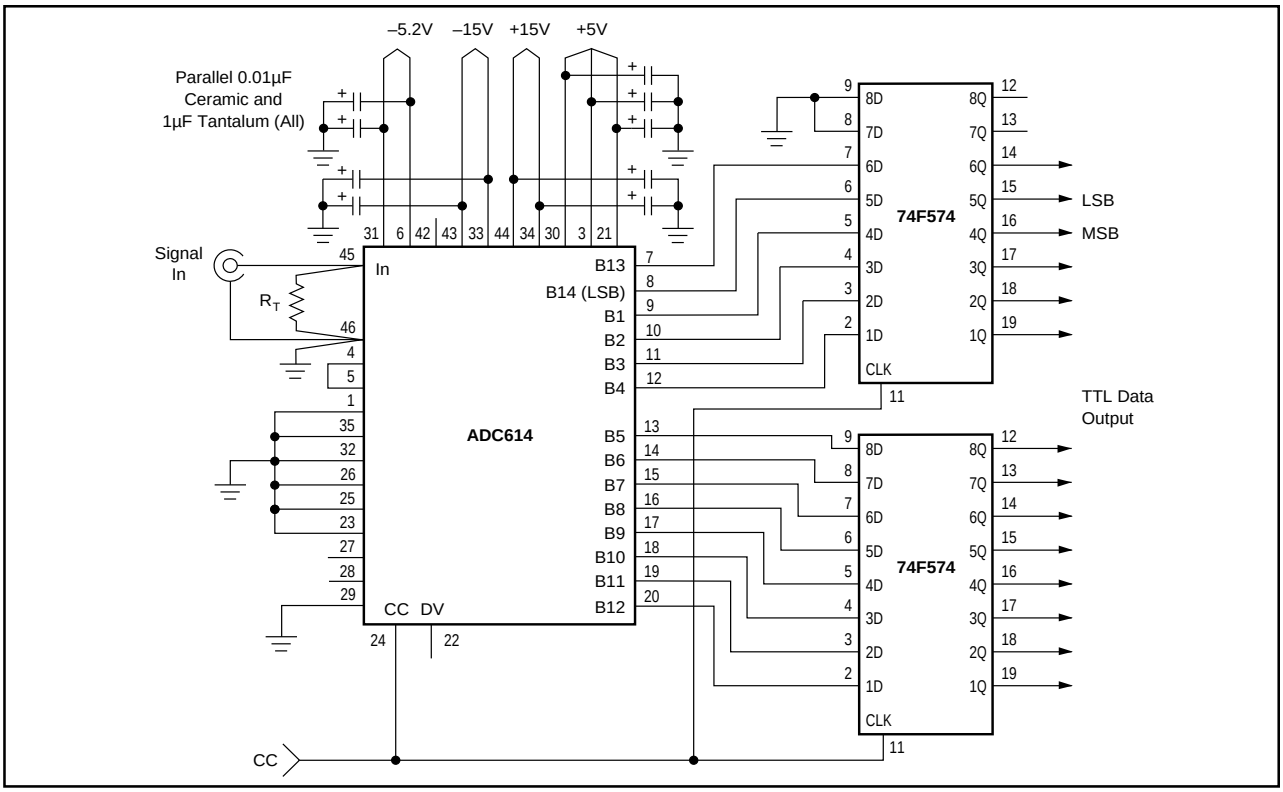


FIGURE 10. Interface Circuit—Digital Output Strobed by Convert Command. Supply connection shown: power supplies and grounds shared by analog and digital pins using common ground plane. Optimum noise performance is achieved when strobing the output data with the convert command.

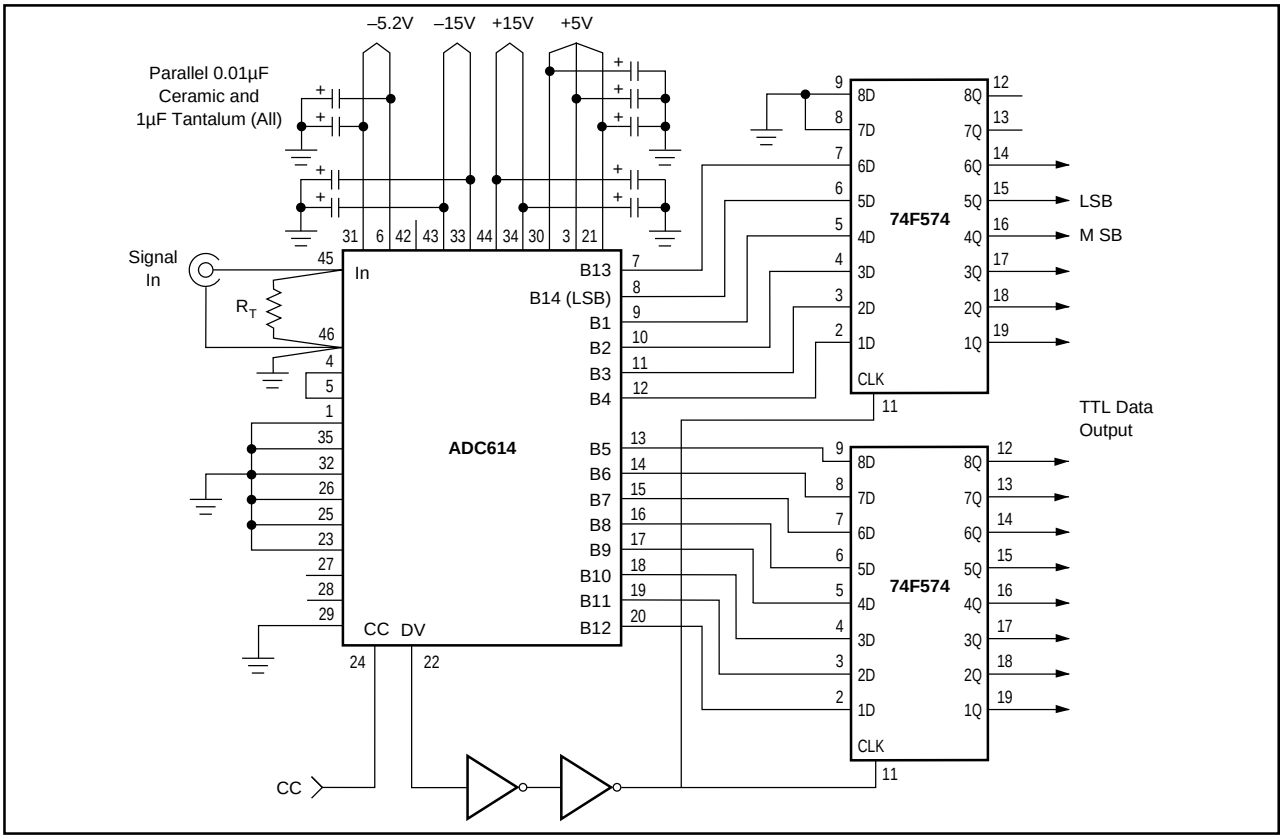
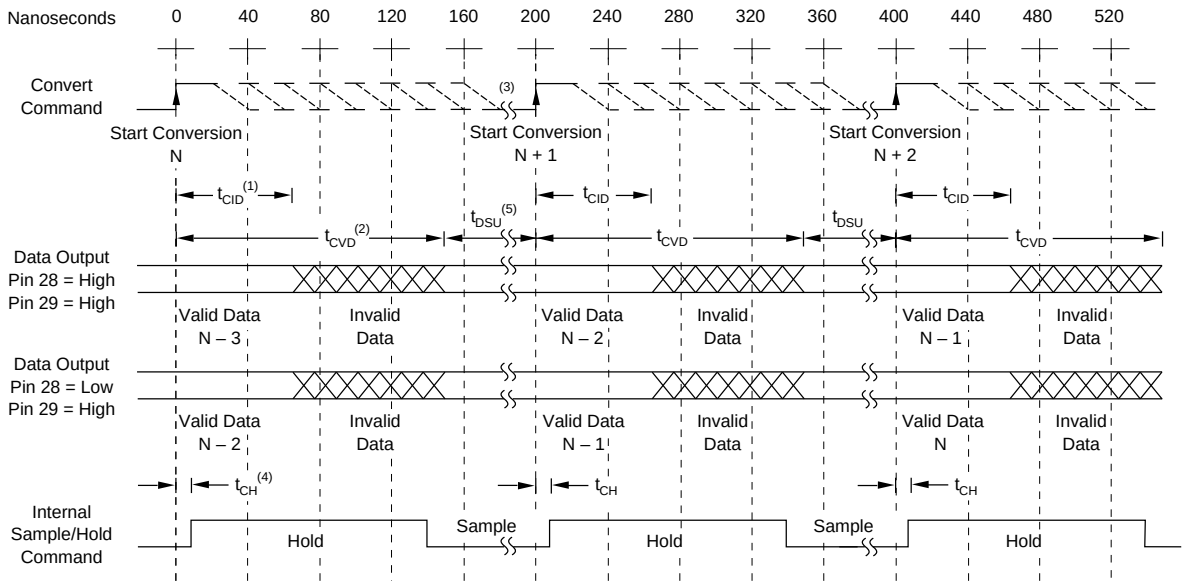


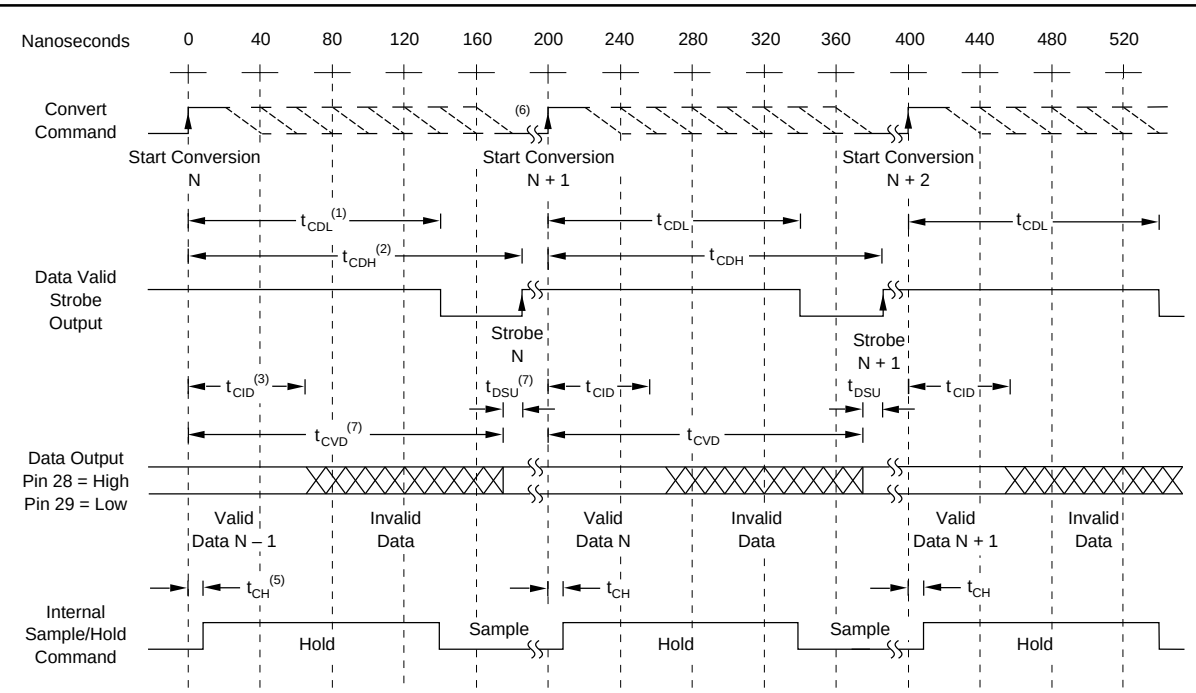
FIGURE 11. Interface Circuit—Digital Output Strobed by Data Valid Pulse. Supply connection shown: power supplies and grounds shared by analog and digital pins, using common ground plane.



NOTES: (1) t_{CID} = delay time from Convert Command to Invalid Data. Typical value = 65ns. Independent of conversion rate. (2) t_{CVD} = Delay time from Convert Command to Valid Data. Typical Value = 150ns. Independent of conversion rate. (3) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (4) t_{CH} = delay time from Convert Command to the internal hold command. Typical value = 6ns. Independent of conversion rate. (5) t_{DSU} = data set-up time. This depends on conversion rate and may be calculated by:

$$t_{DSU} = \frac{1}{f_{SAMPLE}} - t_{CVD}$$

FIGURE 12. Convert Command Strobe Timing for a 5MHz Conversion Rate.



NOTES: (1) t_{CDL} = delay time from Convert Command to the falling edge of Data Valid strobe. Typical value = 140ns. Independent of conversion rate. (2) t_{CDH} = delay time from Convert Command to the rising edge of Data Valid strobe. Typical value = 195ns. Independent of conversion rate. (3) t_{CID} = delay time from Convert Command to Invalid Data. Typical value = 65ns. Independent of conversion rate. (4) t_{CVD} = delay time from Convert Command to Valid Data. Typical Value = 188ns. Independent of conversion rate. (5) t_{CH} = delay time from Convert Command to the internal hold command. Typical value = 6ns. Independent of conversion rate. (6) The ⟆ symbol indicates the portion of the waveform that will "stretch out" at lower conversion rates. (7) t_{DSU} = data setup time. Typical value = 7ns. Independent of conversion rate.

FIGURE 13. Data Valid Strobe Timing for a 5MHz Conversion Rate.

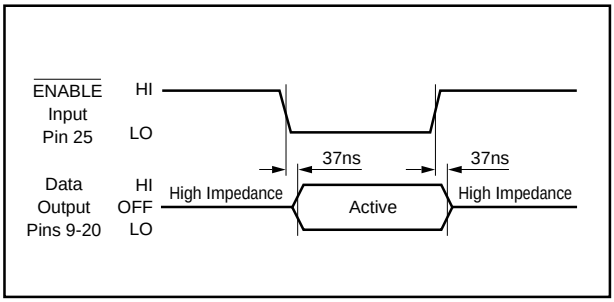


FIGURE 14. Digital Data 3-State Output.

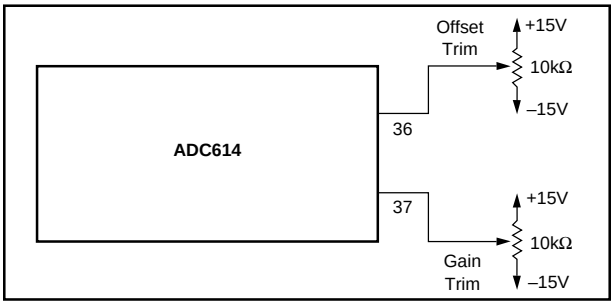


FIGURE 15. Optional Gain and Offset Trim.

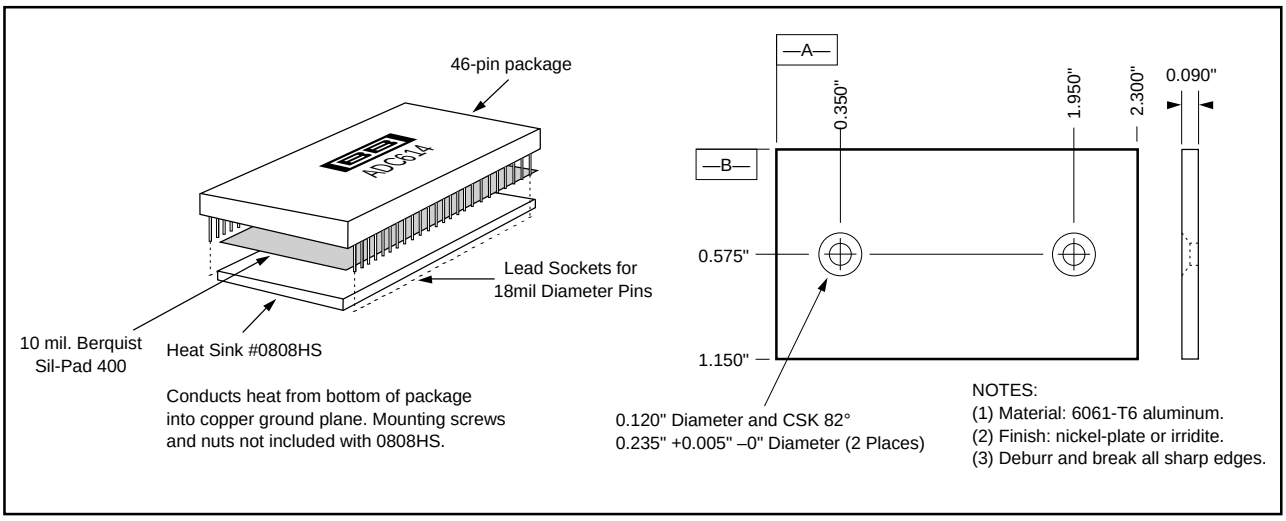


FIGURE 16. Heat Sink Transfers Heat from the DIP Package into a Copper Ground Plane.