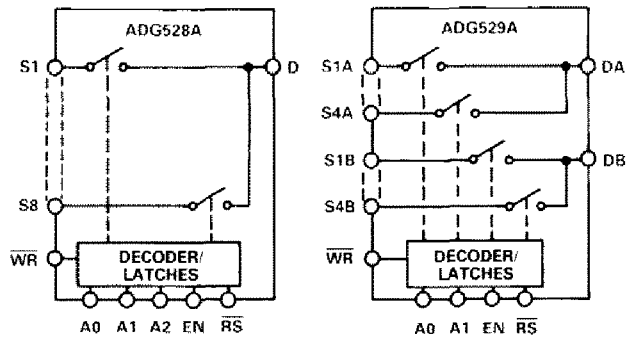
ANALOG DEVICES

# CMOS
# Latched 4/8 Channel Analog Multiplexers

## ADG528A/ADG529A

**FEATURES**
**44V Supply Maximum Rating**
**$V_{SS}$ to $V_{DD}$ Analog Signal Range**
**Single/Dual Supply Specifications**
**Wide Supply Ranges (10.8V to 16.5V)**
**Microprocessor Compatible (100ns $\overline{WR}$ Pulse)**
**Extended Plastic Temperature Range**
**(−40°C to +85°C)**
**Low Leakage (20pA typ)**
**Low Power Dissipation (28mW max)**
**Available in 16-Lead DIP and**
**20-Lead LCCC/PLCC Packages**
**Superior Alternative to:**
**DG528**
**DG529**

**FUNCTIONAL BLOCK DIAGRAMS**




## GENERAL DESCRIPTION

The ADG528A and ADG529A are CMOS monolithic analog multiplexers with 8 channels and dual 4 channels respectively. On-chip latches facilitate microprocessor interfacing. The ADG528A switches one of 8 inputs to a common output depending on the state of three binary addresses and an enable input. The ADG529A switches one of 4 differential inputs to a common differential output depending on the state of two binary addresses and an enable input. Both devices have TTL and 5V CMOS logic compatible digital inputs.

The ADG528A and ADG529A are designed on an enhanced LC$^2$MOS process which gives an increased signal capability of $V_{SS}$ to $V_{DD}$ and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8V to 16.5V single or dual supply range. These multiplexers also feature high switching speeds and low $R_{ON}$.

## PRODUCT HIGHLIGHTS

1. Single/Dual Supply Specifications with a Wide Tolerance:
   The devices are specified in the 10.8V to 16.5V range for both single and dual supplies.
2. Easily Interfaced:
   The ADG528A and ADG529A can be easily interfaced with microprocessors. The $\overline{WR}$ signal latches the state of the address control lines and the enable line. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off). $\overline{RS}$ can be tied to the microprocessor reset pin.
3. Extended Signal Range:
   The enhanced LC$^2$MOS processing results in a high breakdown and an increased analog signal range of $V_{SS}$ to $V_{DD}$.
4. Break-Before-Make Switching:
   Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
5. Low Leakage:
   Leakage currents in the range of 20pA make these multiplexers suitable for high precision circuits.

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Option[2] |
|---|---|---|
| ADG528AKN | −40°C to +85°C | N-28 |
| ADG528AKP | −40°C to +85°C | P-20A |
| ADG528ABQ | −40°C to +85°C | Q-18 |
| ADG528ATQ[3] | −55°C to +125°C | Q-18 |
| ADG528ATE[3] | −55°C to +125°C | E-20A |
| ADG529AKN | −40°C to +85°C | N-18 |
| ADG529AKP | −40°C to +85°C | P-20A |
| ADG529ABQ | −40°C to +85°C | Q-18 |
| ADG529ATQ[3] | −55°C to +125°C | Q-18 |
| ADG529ATE[3] | −55°C to +125°C | E-20A |

NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. See Analog Devices Military Products Databook (1990) for military data sheet.
[2]E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip.

REV. A



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# ADG528A/ADG529A—SPECIFICATIONS

## Dual Supply ($V_{DD}$ = +10.8V to +16.5V, $V_{SS}$ = −10.8V to −16.5V unless otherwise noted.)

| Parameter | ADG528A ADG529A K Version +25°C | ADG528A ADG529A K Version −40°C to +85°C | ADG528A ADG529A B Version +25°C | ADG528A ADG529A B Version −40°C to +85°C | ADG528A ADG529A T Version +25°C | ADG528A ADG529A T Version −55°C to +125°C | Units | Comments |
|---|---|---|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | | | | |
| Analog Signal Range | $V_{SS}$ $V_{DD}$ | $V_{SS}$ $V_{DD}$ | $V_{SS}$ $V_{DD}$ | $V_{SS}$ $V_{DD}$ | $V_{SS}$ $V_{DD}$ | $V_{SS}$ $V_{DD}$ | V min V max | |
| $R_{ON}$ | 280 | | 280 | | 280 | | Ω typ | −10V≤$V_S$≤+10V, $I_{DS}$ = 1mA; Test Circuit 1 |
| | 450 | 600 | 450 | 600 | 450 | 600 | Ω max | |
| | 300 | 400 | 300 | 400 | | | Ω max | $V_{DD}$ = 15V(±10%), $V_{SS}$ = −15V(±10%) |
| | | | | | 300 | 400 | Ω max | $V_{DD}$ = 15V(±5%), $V_{SS}$ = −15V(±5%) |
| $R_{ON}$ Drift | 0.6 | | 0.6 | | 0.6 | | %/°C typ | −10V≤$V_S$≤+10V, $I_{DS}$ = 1mA |
| $R_{ON}$ Match | 5 | | 5 | | 5 | | % typ | −10V≤$V_S$≤+10V, $I_{DS}$ = 1mA |
| $I_S$(OFF), Off Input Leakage | 0.02 | | 0.02 | | 0.02 | | nA typ | V1 = ±10V, V2 = ∓10V; Test Circuit 2 |
| | 1 | 50 | 1 | 50 | 1 | 50 | nA max | |
| $I_D$(OFF), Off Output Leakage | 0.04 | | 0.04 | | 0.04 | | nA typ | V1 = ±10V, V2 = ∓10V; Test Circuit 3 |
| ADG528A | 1 | 100 | 1 | 100 | 1 | 100 | nA max | |
| ADG529A | 1 | 50 | 1 | 50 | 1 | 50 | nA max | |
| $I_D$(ON), On Channel Leakage | 0.04 | | 0.04 | | 0.04 | | nA typ | V1 = ±10V, V2 = +10V; Test Circuit 4 |
| ADG528A | 1 | 100 | 1 | 100 | 1 | 100 | nA max | |
| ADG529A | 1 | 50 | 1 | 50 | 1 | 50 | nA max | |
| $I_{DIFF}$, Differential Off Output Leakage (ADG529A only) | | 25 | | 25 | | 25 | nA max | V1 = ±10V, V2 = ∓10V; Test Circuit 5 |
| DIGITAL CONTROL | | | | | | | | |
| $V_{INH}$, Input High Voltage | | 2.4 | | 2.4 | | 2.4 | V min | |
| $V_{INL}$, Input Low Voltage | | 0.8 | | 0.8 | | 0.8 | V max | |
| $I_{INL}$ or $I_{INH}$ | | 1 | | 1 | | 1 | μA max | $V_{IN}$ = 0 to $V_{DD}$ |
| $C_{IN}$ Digital Input Capacitance | 8 | | 8 | | 8 | | pF max | |
| DYNAMIC CHARACTERISTICS[1] | | | | | | | | |
| $t_{TRANSITION}$ | 200 | | 200 | | 200 | | ns typ | V1 = ±10V, V2 = ∓10V; Test Circuit 6 |
| | 300 | 400 | 300 | 400 | 300 | 400 | ns max | |
| $t_{OPEN}$ | 50 | | 50 | | 50 | | ns typ | Test Circuit 7 |
| | 25 | 10 | 25 | 10 | 25 | 10 | ns min | |
| $t_{ON}$(EN, $\overline{WR}$) | 200 | | 200 | | 200 | | ns typ | Test Circuits 8 and 9 |
| | 300 | 400 | 300 | 400 | 300 | 400 | ns max | |
| $t_{OFF}$(EN, $\overline{RS}$) | 200 | | 200 | | 200 | | ns typ | Test Circuits 8 and 10 |
| | 300 | 400 | 300 | 400 | 300 | 400 | ns max | |
| $t_W$ Write Pulse Width | 100 | 120 | 100 | 120 | 100 | 130 | ns min | See Figure 1 |
| $t_S$ Address, Enable Setup Time | | 100 | | 100 | | 100 | ns min | See Figure 1 |
| $t_H$ Address, Enable Hold Time | | 10 | | 10 | | 10 | ns min | See Figure 1 |
| $t_{RS}$ Reset Pulse Width | | 100 | | 100 | | 100 | ns min | See Figure 2 |
| OFF Isolation | 68 | | 68 | | 68 | | dB typ | $V_{EN}$ = 0.8V, $R_L$ = 1kΩ, $C_L$ = 15pF, |
| | 50 | | 50 | | 50 | | dB min | $V_S$ = 7V rms, f = 100kHz |
| $C_S$(OFF) | 5 | | 5 | | 5 | | pF typ | $V_{EN}$ = 0.8V |
| $C_D$(OFF) | | | | | | | | |
| ADG528A | 22 | | 22 | | 22 | | pF typ | $V_{EN}$ = 0.8V |
| ADG529A | 11 | | 11 | | 11 | | pF typ | |
| $Q_{INJ}$, Charge Injection | 4 | | 4 | | 4 | | pC typ | $R_S$ = 0Ω, $V_S$ = 0V; Test Circuit 11 |
| POWER SUPPLY | | | | | | | | |
| $I_{DD}$ | 0.6 | | 0.6 | | 0.6 | | mA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | 1.5 | | 1.5 | | 1.5 | mA max | |
| $I_{SS}$ | 20 | | 20 | | 20 | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | 0.2 | | 0.2 | | 0.2 | mA max | |
| Power Dissipation | 10 | | 10 | | 10 | | mW typ | |
| | | 28 | | 28 | | 28 | mW max | |

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

## Single Supply ($V_{DD}$ = +10.8V to +16.5V, $V_{SS}$ = GND = 0V unless otherwise noted.)

| Parameter | ADG528A ADG529A K Version +25°C | ADG528A ADG529A K Version −40°C to +85°C | ADG528A ADG529A B Version +25°C | ADG528A ADG529A B Version −40°C to +85°C | ADG528A ADG529A T Version +25°C | ADG528A ADG529A T Version −55°C to +125°C | Units | Comments |
|---|---|---|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | | | | |
| Analog Signal Range | GND | GND | GND | GND | GND | GND | V min | |
| | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | V max | |
| $R_{ON}$ | 500 | | 500 | | 500 | | Ω typ | GND≤$V_S$≤+10V, $I_{DS}$ = 0.5mA; Test Circuit 1 |
| | 700 | 1000 | 700 | 1000 | 700 | 1000 | Ω max | |
| $R_{ON}$ Drift | 0.6 | | 0.6 | | 0.6 | | %/°C typ | GND≤$V_S$≤+10V, $I_{DS}$ = 0.5mA |
| $R_{ON}$ Match | 5 | | 5 | | 5 | | % typ | GND≤$V_S$≤+10V, $I_{DS}$ = 0.5mA |
| $I_S$(OFF), Off Input Leakage | 0.02 | | 0.02 | | 0.02 | | nA typ | V1 = +10V/GND, V2 = GND/+10V |
| | 1 | 50 | 1 | 50 | 1 | 50 | nA max | Test Circuit 2 |
| $I_D$(OFF), Off Output Leakage | 0.04 | | 0.04 | | 0.04 | | nA typ | V1 = +10V/GND, V2 = GND/+10V |
| ADG528A | 1 | 100 | 1 | 100 | 1 | 100 | nA max | Test Circuit 3 |
| ADG529A | 1 | 50 | 1 | 50 | 1 | 50 | nA max | |
| $I_D$(ON), On Channel Leakage | 0.04 | | 0.04 | | 0.04 | | nA typ | V1 = +10V/GND, V2 = GND/+10V |
| ADG528A | 1 | 100 | 1 | 100 | 1 | 100 | nA max | Test Circuit 4 |
| ADG529A | 1 | 50 | 1 | 50 | 1 | 50 | nA max | |
| $I_{DIFF}$, Differential Off Output Leakage (ADG529A only) | | 25 | | 25 | | 25 | nA max | V1 = +10V/GND, V2 = GND/+10V Test Circuit 5. |
| DIGITAL CONTROL | | | | | | | | |
| $V_{INH}$, Input High Voltage | | 2.4 | | 2.4 | | 2.4 | V min | |
| $V_{INL}$, Input Low Voltage | | 0.8 | | 0.8 | | 0.8 | V max | |
| $I_{INL}$ or $I_{INH}$ | | 1 | | 1 | | 1 | μA max | $V_{IN}$ = 0 to $V_{DD}$ |
| $C_{IN}$ Digital Input Capacitance | 8 | | 8 | | 8 | | pF max | |
| DYNAMIC CHARACTERISTICS[1] | | | | | | | | |
| $t_{TRANSITION}$ | 300 | | 300 | | 300 | | ns typ | V1 = +10V/GND, V2 = GND/+10V; Test Circuit 6 |
| | 450 | 600 | 450 | 600 | 450 | 600 | ns max | |
| $t_{OPEN}$ | 50 | | 50 | | 50 | | ns typ | Test Circuit 7 |
| | 25 | 10 | 25 | 10 | 25 | 10 | ns min | |
| $t_{ON}$(EN, $\overline{WR}$) | 250 | | 250 | | 250 | | ns typ | Test Circuits 8 and 9 |
| | 450 | 600 | 450 | 600 | 450 | 600 | ns max | |
| $t_{OFF}$(EN, $\overline{RS}$) | 250 | | 250 | | 250 | | ns typ | Test Circuits 8 and 10 |
| | 450 | 600 | 450 | 600 | 450 | 600 | ns max | |
| $t_W$ Write Pulse Width | 100 | 120 | 100 | 120 | 100 | 130 | ns min | See Figure 1 |
| $t_S$ Address, Enable Setup Time | | 100 | | 100 | | 100 | ns min | See Figure 1 |
| $t_H$ Address, Enable Hold Time | | 10 | | 10 | | 10 | ns min | See Figure 1 |
| $t_{RS}$ Reset Pulse Width | | 100 | | 100 | | 100 | ns min | See Figure 2 |
| OFF Isolation | 68 | | 68 | | 68 | | dB typ | $V_{EN}$ = 0.8V, $R_L$ = 1kΩ, $C_L$ = 15pF, |
| | 50 | | 50 | | 50 | | dB min | $V_S$ = 3.5V rms, f = 100kHz |
| $C_S$(OFF) | 5 | | 5 | | 5 | | pF typ | $V_{EN}$ = 0.8V |
| $C_D$(OFF) | | | | | | | | |
| ADG528A | 22 | | 22 | | 22 | | pF typ | $V_{EN}$ = 0.8V |
| ADG529A | 11 | | 11 | | 11 | | pF typ | |
| $Q_{INJ}$, Charge Injection | 4 | | 4 | | 4 | | pC typ | $R_S$ = 0Ω, $V_S$ = 0V; Test Circuit 11 |
| POWER SUPPLY | | | | | | | | |
| $I_{DD}$ | 0.6 | | 0.6 | | 0.6 | | mA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | 1.5 | | 1.5 | | 1.5 | mA max | |
| Power Dissipation | 11 | | 11 | | 11 | | mW typ | |
| | | 25 | | 25 | | 25 | mW max | |

NOTE
[1]Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS***
($T_A$ = +25°C unless otherwise noted)

| | |
|---|---|
| $V_{DD}$ to $V_{SS}$ | 44V |
| $V_{DD}$ to GND | 25V |
| $V_{SS}$ to GND | −25V |
| Analog Inputs[1] | |
| Voltage at S, D | $V_{SS}$ −2V to $V_{DD}$ +2V or 20mA, Whichever Occurs First |
| Continuous Current, S or D | 20mA |
| Pulsed Current S or D | |
| 1ms Duration, 10% Duty Cycle | 40mA |
| Digital Inputs[1] | |
| Voltage at A, EN, $\overline{WR}$, $\overline{RS}$ | $V_{SS}$ −4V to $V_{DD}$ +4V or 20mA, Whichever Occurs First |
| Power Dissipation (Any Package) | |
| Up to +75°C | 470mW |
| Derates above +75°C by | 6mW/°C |
| Operating Temperature | |
| Commerical (K Version) | −40°C to +85°C |
| Industrial (B Version) | −40°C to +85°C |
| Extended (T Version) | −55°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10sec) | +300°C |

NOTE
[1]Overvoltage at A, EN, $\overline{WR}$, $\overline{RS}$, S or D will be clamped by diodes. Current should be limited to the maximum rating above.

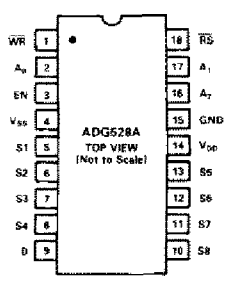
*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

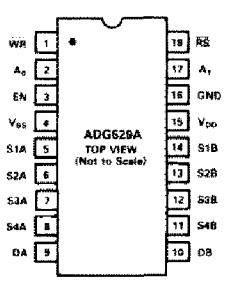
**CAUTION**

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

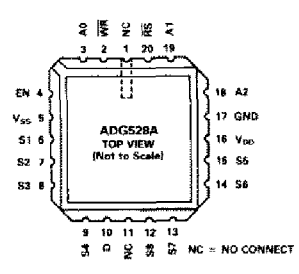

**PIN CONFIGURATIONS**

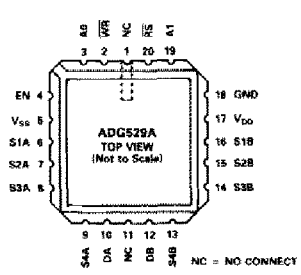
DIP



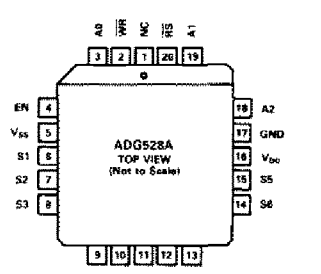



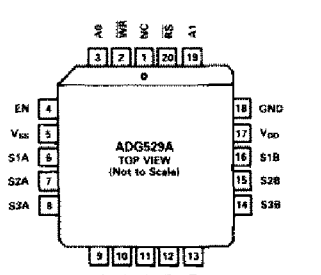

LCCC




PLCC




**TRUTH TABLES**

| A2 | A1 | A0 | EN | $\overline{WR}$ | $\overline{RS}$ | ON SWITCH PAIR |
|---|---|---|---|---|---|---|
| X | X | X | X | ↓ | 1 | Retains Previous Switch Condition |
| X | X | X | X | X | 0 | NONE (Address and Enable Latches Cleared) |
| X | X | X | 0 | 0 | 1 | NONE |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 2 |
| 0 | 1 | 0 | 1 | 0 | 1 | 3 |
| 0 | 1 | 1 | 1 | 0 | 1 | 4 |
| 1 | 0 | 0 | 1 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 0 | 1 | 8 |

X = Don't Care *ADG528A*

| A1 | A0 | EN | $\overline{WR}$ | $\overline{RS}$ | ON SWITCH PAIR |
|---|---|---|---|---|---|
| X | X | X | ↓ | 1 | Retains Previous Switch Condition |
| X | X | X | X | 0 | NONE (Address and Enable Latches Cleared) |
| X | X | 0 | 0 | 1 | NONE |
| 0 | 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 2 |
| 1 | 0 | 1 | 0 | 1 | 3 |
| 1 | 1 | 1 | 0 | 1 | 4 |

X = Don't Care *ADG529A*

## TIMING DIAGRAMS

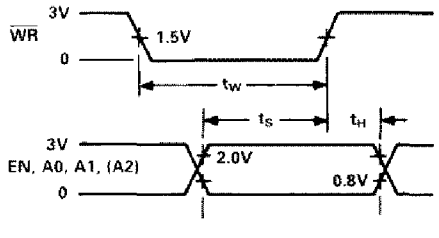



*Figure 1*

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

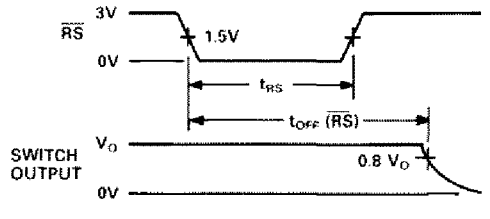


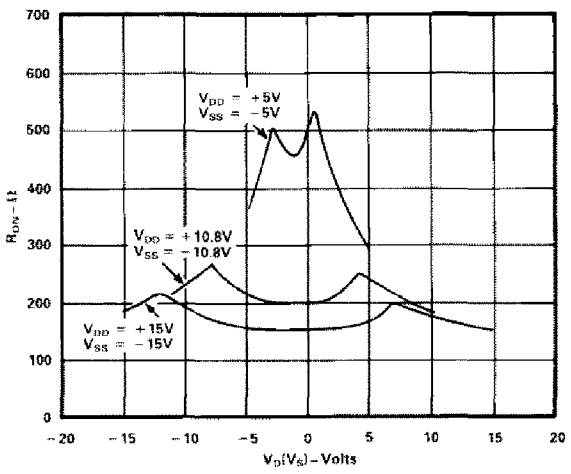

*Figure 2*

Figure 2 shows the Reset Pulse Width, $t_{RS}$, and Reset Turn-off Time, $t_{OFF}$ ($\overline{RS}$).

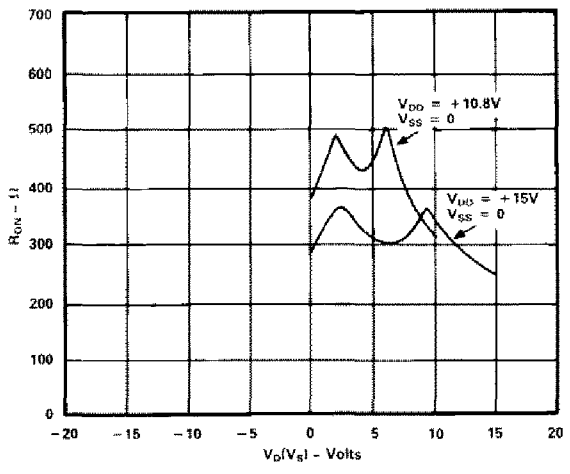
Note: All digital input signals rise and fall times measured from 10% to 90% of 3V. $t_R = t_F = 20ns$.

# Typical Performance Characteristics

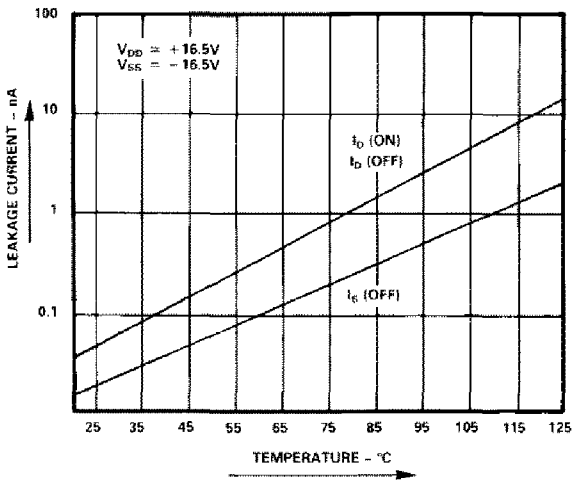
The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5V.



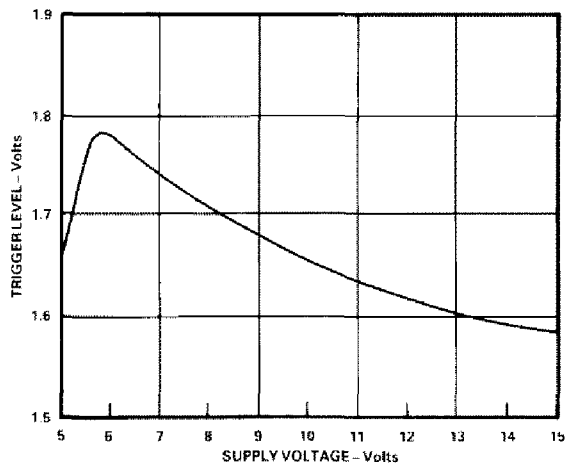

*$R_{ON}$ as a Function of $V_D(V_S)$: Dual Supply Voltage, $T_A$ = +25°C*



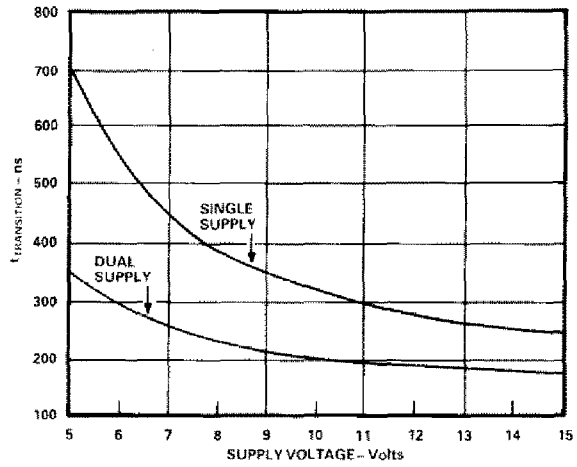

*$R_{ON}$ as a Function of $V_D(V_S)$: Single Supply Voltage, $T_A$ = +25°C*



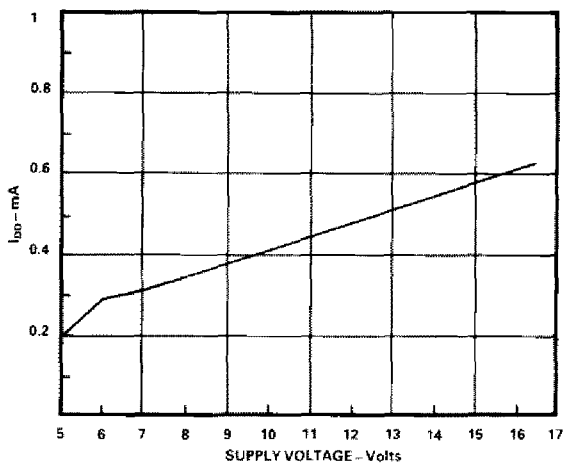

*Leakage Current as a Function of Temperature (Note: Leakage Currents Reduce as the Supply Voltages Reduce)*




*Trigger Levels vs. Power Supply Voltage, Dual or Single Supply, $T_A$ = +25°C*



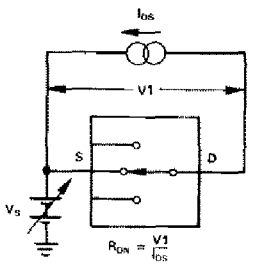

*$t_{TRANSITION}$ vs. Supply Voltage: Dual and Single Supplies, $T_A$ = +25°C*
*(Note: For $V_{DD}$ and $|V_{SS}| < 10V$; V1 = $V_{DD}/V_{SS}$, V2 = $V_{SS}/V_{DD}$. See Test Circuit 6)*



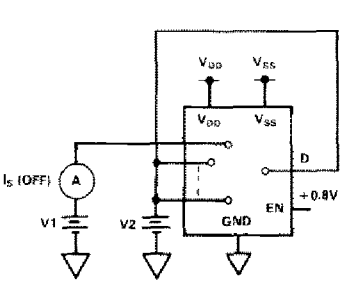

*$I_{DD}$ vs. Supply Voltage: Dual or Single Supply, $T_A$ = +25°C*

## Test Circuits

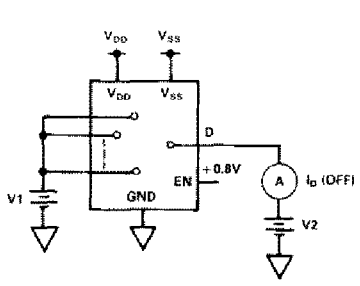
**TEST CIRCUIT 1**
**$R_{ON}$**



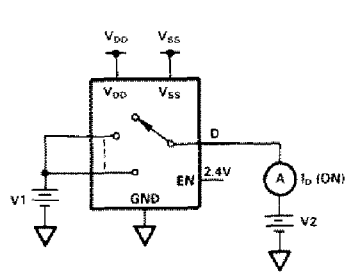

**TEST CIRCUIT 2**
**$I_S$(OFF)**



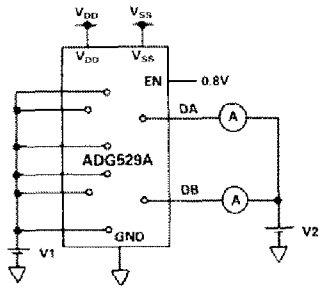

**TEST CIRCUIT 3**
**$I_D$(OFF)**




**TEST CIRCUIT 4**
**$I_D$(ON)**

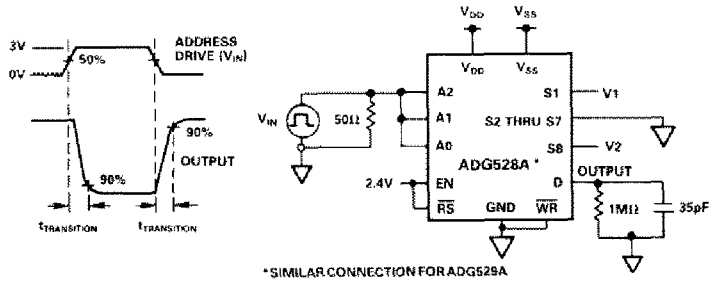



**TEST CIRCUIT 5**
**$I_{DIFF}$**

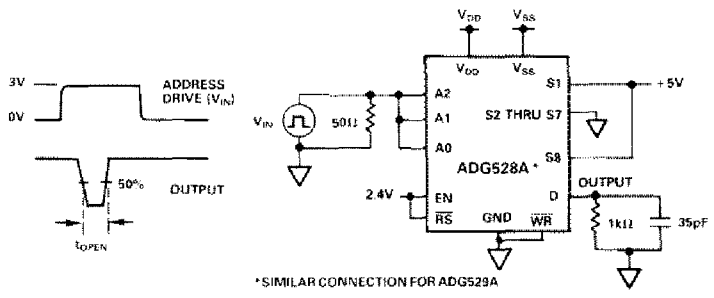



$I_{DIFF} = I_{DA}(OFF) - I_{DB}(OFF)$

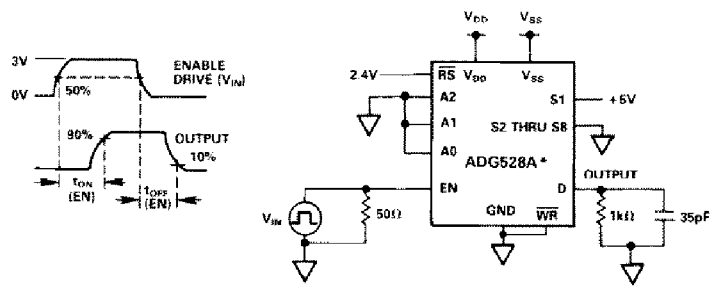
**TEST CIRCUIT 6**
**SWITCHING TIME OF MULTIPLEXER, $t_{TRANSITION}$**




**TEST CIRCUIT 7**
**BREAK-BEFORE-MAKE DELAY, $t_{OPEN}$**

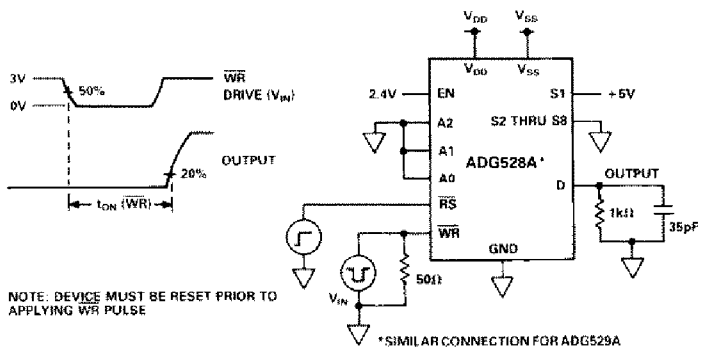


## TEST CIRCUIT 8
## ENABLE DELAY, $t_{ON}$ (EN), $t_{OFF}$ (EN)

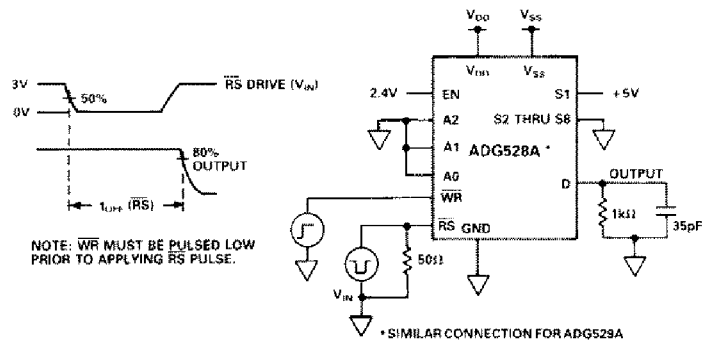



*SIMILAR CONNECTION FOR ADG529A

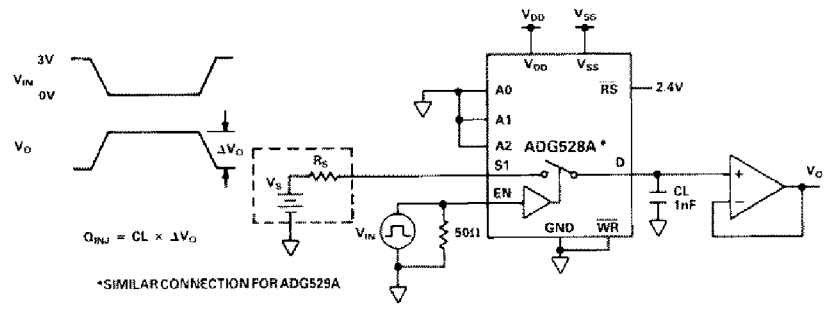
## TEST CIRCUIT 9
## WRITE TURN-ON TIME, $t_{ON}$ ($\overline{WR}$)




## TEST CIRCUIT 10
## RESET TURN-OFF TIME, $t_{OFF}$ ($\overline{RS}$)




## TEST CIRCUIT 11
## CHARGE INJECTION



### TERMINOLOGY

| | |
|---|---|
| $R_{ON}$ | Ohmic resistance between terminals D and S |
| $R_{ON}$ Match | Difference between the $R_{ON}$ of any two channels |
| $R_{ON}$ Drift | Change in $R_{ON}$ versus temperature |
| $I_S$ (OFF) | Source terminal leakage current when the switch is off |
| $I_D$ (OFF) | Drain terminal leakage current when the switch is off |
| $I_D$ (ON) | Leakage current that flows from the closed switch into the body |
| $V_S$ ($V_D$) | Analog voltage on terminal S or D |
| $C_S$ (OFF) | Channel input capacitance for "OFF" condition |
| $C_D$ (OFF) | Channel output capacitance for "OFF" condition |
| $C_{IN}$ | Digital input capacitance |
| $t_{ON}$ (EN) | Delay time between the 50% and 90% points of the digital input and switch "ON" condition |
| $t_{OFF}$ (EN) | Delay time between the 50% and 10% points of the digital input and switch "OFF" condition |
| $t_{TRANSITION}$ | Delay time between the 50% and 90% points of the digital inputs and switch "ON" condition when switching from one address state to another |
| $t_{OPEN}$ | "OFF" time measured between 50% points of both switches when switching from one address state to another |
| $V_{INL}$ | Maximum input voltage for Logic "0" |
| $V_{INH}$ | Minimum input voltage for Logic "1" |
| $I_{INL}$ ($I_{INH}$) | Input current of the digital input |
| $V_{DD}$ | Most positive voltage supply |
| $V_{SS}$ | Most negative voltage supply |
| $I_{DD}$ | Positive supply current |
| $I_{SS}$ | Negative supply current |

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## MECHANICAL INFORMATION
### OUTLINE DIMENSIONS