Dual PWM Fan Controller and Temperature Monitor for Servers

Preliminary Technical Data — ADM1029

FEATURES

Programmable and Automatic Fan Speed Control

Fan Speed Measurement

Supports Backup and Redundant Fans

Supports Hot Swapping of Fans

Cascadable Fault Output Allows Linking of Multiple ADM1029s

Remote and Local Temperature Monitoring

Small 24 pin QSOP Package

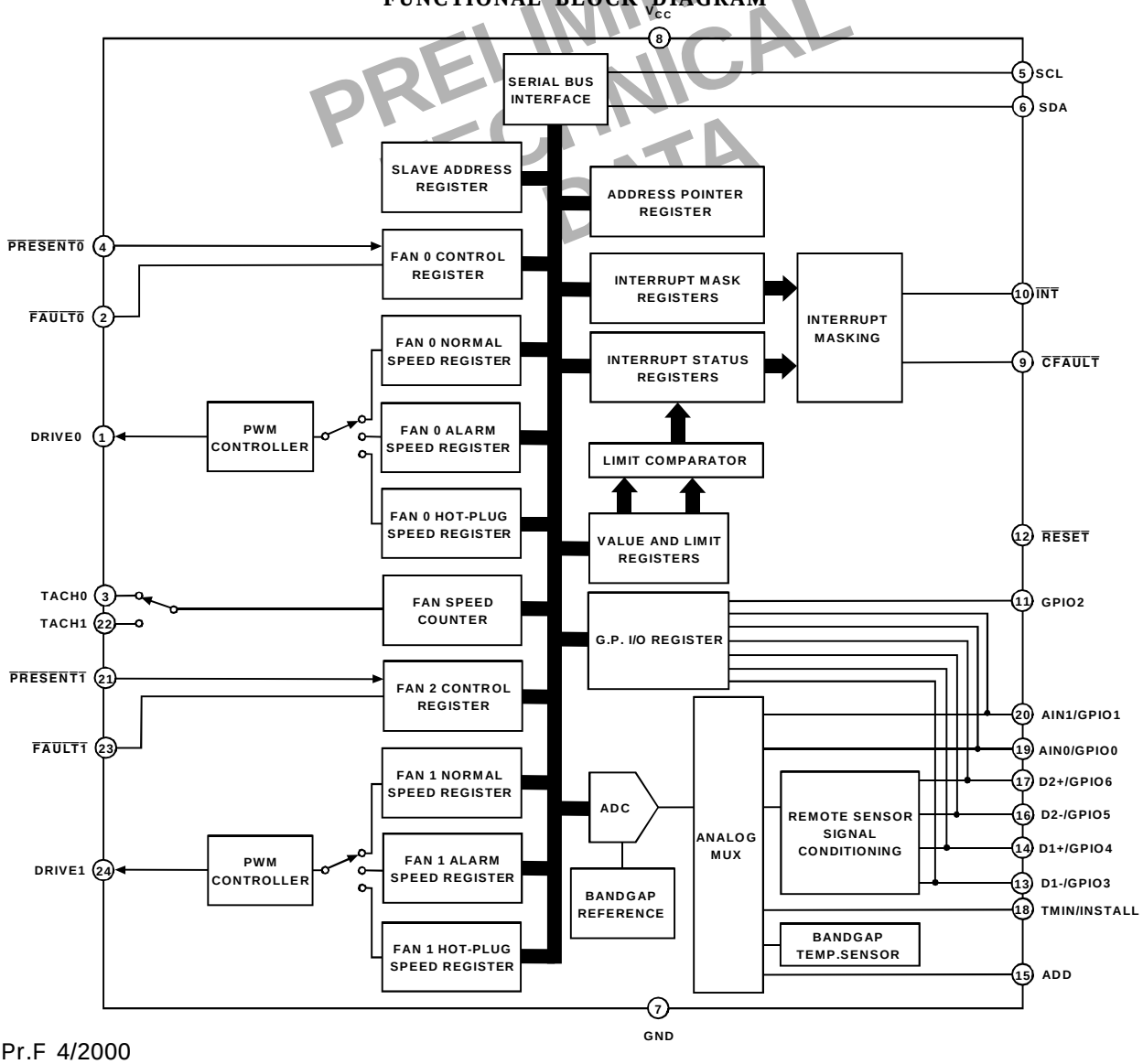
APPLICATIONS

Network Servers and Personal Computers

Microprocessor-Based Office Equipment

Test Equipment and Measuring Instruments

FUNCTIONAL BLOCK DIAGRAM



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

PRODUCT DESCRIPTION

The ADM1029 is a versatile fan controller and monitor for use in personal computers, servers, network hubs, or any system where reliable control and monitoring of multiple cooling fans is required. Each ADM1029 can control the speed of one or two fans and can measure the speed of fans that have a tachometer output. The ADM1029 can also measure the temperature of one or two external sensing diodes or an internal temperature sensor, allowing fan speed to be adjusted to keep system temperature within acceptable limits. The ADM1029 has FAULT inputs for use with fans that can signal failure conditions, and inputs to detect if fans are connected or not.

The ADM1029 communicates with the host processor over an SMBus/I^2C-compatible serial bus. It supports 8 different serial bus addresses, so that up to 8 devices can be connected to a single serial bus segment, controlling up to 16 fans.

The ADM1029 has an interrupt output ($\overline{INT}$) that allows it to signal fault conditions to the host processor. It also has a separate, cascadable fault output ($\overline{CFAULT}$) that allows the ADM1029 to signal a fault condition to other ADM1029s.

The ADM1029 has a number of useful features including automatic temperature control option implemented in hardware with no software requirement, automatic use of backup fans in the event of fan failure, and supports hot-swapping of failed fans.

ADM1029–SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
POWER SUPPLY					
Supply Voltage, V_{CC}	2.8	3.30	6	V	
Supply Current, I_{CC}		1.4	2.0	mA	Interface Inactive, ADC Active
		1.0		mA	ADC Inactive, DAC Active
		32	100	µA	Shutdown Mode
TEMP. -TO-DIGITAL CONVERTER					
Internal Sensor Accuracy		±1	±3	°C	
Resolution		1		°C	
External Diode Sensor Accuracy		±3	±5	°C	0 °C ≤ T_A ≤ +100°C
Resolution		1		°C	
Remote Sensor Source Current	60	90	130	µA	High Level
	3.5	5.5	7.5	µA	Low Level
ANALOG-TO-DIGITAL CONVERTER					
Total Unadjusted Error, TUE			±2	%	Note 3
Differential Non-Linearity, DNL			±1	LSB	
Power Supply Sensitivity		±1		%/V	
Conversion Time (Analog Input or Int.Temp)		11.6		ms	
Conversion Time (External Temperature)		185.6		ms	
Input Resistance (AIN0/1)		High Resistance			
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy			±6	%	
Full-Scale Count			255		
FAN0 and FAN1 Nominal Input RPM		8800		RPM	Divisor = 1, Fan Count = 153
(Note 4)		4400		RPM	Divisor = 2, Fan Count = 153
		2200		RPM	Divisor = 4, Fan Count = 153
		1100		RPM	Divisor = 8, Fan Count = 153
Internal Clock Frequency	56.4	60.0	63.6	kHz	

Specifications (Continued)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	I_{OUT} = 3.0mA, V_{CC} = 2.85V - 3.60V
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = -3.0mA, V_{CC} = 2.85V - 3.60V
OPEN-DRAIN DIGITAL OUTPUTS ($\overline{INT}$, $\overline{CFAULT}$)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = -3.0mA, V_{CC} = 3.60V
High Level Output Current, I_{OH}		0.1	100	µA	$V_{OUT} = V_{CC}$
$\overline{RESET}$ And CI Pulse Width	20	45		ms	
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}			0.4	V	I_{OUT} = -3.0mA, V_{CC} = 2.85V - 3.60V
High Level Output Current, I_{OH}		0.1	100	µA	$V_{OUT} = V_{CC}$
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}	2.2			V	
Input Low Voltage, V_{IL}			0.8	V	
Hysteresis		500		mV	
DIGITAL INPUT LOGIC LEVELS $\overline{RESET}$, GPIO1-6,FAULT0/1, TACH0/1 SHDN, PRESENT0/1					
Input High Voltage, V_{IH}	2.2			V	V_{CC} = 2.85V - 5.5V
Input Low Voltage, V_{IL}			0.8	V	V_{CC} = 2.85V - 5.5V
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	-1			µA	$V_{IN} = V_{CC}$
Input Low Current, I_{IL}			1	µA	V_{IN} = 0
Input Capacitance, C_{IN}		20		pF	
SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}			400	kHz	See Figure 1
Glitch Immunity, t_{SW}			50	ns	See Figure 1
Bus Free Time, t_{BUF}	1.3			µs	See Figure 1
Start Setup Time, $t_{SU;STA}$	600			ns	See Figure 1
Start Hold Time, $t_{HD;STA}$	600			ns	See Figure 1
SCL Low Time, t_{LOW}	1.3			µs	See Figure 1
SCL High Time, t_{HIGH}	0.6			µs	See Figure 1
SCL, SDA Rise Time, t_r			300	ns	See Figure 1
SCL, SDA Fall Time, t_f			300	ns	See Figure 1
Data Setup Time, $t_{SU;DAT}$	100			ns	See Figure 1
Data Hold Time, $t_{HD;DAT}$			900	ns	See Figure 1

NOTES

1 All voltages are measured with respect to GND, unless otherwise specified

2 Typicals are at T_A=25°C and represent most likely parametric norm. Shutdown current typ is measured with V_{CC} = 3.3V

3 TUE (Total Unadjusted Error) includes Offset, Gain and Linearity errors of the ADC and multiplexer.

4 The total fan count is based on 2 pulses per revolution of the fan tachometer output.

5 Timing specifications are tested at logic levels of V_{IL} = 0.8V for a falling edge and V_{IH} = 2.2V for a rising edge.

ABSOLUTE MAXIMUM RATINGS*

Positive Supply Voltage (V_{CC}) ..... 6.5 V
Voltage on Pin 13, 14, 15, 16, 17, 18 . . -0.3V to (V_{CC}+0.3V)
Voltage on Any Other Input or Output Pin . . -0.3V to 6.5V
Input Current at any pin (Note 2) ..... ±5mA
Package Input Current (Note 2) ..... ±20mA
Maximum Junction Temperature ($T_J$max) ..... 150 °C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature, Soldering
Vapor Phase 60 sec ..... +215°C
Infra-Red 15 sec ..... +200°C
ESD Rating all pins ..... 2000 V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

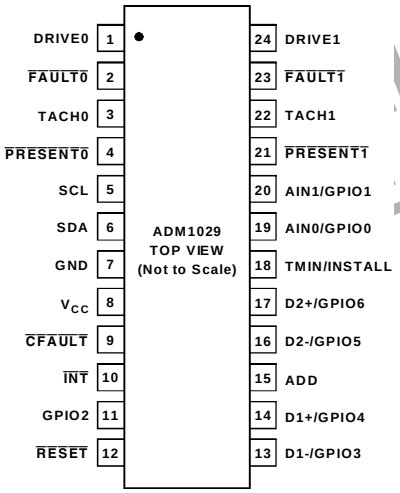
THERMAL CHARACTERISTICS

24-QSOP Package:
θ_{JA} = 105°C/Watt, θ_{JC} = 39°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1029ARQ	0°C to +100°C	24-Pin QSOP Package	RQ-24

PIN CONFIGURATION



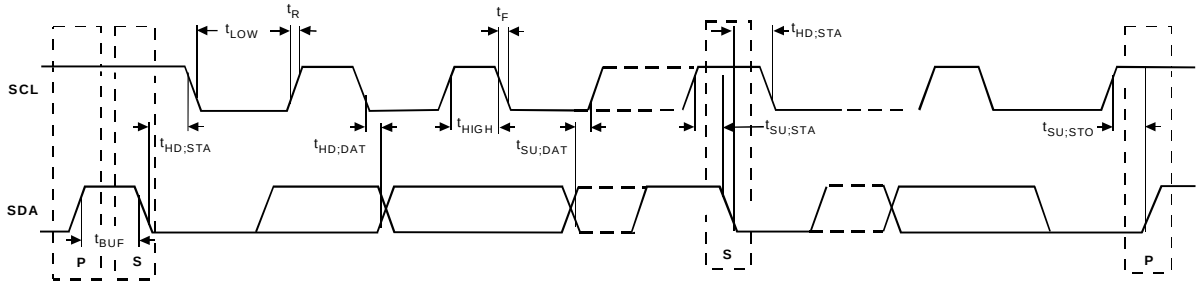


Figure 1. Diagram for Serial Bus Timing

PIN FUNCTION DESCRIPTION

PIN NO.	MNEMONIC	DESCRIPTION
1	DRIVE0	Digital Output. Pulse-Width Modulated (PWM) output to control the speed of fan 0.
2	$\overline{\text{FAULT0}}$	Digital I/O. When used with a fan having a fault output, a logic 0 input to this pin signals a fault on fan 0. Also used as a fault output.
3	TACH0	Digital Input. Digital fan tachometer input for fan 0. Will accept logic signals up to +5V even when V_{CC} is lower than 5V.
4	$\overline{\text{PRESENT0}}$	Digital Input. A shorting link in the fan connector holds this pin low when fan 0 is connected.
5	SCL	Digital Input. Serial Bus Clock.
6	SDA	Digital I/O. Serial Bus bidirectional data. Open-drain output.
7	GND	System Ground.
8	V_{CC}	POWER (+2.8V to +5.5V). Typically powered from +3.3V power rail. Bypass with the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors.
9	$\overline{\text{CFAULT}}$	Digital I/O. Cascade fault input/output used for fault signalling between ADM1029s.
10	$\overline{\text{INT}}$	Digital Output. Interrupt Request (open drain). The output is enabled when Bit 1 of the Configuration Register is set to 0. The default state is enabled.
11	GPIO2	Digital I/O. General-purpose logic I/O pin.
12	$\overline{\text{RESET}}$	Digital Input. Active low reset input.
13	D1-/GPIO3	Analog Input/Digital I/O. Connected to cathode of external temperature sensing diode, or may be re-configured as a general-putpose logic input/output.
14	D1+/GPIO4	Analog Input/Digital I/O. Connected to anode of external temperature sensing diode, or may be re-configured as a general-putpose logic input/output.
15	ADD	8-level Analog Input. Used to set the three LSBs of the serial bus address.
16	D2-/GPIO5	Analog Input/Digital I/O. Connected to cathode of external temperature sensing diode, or may be re-configured as a general-putpose logic input/output.
17	D2+/GPIO6	Analog Input/Digital I/O. Connected to anode of external temperature sensing diode, or may be re-configured as a general-putpose logic input/output.
18	TMIN/INSTALL	8-level Analog Input. The voltage on this pin defines if automatic fan speed control is enabled, the minimum temperature at which the fan(s) will turn on in automatic speed control mode, and also the number of fans that should be installed.
19	AIN0/GPIO0	Analog Input/Digital I/O. May be configured as a 0 to +2.5V analog input or as a general-purpose digital I/O pin.
20	AIN1/GPIO1	Analog Input/Digital I/O. May be configured as a 0 to +2.5V analog input or as a general-purpose digital I/O pin.
21	$\overline{\text{PRESENT1}}$	Digital Input. A shorting link in the fan connector holds this pin low when fan 1 is connected.
22	TACH1	Digital Input. Digital fan tachometer input for fan 1. Will accept logic signals up to +5V even when V_{CC} is lower than 5V.
23	$\overline{\text{FAULT1}}$	Digital I/O. Dual Function pin. When used with a fan having a fault output, a logic 0 input to this pin signals a fault on fan 1. Also used as a fault output.
24	DRIVE1	Digital Output. Pulse-Width Modulated (PWM) output to control the speed of fan 1.

FUNCTIONAL DESCRIPTION

SERIAL BUS INTERFACE

Control of the ADM1029 is carried out via the serial bus. The ADM1029 is connected to this bus as a slave device, under the control of a master device.

The ADM1029 has a 7-bit serial bus address. The four MSBs of the address are set to 0101. The three LSBs can be set by the user to give a total of 8 different addresses, allowing up to 8 ADM1029s to be connected to a single serial bus segment. To minimize device pin count and size, the three LSBs are set using a single pin (ADD, pin 13). This is an 8-level input whose input voltage is set by a potential divider. The voltage on ADD is sampled immediately after power up and digitized by the on-chip ADC to determine the value of the three LSBs. Since ADD is sampled only at power-up, any changes made while power is on will have no effect.

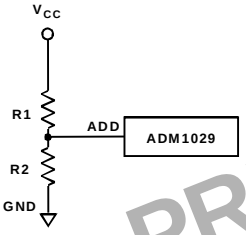


Figure 2. Setting The Serial Address

Table 1 shows resistor values for setting the 3 LSBs of the serial bus address. The same principle is used to set the voltage on pin 18 (TMIN/INSTALL), which controls the automatic fan speed control function, and also tells the ADM1029 how many fans should be installed, as described later.

If several ADM1029s are used in a system, their ADD inputs can tap off a single potential divider, as shown in Figure 3.

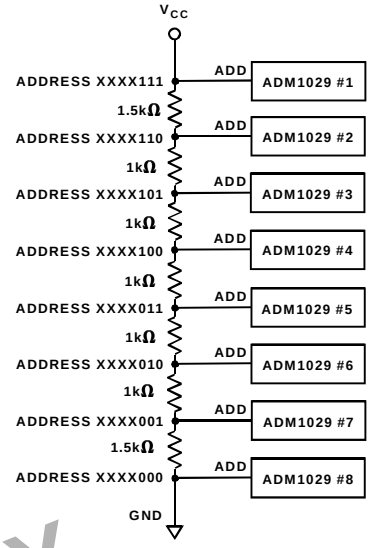


Figure 3. Setting Address Of Up To 8 ADM1029s

The serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA whilst the serial clock line SCL remains high. This indicates that an address/data stream will follow. All slave peripherals connected to the serial bus respond to the START condition, and shift in the next 8 bits, consisting of a 7-bit address (MSB first) plus a R/$\overline{W}$ bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device.

The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the Acknowledge Bit. All other devices on the bus now remain idle whilst the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0 then the master will write to the slave device. If the R/$\overline{W}$ bit is a 1 the master will read from the slave device.

2. Data is sent over the serial bus in sequences of 9 clock

TABLE 1. Resistor Ratios for Setting Serial Bus Address, T_{MIN} and Number of Fans Installed

3 MSBs of ADC	Ideal Ratio R2/(R1+R2)	R1	R2	Actual R2/(R1+R2)	Error	TMIN	Fans Installed	Address
111	n/a	0	∞	1	0	Disabled	2	0101111
110	0.8125	18k	82k	0.82	0.75%	48°C	2	0101110
101	0.6875	22k	47k	0.6812	-0.63%	40°C	2	0101101
100	0.5625	12k	15k	0.5556	-0.69%	32°C	2	0101100
011	0.4375	15k	12k	0.4444	0.69%	32°C	1	0101011
010	0.3125	47k	22k	0.3188	0.63%	40°C	1	0101010
001	0.1875	82k	18k	0.18	-0.75%	48°C	1	0101001
000	n/a	∞	0	0	0	Disabled	1	0101000

pulses, 8 bits of data followed by an Acknowledge Bit from the slave device.Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal. The number of data bytes that can be transmitted over the serial bus in a single READ or WRITE operation is limited only by what the master and slave devices can handle.

3.When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will override the acknowldge bit by pulling the data line high during the low period before the 9th clock pulse. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

Any number of bytes of data may be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the case of the ADM1029, write operations contain either one or two bytes, and read operations contain one byte, and perform the following functions:

To write data to one of the device data registers or read data from it, the Address Pointer Register must be set so that the correct data register is addressed, then data can be written into that register or read from it. The first byte of a write operation always contains an address that is stored in the Address Pointer Register. If data is to be written to the device, then the write operation contains a second data byte that is written to the register selected by the address pointer register.

This is illustrated in figure 4a. The device address is sent over the bus followed by R/$\overline{W}$ set to 0. This is followed by two data bytes.The first data byte is the address of the internal data register to be written to, which is stored in the Address Pointer Register. The second data byte is the data to be written to the internal data register.

When reading data from a register there are two possibilities:

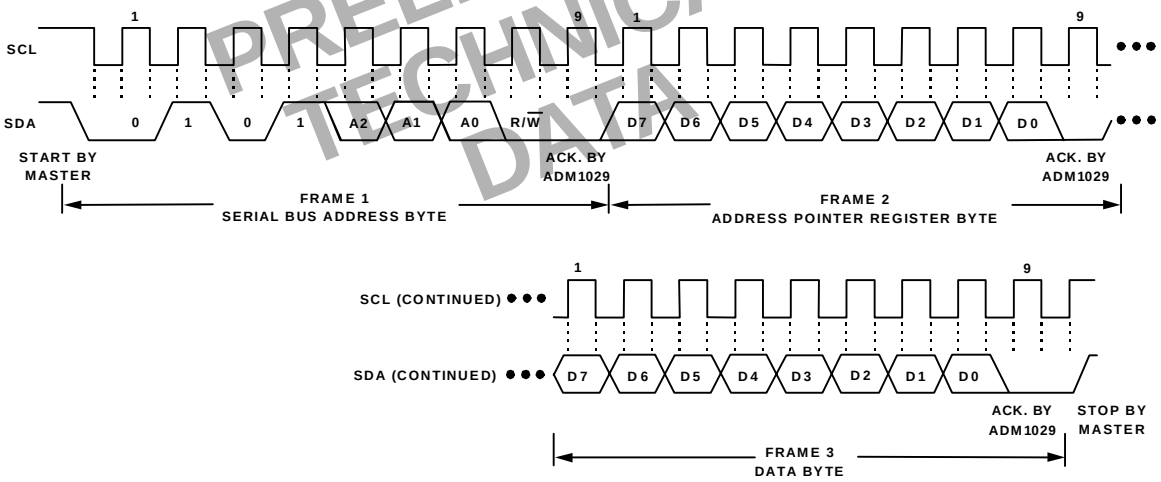


Figure 4a. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

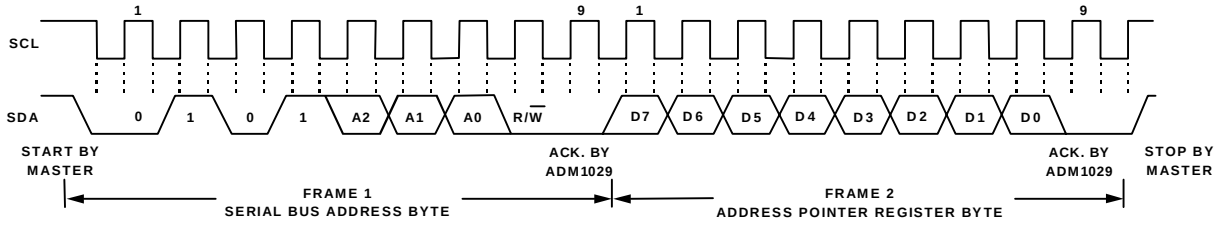


Figure 4b. Writing to the Address Pointer Register only

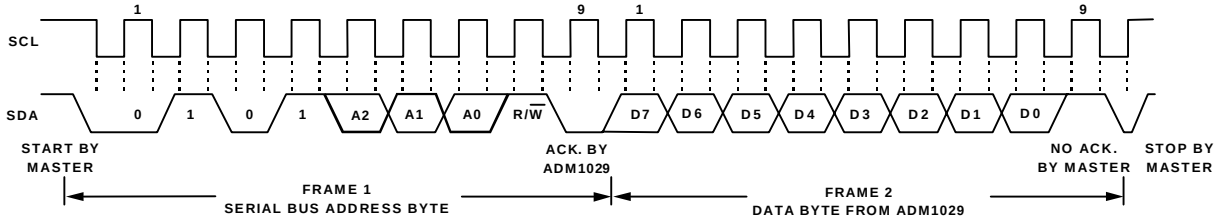


Figure 4c. Reading Data from a Previously Selected Register

1. If the ADM1029's Address Pointer Register value is unknown or not the desired value, it is first necessary to set it to the correct value before data can be read from the desired data register. This is done by performing a write to the ADM1029 as before, but only the data byte containing the register address is sent, as data is not to be written to the register. This is shown in figure 4b.

   A read operation is then performed consisting of the serial bus address, R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in figure 4c.

2. If the Address Pointer Register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the Address Pointer Register, so figure 4b can be omitted.

Note:

Although it is possible to read a data byte from a data register without first writing to the Address Pointer Register, if the Address Pointer Register is already at the correct value, it is not possible to write data to a register without writing to the Address Pointer Register, because the first data byte of a write is always written to the Address Pointer Register.

ALERT RESPONSE ADDRESS

The ADM1029 has an interrupt ($\overline{INT}$) output that is asserted low when a fault condition occurs. Several $\overline{INT}$ outputs can be wire OR'd to a common interrupt line. When the host processor receives an interrupt request, it would normally need to read the $\overline{INT}$ bit of each device status register to identify which device had made the interrupt request. However the ADM1029 supports the optional Alert Response Address function of the SMBus protocol. When the host processor receives an interrupt request it can send a general call address (0001100) over the bus. The device asserting $\overline{INT}$ will then send its own slave address back to the host processor, so the device asserting $\overline{INT}$ can be identified immediately.

If more than one device is asserting $\overline{INT}$, all devices will try to respond with their slave address, but an arbitration process ensures that only the lowest address will be received by the host.

After sending its slave address, the first device will then clear its $\overline{INT}$ output. The host can then check if the $\overline{INT}$ is still low and send the general call again if necessary until all devices asserting $\overline{INT}$ have responded.

The ARA function can be disabled by setting bit 2 of the Configuration Register (address 01h).

TEMPERATURE MEASUREMENT SYSTEM

INTERNAL TEMPERATURE MEASUREMENT

The ADM1029 contains an on-chip bandgap temperature sensor, whose output is digitised by the on-chip ADC. The temperature data is stored in the Temp0 Value Register (address A0h). As both positive and negative temperatures can be measured, the temperature data is stored in two's complement format, as shown in Table 2. Theoretically, the temperature sensor and ADC can measure temperatures from -128°C to +127°C with a resolution of 1°C, but temperatures outside the operating temperature range of the device cannot be measured by the internal sensor.

EXTERNAL TEMPERATURE MEASUREMENT

The ADM1029 can measure the temperature of one or two external diode sensor or diode-connected transistor, connected to pins 13 and 14 and/or 16 and 17. The data from the temperature measurements is stored in the Temp1 and Temp2 Value Registers (addresses A1h and A2h).

If two external temperature measurements are not required, then pins 16 and 17 can be re-configured as general-purpose logic I/O pins, as explained later.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about -2mV/°C. Unfortunately, the absolute value of V_{be}, varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass-production.

The technique used in the ADM1029 is to measure the change in V_{be} when the device is operated at two different currents.

This is given by:

$\Delta V_{be} = KT/q \times \ln(N)$

where:

K is Boltzmann's constant

q is charge on the carrier

T is absolute temperature in Kelvins

N is ratio of the two currents

Figure 5 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor.

If a discrete transistor is used, the collector will not be grounded, and should be linked to the base. If a PNP transistor is used the base is connected to the D- input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D- input and the base to the D+ input.

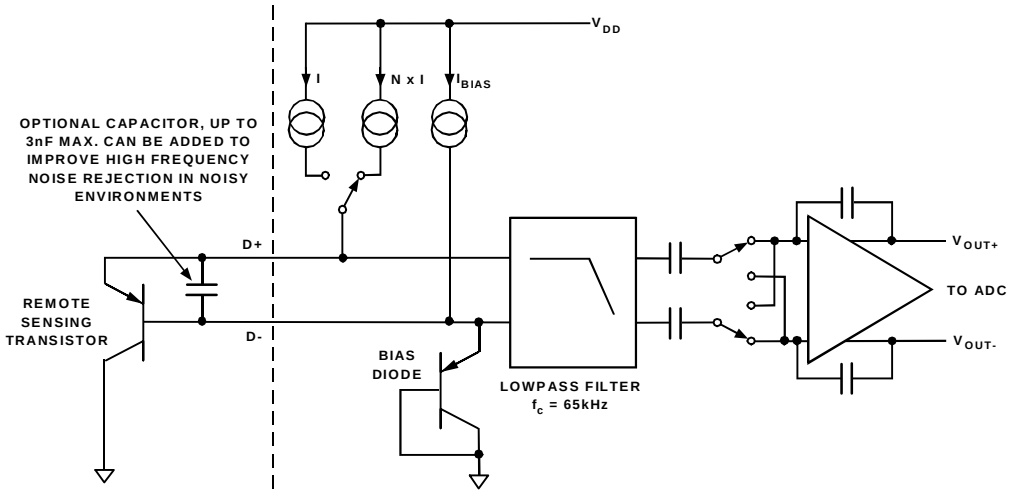


Figure 5. Signal Conditioning for Remote Diode temperature Sensors

To prevent ground noise interfering with the measurement, the more negative terminal of the sensor is not referenced to ground, but is biased above ground by an internal diode at the D- input. As the sensor is operating in a noisy environment, C1 is provided as a noise filter. See the section on layout considerations for more information on C1.

To measure ΔV_{be}, the sensor is switched between operating currents of I and N x I. The resulting waveform is passed through a 65kHz lowpass filter to remove noise, thence to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a DC voltage proportional to ΔV_{be}. This voltage is measured by the ADC to give a temperature output in 8-bit two's complement format. To further reduce the effects of noise. digital filtering is performed by averaging the results of 16 measurement cycles. An external temperature measurement takes nominally 9.6ms.

The results of external temperature measurements are stored in 8 bit, twos-complement format, as illustrated in Table 2.

OFFSET REGISTERS

Digital noise and other error sources can cause offset errors in the temperature measurement, particularly on the remote sensors. The ADM1029 offers a way to minimize these effects. The offsets on the three temperature channels can be measured during system characterization and stored as two's complement values in three offset registers at addresses 30h to 32h. The offset values are automatically added to, or subtracted from, the temperature values, depending on whether the two's complement number corresponds to a positive or negative offset. Offset values from -15°C to +15°C are allowed.

The default value in the offset registers is zero, so if no offsets are programmed the temperature measurements are unaltered.

TEMPERATURE LIMITS

The contents of the Local and Remote Temperature Value Registers (addresses A0h to A2h) are compared to the contents of the High and Low Limit Registers at addresses 90h to 92h and 98h to 9Ah. How the ADM1029 responds to overtemperature/undertemperature conditions depends on the status of the Temp0 to Temp2 Control Registers (addresses 40h to 42h). The response of $\overline{\text{CFAULT}}$, $\overline{\text{INT}}$ and fans speed to temperature events depends on the setting of these registers, as explained later.

TABLE 2. TEMPERATURE DATA FORMAT

Temperature	Digital Output
-128 °C	1000 0000
-125 °C	1000 0011
-100 °C	1001 1100
-75 °C	1011 0101
-50 °C	1100 1110
-25 °C	1110 0111
0 °C	0000 0000
+10 °C	0000 1010
+25 °C	0001 1001
+50 °C	0011 0010
+75 °C	0100 1011
+100 °C	0110 0100
+125 °C	0111 1101
+127 °C	0111 1111

FAN INTERFACING

The ADM1029 can be interfaced to many types of fan. It can be used simply to control the speed of a two-wire fan. It can measure the speed of a fan with a tach output and it can accept a logic input from fans with a FAULT output. By means of a shorting link in the fan connector it can also determine if a fan is present or not and if fans have been hot-swapped.

The ADM1029 can control or monitor one or two fans. Bits 0 and 1 of the Fans Supported In System Register (03h) tell the ADM1029 how many fans it should be controlling/monitoring.

In the following descriptions "installed" means that the corresponding bit of register 03h is set and the ADM1029 *expects* to see a fan interfaced to it. It does not necessarily mean that the fan is actually, physically connected.

If a fan is installed then events such as a fault output and hot-swapping of the fan can cause $\overline{INT}$ and $\overline{CFAULT}$ to be asserted, unless they are masked for that particular event. If a fan is not installed, but is still physically connected to the ADM1029, then these events will be ignored as far as asserting $\overline{INT}$ or $\overline{CFAULT}$ goes, but will still be reflected in the corresponding Fan Status Register.

Setting bit 0 indicates that fan 0 is installed and is set to 1 at power up by default. Setting bit 1 indicates that fan 1 is installed and depends on the state of pin 18 (TMIN/INSTALL) at power up.

If two fans are installed then bit 0 would be 1 by default and pin 18 would be tied high* to set bit 0. If only one fan is installed then it would normally be fan 0 and pin 18 would be tied low* to clear bit 1. However, both these bits can be modified by writing to the register, so it is perfectly possible to have fan 1 installed and not fan 0, or even no fans at all installed.

*Note that pin 18 also sets TMIN for automatic fan speed control. If this function is used then pin 18 would be set to some other level according to Table 1.

FAULT INPUTS/OUTPUTS

The ADM1029 can be used with fans that have a fault output that indicates if the fan has stalled or failed. If one or both of the FAULT inputs (pin 2 or 23) goes low then both $\overline{INT}$ and $\overline{CFAULT}$ will be asserted.

Events on the fault inputs are also reflected in bits 2 and 3 of the corresponding Fan Status Registers at addresses 10h and 11h. Bit 2 reflects the inverse state of the FAULT pin (0 if FAULT high, 1 of FAULT low), whilst bit 3 is latched high if a FAULT input goes low. It must be cleared by writing a zero to it.

If the fan(s) being used do not have a FAULT output, then the FAULT input(s) on the ADM1029 should be tied to V_{CC}.

The FAULT pins can also be configured as open-drain outputs by setting bit 5 of the corresponding Fan Control Register (18h or 19h). If a FAULT pin is configured as an output it will still function as an input. This means that when a fault input occurs it will be latched low by the fault output, even if the fault input is removed. The fault output can be used to drive a fan failure indicator such as a LED.

If the FAULT pin is used as an output, then any input to the FAULT pin should also be open-drain. This will avoid the fault input trying to source a high current into the FAULT pin if the fault input goes high whilst the fault output is low.

FAN PRESENT INPUTS

The fan $\overline{PRESENT}$ signal is implemented by a shorting link to ground in the fan connector. When the fan is plugged in, the correspnding PRESENT input (pin 4 or 21) on the ADM1029 is pulled low. If the fan is unplugged the $\overline{PRESENT}$ input will be pulled high. $\overline{INT}$ and $\overline{CFAULT}$ will be asserted (unless masked) and the event will be reflected in bits 0 and 1 of the corresponding Fan Status Register.

Appearance or disappearance of a $\overline{PRESENT}$ input signal during normal operation signals to the ADM1029 that a fan has been hot plugged or unplugged. $\overline{INT}$ and $\overline{CFAULT}$ will be asserted (unless masked). When a fan is hot plugged, bit 7 of the corresponding Fan Status Register will be set.

FAN SPEED MEASUREMENT

The fan counter does not count the fan tach output pulses directly, because at low fan speeds it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip oscillator into the input of an 8-bit counter.

The fan speed measuring circuit is initialized on the first rising edge of a fan tach pulse after monitoring is enabled by setting bit 4 of the Configuration Register. It then starts counting on the rising edge of the second tach pulse and counts for four fan tach periods, until the rising edge of the sixth tach pulse, or until the counter overranges if the fan tach period is too long. After the speed of the first fan has been measured, the speed of the second fan (if installed) will be measured in the same way. The measurement cycle will repeat until monitoring is disabled. The fan speed measurements are stored in the Fan Tach Value registers at addreses 70h and 71h.

If both fans are installed then Fan 0 will be measured first. If only one fan is installed then the ADM1029 will still try to measure both fans, starting with Fan 0, but the measurement on the non-installed fan will time out when the Fan 1 Tach Value count overranges.

The fan speed count is given by:

$$Count = f \times 4 \times 60/R/N$$

Where:

f is oscillator frequency in Hz

factor 4 is because 4 tach periods are counted

factor 60 is to convert minutes to seconds

R = fan speed in r.p.m.

N is number of tach pulses per revolution

The frequency of the oscillator can be adjusted to suit the expected frequency range of the fan tach pulses, which depends on the fan speed and the number of tach pulses produced for each revolution of the fan, which is either 1, 2 or 4. The oscillator frequency is set by bits 7 and 6 of the Fan Speed Registers (68h for Fan 0 and 69h for Fan 1).

TABLE 3. OSCILLATOR FREQUENCIES

Bit 7	Bit 6	Oscillator Frequency (Hz)
0	0	Measurement disabled
0	1	470
1	0	940
1	1	1880

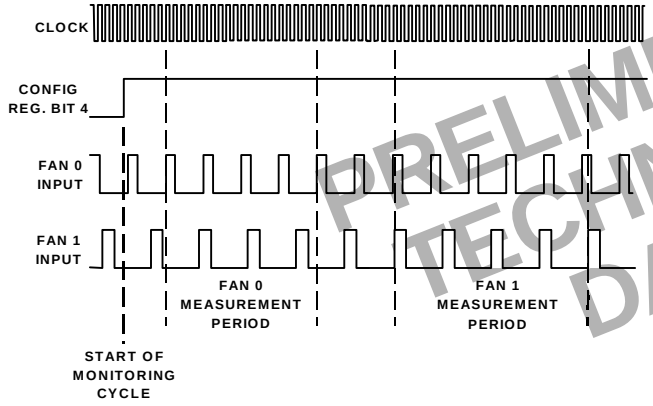


Figure 6. Fan Speed Measurement

FAN SPEED LIMITS

Fans in general will not overspeed if run from the correct voltage, so the failure condition of interest is underspeed due to electrical or mechanical failure. For this reason only low-speed limits are programmed into the Tach Limit Registers for the fans. These registers are at address 78h for fan 0 and 79h for fan 1. It should be noted that, since fan period rather than speed is being measured, the fan speed count will be larger the lower the fan speed. Therefore a fan failure fault will occur when the measurement *exceeds* the limit value.

To get the most accurate fan failure indication, the oscillator frequency should be chosen to give as large a limit value as possible without the counter overranging. A count close to 3/4 full-scale or 191 is the optimum value.

For example, if a fan produces two tach pulses per revolution and the fan failure speed is to be 600 r.p.m. the oscillator frequency should be set to 940Hz. This will give a count at the fail speed of:

$940 \times 4 \times 60/600/2 = 188$

If the oscillator frequency was only 470Hz then the count would be only 94, whilst an oscillator frequency of 1880Hz cannot be used because the count would be 376 and the counter would overrange.

FAN MONITORING CYCLE TIME

Five complete tach periods are required to carry out a fan speed measurement Therefore, if the start of a fan measurement just misses a rising edge, the measurement can taken almost six tach periods for each fan.

The worst-case monitoring cycle time is when both fans are under speed and the fan speed counter counts up to its maximum value. The actual count takes 256 oscillator pulses over 4 tach periods, plus a further two tach periods or 128 oscillator pulses before the count starts. The total monitoring cycle time is therefore:

$t_{MEAS} = 384/f_{OSC(FAN\ 0)} + 384/f_{OSC(FAN\ 1)}$

In order to read a valid result from the Fan Tach Value Registers, the total monitoring time allowed after starting the monitoring cycle should be greater than this.

TACH SIGNAL CONDITIONING

Signal conditioning in the ADM1029 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 to +5V, even if V_{CC} is less than 5V. In the event that these inputs are supplied from fan outputs which exceed 0 to +5V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figures 7a to 7d show circuits for most common fan tach outputs.

If the fan tach output has a resistive pullup to V_{CC} then it can be connected directly to the fan input, as shown in figure 7a.

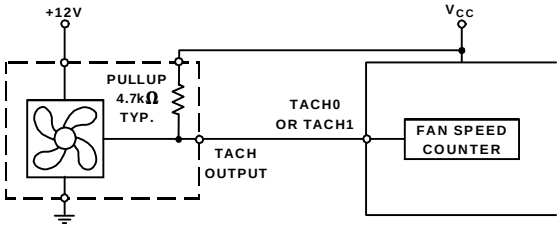


Figure 7a. Fan With Tach Pullup To $+V_{CC}$.

If the fan output has a resistive pullup to +12V (or other voltage greater than 6.5V) then the fan output can be clamped with a zener diode, as shown in figure 7b. The zener voltage should be chosen so that it is greater than V_{IH} but less than 6.5V, allowing for the voltage tolerance of the zener. A value of between 3V and 5V is suitable.

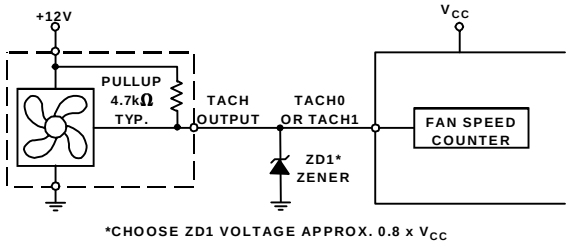


Figure 7b. Fan with Tach. Pullup to Voltage >6.5V e.g. 12V) Clamped with Zener Diode

If the fan has a strong pullup (less than 1kΩ) to +12V, or a totem-pole output, then a series resistor can be added to limit the zener current, as shown in figure 7c. Alternatively,

a resistive attenuator may be used, as shown in figure 7d.

R1 and R2 should be chosen such that:

$2V < V_{PULLUP} \times R2/(R_{PULLUP} + R1 + R2) < 5V$

The fan inputs have an input resistance of nominally 160kΩ to ground, so this should be taken into account when calculating resistor values.

With a pullup voltage of 12V and pullup resistor less than 1kΩ, suitable values for R1 and R2 would be 100kΩ and 47kΩ.This will give a high input voltage of 3.83V.

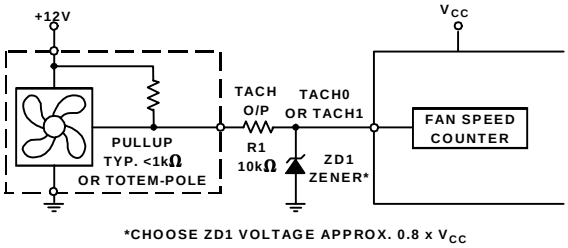


Figure 7c. Fan with Strong Tach. Pullup to >V_{CC} or Totem-Pole Output, Clamped with Zener and Resistor

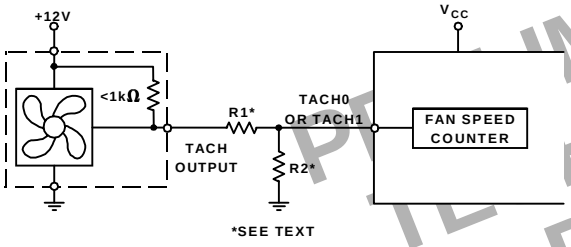


Figure 7d. Fan with Strong Tach. Pullup to >V_{CC} or Totem-Pole Output, Attenuated with R1/R2

FAN SPEED CONTROL

Fan speed is controlled using pulse-width modulation (PWM). The PWM outputs (pins 1 and 20) give a pulse output with a programmable frequency (default 250Hz) and a duty-cycle defined by the contents of the relevant fan speed register, or by the automatic fan speed control when this mode is enabled. The speed at which a fan runs is determined by fault conditions and the settings of various control and mask registers.

A fan can only be driven if it is defined as being supported by the controller in register 02h. The ADM1029 supports up to 2 fans, so bits 0 and 1 of this register are permanently set. This register is read-only.

A fan will only be driven if it is defined as being supported by the system in register 03h. If bit 0 of this register is set it indicates that Fan 0 is installed. This is the power-on default. If bit 1 is set it indicates that Fan 1 is installed. This bit is set by the state of pin 18 at power-up. This register is read/write and the default/power-on setting can be overwritten. If a fan is not supported in register 03h it will not be driven, even if it is physically installed.

The PWM outputs are open-drain outputs. They require pullup resistors and must be amplified and buffered to drive the fans.

Normal Speed

The normal fan speed is set by the four LSBs of the Fan 0 and Fan 1 Normal/Alarm Speed Registers (addresses 60h, 61h). These bits also set the minimum speed at which a fan will run in automatic control mode. The power-on default for these bits is 0101 (5h). This corresponds to 33% PWM duty-cycle, which is the lowest speed at which most fans will run reliably.

Fan(s) will run at normal speed if there is no fault condition, automatic fan speed is disabled and there are no other overriding conditions.

Alarm Speed

Alarm speed is set by the four MSBs of the Fan 0 and Fan 1 Normal/Alarm Speed Registers (addresses 60h, 61h). Fan(s) will run at alarm speed if any of the following conditions occurs, assuming the condition has not been masked in one of the fan mask registers:

- Setting bit 0 of register 07h forces Fan 0 to run at alarm speed.
- Setting bit 1 of register 07h forces Fan 1 to run at alarm speed.
- If monitoring is disabled by clearing bit 4 of the Configuration Register, all fans controlled by the ADM1029 will run at alarm speed.
- When a GPIO pin is configured as an input by setting bit 0 of the corresponding GPIO Control Register and bit 4 of the GPIO Control Register is also set, all fans controlled by the ADM1029 will go to alarm speed when the logic input is asserted (high or low depending on the polarity bit, bit 1 of the corresponding GPIO Control Register).
- If bit 7 of a Fan Control Register is set (18h - Fan 0, 19h - Fan 1) the corresponding fan will go to alarm speed when $\overline{\text{CFAULT}}$ is pulled low by an external source.
- If a tach measurement exceeds the set limit, all fans controlled by the ADM1029 will run at alarm speed.
- If a fan fault input pin is asserted (low), all fans controlled by the ADM1029 will run at alarm speed.
- If bit 1 of a Temp. Control Register is set (40h – Local Sensor, 41h – Remote 1, 42h – Remote 2), all fans controlled by the ADM1029 will go to alarm speed if the corresponding temperature high limit is exceeded.
- If bit 5 of a Temp. Control register is set, all fans controlled by the ADM1029 will go to alarm speed if a temperature input crosses the corresponding temperature low limit, the direction depending on the setting of bit 3 of the Temp. control register. (0 = alarm when input goes below low limit, 1 = alarm when input goes above low limit).
- If bit 1 of an AIN Control Register is set (50h – AIN0, 51h – AIN1), all fans controlled by the ADM1029 will go to alarm speed if the corresponding AIN high limit is exceeded.
- If bit 5 of an AIN Control register is set, all fans controlled by the ADM1029 will go to alarm speed if an analog input crosses the corresponding AIN low limit,

the direction depending on the setting of bit 3 of the AIN control register. (0 = alarm when input goes below low limit, 1 = alarm when input goes above low limit).

- If a thermal override occurs while the ADM1029 is in sleep mode, all fans controlled by the ADM1029 will run at alarm speed.

Hot Plug Speed

Hot plug speed is set by the four LSBs of the Fan 0 and Fan 1 Hot Plug Speed Registers (addresses 68h and 69h). The PWM frequency is set by bits 4 and 5 of these registers, while bits 6 and 7 set the number of pulse per revolution for fan speed measurement.

Fan(s) will run at hot plug speed if any of the following conditions occurs, assuming the condition has not been masked on one of the fan mask registers:

- If a fan is unplugged then the other fan (if any) controlled by the ADM1029 will run at hot plug speed.
- Setting bit 0 of register 08h forces Fan 0 to run at hot plug speed.
- Setting bit 1 of register 08h forces Fan 1 to run at hot plug speed.
- When a GPIO pin is configured as an input by setting bit 0 of the corresponding GPIO Control Register and bit 5 of the GPIO Control Register is also set, all fans controlled by the ADM1029 will go to hot plug speed when the logic input is asserted (high or low depending on the polarity bit, bit 1 of the corresponding GPIO Control Register).
- If bit 6 of a Fan Control Register is set (18h for Fan 0, 19h for Fan 1) the corresponding fan will go to hot plug speed when $\overline{\text{CFAULT}}$ is pulled low by an external source.

Note: If operating conditions and register settings are such that both alarm speed and hot plug speed would be triggered, which one takes priority is determined by bit 5 of the Fan 0 and Fan 1 Status Registers (addresses 10h and 11h). If this bit is set then hot plug speed takes priority. If it is cleared then alarm speed takes priority.

Full Speed

Fans will run at full speed if the corresponding bits in the Fan Full Speed Register (address 09h) are set, bit 0 for Fan 0 and bit 1 for Fan 1.

Fan Mask Registers

The effect of various conditions on fan speed can be enabled or disabled by mask registers. In all these registers, setting bit 0 of the register enables Fan 0 to go to alarm speed or hot plug speed if the corresponding event occurs, while setting bit 1 enables Fan 1. Clearing these bits masks the effect of the corresponding event on fan speed.

Registers 20h and 21h are Fan Fault to Fan Mask Registers. Bits 0 and 1 of register 20h enable (bit set) or mask (bit clear) the effect of a Fan 0 fault (underspeed or fault input) on Fan 0 and Fan 1 speed. Similarly, Bits 0 and 1 of register 21h enable (bit set) or mask (bit clear) the effect of a Fan 1 fault on Fan 0 and Fan 1 speed.

Registers 38h to 3Eh are GPIO to Fan Mask registers. Bits 0 and 1 of these registers enable or mask the effect of an AIN fault on Fan 0 and Fan 1 speed.

Registers 48h to 4Ah are Temp. to Fan Mask Registers. Bits 0 and 1 of these registers enable or mask the effect of Temp 0 (local sensor), Temp 1 and Temp 2 faults on Fan 0 and Fan 1 speed. These registers also determine which temperature channel controls which fan in automatic fan speed control mode, as described later.

Registers 58h and 59h are AIN to Fan Mask Registers. Bits 0 and 1 of these registers enable or mask the effect of an AIN fault on Fan 0 and Fan 1 speed.

AUTOMATIC FAN SPEED CONTROL

The ADM1029 offers a simple method of controlling fan speed according to temperature without intervention from the host processor.

Operation of the automatic fan speed control is controlled by 10 registers.

Setting Bit 4 of the Configuration Register (address 01h) enables monitoring, which is necessary for automatic fan speed control.

Automatic fan speed control can be set up so that different temperature sensors can control either or both fans.

Bits 0 and 1 of the three Temp. to Fan Mask Registers (addresses 48h to 4Ah) determine which temperature channel controls which fan(s). As there are six bits there are theoretically 64 possibilities for which temperature sensors control which fans, but only a subset of these are supported, as explained in the description of the Temp. to Fan Mask Registers.

If more than one temperature channel is set to control a fan the channel calculating the highest speed takes priority and the fan speed is set according to the temperature measured by that channel.

The TMIN registers (addresses 80h to 82h) contain minimum temperature values for the three temperature channels. This is the temperature at which a fan will start to operate when the temperature sensed by the controlling sensor exceeds TMIN.

TMIN can be set by writing a two's complement temperature value to the TMIN registers, or a power-up default value can be programmed, as decribed later.

The temperature range over which automatic fan speed control will operate for a particular temperature sensor is defined by the four LSB's of the three TRANGE/THYST registers. (addresses 88h to 8Ah).

TABLE 4. AUTOMATIC FAN SPEED CONTROL TEMPERATURE RANGES

Register Bits 3 - 0	Temperature Range (°C)
0000	5
0001	10
0010	20
0011	40
0100	80

When the temperature exceeds TMIN, the fan is spun up for two seconds with 100% PWM duty-cycle. It is then run at the speed set by the Fan (X) Speed 1 Registers (60h and 61h). As the temperature increases, the PWM duty-cycle will increase until it reaches 100% when the temperature reaches TMIN + TRANGE.

The four MSBs of the TRANGE/THYST registers contain a temperature hysteresis value, which can be set programmed from 0000 to 1111 (0 to 15°C). If the temperature falls, the fan will not turn off until the temperature has fallen to TMIN – THYST. This prevents the fan from cycling on and off continuously when the temperature is close to TMIN.

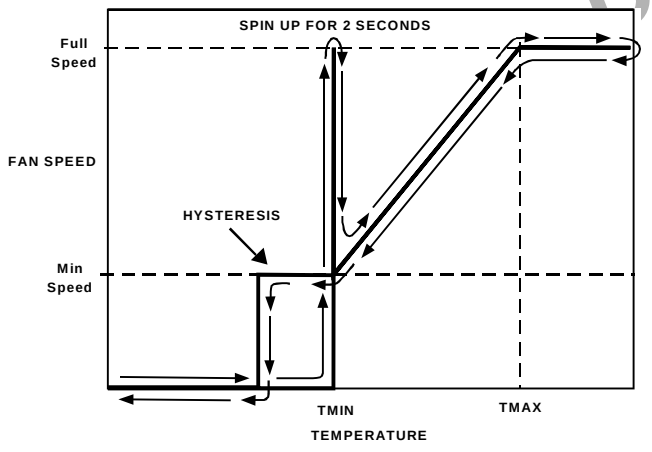


Figure 8. Automatic Fan Speed Control Transfer Function

Automatic fan control can also be enabled in hardware by pin 18 (TMIN/INSTALL). This is an 8-level input with multiple functions, which is sampled only at power-up.

If only one fan is installed, the voltage on pin 18 should be less than $V_{CC}/2$, which clears bit 1 of register 03h. Within this voltage range, four voltage levels define the minimum temperature at which the fan will operate in automatic speed control mode.

If two fans are installed, the voltage on pin 18 should be between $V_{CC}/2$ and V_{CC}, which sets bit 1 of register 03h. Within this voltage range, four voltage levels define the minimum temperature at which the fans will operate in automatic speed control mode.

Resistor values for setting the voltage on pin 18 are given in Table 1. If automatic fan speed control is not used Pin 18 can simply be strapped to ground or V_{CC} depending on how many fans are installed.

When automatic fan speed control is enabled at power-up by the TMIN/INSTALL pin, bit 4 of the Configuration register is set to enable monitoring, and bits 0 and 1 of all Temp. to Fan Mask Registers are set, so any temperature channel will control all fans that are installed.

Note:

If automatic fan speed control is enabled and an event occurs that would cause a fan to go to alarm or hot plug speed (e.g. temperature fault), that event will override the automatic fan speed control. If the event affects only one fan, the other fan will remain under automatic control.

RESET INPUT

Pin 12 is an active-low system RESET. Taking this pin low will generate a system reset, which will reset all registers to their default values.

ANALOG INPUTS

Pins 19 and 20 of the ADM1029 are dual-function pins. They may be configured as general-purpose logic I/O pins by setting bits 0 and/or 1 of the GPIO Present/AIN register (address 05h) or as 0 to +2.5V analog inputs by clearing these bits.

In the analog input mode, pins 19 and 20 have an input range of 0 to +2.5V. By suitable input scaling, the analog input may be configured to measure other voltage ranges such as system power supply voltages. If more than one ADM1029 is used in a system, several such voltages may be monitored.

The measured values of AIN0 and AIN 1 are stored in the AIN0 and AIN1 Value registers (addresses B8h and B9h) and are compared to high and low limits stored in the AIN0 and AIN1 High and Low Limit Registers (addresses A8h, A9h and B0h, B1h).

The response of the ADM1029 to an out-of-limit measurement on AIN0 or AIN1 depend on the status of the AIN0 and AIN1 control registers. The response of $\overline{\text{CFAULT}}$, $\overline{\text{INT}}$ and fan speed to temperature events depends on the setting of these registers, as detailed in the register tables later in this data sheet.

ANALOG MONITORING CYCLE

The ADM1029 performs a sequential "round-robin", monitoring cycle on all analog inputs and temperature inputs that are enabled. A conversion on AIN0 or AIN1 takes typically 11.6ms, whilst an external temperature conversion takes 185.6ms.

Conversion is enabled by setting bit 4 of the Configuration register and disabled by clearing this bit.

GENERAL PURPOSE LOGIC INPUT/OUTPUTS

The ADM1029 has six dual-function pins (see Pin Function description) that may be configured as general-pur-

pose logic I/O pins by setting the appropriate bit(s) of the GPIO Present Register (address 05h) or as their alternate functions by clearing these bits.
When configured as GPIO pins, each GPIO pin has a Control Register associated with it (registers 28h to 2Eh) that may be used to configure the operation of the pin.

The GPIO pins may be configured as inputs or outputs. When used as inputs, they may be configured to:

- be active high or active low.
- set/clear a bit in the Control Register when GP input is asserted/de-asserted.
- Latch a bit in the control register when GP input is asserted (must be cleared by software).
- assert $\overline{\text{CFAULT}}$ when GP input asserted.
- assert $\overline{\text{INT}}$ when GP input asserted.
- set fan(s) to alarm speed when GP input asserted.
- set fan(s) to hot-plug speed when GP input asserted.

When used as outputs, they may be configured to:

- be active high or low
- be asserted if a High Temperature Limit is exceeded.
- be asserted if a temperature measurement falls below a low limit.
- be asserted if a fan fault is detected.
- be asserted if a fan tach limit is exceeded.
- be asserted if an AIN high limit is exceeded.
- be asserted if an analog input falls below a low limit.

$\overline{\text{CFAULT}}$ OUTPUT

The Cascade Fault output ($\overline{\text{CFAULT}}$), is an open-drain, active low output, intended to communicate fault conditions to other ADM1029's in a system, without the intervention of the host processor. The other ADM1029's may then adjust their fans' speed to compensate, depending on the settings of various registers.

$\overline{\text{CFAULT}}$ is asserted if any of the following conditions occurs:

- A hot plug event.
- Setting bit 5 of the Configuration Register (address 01h) forces $\overline{\text{CFAULT}}$ to be asserted.
- When a GPIO pin is configured as an input by setting bit 0 of the corresponding GPIO Control Register and bit 2 of the GPIO Control Register is also set, $\overline{\text{CFAULT}}$ will be asserted when the logic input is asserted (high or low depending on the polarity bit, bit 1 of the corresponding GPIO Control Register).
- If bit 0 of a Temp. Control Register is set (40h – Local Sensor, 41h – Remote 1, 42h – Remote 2), $\overline{\text{CFAULT}}$ will be asserted if the corresponding temperature high limit is exceeded.
- If bit 4 of a Temp. Control register is set, $\overline{\text{CFAULT}}$ will be asserted if a temperature input crosses the corresponding temperature low limit, the direction depending on the setting of bit 3 of the Temp. control register. (0 = $\overline{\text{CFAULT}}$ when input goes below low limit, 1 = $\overline{\text{CFAULT}}$ when input goes above low limit).
- If bit 0 of a Fan Control Register (18h or 19h) is set, $\overline{\text{CFAULT}}$ will be asserted when a tach measurement for the corresponding fan exceeds the set limit.
- If bit 0 of a Fan Control Register (18h or 19h) is set, $\overline{\text{CFAULT}}$ will be asserted, when the fan fault input pin for the coresponding fan is asserted (low).
- If bit 0 of an AIN Control Register is set (50h – AIN0, 51h – AIN1), $\overline{\text{CFAULT}}$ will be asserted if the corresponding AIN high limit is exceeded.
- If bit 4 of an AIN Control register is set, $\overline{\text{CFAULT}}$ will be asserted if an analog input crosses the corresponding AIN low limit, the direction depending on the setting of bit 3 of the AIN control register. (0 = $\overline{\text{CFAULT}}$ when input goes below low limit, 1 = $\overline{\text{CFAULT}}$ when input goes above low limit).

INTERRUPT ($\overline{\text{INT}}$) OUTPUT

The $\overline{\text{INT}}$ output is an open-drain output with selectable polarity, intended to communicate fault conditions to the host processor. The polarity is set to active low by clearing bit 7 of the Configuration Register (address 01h) or to active high by setting this bit.
$\overline{\text{INT}}$ is asserted if any of the following conditions occurs:

- A hot plug event.
- Setting bit 6 of the Configuration Register (address 01h) forces $\overline{\text{INT}}$ to be asserted.
- When a GPIO pin is configured as an input by setting bit 0 of the corresponding GPIO Control Register and bit 3 of the GPIO Control Register is also set, $\overline{\text{INT}}$ will be asserted when the logic input is asserted (high or low depending on the polarity bit, bit 1 of the corresponding GPIO Control Register).
- If bit 2 of a Temp. Control Register is set (40h – Local Sensor, 41h – Remote 1, 42h – Remote 2), $\overline{\text{INT}}$ will be asserted if the corresponding temperature high limit is exceeded.
- If bit 6 of a Temp. Control register is set, $\overline{\text{INT}}$ will be asserted if a temperature input crosses the corresponding temperature low limit, the direction depending on the setting of bit 3 of the Temp. control register. (0 = $\overline{\text{INT}}$ when temperature goes below low limit, 1 = $\overline{\text{INT}}$ when temperature goes above low limit).
- If bit 1 of a Fan Control Register (18h or 19h) is set, $\overline{\text{INT}}$ will be asserted when a tach measurement for the corresponding fan exceeds the set limit .
- If bit 1 of a Fan Control Register (18h or 19h) is set, $\overline{\text{INT}}$ will be asserted when the fan fault input pin for the corresponding fan is asserted (low).
- If bit 2 of an AIN Control Register is set (50h – AIN0, 51h – AIN1), $\overline{\text{INT}}$ will be asserted if the corresponding AIN high limit is exceeded.
- If bit 6 of an AIN Control register is set, $\overline{\text{INT}}$ will be

asserted if the corresponding analog input crosses its AIN low limit, the direction depending on the setting of bit 3 of the AIN control register. (0 = $\overline{INT}$ when input goes below low limit, 1 = $\overline{INT}$ when input goes above low limit).

FREE-WHEELING FAN TEST

Where two fans are tightly coupled in a duct, a fan that is turned off or failed may "windmill" and freewheel at close to normal speed. To detect such a failed fan, it is necessary to power up one fan at a time and check the tach output. With no other airflow to drive it, a failed fan will not rotate. To carry out this test, all fans in the system are turned off. The test is then initiated on each ADM1029 in turn by setting bit 1 of the Configuration register (address 0Bh). The ADM1029 will spin up each fan it controls in turn, and measure the tach output. If the tach output is below the limit programmed in the Fan Tach Limit Register (address 31h for fan 1 and 32h for fan 2), then the Fan-fail bit will be set in the Configuration register (bit 2 for fan 1 and bit 3 for fan 2). This test takes about 10 seconds for each ADM1029.

LAYOUT CONSIDERATIONS

Digital boards can be electrically noisy environments, and care must be taken to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor. The following precautions should be taken:

1. Place the ADM1029 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses and CRTs are avoided, this distance can be 4 to 8 inches.
2. Route the D+ and D- tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
3. Use wide tracks to minimize inductance and reduce noise pickup. 10 mil track minimum width and spacing is recommended.

Figure 9. Arrangement of Signal Tracks

4. Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D- path and at the same temperature.

   Thermocouple effects should not be a major problem as 1°C corresponds to about 240µV, and thermocouple voltages are about 3µV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200µV.
5. Place 0.1µF bypass and 1000pF input filter capacitors close to the ADM1029.
6. If the distance to the remote sensor is more than 8 inches, the use of twisted pair cable is recommended. This will work up to about 6 to 12 feet.
7. For really long distances (up to 100 feet) use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D- and the shield to GND close to the ADM1029. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed.

Cable resistance can also introduce errors. 1Ω series resistance introduces about 0.5°C error.

REGISTER MAP

Address	Name	Default Value	Description
00	Main Status Register	00h	Contains the status of various fault conditions.
01	Config Register	0000 0000	Configures the operation of the device.
02	Fan Supported By controller	03h	Contains the number of fans the device can support.
03	Fans supported in system	0000 00?1	Contains the number of fans actually supported by the device.
04	GPIOs Supported By Controller	7Fh	Contains the number of GPIO pins the device can support.
05	GPIO Present / AIN	0????111	Used to configure GPIO pins as GPIO or as their alternate function.
06	Temp Devices Installed	0000 0??1	Contains number of temperature sensors installed.
07	Set Fan X Alarm Speed	00h	Writing to appropriate bit(s) makes fan(s) run at alarm speed.
08	Set Fan X Hot Plug Speed	00h	Writing to appropriate bit(s) makes fan(s) run at hot-plug speed.
09	Set Fan X Full Speed	00h	Writing to appropriate bit(s) makes fan(s) run at full-speed.
0B	S/W RESET	00h	Writing A6h to this register causes a a software reset.
0D	Manufacturer's ID	41h	This register contains the manufacturer's ID code for the device.
0E	Major/Minor Revision	00h	Contains the manufacturer's code for major and minor revisions to the device in two nibbles..
0F	Manufacturer's Test Register	00h	This register is used by the manufacturer for test purposes. It should not be read from or written to in normal operation.
10	Fan0 Status	0000 0?0?	Contains status information for FAN 0
11	Fan1 Status	0000 0?0?	Contains status information for FAN 1
18	Fan0 Control	BFh	Sets operation of $\overline{\text{INT}}$, $\overline{\text{CFAULT}}$ etc. for FAN 0 fault.
19	Fan1 Control	BFh	Sets operation of $\overline{\text{INT}}$, $\overline{\text{CFAULT}}$ etc. for FAN 1 fault.
20	Fan Fault 0 to Fan mask	FFh	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to a fault or hot plug event on FAN 0
21	Fan Fault 1 to Fan mask	FFh	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to a fault or hot plug event on FAN 1
28	GPIO0 Control	00h	Configures the operation of GPIO0
29	GPIO1 Control	00h	Configures the operation of GPIO1
2A	GPIO2 Control	00h	Configures the operation of GPIO2
2B	GPIO3 Control	00h	Configures the operation of GPIO3
2C	GPIO4 Control	00h	Configures the operation of GPIO4
2D	GPIO5 Control	00h	Configures the operation of GPIO5
2E	GPIO6 Control	00h	Configures the operation of GPIO6
30	Temp0 Offset	00h	Offset register for local temperature measurement. The value in this register is added to the local temperature value to reduce systemic offset effects.

REGISTER MAP

Address	Name	Default Value	Description
31	Temp1 Offset	00h	Offset register for 1st remote temperature channel (D1). The value in this register is added to the temperature value to reduce systemic offset effects.
32	Temp2 Offset	00h	Offset register for 2nd remote temperature channel (D2). The value in this register is added to the temperature value to reduce systemic offset effects.
38	GPIO0 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to GPIO0 being asserted.
39	GPIO1 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to GPIO1 being asserted.
3A	GPIO2 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to GPIO2 being asserted.
3B	GPIO3 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to GPIO3 being asserted.
3C	GPIO4 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to GPIO4 being asserted.
3D	GPIO5 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to GPIO5 being asserted.
3E	GPIO6 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to GPIO6 being asserted.
40	Temp0 Control	08h	Configures the operation of $\overline{\text{INT}}$, $\overline{\text{CFAULT}}$, etc. for a Temp 0 fault (internal temperature sensor)
41	Temp1 Control	08h	Configures the operation of $\overline{\text{INT}}$, $\overline{\text{CFAULT}}$, etc. for a Temp 0 fault (D1 temperature sensor).
42	Temp2 Control	08h	Configures the operation of $\overline{\text{INT}}$, $\overline{\text{CFAULT}}$, etc. for a Temp 0 fault (D2 temperature sensor).
48	Temp0 Fan Mask	0?00 ?00?	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to a Temp0 fault condition (internal temperature sensor)
49	Temp1 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to a Temp0 fault condition (D1 temperature sensor)
4A	Temp2 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to a Temp0 fault condition (D2 temperature sensor)
50	AIN0 Control	00h	Configures the operation of $\overline{\text{INT}}$, $\overline{\text{CFAULT}}$, etc. for a fault on analog channel 0.
51	AIN1 Control	00h	Configures the operation of $\overline{\text{INT}}$, $\overline{\text{CFAULT}}$, etc. for a fault on analog channel 1.
58	AIN0 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to a fault on analog channel 0.
59	AIN1 Fan Mask	00h	Enables/disables FAN 0 and/or FAN 1 alarm/hot-plug speed in response to a fault on analog channel 1.
60	Fan0 Speed 1	FFh	Contains the normal speed values for FAN 0.
61	Fan1 Speed 1	FFh	Contains the normal speed values for FAN 1.
68	Fan0 Speed 2	2Fh	Contains the hot-plug speed value for FAN 0.
69	Fan1 Speed 2	2Fh	Contains the hot-plug speed value for FAN 1.

REGISTER MAP

Address	Name	Default Value	Description
70	Fan0 Tach Value	00h	Contains the measured value from the FAN 0 tachometer output.
71	Fan1 Tach Value	00h	Contains the measured value from the FAN 1 tachometer output.
78	Fan0 Tach High Limit	FFh	Contains the high limit for FAN 0 tachometer measurement.
79	Fan1 Tach High Limit	FFh	Contains the high limit for FAN 1 tachometer measurement.
80	Temp0 Tmin	??h	Contains the minimum temperature value for automatic fan speed control based on the Temp0 temperature measurement (internal temperature sensor).
81	Temp1 Tmin	??h	Contains the minimum temperature value for automatic fan speed control based on the Temp1 temperature measurement (D1 temperature sensor).
82	Temp2 Tmin	??h	Contains the minimum temperature value for automatic fan speed control based on the Temp2 temperature measurement (D2 temperature sensor).
88	Temp0 Tstep/Hyst	51h	Two nibbles of this register contain the temperature step value for automatic fan speed control based on the Temp0 measured temperature and hysteresis for Tmin.
89	Temp1 Trange/Hyst	51h	Two nibbles of this register contain the temperature range for automatic fan speed control based on the Temp1 measured temperature and hysteresis for Tmin.
8A	Temp2 Trange/Hyst	51h	Two nibbles of this register contain the temperature range for automatic fan speed control based on the Temp2 measured temperature and hysteresis for Tmin.
90	Temp0 High Limit	50h (+80°C)	High limit for Temp0 measurement (internal sensor).
91	Temp1 High Limit	64h (+100°C)	High limit for Temp1 measurement (D1 sensor).
92	Temp2 High Limit	64h (+100°C)	High limit for Temp2 measurement (D2 sensor).
98	Temp0 Low Limit	3Ch (+60°C)	Low limit for Temp0 measurement (internal sensor).
99	Temp1 Low Limit	46h (+70°C)	Low limit for Temp1 measurement (D1 sensor).
9A	Temp2 Low Limit	46h (+70°C)	Low limit for Temp2 measurement (D2 sensor).
A0	Temp0 Measured Value	00h	Measured value from internal sensor.
A1	Temp1 Measured Value	00h	Measured value from D1 externalsensor.
A2	Temp2 Measured Value	00h	Measured value from D2 externalsensor.
A8	AIN0 High Limit	FFh	High limit for measurement on analog channel 0.
A9	AIN1 High Limit	FFh	High limit for measurement on analog channel 1.
B0	AIN0 Low Limit	00h	Low limit for measurement on analog channel 0.
B1	AIN1 Low Limit	00h	Low limit for measurement on analog channel 1.
B8	AIN0 Measured Value	00h	Measured value of analog channel 0.
B9	AIN1 Measured Value	00h	Measured value of analog channel 1.

DETAILED REGISTER DESCRIPTIONS

Register 00h - Main Status Register (Power-On Default 00h)

Bit	Name	R/W	Description
0	$\overline{INT}$	R	This bit is set to 1 when the device is asserting $\overline{INT}$ low. This bit is the logical OR of several bits in other registers and is cleared when these bits are cleared.
1	CFAULT_in	R	This bit is set to 1 when the device is receiving $\overline{CFAULT}$ low from another device.
2	CFAULT_out	R	This bit is set to 1 when the device is asserting $\overline{CFAULT}$ low. This bit is the logical OR of several bits in other registers and is cleared when these bits are cleared.
3	In Alarm_speed	R	This bit is set to 1 when either fan is running at Alarm Speed. This bit is the logical OR of several bits in other registers and is cleared when these bits are cleared.
4	In Hot Plug Speed	R	This bit is set to 1 when either fan is running at Hot Plug Speed. This bit is the logical OR of several bits in other registers and is cleared when these bits are cleared.
5	Hot Plug/Fan Fault	R	This bit is a logical OR of bits 1,3,6 and 7 in the FanX Status Registers at 10h and 11h. It will be set when any of these bits are set and cleared when all of these bits are cleared.
6	GPIO/AIN Event	R	This bit is a logical OR of bits 1, 3, 6 and 7 in the GPIO Control Registers at 28h to 2Eh while they are configured as inputs and bit 7 in the AINX Control registers at 50h and 51h. It will be set when any of these bits are set and cleared when all of these bits are cleared.
7	Thermal Event	R	This bit is a logical OR of bit 7 in the TempX Control Registers at 40h, 41h and 42h. It will be set when any of these bits are set and cleared when all of these bits are cleared.

Register 01h - Config Register (Power-On Default 000? 000?)

Bit	Name	R/W	Description
0	Install = ?	R/W	This bit reflects bit 1 of Register 0x03 (Fans Supported In System)
1	Global $\overline{INT}$ mask = 0	R/W	Setting this bit to 1 will disable the $\overline{INT}$ output for all interrupt sources.
2	ARA Disable = 0	R/W	Setting this bit to 1 will disable the SMBus Alert Response Address feature.
3	Perform Free-Wheel Test = 0	R/W	Setting this bit to 1 will initiate the Fan Free-Wheeling Test. While this test is being performed normal monitoring of fan speeds, temperature and voltages will be temporarily halted. This bit will automatically reset to 0 once the test is complete which will take about 10 seconds.
4	Start Monitoring = 0	R/W	Set to 1 to start round robin monitoring cycle of voltage temperature and fan speeds, fault detection, etc. While this bit is 0, all fans will run at Alarm Speed. This bit is set at power-up if automatic fan speed control is enabled by pin 18, cleared otherwise.
5	Force $\overline{CFAULT}$ = 0	R/W	Setting this bit to 1 forces $\overline{CFAULT}$ to be asserted (Low).
6	Force $\overline{INT}$ = 0	R/W	Setting this bit to 1 forces $\overline{INT}$ to be asserted (Polarity depends on Bit 2).
7	$\overline{INT}$ Polarity = 0	R/W	Polarity of $\overline{INT}$ when asserted. 1 means High and 0 means Low.

Register 02h - Fan Supported By Controller (Power-On Default 03h)

Bit	Name	R/W	Description
0	Fan0 = 1	R	This bit being set to 1 means the ADM1029 can support Fan0.
1	Fan1 = 1	R	This bit being set to 1 means the ADM1029 can support Fan1.
2	0	R	Unused. Will read back 0.
3	0	R	Unused. Will read back 0.
4	0	R	Unused. Will read back 0.
5	0	R	Unused. Will read back 0.
6	0	R	Unused. Will read back 0.
7	0	R	Unused. Will read back 0.

Register 03h - Fans Supported In System (Power-On Default 0000 00?1)

Bit	Name	R/W	Description
0	Fan 0 = 1	R/W	Indicates that Fan0 is being used. Set to 1 on Powerup, but can be overwritten by software.
1	Fan 1 = ?	R/W	Indicates that Fan1 is being used. Set by Pin 18 (Tmin/Install) on Powerup, but can be overwritten by software.
2	0	R	Unused. Will read back 0.
3	0	R	Unused. Will read back 0.
4	0	R	Unused. Will read back 0.
5	0	R	Unused. Will read back 0.
6	0	R	Unused. Will read back 0.
7	0	R	Unused. Will read back 0.

Register 04h - GPIOs Supported By Controller (Power-On Default 7Fh)

Bit	Name	R/W	Description
0	GPIO 0 = 1 (Pin 19)	R	This bit being set to 1 means the ADM1029 can support GPIO0, available on Pin 19.
1	GPIO 1 = 1 (Pin 20)	R	This bit being set to 1 means the ADM1029 can support GPIO1, available on Pin 20.
2	GPIO 2 = 1 (Pin 11)	R	This bit being set to 1 means the ADM1029 can support GPIO2, available on Pin 11.
3	GPIO 3 = 1 (Pin 13)	R	This bit being set to 1 means the ADM1029 can support GPIO3, available on Pin 13.
4	GPIO 4 = 1 (Pin 14)	R	This bit being set to 1 means the ADM1029 can support GPIO4, available on Pin 14.
5	GPIO 5 = 1 (Pin 16)	R	This bit being set to 1 means the ADM1029 can support GPIO5, available on Pin 16.
6	GPIO 6 = 1 (Pin 17)	R	This bit being set to 1 means the ADM1029 can support GPIO6, available on Pin 17.
7	GPIO 7 = 0	R	Unused. Will read back 0.

Register 05h - GPIO Present / AIN (Power-On Default 0????111)

Bit	Name	R/W	Description
0	GPIO 0 = 1	R/W	Indicates that GPIO0 is being used. Set to 1 on Powerup, but can be overwritten by software. Setting this bit to 0 means AIN0 is being used.
1	GPIO 1 = 1	R/W	Indicates that GPIO1 is being used. Set to 1 on Powerup, but can be overwritten by software. Setting this bit to 0 means AIN1 is being used.
2	GPIO 2 = 1	R/W	Indicates that GPIO2 is being used. Set to 1 on Powerup, but can be overwritten by software.
3	GPIO 3 = ?	R/W	Indicates that GPIO3 is being used. Setting this bit to 0 means TDM1 is being used. The ADM1029 can detect on powerup if TDM1 is connected. If so then this bit is set to 0, else it is set to 1. The default setting can be overwritten by software.
4	GPIO 4 = ?	R/W	Indicates that GPIO4 is being used. Setting this bit to 0 means TDM1 is being used. The ADM1029 can detect on powerup if TDM1 is connected. If so then this bit is set to 0, else it is set to 1. The default setting can be overwritten by software.
5	GPIO 5 = ?	R/W	Indicates that GPIO5 is being used. Setting this bit to 0 means TDM2 is being used. The ADM1029 can detect on powerup if TDM2 is connected. If so then this bit is set to 0, else it is set to 1. The default setting can be overwritten by software.
6	GPIO 6 = ?	R/W	Indicates that GPIO6 is being used. Setting this bit to 0 means TDM2 is being used. The ADM1029 can detect on powerup if TDM2 is connected. If so then this bit is set to 0, else it is set to 1. The default setting can be overwritten by software.
7	0	R	Unused. Will read back 0.

Register 06h - Temp Devices Installed (Power-On Default 0000 0??1)

Bit	Name	R/W	Description
0	Temp Loc = 1	R	This bit is permanently set to 1 since the local temperature sensor is always available.
1	Temp R0 = ?	R	This bit is set to 1 if the first remote temperature sensor (TDM1) is installed. (Automatically detected on powerup.)
2	Temp R1 = ?	R	This bit is set to 1 if the second remote temperature sensor (TDM2) is installed. (Automatically detected on powerup.)
3	0	R	Unused. Will read back 0.
4	0	R	Unused. Will read back 0.
5	0	R	Unused. Will read back 0.
6	0	R	Unused. Will read back 0.
7	0	R	Unused. Will read back 0.

Register 07h - Set Fan X Alarm Speed (Power-On Default 00h)

Bit	Name	R/W	Description
0	Fan 0 Alarm Speed = 0	R/W	When set to 1 Fan0 will run at Alarm Speed.
1	Fan 1 Alarm Speed = 0	R/W	When set to 1 Fan1 will run at Alarm Speed.
2	0	R	Unused. Will read back 0.
3	0	R	Unused. Will read back 0.
4	0	R	Unused. Will read back 0.
5	0	R	Unused. Will read back 0.
6	0	R	Unused. Will read back 0.
7	0	R	Unused. Will read back 0.

Register 08h - Set Fan X Hot Plug Speed (Power-On Default 00h)

Bit	Name	R/W	Description
0	Fan 0 Hot Plug Speed = 0	R/W	When set to 1 Fan0 will run at Hot Plug Speed.
1	Fan 1 Hot Plug Speed = 0	R/W	When set to 1 Fan1 will run at Hot Plug Speed.
2	0	R	Unused. Will read back 0.
3	0	R	Unused. Will read back 0.
4	0	R	Unused. Will read back 0.
5	0	R	Unused. Will read back 0.
6	0	R	Unused. Will read back 0.
7	0	R	Unused. Will read back 0.

Register 09h - Set Fan X Full Speed (Power-On Default 00h)

Bit	Name	R/W	Description
0	Fan 0 Full Speed = 0	R/W	When set to 1 Fan0 will run at Full Speed.
1	Fan 1 Full Speed = 0	R/W	When set to 1 Fan1 will run at Full Speed.
2	0	R	Unused. Will read back 0.
3	0	R	Unused. Will read back 0.
4	0	R	Unused. Will read back 0.
5	0	R	Unused. Will read back 0.
6	0	R	Unused. Will read back 0.
7	0	R	Unused. Will read back 0.

Register 0Bh - S/W RESET (Power-On Default 00h)

Bit	Name	R/W	Description
7 - 0	S/W Reset	R/W	Writing A6hex to this register location causes a software reset identical to a power-on reset. This register is self-clearing so reading from it after the software reset has completed will result in 00hex being read.

Register 0Ch - Fan Spin-up Register (Power-On Default 03h)

Bit	Name	R/W	Description
7 - 4	Unused	R	Unused
3	Spin-up Disable	R/W	When this bit is set to 1, fan spin-up to full speed will be disabled.
2 - 0	Fan Spin-up Time	R/W	These bits select the spin-up time for the fans 000 = 16 seconds 001 = 8 seconds 010 = 4 seconds 011 = 2 seconds 100 = 1 second 101 = 0.25 seconds 110 = 1/16 second 111 = 1/64 second

Register 0Dh - Manufacturer's ID (Power-On Default 41h)

Bit	Name	R/W	Description
7 - 0	Manufacturer's ID Code	R	This register contains the manufacturer's ID code for the device.

Register 0Eh - Revision (Power-On Default 00h)

Bit	Name	R/W	Description
3 – 0	Minor Revision Code	R	This nibble contains the manufacturer's code for minor revisions to the device.
7 – 4	Major Revision Code	R	This nibble contains the manufacturer's code for major revisions to the device which would likely require a S/W revision.

Register 0Fh - Manufacturer's Test Register (Power-On Default 00h)

Bit	Name	R/W	Description
7 - 0	Manufacturer's Test	R/W	This register is used by the manufacturer for test purpose. It should not be read from or written to in normal operation.

Register 10h, 11h - FanX* Status (Power-On Default 0000 0?0?)

Bit	Name	R/W	Description
0	Missing = x	R	Reflects the state of Pins 4/21. Low means FanX* is installed, High means it is missing. This bit will automatically return Low if a missing fan is replaced.
1	Missing _L = 0	R/W	This bit is edge-triggered and latches a FanX* missing event on removal of FanX. This bit is cleared by writing a 0 to it.
2	Fault_ = x	R	Inverse of Pin 2/23. Low on pin means FanX* has a fault (Pin 2/23 Low), High on pin means it is OK. This bit will automatically return Low if pin 2/23 goes high.
3	Fault_L_ = 0	R/W	This bit is edge-triggered and latches a FanX* fault event on Pin 2/23. This bit is cleared by writing a 0 to it. If the PRESENT pin for a fan input is high (fan not installed) this bit will be cleared automatically.

4	Sleep = 0	R/W	When this bit is set, FanX* will be stopped and no FanX* faults will be monitored. If Bit4 in FanX* Control Register is set then FanX* will go to Alarm Speed if an overtemperature event is detected as per settings in TempX Control Register.
5	Hot Plug Priority	R/W	This bit indicates whether FanX runs at Hot Plug Speed (bit set to 1) or Alarm Speed (bit set to 0) if both modes are triggered.
6	Tach_Fault_L	R/W	Latches a FanX Tach fault. This bit is cleared by writing a 0 to it. If the PRESENT pin for a fan input is high (fan not installed) this bit will be cleared automatically.
7	Hot_Plug_L	R/W	This bit is edge-triggered and latches a FanX Hot Plug event which is the insertion of FanX. (Note difference to Bit 1) This bit is cleared by writing a 0 to it. If a fan is Hot Plug installed, it will run at Normal Speed.

*Note: "X" denotes the fan number. Register 10h is for Fan 0 and Register 11h is for Fan 1.

Register 18h, 19h - FanX* Control (Power-On Default BFh)

Bit	Name	R/W	Description
0	Assert $\overline{\text{CFAULT}}$ on Fault = 1	RW	If this bit is set, $\overline{\text{CFAULT}}$ will be asserted, when there is a fault (Tach or Pin 2/23) on FanX*.
1	Assert $\overline{\text{INT}}$ on Fault = 1	RW	If this bit is set, $\overline{\text{INT}}$ will be asserted, when there is a fault (Tach or Pin 2/23) on FanX*.
2	Assert $\overline{\text{CFAULT}}$ on Hot Unplug = 1	R/W	If this bit is set, $\overline{\text{CFAULT}}$ will be asserted, when there is a hot unplug event on FanX*.
3	Assert $\overline{\text{INT}}$ on Hot Unplug = 1	R/W	If this bit is set, $\overline{\text{INT}}$ will be asserted, when there is a hot unplug event on FanX*.
4	Thermal Over-ride in Sleep = 1	R/W	If Bit4 in FanX Status Register is set then FanX* will go to Alarm Speed if an overtemperature event is detected as per settings in TempX Control Register, while this bit is set.
5	Drive Fault_ on Fault_L = 1	R/W	If Bit 3 or Bit 6 of Reg 10 is set then drive Pin 2,23 low, if a fault is generated
6	Hot Plug Speed on $\overline{\text{CFAULT}}$ in = 0	R/W	When this bit is set, FanX* will go to Hot Plug Speed when $\overline{\text{CFAULT}}$ is pulled low externally.
7	Alarm on $\overline{\text{CFAULT}}$ = 1	R/W	When this bit is set, FanX* will go to Alarm Speed when $\overline{\text{CFAULT}}$ is pulled low externally.

*Note: "X" denotes the fan number. Register 18h is for Fan 0 and Register 19h is for Fan 1.

Register 20h, 21h - Fan Fault X* to Fan Mask (Power-On Default FFh)

Bit	Name	R/W	Description
0	Fan 0 = 1	R/W	If a fault (Tach or Pin2/23) is detected on FanX* then Fan 0 will be driven to Alarm Speed, when this bit is set.
1	Fan 1 = 1	R/W	If a fault (Tach or Pin2/23) is detected on FanX* then Fan 1 will be driven to Alarm Speed, when this bit is set.
2	1	R	Unused. Will read back 1.
3	1	R	Unused. Will read back 1.
4	1	R	Unused. Will read back 1.
5	1	R	Unused. Will read back 1.
6	1	R	Unused. Will read back 1.
7	1	R	Unused. Will read back 1.

*Note: "X" denotes the fan number. Register 20h is for Fan 0 and Register 21h is for Fan 1.

Register 28h,29h,2Ah,2Bh,2Ch,2Dh,2Eh - GPIOX* Control (Power-On Default 00h)

Bit	Name	R/W	Description
0	Direction = 0	R/W	This bit indicates the direction for GPIOX* pin. When set to 1 GPIOX will function as an input, when 0 GPIOX* will function as an output.
1	Polarity = 0	R/W	This bit indicates the polarity of the GPIOX* pin. When set to 1 GPIOX* will be active high, when 0 GPIOX* will be active low.
2	Bit 2 = 0	R/W	If GPIOX* is configured as an input, then $\overline{\text{CFAULT}}$ will be asserted if GPIOX* pin is asserted while this bit is set. If GPIO2 is configured as an output, then GPIO2 will be asserted if a temperature High limit is exceeded while this bit is set. If automatic fan speed control is enabled, this bit will be set by default. This can be used as a SHUTDOWN signal for a catastrophic over-temperature event.
3	Bit 3 = 0	R/W	If GPIOX* is configured as an input, then $\overline{\text{INT}}$ will be asserted if GPIOX* pin is asserted while this bit is set. If GPIOX* is configured as an output, then GPIOX* will be asserted if a temperature Low limit is exceeded while this bit is set.
4	Bit 4 = 0	R/W	If GPIOX* is configured as an input, then Fans will go to Alarm Speed if GPIOX* pin is asserted while this bit is set. If GPIOX* is configured as an output, then GPIOX* will be asserted if a Fan Tach limit is exceeded while this bit is set.
5	Bit 5 = 0	R/W	If GPIOX* is configured as an input, then Fans will go to Hot Plug Speed if GPIOX* pin is asserted while this bit is set. If GPIOX* is configured as an output, then GPIOX* will be asserted if a Fan Fault (Pins 2/23) is detected while this bit is set.
6	Bit 6 = 0	R R/W	If GPIOX* is configured as an input, then this bit will reflect state of GPIOX* pin. If GPIOX* is configured as an output, then GPIOX will be asserted if an AIN high limit is exceeded while this bit is set.
7	Bit 7 = 0	R/W	If GPIOX* is configured as an input, then this bit will latch a GPIOX* assertion event. This bit is cleared by writing a 0 to it. If GPIOX* is configured as an output, then GPIOX* will be asserted if an AIN Low limit is exceeded while this bit is set.

*Note: "X" denotes the number of the GPIO pin. Register 28h controls GPIO0, 29h controls GPIO1 etc.

Register 30h, 31h, 32h - TempX Offset Registers (Power-On Default 00h)

Bit	Name	R/W	Description
7-0	Offset	R/W	This register contains an offset value that is automatically added to the temperature value to reduce the effects of systemic offset errors.

*Note: "X" denotes the number of the temperature channel. Register 30h is for Temp0, the internal temperature channel. 31h is for Temp1 (D1), 32h is for Temp2 (D2).

Register 38h,39h,3Ah,3Bh,3Ch,3Dh,3Eh - GPIOX* Fan Mask (Power-On Default 00h)

Bit	Name	R/W	Description
0	Fan 0 = 0	R/W	If GPIOX* is asserted such that fans should be driven at Aalrm or Hot Plug Speed then Fan0 will be set to this speed when this bit is set.
1	Fan 1 = 0	R/W	If GPIOX* is asserted such that fans should be driven at Aalrm or Hot Plug Speed then Fan1 will be set to this speed when this bit is set.
2	0	R	Unused. Will read back 0.
3	0	R	Unused. Will read back 0.
4	0	R	Unused. Will read back 0.
5	0	R	Unused. Will read back 0.
6	0	R	Unused. Will read back 0.
7	0	R	Unused. Will read back 0.

*Note: "X" denotes the number of the GPIO pin. Register 38h is for GPIO0, 29h is for GPIO1 etc.

Register 40h, 41h, 42h - TempX* Control (Power-On Default 08h)

Bit	Name	R/W	Description
0	Assert $\overline{\text{CFAULT}}$ on OT = 0	R/W	When this bit is set, $\overline{\text{CFAULT}}$ will be asserted when the TempX* temperature exceeds the TempX* Temperature High Limit, not otherwise.
1	Alarm speed on OT = 0	R/W	When this bit is set, the fans(s) will go to alarm speed when the TempX* temperature exceeds the TempX* Temperature High limit, not otherwise.
2	$\overline{\text{INT}}$ on OT = 0	R/W	When this bit is set, $\overline{\text{INT}}$ will be asserted when the TempX* temperature exceeds the TempX* Temperature High Limit, not otherwise.
3	Alarm below low = 0	R/W	This bit indicates whether an alarm ($\overline{\text{INT}}$, $\overline{\text{CFAULT}}$ or Alarm Speed) is asserted when temperature goes above or below the Low Limit. 1 = above. 0 = below. This bit is set to 1 at power-up if automatic fan speed control is enabled by pin 18, cleared otherwise.
4	Assert $\overline{\text{CFAULT}}$ on UT = 0	R/W	When this bit is set, $\overline{\text{CFAULT}}$ will be asserted when the TempX* temperature crosses the TempX* Temperature Low Limit, not otherwise. Bit 3 decides whether $\overline{\text{CFAULT}}$ is asserted for going above or below the Low Limit. This bit is set to 1 if Automatic Fan Speed Control is enabled on power-up.
5	Alarm speed on UT = 0	R/W	When this bit is set, the fans(s) will go to alarm speed when the TempX * temperature crosses the TempX* Temperature Low Limit, not otherwise. Bit 3 decides whether Alarm Speed is asserted for going above or below the Low Limit.
6	$\overline{\text{INT}}$ on UT = 0	R/W	When this bit is set, $\overline{\text{INT}}$ will be asserted when the TempX* temperature crosses the TempX* Temperature Low Limit, not otherwise. Bit 3 decides whether $\overline{\text{INT}}$ is asserted for going above or below the Low Limit.
7	Latch Temp Fault = 0	R/W	This bit latches a temperature out of limit event (ie when the temperature goes above the high limit or crosses the low limit) on the TempX* channel. This bit is cleared by writing a 0 to it.

*Note: "X" denotes the number of the temperature channel. Register 40h is for Temp0, the internal temperature channel. 41h is for Temp1 (D1), 42h is for Temp2 (D2).

Register 48h, 49h, 4Ah - TempX* Fan Mask (Power-On Default 00h)

Bit	Name	R/W	Description
0	Fan 0 = 0	R/W	If a TempX* out of limit event is generated such that fans should be driven at Alarm Speed then Fan0 will be set to this speed when this bit is set. If no TempX* out of limit event is present then Fan0 will be set to the speed determined by the automatic fan speed control circuit as a result of temperature measurements on the TempX* channel when this bit is set. If this bit is not set then TempX* temperature measurements will have no effect on the speed of Fan0.
1	Fan 1 = 0	R/W	If a TempX out of limit event is generated such that fans should be driven at Alarm Speed then Fan1 will be set to this speed when this bit is set. If no TempX* out of limit event is present then Fan1 will be set to the speed determined by the automatic fan speed control circuit as a result of temperature measurements on the TempX channel when this bit is set. If this bit is not set then TempX temperature measurements have no effect on the speed of Fan1. While in theory it is possible through setting of bits 0 and 1 in registers 48h to 4Ah to have any temperature channel controlling any fan, in practice this is not feasible. A subset of possibilities only are supported as follows: Case 1: TDM1 controlling Fan0, TDM2 controlling Fan1 (Bit 0 in 49h set and/or Bit 1 in 4Ah set, only) Case 2a: Local controlling Fan0 and/or Fan 1 (Bits 0,1 in 48h only set) Case 2b: TDM1 controlling Fan0 and/or Fan 1 (Bits 0,1 in 49h only set) Case 2c: TDM2 controlling Fan0 and/or Fan 1 (Bits 0,1 in 4Ah only set) Case 3: (Default) Fan0 and/or Fan1 set to max speed determined by temperature measurements on all 3 channels. (Bits 0,1 in 48h,49h,4Ah all set) Other: If Bits 0,1 in registers 48h,49h,4Ah are set inconsistent with these cases then fans will run at the speeds determined by the normal speed registers.
2	0	R	Unused. Will read back 0.
3	0	R	Unused. Will read back 0.
4	0	R	Unused. Will read back 0.
5	0	R	Unused. Will read back 0.
6	0	R	Unused. Will read back 0.
7	0	R	Unused. Will read back 0.

*Note: "X" denotes the number of the temperature channel. Register 48h is for Temp0, the internal temperature channel. 49h is for Temp1 (D1), 4Ah is for Temp2 (D2).

Register 50h, 51h - AINX* Control (Power-On Default 00h)

Bit	Name	R/W	Description
0	Assert $\overline{\text{CFAULT}}$ on HI_LIM = 0	R/W	When this bit is set, $\overline{\text{CFAULT}}$ is asserted when AINX* exceeds the AINX* high limit.
1	Alarm speed on HI_LIM = 0	R/W	When this bit is set, the fans go to alarm speed when AINX* exceeds the AINX* high limit.
2	$\overline{\text{INT}}$ on HI_LIM = 0	R/W	When this bit is set, $\overline{\text{INT}}$ is asserted when AINX* exceeds the AINX* high limit.
3	Alarm below low = 0	R/W	This bit indicates whether an alarm ($\overline{\text{INT}}$, $\overline{\text{CFAULT}}$ or Alarm Speed) is asserted when AINX* goes above or below the Low Limit. 1 = above. 0 = below.
4	Assert $\overline{\text{CFAULT}}$ on LO_LIM = 0	R/W	When this bit is set, $\overline{\text{CFAULT}}$ is asserted when AINX* crosses the AINX* low limit. Bit 3 decides whether $\overline{\text{CFAULT}}$ is asserted for going above or below the Low Limit.
5	Alarm speed on LO_LIM = 0	R/W	When this bit is set, the fans go to alarm speed when AINX* crosses the AINX* low limit. Bit 3 decides whether Alarm Speed is asserted for going above or be low the Low Limit.
6	$\overline{\text{INT}}$ on LO_LIM = 0	R/W	When this bit is set, $\overline{\text{INT}}$ is asserted when AINX* crosses the AINX* low limit. Bit 3 decides whether $\overline{\text{INT}}$ is asserted for going above or below the Low Limit.
7	Latch AIN Fault = 0	R/W	This bit latches an out of limit event (ie when AINX* goes above the high limit or crosses the low limit) on the AINX* channel. This bit is cleared by writing a 0 to it.

*Note: "X" denotes the number of the AIN channel. Register 50h controls AIN0 and 51h controls AIN1.

Register 58h, 59h - AINX Fan Mask (Power-On Default 00h)

Bit	Name	R/W	Description
0	Fan 0 = 0	R/W	If an AINX* out of limit event is generated such that fans should be driven at Alarm Speed then Fan0 will be set to this speed when this bit is set.
1	Fan 1 = 0	R/W	If an AINX* out of limit event is generated such that fans should be driven at Alarm Speed then Fan1 will be set to this speed when this bit is set.
2	Reserved	R/W	Undefined
3	Reserved	R/W	Undefined
4	Reserved	R/W	Undefined
5	Reserved	R/W	Undefined
6	Reserved	R/W	Undefined
7	Reserved	R/W	Undefined

*Note: "X" denotes the number of the AIN channel. Register 58h is for AIN0 and 59h is for AIN1.

Register 60h, 61h FanX Speed 1 Power-On Default FFh

Bit	Name	R/W	Description
3 - 0	FanX Normal Speed/ Min Speed	R/W	This nibble contains the Normal speed value for FanX. When in automatic fan speed control mode this nibble will contain the minimum speed which FanX will run at. The power-up default for the Min Speed should be 5hex which corresponds to 33% PWM duty cycle.
7 - 4	FanX Alarm Speed	R/W	This nibble contains the Alarm speed value for FanX.

*Note: "X" denotes the fan number. Register 60h is forFAN 0 and 61h is for FAN 1.

Register 68h, 69h - FanX* Speed 2 (Power-On Default 2Fh)

Bit	Name	R/W	Description
3 - 0	FanX Hot Plug Speed	R/W	This nibble contains the Hot Plug speed value for FanX*. This is the speed the other fan(s) runs at if FanX* is Hot Plug removed. If a fan is Hot Plug installed, it will run at Normal Speed.
5 – 4	PWM Frequency	R/W	This nibble allows programmability of the Nominal PWM Frequency for FanX*. The following options are supprted: Bits 5 –4 PWM Freq 00 15.625Hz 01 62.5Hz 10 250Hz - Default 11 1000Hz
7 - 6	Oscillator Frequency	R/W	These bits contain the oscillator frequency for the FanX* tach measurement. If set to 00 then tach measurement is disabled for FanX. Bit 7 Bit 6 Oscillator Frequency (Hz) 0 0 Measurement disabled 0 1 470 1 0 940 1 1 1880

*Note: "X" denotes the fan number. Register 68h is forFAN 0 and 69h is for FAN 1.

Register 70h, 71h - FanX* Tach Value (Power-On Default 00h)

Bit	Name	R/W	Description
7 - 0	FanX Tach Value	R	This register contains the value of the FanX* tachometer measurement.

*Note: "X" denotes the fan number. Register 70h is forFAN 0 and 71h is for FAN 1.

Register 78h, 79h - FanX Tach High Limit (Power-On Default FFh)

Bit	Name	R/W	Description
7 - 0	FanX Tach High Limit	R/W	This register contains the limit value for the FanX* tachometer measurement. Since the tachometer circuit counts between tach pulses, a slow fan will result in a larger measured value, so exceeding the limit is the way to detect a slow or stopped fan.

*Note: "X" denotes the fan number. Register 78h is for FAN 0 and 79h is for FAN 1.

Register 80h, 81h, 82h - TempX* Tmin (Power-On Default 001??000)

Bit	Name	R/W	Description
7 - 0	TempX Tmin	R/W	This register contains the minimum temperature value for automatic fan speed control based on the TempX* temperature. On power-up pin 18 is sampled by the ADC to determine the default value for TempX* Tmin. If pin 18 is strapped to GND or V_{CC} then this register defaults to 32ºC. There are 8 strappable options on pin 18. These options are used to set TempX Tmin and the Install bit in the Config Register (Reg 01h, Bit 0). The options are as follows:

ADC MSBs	R1	R2	Install	TempX* Tmin
111	0	∞	1	Disabled
101	18k	82k	1	48ºC
110	22k	47k	1	40ºC
100	12k	15k	1	32ºC
011	15k	12k	0	32ºC
010	47k	22k	0	40ºC
001	82k	18k	0	48ºC
000	∞	0	0	Disabled

*Note: "X" denotes the number of the temperature channel. Register 80h is for Temp0, the internal temperature channel. 81h is for Temp1 (D1), 82h is for Temp2 (D2).

Register 88h, 89h, 8Ah TempX* Trange / Hyst Power-On Default 51h

Bit	Name	R/W	Description
3 - 0	TempX Trange	R/W	This nibble contains the temperature range over which automatic fan speed control operates based on the TempX* measured temperature. Only a limited number of temperature ranges are supported as follows: Bits 3-0 TRANGE 0000 5ºC 0001 10ºC 0010 20ºC 0011 40ºC 0100 80ºC
7 – 4	TempX Hyst	R/W	This nibble allows programmability of the Hysteresis level around the temperature at which the fan being controlled by TempX will switch on in automatic fan speed control mode. Values from 0ºC to 14ºC are possible. If a value other than 0C is programmed as a Hysteresis value then the fan will switch on when TempX goes above Tmin, but will remain on until TempX falls below Tmin - Thyst. Between Tmin – Thyst to Tmin the fan will run at the programmed minimum pulse width in the FanX Speed 1 register.

*Note: "X" denotes the number of the temperature channel. Register 88h is for Temp0, the internal temperature channel. 89h is for Temp1 (D1), 8Ah is for Temp2 (D2).

Register 90h, 91h, 92h - TempX* High Limit (Power-On Default 60ºC for Local Sensor, 70ºC for Remote Sensors)

Bit	Name	R/W	Description
7 - 0	TempX High Limit	R/W	This register contains the high limit value for the TempX* measurement.

*Note: "X" denotes the number of the temperature channel. Register 90h is for Temp0, the internal temperature channel. 91h is for Temp1 (D1), 92h is for Temp2 (D2).

Register 98h, 99h, 9Ah - TempX* Low Limit (Power-On Default 80ºC for Local Sensor, 100ºC for Remote Sensors)

Bit	Name	R/W	Description
7 - 0	TempX Low Limit	R/W	This register contains the low limit value for the TempX* measurement.

*Note: "X" denotes the number of the temperature channel. Register 98h is for Temp0, the internal temperature channel. 99h is for Temp1 (D1), 9Ah is for Temp2 (D2).

Register A0h, A1h, A2h - TempX* Measured Value (Power-On Default 00h)

Bit	Name	R/W	Description
7 - 0	TempX Value	R	This register contains the actual TempX* measured value.

*Note: "X" denotes the number of the temperature channel. Register A0h is for Temp0, the internal temperature channel. A1h is for Temp1 (D1), A2h is for Temp2 (D2).

Register A8h, A9h - AINX* High Limit (Power-On Default FFh)

Bit	Name	R/W	Description
7 - 0	AINX High Limit	R/W	This register contains the high limit value for the AINX* analog input channel.

*Note: "X" denotes the number of the AIN channel. Register A8h is for AIN0 and A9h is for AIN1.

Register B0h, B1h - AINX* Low Limit (Power-On Default 00h)

Bit	Name	R/W	Description
7 - 0	AINX Low Limit	R/W	This register contains the low limit value for the AINX* analog input channel.

*Note: "X" denotes the number of the AIN channel. Register B0h is for AIN0 and B1h is for AIN1.

Register B8h, B9h - AINX* Measured Value (Power-On Default 00h)

Bit	Name	R/W	Description
7 – 0	AINX value	R	This register contains the measured value of the AINX* analog input channel.

*Note: "X" denotes the number of the AIN channel. Register B8h is for AIN0 and B9h is for AIN1.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Pin QSOP Package (RQ-24)