CDMA Power Management System

ADP3510

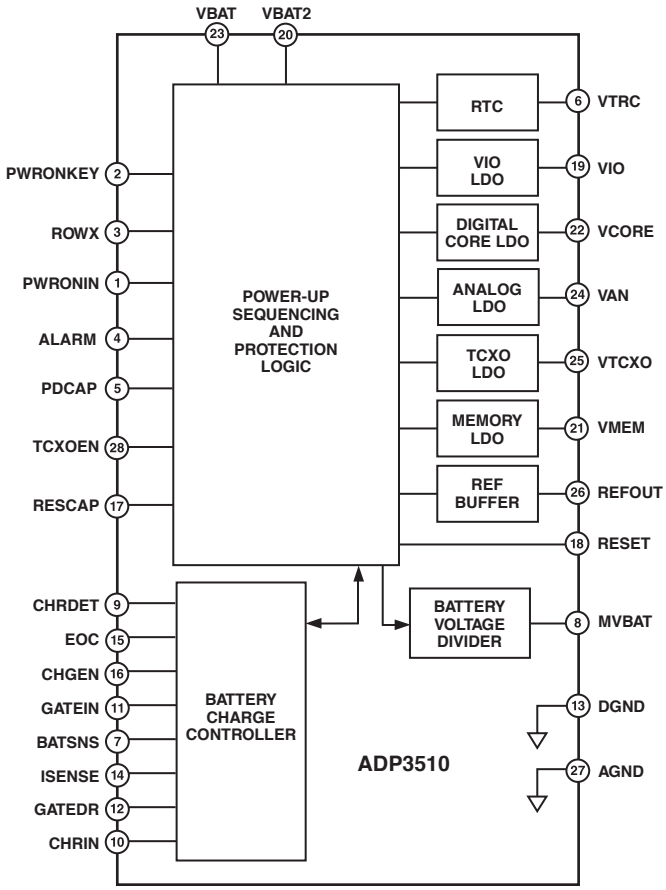
FEATURES

Handles All CDMA Baseband Power Management
Six LDOs Optimized for Specific CDMA Subsystems
Li-Ion and NiMH Battery Charge Function
Ambient Temperature: –20°C to +85°C
TSSOP 28-Lead Package
Optimized for LSI Logic Baseband Chipset

APPLICATIONS

CDMA Handsets

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3510 is a multifunction power system chip optimized for CDMA handset power management. It contains six specialized LDOs, one to power each of the critical CDMA subblocks. Sophisticated controls are available for power-up during battery charging, keypad interface, and RTC alarm. If a Li-Ion battery is being charged, the charge circuit maintains low current charging during the initial charge phase and provides an end of charge (EOC) signal when the cell has been fully charged.

The ADP3510 is specified over the temperature range of –20°C to +85°C and is available in a narrow body TSSOP 28-Lead package.

REV. 0

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ADP3510–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS[1] (–20°C ≤ T_A ≤ +85°C, VBAT = VBAT2 = 3.2 V–7.5 V, CVIO = CVCORE = CVAN = CVMEM = 2.2 μF, VTCXO = 0.47 μF, CVBAT = 10 μF, min. loads applied on all outputs, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SHUTDOWN SUPPLY CURRENT	ICC					
VBAT ≤ 2.5 V		VBAT = VBAT2 = 2.3 V		5	15	μA
(Deep Discharged Lockout Active)						
2.5 V < VBAT ≤ 3.2 V (UVLO Active)		VBAT = VBAT2 = 3.15 V		30	55	μA
VBAT >3.2 V		VBAT = VBAT2 = 4.0 V		45	60	μA
OPERATING GROUND CURRENT	IGND					
All LDOs On Except TCXO		Minimum Loads		300	390	mA
All LDOs On		Minimum Loads		340	430	mA
All LDOs On		Maximum Loads		2.0	3.5	% of Max Load Current
UVLO ON THRESHOLD	VBAT		3.1	3.2	3.3	V
UVLO HYSTERESIS	VBAT			200		mV
DEEP DISCHARGED LOCKOUT ON THRESHOLD	VBAT		2.0	2.4	2.75	V
DEEP DISCHARGED LOCKOUT HYSTERESIS	VBAT			100		mV
INPUT HIGH VOLTAGE (PWRONIN, TCXOEN, CHGEN, GATEIN)	V_{IH}		2.0			V
INPUT LOW VOLTAGE (PWRONIN, TCXOEN, CHGEN, GATEIN)	V_{IL}				0.4	V
INPUT HIGH BIAS CURRENT (PWRONIN, TCXOEN, CHGEN, GATEIN)	I_{IH}				1.0	μA
INPUT LOW BIAS CURRENT (PWRONIN, TCXOEN, CHGEN, GATEIN)	I_{IL}		–1.0			μA
PWRONKEY INPUT HIGH VOLTAGE	V_{IH}		0.7 × VBAT			V
PWRONKEY INPUT LOW VOLTAGE	V_{IL}				0.3 × VBAT	V
PWRONKEY INPUT PULLUP RESISTANCE TO VBAT			70	105	145	kΩ
THERMAL SHUTDOWN THRESHOLD[2]				150		°C
THERMAL SHUTDOWN HYSTERESIS				25		°C
ROWX CHARACTERISTICS						
ROWX Output Low Voltage	V_{OL}	PWRONKEY = Low I_{OL} = 200 μA			0.4	V
ROWX Output High Leakage Current	I_L	PWRONKEY = High V(ROWX) = 5 V			1	μA
I/O LDO (VIO)						
Output Voltage	VIO	Line, Load, Temp	2.85	2.935	3.02	V
Line Regulation	ΔVIO	Minimum Load		1		mV
Load Regulation	ΔVIO	50 μA ≤ I_{LOAD} ≤ 25 mA		3		mV
Output Capacitor Required for Stability	C_O		2.2			μF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV I_{LOAD} = 25 mA		50	150	mV
DIGITAL CORE LDO (VCORE)						
Output Voltage	VCORE	Line, Load, Temp	1.78	1.85	1.92	V
Line Regulation	ΔVCORE	Minimum Load		1		mV
Load Regulation	ΔVCORE	50 μA ≤ I_{LOAD} ≤ 120 mA		8		mV
Output Capacitor Required for Stability	C_O		2.2			μF

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
ANALOG LDO (VAN)						
Output Voltage	VAN	Line, Load, Temp	2.85	2.935	3.02	V
Line Regulation	ΔVAN	Minimum Load		1		mV
Load Regulation	ΔVAN	50 µA ≤ I_{LOAD} ≤ 75 mA		6		mV
Output Capacitor Required for Stability	C_O		2.2			µF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ 100 mV				
		I_{LOAD} = 75 mA		100	175	mV
Ripple Rejection	ΔVBAT/	f = 217 Hz (T = 4.6 ms)		75		dB
	ΔVAN	VBAT = 3.6 V				
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz		80		µV rms
		I_{LOAD} = 75 mA				
		VBAT = 3.6 V				
TCXO LDO (VTCXO)						
Output Voltage	VTCXO	Line, Load, Temp	2.71	2.765	2.82	V
Line Regulation	ΔVTCXO	Minimum Load		1		mV
Load Regulation	ΔVTCXO	50 µA ≤ I_{LOAD} ≤ 10 mA		3		mV
Output Capacitor Required for Stability	C_O		0.47			µF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV			175	mV
		I_{LOAD} = 10 mA				
Ripple Rejection	ΔVBAT/	f = 217 Hz (T = 4.6 ms)		75		dB
	ΔVTCXO	VBAT = 3.6 V				
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz		80		µV rms
		I_{LOAD} = 10 mA				
		VBAT = 3.6 V				
REAL-TIME CLOCK LDO/ BATTERY CHARGER (VRTC)						
Maximum Output Voltage	VRTC	1 µA ≤ I_{LOAD} ≤ 6 µA	2.77	2.85	2.93	V
Off Reverse Input Current	I_L	2.0 V < VBAT < UVLO			1	µA
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV			175	mV
		I_{LOAD} = 10 µA				
MEMORY LDO (VMEM)						
Output Voltage	VMEM	Line, Load, Temp	2.85	2.935	3.02	V
Line Regulation	ΔVMEM	Minimum Load		1		mV
Load Regulation	ΔVMEM	50 µA ≤ I_{LOAD} ≤ 60 mA		5		mV
Output Capacitor Required for Stability	C_O			2.2		µF
Dropout Voltage	V_{DO}	V_O = $V_{INITIAL}$ – 100 mV		100	175	mV
		I_{LOAD} = 60 mA				
REFOUT						
Output Voltage	VREFOUT	Line, Load, Temp	1.19	1.210	1.23	V
Line Regulation	ΔVREFOUT	Minimum Load		0.3		mV
Load Regulation	ΔVREFOUT	0 µA ≤ I_{LOAD} ≤ 50 µA		0.6		mV
		VBAT = 3.6 V				
Ripple Rejection	ΔVBAT/	f = 217 Hz (T = 4.6 ms)		75		dB
	ΔVREFOUT	VBAT = 3.6 V				
Maximum Capacitive Load	C_O			100		pF
Output Noise Voltage	V_{NOISE}	f = 10 Hz to 100 kHz		40		mV rms
RESET GENERATOR (RESET)						
Output High Voltage	V_{OH}	I_{OH} = +500 µA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = –500 µA			0.25	V
Output Current	I_{OL}/I_{OH}				1	mA
Delay Time per Unit Capacitance Applied to RESCAP Pin	T_D		0.8	1.5	4.0	ms/nF
SEQUENCING						
Delay Time per Unit Capacitance Applied to PDCAP Pin	T_D		0.3	0.8	3.0	ms/nF
PDCAP Charging Current	I_{OH}	V_{PDCAP} = 0	2.5	5	8	µA
VAN Discharge Resistance				200		Ω
VIO Discharge Resistance				200		Ω

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
BATTERY VOLTAGE DIVIDER						
Divider Ratio	BATSNS/MVBAT	TCXOEN = High	2.94	3.00	3.06	
Divider Impedance at MVBAT	Z_O		50	80	110	kΩ
Divider Leakage Current		TCXOEN = Low			1	µA
Divider Resistance		TCXOEN = High	230	350	430	kΩ
BATTERY CHARGER						
Charger Output Voltage	BATSNS	4.5 V < CHRIN < 10 V, CHGEN = Low, T_A = 0°C to 50°C	4.158	4.200	4.242	V
Charger Output Voltage	BATSNS	CHRIN = 10 V, V_{SENSE} = 10 mV, T_A = 0°C to 50°C	4.162	4.200	4.238	V
Load Regulation	ΔBATSNS	CHRIN = 5 V, 0 < CHRIN – ISENSE < Current Limit Threshold, CHGEN = Low		2	8	mV
CHRDET on Threshold	CHRIN–VBAT	VBAT = 3.6 V		260		mV
CHRDET Hysteresis				70		mV
CHRDET Off Delay[3]		CHRIN < VBAT		6		ms/nF
CHRIN Supply Current		CHRIN = 5 V		0.6	1	mA
Current Limit Threshold	CHRIN–ISENSE					
High Current Limit (100%: UVLO Not Active)		CHRIN = 5 V dc, VBAT = 3.6 V, CHGEN = Low	150	172	195	mV
Low Current Limit (10%: UVLO Active)		CHRIN = 5 V, VBAT = 2 V, CHGEN = Low	2	15	30	mV
ISENSE Bias Current		CHRIN = 5 V		180	250	µA
End of Charge Signal Threshold	CHRIN–ISENSE	CHRIN = 5 V dc, VBAT > 4.0 V, CHGEN = Low	2	12	26	mV
End of Charge Reset Threshold	VBAT	CHGEN = Low	3.82	3.96	4.10	V
GATEDR Transition Time	t_R, t_F	CHRIN = 5 V, VBAT > 3.6 V, CHGEN = High, C_L = 2 nF	1		10	µs
GATEDR High Voltage	V_{OH}	CHRIN = 5 V, VBAT = 3.6 V, CHGEN = High, GATEIN = High, I_{OH} = –1 mA	4.5			V
GATEDR Low Voltage	V_{OL}	CHRIN = 5 V, VBAT = 3.6 V, CHGEN = High, GATEIN = Low, I_{OL} = +1 mA			0.5	V
Output High Voltage (EOC, CHRDET)	V_{OH}	I_{OH} = –250 µA	2.4			V
Output Low Voltage (EOC, CHRDET)	V_{OL}	I_{OL} = +250 µA			0.25	V
Battery Overvoltage Protection Threshold (GATEDR→High)	BATSNS	CHRIN = 7.5 V, CHGEN = High, GATEIN = Low	5.30	5.50	5.70	V
Battery Overvoltage Protection Hysteresis	BATSNS	CHRIN = 7.5 V, CHGEN = High, GATEIN = Low		400		mV

NOTES

[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

[2]This feature is intended to protect against catastrophic failure of the device. Maximum allowed operating junction temperature is 125°C. Operation beyond 125°C could cause permanent damage to the device.

[3]Delay set by external capacitor on the RESCAP pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

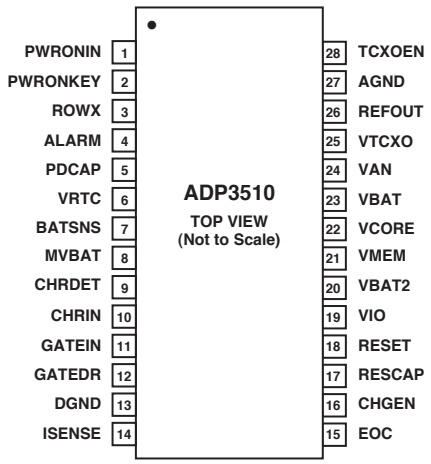
Voltage on any pin with respect to any GND Pin . . . . . –0.3 V to +10 V
Voltage on any pin may not exceed VBAT, with the following exceptions: CHRIN, GATEDR, ISENSE
Storage Temperature Range . . . . . –65°C to +150°C
Operating Ambient Temperature Range . . . . –20°C to +85°C
Maximum Junction Temperature . . . . . 125°C
θ_{JA}, Thermal Impedance (TSSOP-28)
2-Layer PCB . . . . . 98°C/W
4-Layer PCB . . . . . 68°C/W
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADP3510ARU	–20°C to +85°C	RU-28

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1	PWRONIN	Power-On/-Off Signal from Microprocessor
2	PWRONKEY	Power-On/-Off Key
3	ROWX	Power Key Interface Output
4	ALARM	Alternative Power-On
5	PDCAP	Power-On Delay Timer Capacitor
6	VRTC	VRTC LDO Output
7	BATSNS	Battery Voltage Sense Input
8	MVBAT	Divided Battery Voltage Output
9	CHRDET	Charge Detect Output
10	CHRIN	Charger Input Voltage
11	GATEIN	Microprocessor Gate Input Signal
12	GATEDR	Gate Drive Output
13	DGND	Digital Ground
14	ISENSE	Charge Current Sense Input
15	EOC	End of Charge Signal
16	CHGEN	Charger Enable for GATEIN, NiMH Pulse Charging
17	RESCAP	Reset Delay Time
18	RESET	Main Reset
19	VIO	I/O LDO Output
20	VBAT2	Battery Input Voltage 2
21	VMEM	Memory LDO Output
22	VCORE	Digital Core LDO Output
23	VBAT	Battery Input Voltage
24	VAN	Analog LDO Output
25	VTCXO	TCXO LDO Output
26	REFOUT	Output Reference
27	AGND	Analog Ground
28	TCXOEN	TCXO LDO Enable and MVBAT Enable

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3510 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table I. LDO Control Logic

	DDLO	UVLO*	CHRDET	PWRONKEY	PWRONIN or ALARM	TCXOEN	VIO	VCORE	VAN	VTCXO	VMEM	VRTC	MVBAT	REFOUT
Phone Status														
State #1 battery deep discharged	L	X	X	X	X	X	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
State #2 phone off	H	L	X	X	X	X	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
State #3 phone off, turn on allowed	H	H	L	H	L	X	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF
State #4 charger applied	H	H	H	X	X	L	ON	ON	ON	ON	ON	ON	OFF**	ON
State #5 phone turned on by user key	H	H	X	L	X	L	ON	ON	ON	ON	ON	ON	OFF**	ON
State #6 phone turned on by BB	H	H	L	H	H	L	ON	ON	ON	OFF	ON	ON	OFF	ON
State #7 phone and TCXO LDO kept on by BB	H	H	L	H	H	H	ON	ON	ON	ON	ON	ON	ON	ON

*UVLO is only active when phone is turned off. UVLO is ignored once the phone is turned on.
**Controlled by TCXOEN.

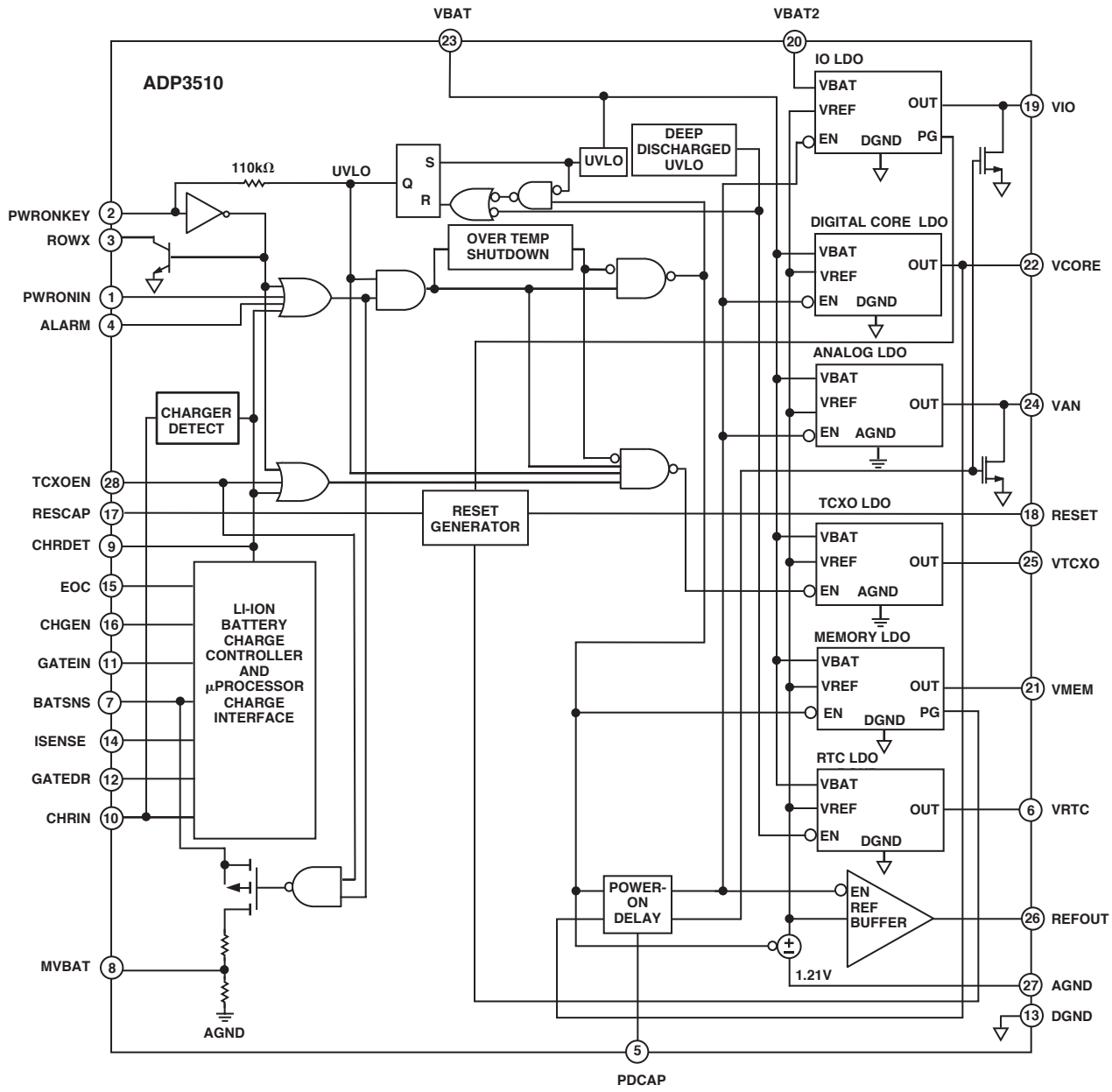


Figure 1. Functional Block Diagram

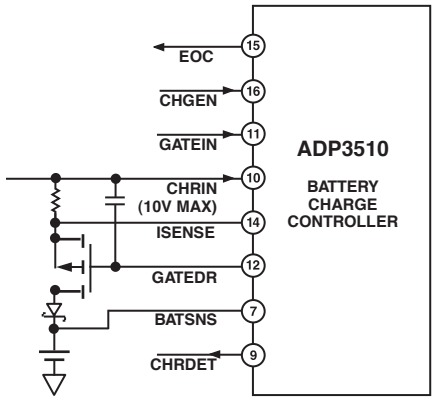
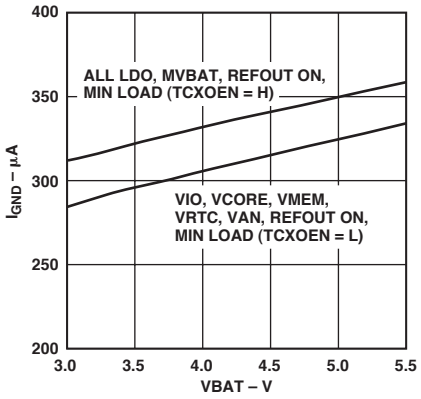
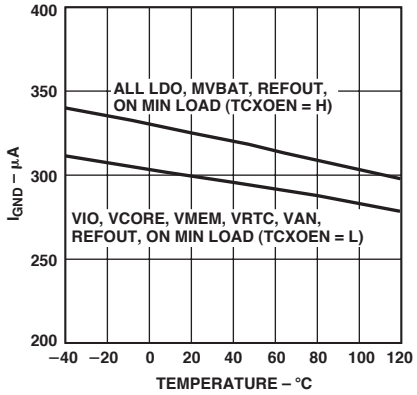


Figure 2. Battery Charger Typical Application

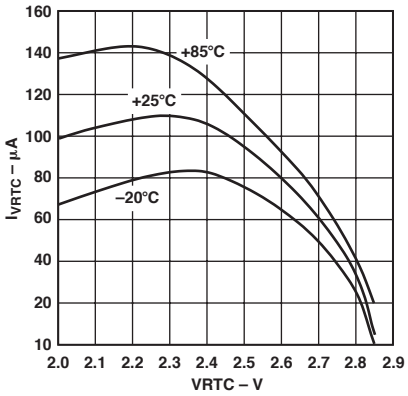
ADP3510—Typical Performance Characteristics (VBAT = 3.6 V, T_A = 25°C, unless otherwise specified.)



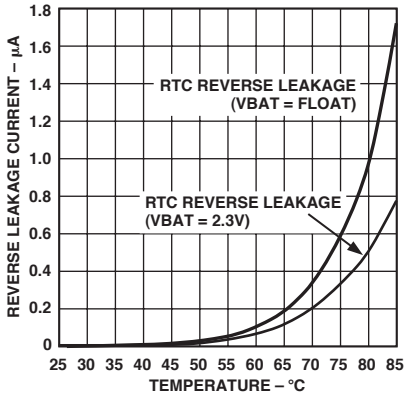
TPC 1. Ground Current vs. Battery Voltage



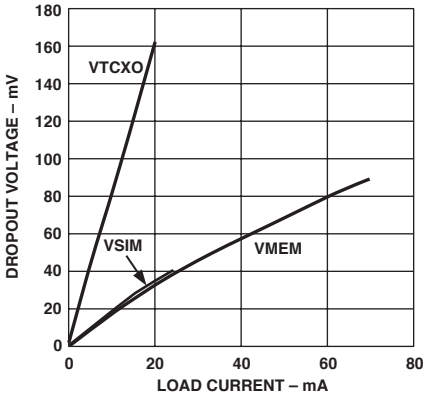
TPC 2. Ground Current vs. Temperature



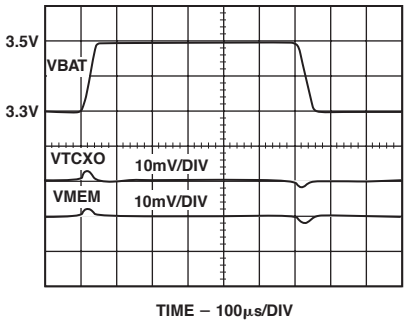
TPC 3. RTC I/V Characteristic



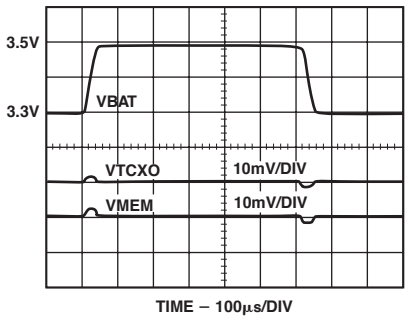
TPC 4. VTRC Reverse Leakage Current vs. Temperature



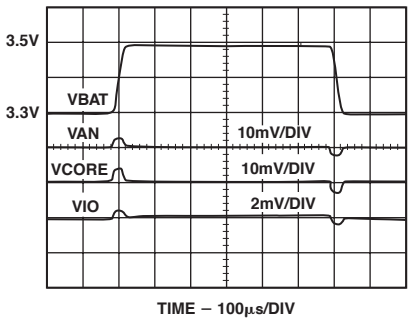
TPC 5. Dropout Voltage vs. Load Current



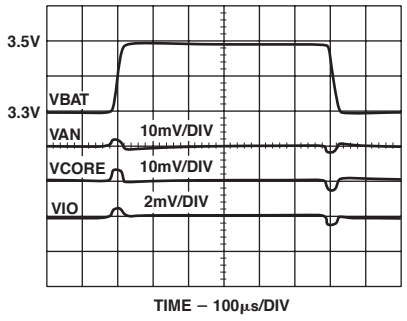
TPC 6. Line Transient Response, Minimum Loads



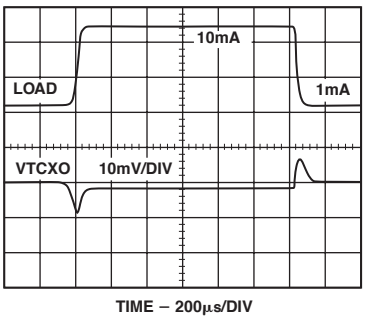
TPC 7. Line Transient Response, Maximum Loads



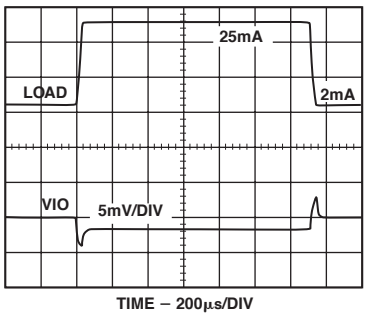
TPC 8. Line Transient Response, Minimum Loads



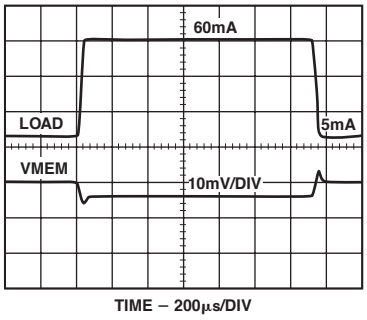
TPC 9. Line Transient Response, Maximum Loads



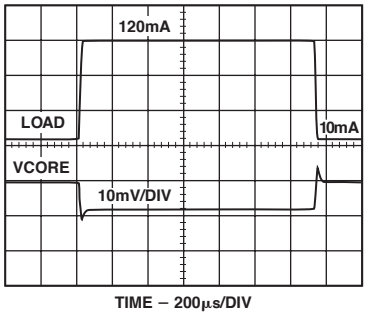
TPC 10. VTCXO Load Step



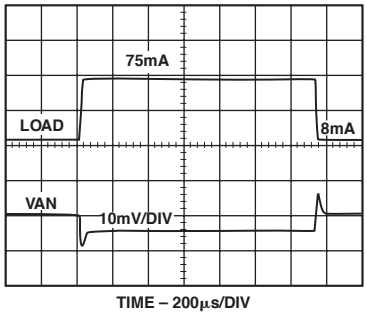
TPC 11. VIO Load Step



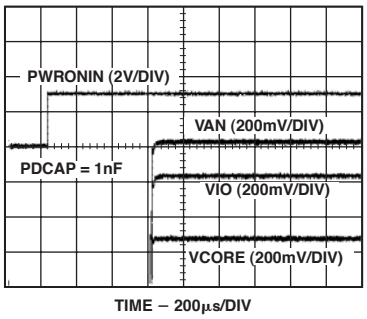
TPC 12. VMEM Load Step



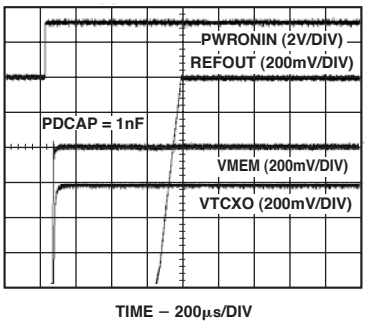
TPC 13. VCORE Load Step



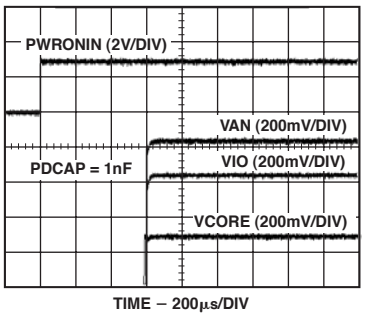
TPC 14. VAN Load Step



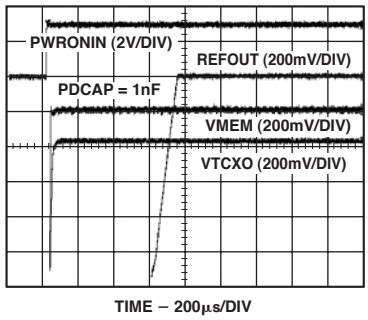
TPC 15. Turn On Transient by PWRONIN, Minimum Load



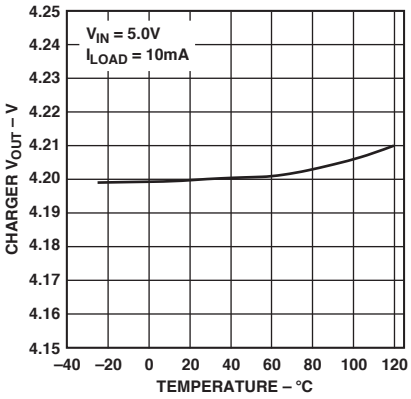
TPC 16. Turn On Transient by PWRONIN, Minimum Load



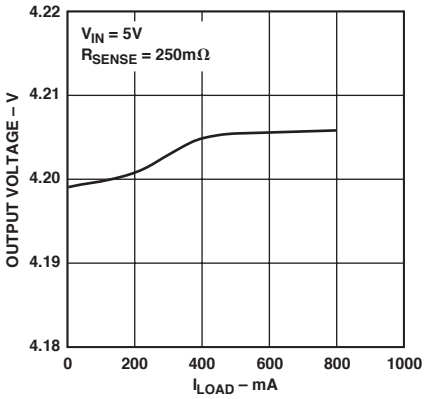
TPC 17. Turn On Transient by PWRONIN, Maximum Load



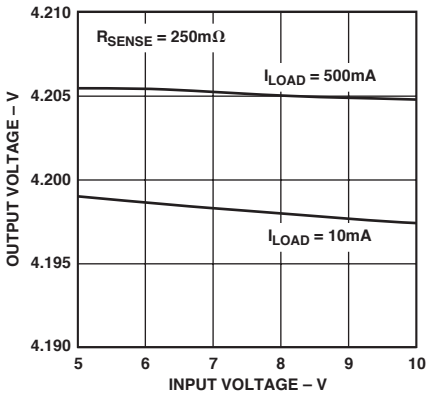
TPC 18. Turn On Transient by PWRONIN, Maximum Load



TPC 19. Charger V_{OUT} vs. Temperature, V_{IN} = 5.0 V, I_{LOAD} = 10mA



TPC 20. Charger V_{OUT} vs. I_{LOAD} (V_{IN} = 5.0 V)



TPC 21. Charger V_{OUT} vs. V_{IN}

THEORY OF OPERATION

The ADP3510 is a total solution power management chip for use with CDMA baseband chipsets and is optimized for the CBP3.0/4.0 type chipsets. Figure 1 shows a block diagram of the ADP3510.

The ADP3510 contains several blocks:

- Six Low Dropout Regulators (Input-Output, Core, Analog, Crystal Oscillator, Memory, Realtime Clock)
- Reset Generator
- Buffered Precision Reference
- Lithium Ion Charge Controller and Processor Interface
- Power-On/-Off Logic
- Undervoltage Lockout
- Deep Discharge Lockout

These functions have traditionally been done either as a discrete implementation or as a custom ASIC design. The ADP3510 combines the benefits of both worlds by providing an integrated standard product where every block is optimized to operate in a CDMA environment while maintaining a cost-competitive solution.

Figure 3 shows the external circuitry associated with the ADP3510. Only a minimal number of support components are required.

Input Voltage

The input voltage range of the ADP3510 is 3.2 V to 7.5 V and is optimized for a single Li-Ion cell or three NiMH cells. The thermal impedance of the ADP3510 is 68°C/W for four layer boards. The end of charge voltage for high capacity NiMH cells can be as high as 5.5 V. Power dissipation should be calculated at maximum ambient temperatures and battery voltage in order not to exceed the 125°C maximum allowable junction temperature. Figure 4 shows the maximum power dissipation as a function of ambient temperature.

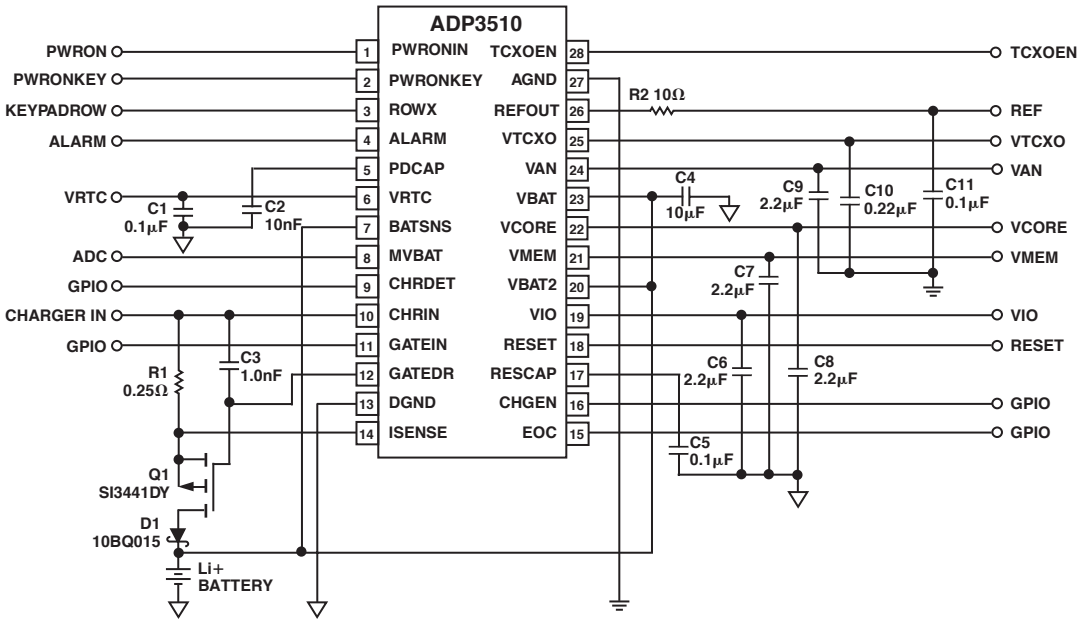


Figure 3. Typical Application Circuit

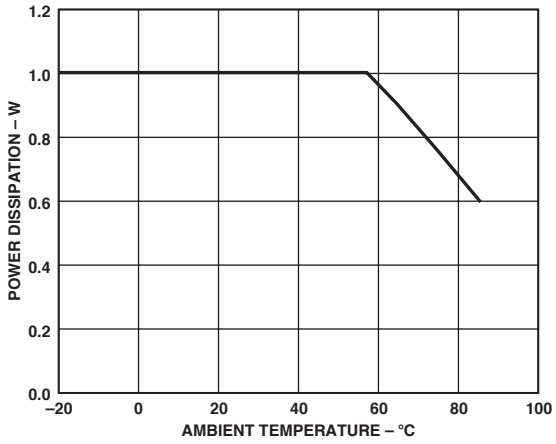


Figure 4. Power Dissipation vs. Temperature

However, high battery voltages normally occur only when the battery is being charged and the handset is not in conversation mode. In this mode, there is a relatively light load on the LDOs. A fully charged Li-Ion battery is 4.245 V, where the ADP3510 can deliver the maximum power (0.52 W) up to 85°C ambient temperature.

Low Dropout Regulators (LDOs)
The ADP3510 high performance LDOs are optimized for their given functions by balancing quiescent current, dropout voltage, regulation, ripple rejection, and output noise. 2.2 μF tantalum or MLCC ceramic capacitors are recommended for use with the core, memory, IO, and analog LDOs. A 0.22 μF capacitor is recommended for the TCXO LDO.

Digital Core LDO (VCORE)
The digital core LDO supplies the baseband circuitry in the handset (baseband processor and baseband converter). The LDO has been optimized for very low quiescent current at light loads as this LDO is on at all times.

Memory LDO (VMEM)
The memory LDO supplies the memory of the baseband processor. The memory LDO is capable of supplying 60 mA of current and has also been optimized for low quiescent current and will power up at the same time as the core LDO.

Analog LDO (VAN)
This LDO has the same features as the core LDO. It has furthermore been optimized for good low frequency ripple rejection for use with the baseband converter sections in order to reject the ripple coming from the RF power amplifier. VAN is rated to 75 mA load, which is sufficient to supply the complete analog section of the baseband converter. The analog LDO is controlled by the power-on delay block of the ADP3510.

TCXO LDO (VTCXO)
The TCXO LDO is intended as a supply for a temperature compensated crystal oscillator, which needs its own ultralow noise supply. VTCXO is rated for 10 mA of output current and is turned on when TCXOEN is asserted.

RTC LDO (VRTC)
The RTC LDO charges up a rechargeable lithium type coin cell to run the realtime clock module. It has been designed to charge manganese lithium batteries such as the ML series (ML614, ML621, or ML1220) from Sanyo. The ML621 has a small physical size (6.8 mm diameter) and will give many hours of backup time.

The ADP3510 supplies current both for charging the coin cell and for the RTC module. The nominal charging voltage is 2.85 V, which ensures long cell life while obtaining in excess of 90% of the nominal capacity. In addition, it features a very low quiescent current since this LDO is running all the time, even when the handset is switched off. It also has reverse current protection with low leakage, which is needed when the main battery is removed and the coin cell supplies the RTC module.

IO LDO (VIO)
The IO LDO generates the voltage needed for the peripheral subsystems of the baseband processor, including GPIO, display, and serial interfaces. It is rated for 25 mA of supply current and is controlled by the power-on delay block of the ADP3510.

Reference Output (REFOUT)
The reference output is a low noise, high precision reference with a guaranteed accuracy of 1.65% over temperature. The reference can be used with the baseband converter, if the converter's own reference is not accurate. This may significantly reduce the calibration time needed for the baseband converter during production.

Power ON/OFF
The ADP3510 handles all issues regarding the powering ON and OFF of the handset. It is possible to turn on the ADP3510 in four different ways:

- Pulling the PWRONKEY Low
- Pulling PWRONIN High
- Pulling ALARM High
- CHRIN Exceeds CHRDET Threshold

Pulling the PWRONKEY low is the normal way of turning on the handset. This will turn on all the LDOs, as long as the PWRONKEY is held low. When the VIO LDO comes into regulation, the RESET timer is started. After timing out, the RESET pin goes high, allowing the baseband processor to start up. With the baseband processor running, it can poll the ROWX pin of the ADP3510 to determine if the PWRONKEY has been depressed and pull PWRONIN high. Once the PWRONIN is taken high, the PWRONKEY can be released. Note that by monitoring the ROWX pin, the baseband processor can detect a second PWRONKEY press and turn the LDOs off in an orderly manner. In this way, the PWRONKEY can be used for ON/OFF control.

Pulling the ALARM pin high is how the alarm in the realtime clock module will turn the handset on. Asserting ALARM will turn the core, IO, memory, and analog LDOs on, starting up the baseband processor.

Applying an external charger can also turn the handset on. This will turn on all the LDOs, again starting up the baseband processor. Note that if the battery voltage is below the undervoltage lockout threshold, applying the adapter will not start up the LDOs.

Power On Delay
The power-on delay block in the ADP3510 controls the turn-on sequence of VCORE, VIO, and VAN. Asserting a power-on in one of the four above methods will start the LDOs in the following sequence:

1. The VMEM LDO will start up.
2. The VIO and VAN outputs will be discharged by the power-on delay block. The discharge delay time is set by the value of the PDCAP.
3. After the discharge time has expired, the VCORE LDO is allowed to start up.
4. When the output of VCORE exceeds 1.2 V, the VIO and VAN LDOs are allowed to start up.

The power-on delay is set by an external capacitor on PDCAP:

$$t_{PD} = 0.8\,\frac{ms}{nF} \times C_{PDCAP} \quad (1)$$

See Figure 5 for the power-up timing sequence.

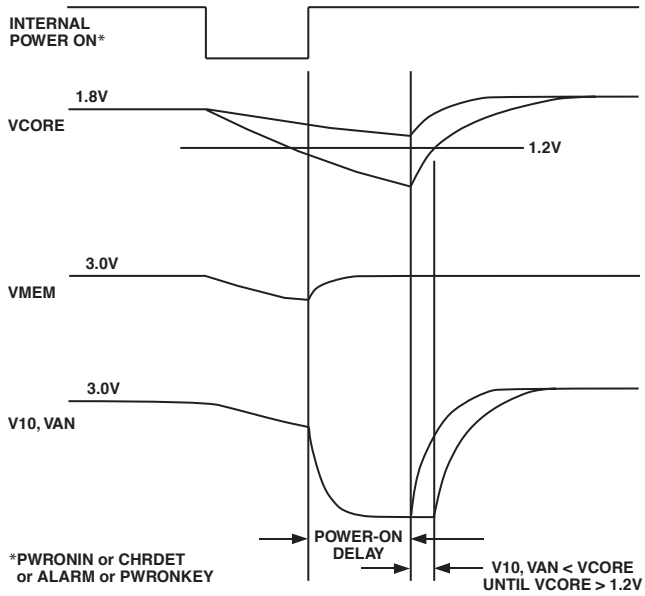


Figure 5. Power-Up Timing Diagram

Deep Discharge Lockout (DDLO)
The DDLO block in the ADP3510 will shut down the handset in the event the software fails to turn off the phone when the battery drops below 2.9 V to 3.0 V. The DDLO will shut down the handset when the battery falls below 2.4 V to prevent further discharge and damage to the cell.

Undervoltage Lockout (UVLO)
The UVLO function in the ADP3510 prevents startup when the initial voltage of the battery is below the 3.2 V threshold. If the battery voltage is this low with no load, there is insufficient capacity left to run the handset. When the battery is greater than 3.2 V, such as inserting a fresh battery, the UVLO comparator trips and the threshold is reduced to 3.0 V. This allows the handset to start normally until the battery decays to below 3.0 V. Note that the DDLO has enabled the RTC LDO under this condition.

Once the system is started and the core, memory, analog, and IO LDOs are up and running, the UVLO function is entirely disabled. The ADP3510 is then allowed to run until the battery voltage reaches the DDLO threshold, typically 2.4 V. Normally, the battery voltage is monitored by the baseband processor and usually shuts the phone off at around 3.0 V.

If the handset is off and the battery voltage drops below 3.0 V, the UVLO circuit disables startup and puts the ADP3510 into UVLO shutdown mode. In this mode, the ADP3510 draws very low quiescent current, typically 30 µA. The RTC LDO is still running until the DDLO disables it. In this mode, the ADP3510 draws 5 µA of quiescent current. NiMH batteries can reverse polarity if the 3-cell battery voltage drops below 3.0 V, which will degrade the battery's performance. Lithium Ion batteries will lose their capacity if over discharged repeatedly so minimizing the quiescent currents helps prevent battery damage.

RESET
The ADP3510 contains a reset circuit that is active both at power-up and power-down. The RESET pin is held low at initial power-up. An internal power good signal is generated by the IO LDO when its output is in regulation which starts the reset delay timer. The delay is set by an external capacitor on RESCAP:

$$t_{RESET} = 1.5\,\frac{ms}{nF} \times C_{RESCAP} \quad (2)$$

Should the IO or MEM LDO drop out of regulation, the RESET signal will go low and remain low until the IO and MEM LDO outputs are back in regulation and the RESET timer has timed out. At power-off, RESET will be kept low to prevent any baseband processor starts.

Over-Temperature Protection
In case of a failure that causes excess power dissipation to the IC, the thermal shutdown function will be activated. The maximum die temperature for the ADP3510 is 125°C. If the die temperature exceeds 160°C, the ADP3510 will disable all the LDOs except the RTC LDO. The LDOs will not be re-enabled before the die temperature is below 125°C, regardless of the state of PWRONKEY, PWRONIN, ALARM, and CHRDET. This ensures that the handset will always power-off before the ADP3510 exceeds its absolute maximum thermal ratings.

Battery Charging
The ADP3510 battery charger can be used with lithium ion (Li+) and nickel metal hydride (NiMH) batteries. The charger initialization, trickle charging, and Li+ charging are implemented in hardware. Battery type determination and NiMH charging must be implemented in software.

The charger block works in three different modes:

- Low Current (Trickle) Charging
- Lithium Ion Charging
- Nickel Metal Hydride Charging

See Figure 6 for the battery charger flowchart.

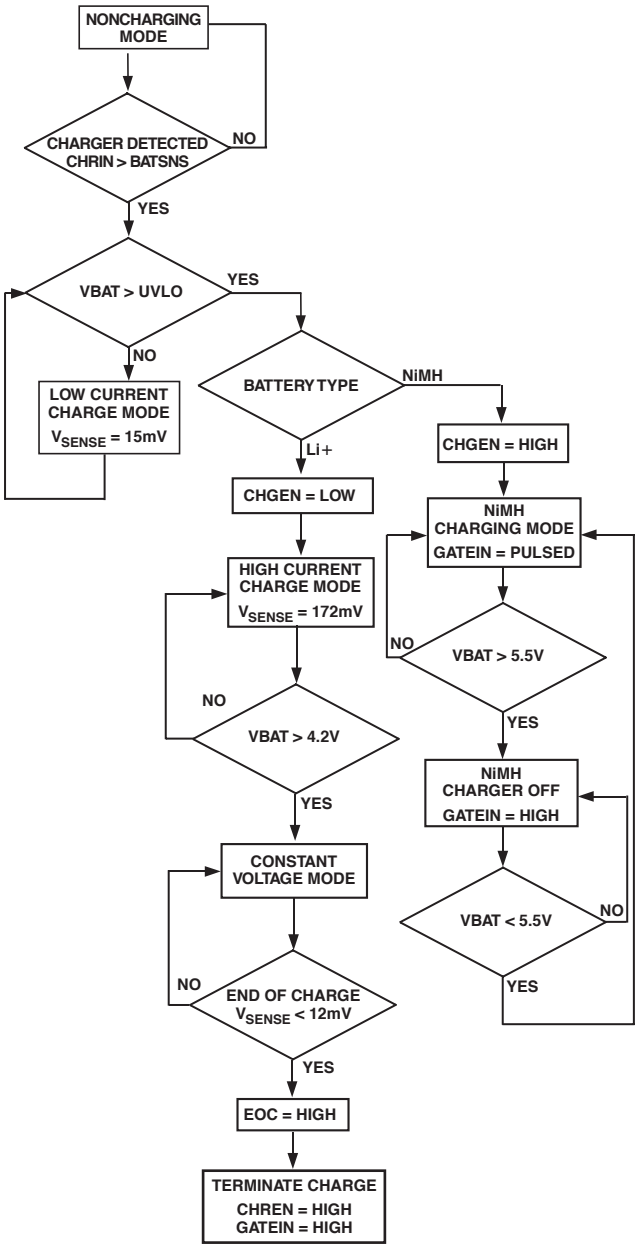


Figure 6. Battery Charger Flowchart

Trickle Charging

When the battery voltage is below the UVLO threshold, the charge current is set to the low current limit, or about 10% of the full charge current. The low current limit is determined by the voltage developed across the current sense resistor. Therefore, the trickle charge current can be calculated by:

$$I_{CHR(TRICKLE)} = \frac{15\ mV}{R_{SENSE}} \quad (3)$$

Trickle charging is performed for deeply discharged batteries to prevent undue stress on either the battery or the charger.

Trickle charging will continue until the battery voltage exceeds the UVLO threshold.

Once the UVLO threshold has been exceeded, the charger will switch to the high current limit, the LDOs will start up, and the baseband processor will start to run. The processor must then poll the battery to determine which chemistry is present and set the charger to the proper mode.

Lithium Ion Charging

For lithium ion charging, the CHGEN input must be low. This allows the ADP3510 to continue charging the battery at the full current. The full charge current can be calculated by using:

$$I_{CHR(FULL)} = \frac{172\ mV}{R_{SENSE}} \quad (4)$$

If the voltage at BATSNS is below the charger's output voltage of 4.2 V, the battery will continue to charge in the constant current mode. If the battery has reached the final charge voltage, a constant voltage is applied to the battery until the charge current has reduced to the charge termination threshold. The charge termination threshold is determined by the voltage across the sense resistor. If the battery voltage is above 4.0 V and the voltage across the sense resistor has dropped to 12 mV, then an end of charge signal is generated and the EOC output goes high (see Figure 7).

The baseband processor can either let the charger continue to charge the battery for an additional amount of time or terminate the charging. To terminate the charging, the processor must pull the GATEIN and CHGEN pins high.

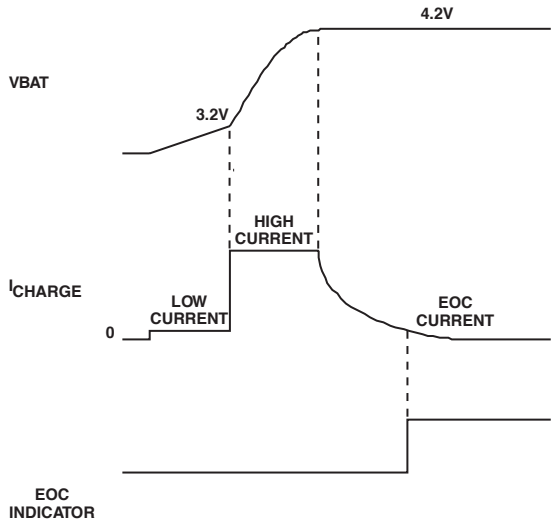


Figure 7. Lithium Ion Charging Diagram

NiMH Charging

For NiMH charging, the processor must pull the CHGEN pin high. This disables the internal Li+ mode control of the gate drive pin. The gate drive must now be controlled by the baseband processor. By pulling GATEIN high, the GATEDR pin is driven high, turning the PMOS off. By pulling the GATEIN pin low, the GATEDR pin is driven low, and the PMOS is turned on. So, by pulsing the GATEIN input, the processor can charge a NiMH battery. Note that when charging NiMH cells, a current limited adapter is required.

During the PMOS off periods, the battery voltage needs to be monitored through the MVBAT pin. The battery voltage is continually polled until the final battery voltage is reached. Then the charge can either be terminated or the frequency of the pulsing reduced. An alternative method of determining the end of charge is to monitor the temperature of the cells and terminate the charging when a rapid rise in temperature is detected.

Battery Voltage Monitoring
The battery voltage can be monitored at MVBAT during charging and discharging to determine the condition of the battery. An internal resistor divider is connected to BATSNS when both the baseband processor and the crystal oscillator are powered up. To enable MVBAT, both PWRONIN and TCXOEN must be high.

The ratio BATSNS/MVBAT of the voltage divider is set to 3.0. The divider will be disconnected from the battery when the baseband processor is powered down.

Charge Detection
The ADP3510 charger block has a detection circuit that determines if an adapter has been applied to the CHRIN pin. If the adapter voltage exceeds the battery voltage by 260 mV, the CHRDET output will go high. If the adapter is then removed or the voltage at the CHRIN pin drops to around 190 mV above the BATSNS pin, then CHRDET goes low.

APPLICATION INFORMATION

Input Capacitor Selection
For the input (VBAT and VBAT2) of the ADP3510, a local bypass capacitor is recommended. Use a 10 µF, low ESR capacitor. Multilayer ceramic chip (MLCC) capacitors provide the best combination of low ESR and small size but may not be cost effective. A lower cost alternative may be to use a 10 µF tantalum capacitor with a small (1 µF to 2 µF) ceramic in parallel.

A separate input for the IO LDO is supplied for additional bypassing or filtering. The IO LDO has VBAT2 as its input.

LDO Capacitor Selection
The performance of any LDO is a function of the output capacitor. The core, memory, IO, and analog LDOs require a 2.2 µF capacitor, and the TCXO LDO requires a 0.22 µF capacitor. Larger values may be used, but the overshoot at startup will increase slightly. If a larger output capacitor is desired, be sure to check that the overshoot and settling time are acceptable for the application.

All the LDOs are stable with a wide range of capacitor types and ESR (any CAP technology). The ADP3510 is stable with extremely low ESR capacitors (ESR ~ 0), such as multilayer ceramic capacitors, but care should be taken in their selection. Note that the capacitance of some capacitor types show wide variations over temperature or with dc voltage. A good quality dielectric capacitor, X7R or better, is recommended.

The RTC LDO can have a rechargeable coin cell or an electric double-layer capacitor as a load, but an additional 0.1 µF ceramic capacitor is recommended for stability and best performance.

RESET Capacitor Selection
RESET is held low at power-up. An internal power-good signal starts the reset delay when the IO LDO is up. The delay is set by an external capacitor on RESCAP:

$$t_{RESET} = 1.5\ ms/nF \times C_{RESCAP} \quad (5)$$

A 100 nF capacitor will produce a 150 ms reset delay. The current capability of RESET is minimal (a few hundred nA) when VIO is off to minimize power consumption. When VIO is on, RESET is capable of driving 500 µA.

Power-On Delay Capacitor Selection
The PDCAP sets the interval that the VAN and VIO LDOs are discharged. To ensure that the baseband processor is properly reset, the VIO and VAN LDOs should be fully discharged before power is reapplied. The discharge time can be estimated using:

$$t_{PD} = 900 \times C_{OUT\,SEC} \quad (6)$$

where t_{PD} is the discharge time, and COUT is the VIO or VAN LDO output capacitor value.

The power-on delay is set by an external capacitor on PDCAP. For worst-case delay:

$$t_{PD} = 0.3\frac{ms}{nF} \times C_{PDCAP} \text{ or}$$

$$C_{PDCAP} = t_{PD} \times 3.33\frac{nF}{ms} \quad (7)$$

So, for a 2.2 µF output capacitor, the required delay is about 2 ms. This results in a 6.8 nF PDCAP value.

Setting the Charge Current
The ADP3510 is capable of charging both lithium ion and NiMH batteries. For NiMH batteries, the charge current is limited by the adapter. For lithium ion batteries, the charge current is programmed by selecting the sense resistor, R1.

The lithium ion charge current is calculated using:

$$I_{CHR} = \frac{V_{SENSE}}{R1} = \frac{172\ mV}{R1} \quad (8)$$

Where V_{SENSE} is the high current limit threshold voltage. Or, if the charge current is known, R1 can be found:

$$R1 = \frac{V_{SENSE}}{I_{CHR}} = \frac{172\ mV}{I_{CHR}} \quad (9)$$

Similarly the trickle charge current and the end of charge current can be calculated:

$$I_{TRICKLE} = \frac{V_{SENSE}}{R1} = \frac{15\,mV}{R1}$$

$$I_{EOC} = \frac{V_{SENSE}}{R1} = \frac{12\ mV}{R1} \quad (10)$$

Example: Assume a 850 mA-H capacity lithium ion battery and a 1 C charge rate. R1 = 200 mΩ. Then $I_{TRICKLE}$ = 75 mA and I_{EOC} = 60 mA.

Appropriate sense resistors are available from the following vendors:

Vishay Dale
IRC
Panasonic

Charger FET Selection
The type and size of the pass transistor is determined by the threshold voltage, input-output voltage differential, and the charge current. The selected PMOS must satisfy the physical, electrical, and thermal design requirements.

To ensure proper operation, the minimum VGS the ADP3510 can provide must be enough to turn on the FET. The available gate drive voltage can be estimated using the following:

$$V_{GS} = V_{ADAPTER(MIN)} - V_{SENSE} - V_{GATEDR} \quad (11)$$

where:

$V_{ADAPTER(MIN)}$ is the minimum adapter voltage.

V_{DIODE} is the maximum forward drop of the charger diode, D1.

V_{GATEDR} is the gate drive "low" voltage, 0.5 V.

V_{SENSE} is the maximum high current limit threshold voltage.

The difference between the adapter voltage ($V_{ADAPTER}$) and the final battery voltage (VBAT) must exceed the voltage drop due to the blocking diode, the sense resistor, and the ON resistance of the FET at maximum charge current.

$$V_{DS} = V_{ADAPTER(MIN)} - V_{DIODE} - V_{SENSE} - V_{BAT} \quad (12)$$

Then the RDS(ON) of the FET can be calculated.

$$R_{DS(ON)} = \frac{V_{DS}}{I_{CHR(MAX)}} \quad (13)$$

The thermal characteristics of the FET must be considered next. The worst-case dissipation can be determined using:

$$P_{DISS} = \left(V_{ADAPTER(MAX)} - V_{DIODE} - V_{SENSE} - UVLO\right) \times I_{CHR}$$

It should be noted that the adapter voltage can be either preregulated or nonregulated. In the preregulated case, the difference between the maximum and minimum adapter voltage is probably not significant. In the unregulated case, the adapter voltage can have a wide range specified. However, the maximum voltage specified is usually with no load applied. So, the worst-case power dissipation calculation will often lead to an over-specified pass device. In either case, it is best to determine the load characteristics of the adapter to optimize the charger design.

For example:

$V_{ADAPTER(MIN)}$ = 5.0 V

$V_{ADAPTER(MAX)}$ = 6.5 V

V_{DIODE} = 0.5 V at 850 mA (14)

V_{GATEDR} = 0.5 V

V_{SENSE} = 170 mV

V_{GS} = 5 V – 0.5 V – 0.170 V = 4.3 V.
So choose a low-threshold voltage FET.

$$V_{DS} = V_{ADAPTER(MIN)} - V_{DIODE} - V_{SENSE} - V_{BAT} \quad (15)$$

= 5 V – 0.5 V – 0.170 V – 4.2 V

= 130 mV

$$R_{DS(ON)} = \frac{V_{DS}}{I_{CHR(MAX)}} = \frac{130\,mV}{850\,mV} \quad (16)$$

= 153 mΩ

$$P_{DISS} = \left(V_{ADAPTER(MAX)} - V_{DIODE} - V_{SENSE} - UVLO\right) \times I_{CHR}$$

$$P_{DISS} = \left(6.5\,V - 0.5\,V - 0.170\,V - 3.2\right) \times 0/85A = 2.24\,W$$

Appropriate PMOS FETs are available from the following vendors:

Siliconix
IR
Fairchild

Charger Diode Selection

The diode, D1, shown in Figure 3, is used to prevent the battery from discharging through the PMOS' body diode into the charger's internal bias circuits. A Schottky diode is recommended to minimize the voltage difference from the charger to the battery and the power dissipation. Choose a diode with a current rating high enough to handle the battery charging current, a voltage rating greater than VBAT, and a low leakage current. The blocking diode is required for both lithium and nickel battery types.

Printed Circuit Board Layout Considerations

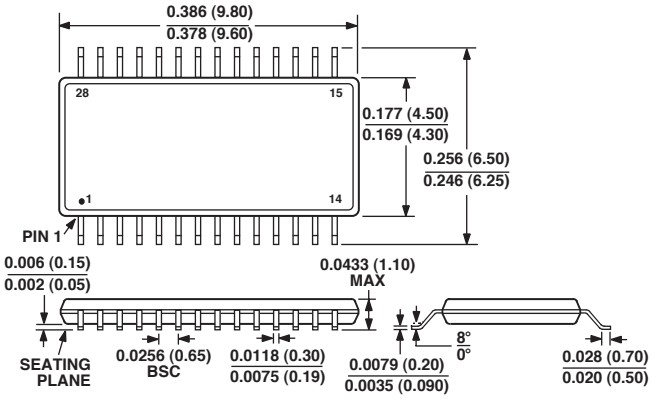
Use the following general guidelines when designing printed circuit boards:

1. Connect the battery to the VBAT and VBAT2 pins of the ADP3510. Locate the input capacitor as close to the pins as possible.
2. VAN and VTCXO capacitors should be returned to AGND.
3. VCORE, VMEM, and VIO capacitors should be returned to DGND.
4. Split the ground connections. Use separate traces or planes for the analog, digital, and power grounds and tie them together at a single point, preferably close to the battery return.
5. Run a separate trace from the BATSNS pin to the battery to prevent voltage drop error in the MVBAT measurement.
6. Kelvin connect the charger's sense resistor by running separate traces to the CHRIN pin and ISENSE pin. Make sure that the traces are terminated as close to the resistor's body as possible.
7. Use the best industry practice for thermal considerations during the layout of the ADP3510 and charger components. Careful use of copper area, weight, and multilayer construction all contribute to improved thermal performance.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Thin Shrink Small Outline (TSSOP)
(RU-28)



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