

16-Bit Analog-to-Digital Converters for Temperature Sensors

 Check for Samples: [ADS1146](#), [ADS1147](#), [ADS1148](#)

FEATURES

- 16 Bits, No Missing Codes
- Data Output Rates Up to 2kSPS
- Single-Cycle Settling for All Data Rates
- Simultaneous 50/60Hz Rejection at 20SPS
- 4 Differential/7 Single-Ended Inputs (ADS1148)
- 2 Differential/3 Single-Ended Inputs (ADS1147)
- Matched Current Source DACs
- Internal Voltage Reference
- Sensor Burnout Detection
- 4/8 General-Purpose I/Os (ADS1147/8)
- Internal Temperature Sensor
- Power Supply and V_{REF} Monitoring (ADS1147/8)
- Self and System Calibration
- SPI™-Compatible Serial Interface
- Analog Supply Operation:
+2.7V to +5.25V Unipolar, $\pm 2.5V$ Bipolar
- Digital Supply: +2.7V to +5.25V
- Operating Temperature $-40^{\circ}C$ to $+125^{\circ}C$

APPLICATIONS

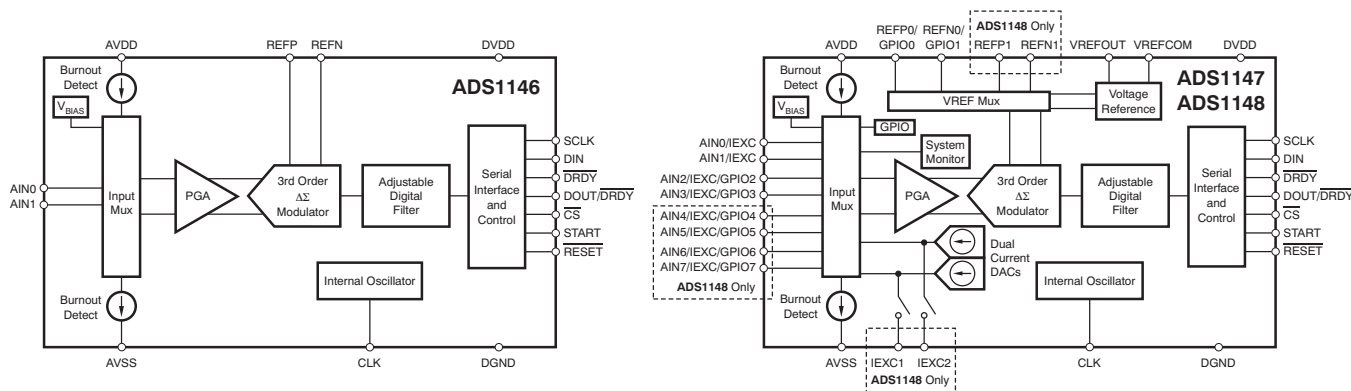
- Temperature Measurement
 - RTDs, Thermocouples, and Thermistors
- Pressure Measurement
- Industrial Process Control

DESCRIPTION

The ADS1146, ADS1147, and ADS1148 are highly-integrated, precision, 16-bit analog-to-digital converters (ADCs). The ADS1146/7/8 feature an onboard, low-noise, programmable gain amplifier (PGA), a precision delta-sigma ADC with a single-cycle settling digital filter, and an internal oscillator. The ADS1147 and ADS1148 also provide a built-in voltage reference with 10mA output capacity, and two matched programmable current digital-to-analog converters (DACs). The ADS1146/7/8 provide a complete front-end solution for temperature sensor applications including thermal couples, thermistors, and resistance temperature detectors (RTDs).

An input multiplexer supports four differential inputs for the ADS1148, two for the ADS1147, and one for the ADS1146. In addition, the multiplexer has a sensor burnout detect, voltage bias for thermocouples, system monitoring, and general-purpose digital I/Os (ADS1147 and ADS1148). The onboard, low-noise PGA provides selectable gains of 1 to 128. The delta-sigma modulator and adjustable digital filter settle in only one cycle, for fast channel cycling when using the input multiplexer, and support data rates up to 2kSPS. For data rates of 20SPS or less, both 50Hz and 60Hz interference are rejected by the filter.

The ADS1146 is offered in a small TSSOP-16 package, the ADS1147 is available in a TSSOP-20 package, and the ADS1148 is available in TSSOP-28 and QFN-32 packages. All three devices operate over the extended specified temperature range of $-40^{\circ}C$ to $+105^{\circ}C$.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

| PRODUCT | RESOLUTION | NUMBER OF INPUTS | VOLTAGE REFERENCE | DUAL SENSOR EXCITATION CURRENT SOURCES | PACKAGE-LEAD |
|---------|------------|--|----------------------|--|--------------|
| ADS1246 | 24 bits | 1 Differential or 1 Single-Ended | External | NO | TSSOP-16 |
| ADS1247 | 24 bits | 2 Differential or 3 Single-Ended | Internal or External | YES | TSSOP-20 |
| ADS1248 | 24 bits | 4 Differential or 7 Single-Ended | Internal or External | YES | TSSOP-28 |
| ADS1146 | 16 bits | 1 Differential or 1 Single-Ended | External | NO | TSSOP-16 |
| ADS1147 | 16 bits | 2 Differential or 3 Single-Ended | Internal or External | YES | TSSOP-20 |
| ADS1148 | 16 bits | 4 Differential or 7 Single-Ended | Internal or External | YES | TSSOP-28 |
| | 16 bits | 4 Differential or 7 Single-Ended | Internal or External | YES | QFN-32 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

| | ADS1146, ADS1147, ADS1148 | UNIT |
|-------------------------------|---------------------------|------|
| AVDD to AVSS | -0.3 to +5.5 | V |
| AVSS to DGND | -2.8 to +0.3 | V |
| DVDD to DGND | -0.3 to +5.5 | V |
| Input current | 100, momentary | mA |
| | 10, continuous | mA |
| Analog input voltage to AVSS | AVSS - 0.3 to AVDD + 0.3 | V |
| Digital input voltage to DGND | -0.3 to DVDD + 0.3 | V |
| Maximum junction temperature | +150 | °C |
| Operating temperature range | -40 to +125 | °C |
| Storage temperature range | -60 to +150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Minimum/maximum specifications apply from -40°C to $+105^{\circ}\text{C}$. Typical specifications are at $+25^{\circ}\text{C}$. All specifications at $\text{AVDD} = +5\text{V}$, $\text{DVDD} = +3.3\text{V}$, $\text{AVSS} = \text{DGND} = 0\text{V}$, $V_{\text{REF}} = +2.048\text{V}$, and oscillator frequency = 4.096MHz, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS1146, ADS1147, ADS1148 | | | UNIT |
|---|--|--|--|-----------------------------------|-------------------------|
| | | MIN | TYP | MAX | |
| ANALOG INPUTS | | | | | |
| Full-scale input voltage ($V_{\text{IN}} = \text{ADCINP} - \text{ADCINN}$) | | | $\pm V_{\text{REF}}/\text{PGA}^{(1)}$ | | V |
| Common-mode input range | | $\text{AVSS} + 0.1\text{V} + \frac{(V_{\text{IN}})(\text{Gain})}{2}$ | $\text{AVDD} - 0.1\text{V} - \frac{(V_{\text{IN}})(\text{Gain})}{2}$ | | V |
| Differential input current | | | 100 | | pA |
| PGA gain settings | | | 1, 2, 4, 8, 16, 32, 64, 128 | | |
| Burnout current source | | | 0.5, 2, or 10 | | μA |
| Bias voltage | | | $(\text{AVDD} + \text{AVSS})/2$ | | V |
| Bias voltage output impedance | | | 400 | | Ω |
| SYSTEM PERFORMANCE | | | | | |
| Resolution | No missing codes | 16 | | | Bits |
| Data rate | | | 5, 10, 20, 40, 80, 160, 320, 640, 1000, 2000 | | SPS |
| Integral nonlinearity (INL) | Differential input, end point fit, PGA = 1 | | ± 0.5 | ± 1 | LSB |
| Offset error | After calibration | | | 1 | LSB |
| Offset drift | PGA = 1 | | 100 | | nV/ $^{\circ}\text{C}$ |
| | PGA = 128 | | 15 | | nV/ $^{\circ}\text{C}$ |
| Gain error | Excluding V_{REF} errors | | | ± 0.5 | % |
| Gain drift | PGA = 1, excludes V_{REF} drift | | 1 | | ppm/ $^{\circ}\text{C}$ |
| | PGA = 128, excludes V_{REF} drift | | -3.5 | | ppm/ $^{\circ}\text{C}$ |
| ADC conversion time | Single-cycle settling | | See Table 12 | | |
| Noise | | | See Table 1 and Table 2 | | |
| Normal-mode rejection | | | See Table 5 | | |
| Common-mode rejection | At dc, PGA = 1 | | 90 | | dB |
| | At dc, PGA = 32 | | 100 | | dB |
| Power-supply rejection | AVDD, DVDD at dc | | 100 | | dB |
| VOLTAGE REFERENCE INPUT | | | | | |
| Voltage reference input ($V_{\text{REF}} = V_{\text{REFP}} - V_{\text{REFN}}$) | | 0.5 | | $(\text{AVDD} - \text{AVSS}) - 1$ | V |
| Negative reference input (REFN) | | $\text{AVSS} - 0.1$ | | $\text{REFP} - 0.5$ | V |
| Positive reference input (REFP) | | $\text{REFN} + 0.5$ | | $\text{AVDD} + 0.1$ | V |
| Reference input current | | | 30 | | nA |
| ON-CHIP VOLTAGE REFERENCE | | | | | |
| Output voltage | | 2.038 | 2.048 | 2.058 | V |
| Output current ⁽²⁾ | | | | ± 10 | mA |
| Load regulation | | | 50 | | $\mu\text{V}/\text{mA}$ |
| Drift ⁽³⁾ | $T_{\text{A}} = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ | | 20 | 50 | ppm/ $^{\circ}\text{C}$ |
| Startup time | | | See Table 6 | | μs |

(1) For $V_{\text{REF}} > 2.7\text{V}$, the analog input differential voltage should not exceed $2.7\text{V}/\text{PGA}$

(2) Do not exceed this loading on the internal voltage reference.

(3) Specified by the combination of design and final production test.

ELECTRICAL CHARACTERISTICS (continued)

Minimum/maximum specifications apply from -40°C to $+105^{\circ}\text{C}$. Typical specifications are at $+25^{\circ}\text{C}$. All specifications at $\text{AVDD} = +5\text{V}$, $\text{DVDD} = +3.3\text{V}$, $\text{AVSS} = \text{DGND} = 0\text{V}$, $V_{\text{REF}} = +2.048\text{V}$, and oscillator frequency = 4.096MHz, unless otherwise noted.

| PARAMETER | CONDITIONS | ADS1146, ADS1147, ADS1148 | | | UNIT | |
|---|---|------------------------------|--|----------------------|--------------------------------|-----|
| | | MIN | TYP | MAX | | |
| CURRENT SOURCES (IDACS) | | | | | | |
| Output current | | | 50, 100, 250, 500, 750, 1000, 1500 | | μA | |
| Voltage compliance | All currents | | $\text{AVDD} - 0.7$ | | V | |
| Initial error | All currents, each IDAC | -6 | ± 1.0 | 6 | % of FS | |
| Initial mismatch | All currents, between IDACs | | ± 0.03 | | % of FS | |
| Temperature drift | Each IDAC | | 200 | | ppm/ $^{\circ}\text{C}$ | |
| Temperature drift matching | Between IDACs | | 10 | | ppm/ $^{\circ}\text{C}$ | |
| SYSTEM MONITORS | | | | | | |
| Temperature sensor reading | Voltage | $T_A = +25^{\circ}\text{C}$ | | 118 | mV | |
| | Drift | | | 405 | $\mu\text{V}/^{\circ}\text{C}$ | |
| GENERAL-PURPOSE INPUT/OUTPUT (GPIO) | | | | | | |
| Logic levels | V_{IH} | | 0.7AVDD | | AVDD | V |
| | V_{IL} | | AVSS | | 0.3AVDD | V |
| | V_{OH} | $I_{\text{OH}} = 1\text{mA}$ | 0.8AVDD | | | V |
| | V_{OL} | $I_{\text{OL}} = 1\text{mA}$ | AVSS | | 0.2AVDD | V |
| DIGITAL INPUT/OUTPUT (other than GPIO) | | | | | | |
| Logic levels | V_{IH} | | 0.7DVDD | | DVDD | V |
| | V_{IL} | | DGND | | 0.3DVDD | V |
| | V_{OH} | $I_{\text{OH}} = 1\text{mA}$ | 0.8DVDD | | | V |
| | V_{OL} | $I_{\text{OL}} = 1\text{mA}$ | DGND | | 0.2DVDD | V |
| Input leakage | $\text{DGND} < V_{\text{DIGITAL IN}} < \text{DVDD}$ | | | ± 10 | μA | |
| Clock input (CLK) | Frequency | | 1 | | 4.5 | MHz |
| | Duty cycle | | 25 | | 75 | % |
| Internal oscillator frequency | | 3.89 | 4.096 | 4.3 | MHz | |
| POWER SUPPLY | | | | | | |
| DVDD | | 2.7 | | 5.25 | V | |
| AVSS | | -2.5 | | 0 | V | |
| AVDD | | $\text{AVSS} + 2.7$ | | $\text{AVSS} + 5.25$ | V | |
| DVDD current | Normal mode, DVDD = 5V, data rate = 20SPS, internal oscillator | | 230 | | μA | |
| | Normal mode, DVDD = 3.3V, data rate = 20SPS, internal oscillator | | 210 | | μA | |
| | Sleep mode | | 0.2 | | μA | |
| AVDD current | Converting, AVDD = 5V, data rate = 20SPS, external reference | | 225 | | μA | |
| | Converting, AVDD = 3.3V, data rate = 20SPS, external reference | | 212 | | μA | |
| | Sleep mode | | 0.1 | | μA | |
| | Additional current with internal reference enabled | | 180 | | μA | |
| Power dissipation | AVDD = DVDD = 5V, data rate = 20SPS, external reference, internal oscillator | | 2.3 | | mW | |
| | AVDD = DVDD = 3.3V, data rate = 20SPS, external reference, internal oscillator | | 1.4 | | mW | |
| TEMPERATURE RANGE | | | | | | |
| Specified | | -40 | | +105 | $^{\circ}\text{C}$ | |
| Operating | | -40 | | +125 | $^{\circ}\text{C}$ | |
| Storage | | -60 | | +150 | $^{\circ}\text{C}$ | |

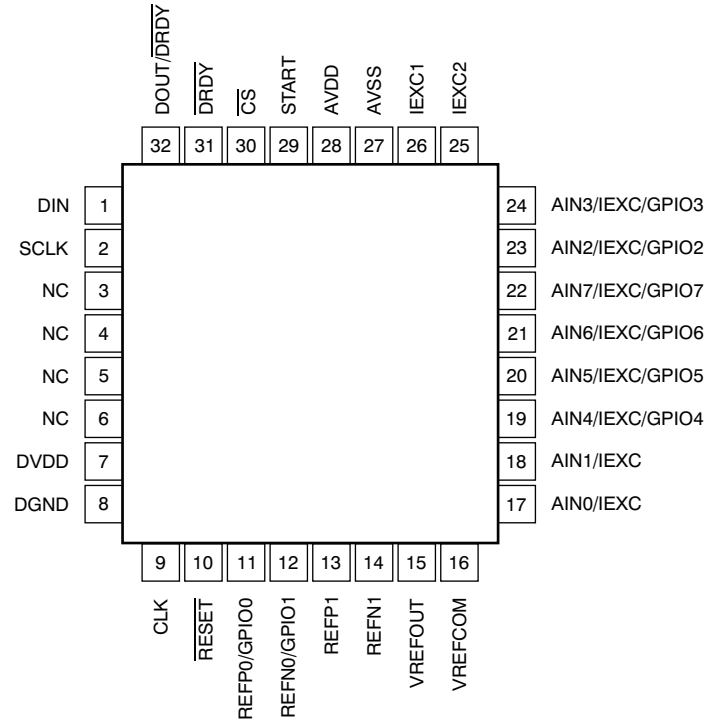
THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | ADS1146, ADS1147, ADS1148 | UNITS |
|-------------------------------|---|---------------------------------|-------|
| | | PW | |
| | | 28 | |
| θ_{JA} | Junction-to-ambient thermal resistance ⁽²⁾ | 79.5 | °C/W |
| $\theta_{JC(top)}$ | Junction-to-case(top) thermal resistance ⁽³⁾ | 31.8 | |
| θ_{JB} | Junction-to-board thermal resistance ⁽⁴⁾ | 40.9 | |
| ψ_{JT} | Junction-to-top characterization parameter ⁽⁵⁾ | 3.0 | |
| ψ_{JB} | Junction-to-board characterization parameter ⁽⁶⁾ | 41.1 | |
| $\theta_{JC(bottom)}$ | Junction-to-case(bottom) thermal resistance ⁽⁷⁾ | n/a | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

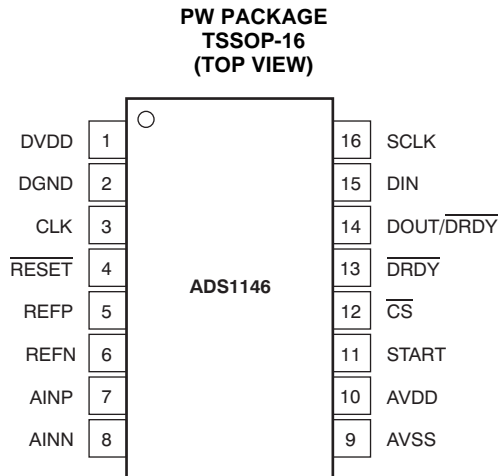
PIN CONFIGURATIONS

RHB PACKAGE QFN-32 (TOP VIEW)



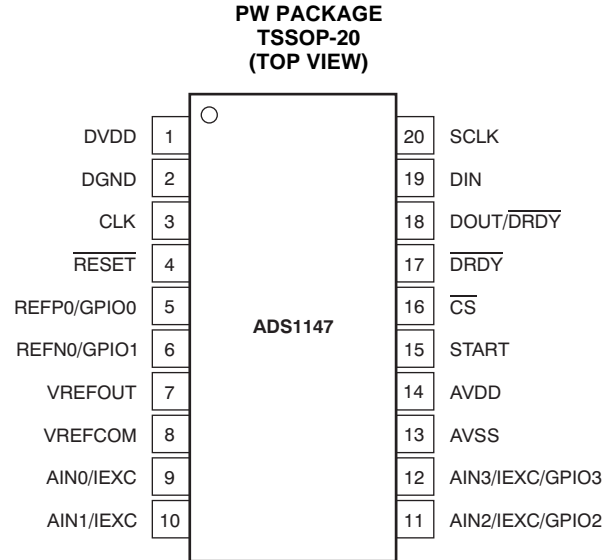
ADS1148 (QFN-32) PIN DESCRIPTIONS

| NAME | PIN NO. | FUNCTION | DESCRIPTION |
|--------------------------------|---------|---|--|
| DIN | 1 | Digital input | Serial data input |
| SCLK | 2 | Digital input | Serial clock input |
| NC | 3 | Not connected | Pin can be grounded or left disconnected |
| NC | 4 | Not connected | Pin can be grounded or left disconnected |
| NC | 5 | Not connected | Pin can be grounded or left disconnected |
| NC | 6 | Not connected | Pin can be grounded or left disconnected |
| DVDD | 7 | Digital | Digital power supply |
| DGND | 8 | Digital | Digital ground |
| CLK | 9 | Digital input | External clock input. Tie this pin to DGND to activate the internal oscillator. |
| $\overline{\text{RESET}}$ | 10 | Digital input | Chip reset (active low). Returns all register values to reset values. |
| REFP0/GPIO0 | 11 | Analog input; Digital in/out | Positive external reference input 0, or general-purpose digital input/output pin 1 |
| REFN0/GPIO1 | 12 | Analog input; Digital in/out | Negative external reference input 0, or general-purpose digital input/output pin 1 |
| REFP1 | 13 | Analog input | Positive external reference 1 input |
| REFN1 | 14 | Analog input | Negative external reference 1 input |
| VREFOUT | 15 | Analog output | Positive internal reference voltage output |
| VREFCOM | 16 | Analog output | Negative internal reference voltage output. Connect this pin to AVSS when using a unipolar supply, or to the midvoltage of the power supply when using a bipolar supply. |
| AIN0/IEXC | 17 | Analog input | Analog input 0, optional excitation current output |
| AIN1/IEXC | 18 | Analog input | Analog input 1, optional excitation current output |
| AIN4/IEXC/GPIO4 | 19 | Analog input; Digital in/out | Analog input 4, optional excitation current output, or general-purpose digital input/output pin 4 |
| AIN5/IEXC/GPIO5 | 20 | Analog input; Digital in/out | Analog input 5, optional excitation current output, or general-purpose digital input/output pin 5 |
| AIN6/IEXC/GPIO6 | 21 | Analog input; Digital in/out | Analog input 6, optional excitation current output, or general-purpose digital input/output pin 6 |
| AIN7/IEXC/GPIO7 | 22 | Analog input; Digital in/out | Analog input 7, optional excitation current output, or general-purpose digital input/output pin 7 |
| AIN2/IEXC/GPIO2 | 23 | Analog input; Digital in/out | Analog input 2, optional excitation current output, or general-purpose digital input/output pin 2 |
| AIN3/IEXC/GPIO3 | 24 | Analog input; Digital in/out | Analog input 3, optional excitation current output, or general-purpose digital input/output pin 3 |
| IEXC2 | 25 | Analog output | Excitation current output 2 |
| IEXC1 | 26 | Analog output | Excitation current output 1 |
| AVSS | 27 | Analog | Negative analog power supply |
| AVDD | 28 | Analog | Positive analog power supply |
| START | 29 | Digital input | Conversion start. See text for complete description. |
| $\overline{\text{CS}}$ | 30 | Digital input Chip select (active low) | Chip select (active low) |
| $\overline{\text{DRDY}}$ | 31 | Digital output | Data ready (active low) |
| DOUT/ $\overline{\text{DRDY}}$ | 32 | Digital output | Serial data output, or data out combined with data ready (active low when $\overline{\text{DRDY}}$ function enabled) |



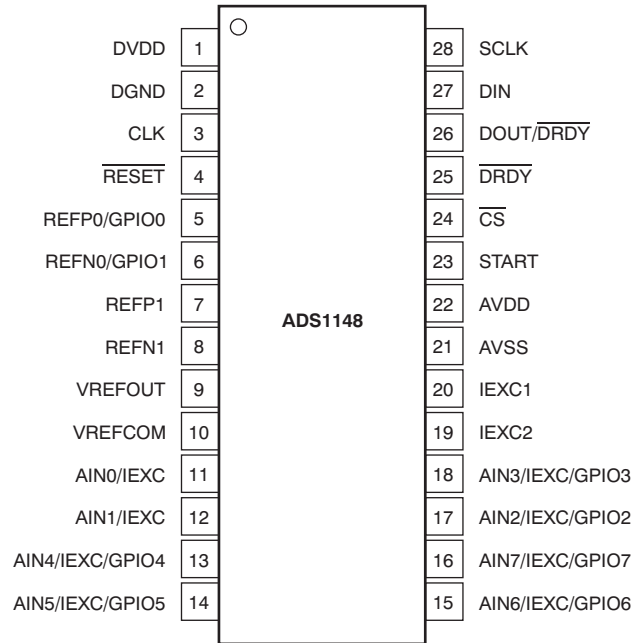
ADS1146 (TSSOP-16) PIN DESCRIPTIONS

| NAME | PIN NO. | FUNCTION | DESCRIPTION |
|--------------------------------|---------|----------------|--|
| DVDD | 1 | Digital | Digital power supply |
| DGND | 2 | Digital | Digital ground |
| CLK | 3 | Digital input | External clock input. Tie this pin to DGND to activate the internal oscillator. |
| $\overline{\text{RESET}}$ | 4 | Digital input | Chip reset (active low). Returns all register values to reset values. |
| REFP | 5 | Analog input | Positive external reference input |
| REFN | 6 | Analog input | Negative external reference input |
| AINP | 7 | Analog input | Positive analog input |
| AINN | 8 | Analog input | Negative analog input |
| AVSS | 9 | Analog | Negative analog power supply |
| AVDD | 10 | Analog | Positive analog power supply |
| START | 11 | Digital input | Conversion start. See text for description of use. |
| $\overline{\text{CS}}$ | 12 | Digital input | Chip select (active low) |
| $\overline{\text{DRDY}}$ | 13 | Digital output | Data ready (active low) |
| DOUT/ $\overline{\text{DRDY}}$ | 14 | Digital output | Serial data out output, or data out combined with data ready (active low when $\overline{\text{DRDY}}$ function enabled) |
| DIN | 15 | Digital input | Serial data input |
| SCLK | 16 | Digital input | Serial clock input |


ADS1147 (TSSOP-20) PIN DESCRIPTIONS

| NAME | PIN NO. | FUNCTION | DESCRIPTION |
|--------------------------------|---------|--------------------------------|--|
| DVDD | 1 | Digital | Digital power supply |
| DGND | 2 | Digital | Digital ground |
| CLK | 3 | Digital input | External clock input. Tie this pin to DGND to activate the internal oscillator. |
| $\overline{\text{RESET}}$ | 4 | Digital input | Chip reset (active low). Returns all register values to reset values. |
| REFP0/GPIO0 | 5 | Analog input Digital in/out | Positive external reference input, or general-purpose digital input/output pin 0 |
| REFN0/GPIO1 | 6 | Analog input Digital in/out | Negative external reference input, or general-purpose digital input/output pin 1 |
| VREFOUT | 7 | Analog output | Positive internal reference voltage output |
| VREFCOM | 8 | Analog output | Negative internal reference voltage output. Connect this pin to AVSS when using a unipolar supply, or to the midvoltage of the power supply when using a bipolar supply. |
| AIN0/IEXC | 9 | Analog input | Analog input 0, optional excitation current output |
| AIN1/IEXC | 10 | Analog input | Analog input 1, optional excitation current output |
| AIN2/IEXC/GPIO2 | 11 | Analog input Digital in/out | Analog input 2, optional excitation current output, or general-purpose digital input/output pin 2 |
| AIN3/IEXC/GPIO3 | 12 | Analog input Digital in/out | Analog input 3, with or without excitation current output, or general-purpose digital input/output pin 3 |
| AVSS | 13 | Analog | Negative analog power supply |
| AVDD | 14 | Analog | Positive analog power supply |
| START | 15 | Digital input | Conversion start. See text for description of use. |
| $\overline{\text{CS}}$ | 16 | Digital input | Chip select (active low) |
| $\overline{\text{DRDY}}$ | 17 | Digital output | Data ready (active low) |
| DOUT/ $\overline{\text{DRDY}}$ | 18 | Digital output | Serial data out output, or data out combined with data ready (active low when $\overline{\text{DRDY}}$ function enabled) |
| DIN | 19 | Digital input | Serial data input |
| SCLK | 20 | Digital input | Serial clock input |

PW PACKAGE
 TSSOP-28
 (TOP VIEW)



ADS1148 (TSSOP-28) PIN DESCRIPTIONS

| NAME | PIN NO. | FUNCTION | DESCRIPTION |
|--------------------------------|---------|--------------------------------|--|
| DVDD | 1 | Digital | Digital power supply |
| DGND | 2 | Digital | Digital ground |
| CLK | 3 | Digital input | External clock input. Tie this pin to DGND to activate the internal oscillator. |
| $\overline{\text{RESET}}$ | 4 | Digital input | Chip reset (active low). Returns all register values to reset values. |
| REFP0/GPIO0 | 5 | Analog input | Positive external reference input 0, or general-purpose digital input/output pin 0 |
| REFN0/GPIO1 | 6 | Analog input | Negative external reference 0 input, or general-purpose digital input/output pin 1 |
| REFP1 | 7 | Analog input | Positive external reference 1 input |
| REFN1 | 8 | Analog input | Negative external reference 1 input |
| VREFOUT | 9 | Analog output | Positive internal reference voltage output |
| VREFCOM | 10 | Analog output | Negative internal reference voltage output. Connect this pin to AVSS when using a unipolar supply, or to the midvoltage of the power supply when using a bipolar supply. |
| AIN0/IEXC | 11 | Analog input | Analog input 0, optional excitation current output |
| AIN1/IEXC | 12 | Analog input | Analog input 1, optional excitation current output |
| AIN4/IEXC/GPIO4 | 13 | Analog input Digital in/out | Analog input 4, optional excitation current output, or general-purpose digital input/output pin 4 |
| AIN5/IEXC/GPIO5 | 14 | Analog input Digital in/out | Analog input 5, optional excitation current output, or general-purpose digital input/output pin 5 |
| AIN6/IEXC/GPIO6 | 15 | Analog input Digital in/out | Analog input 6, optional excitation current output, or general-purpose digital input/output pin 6 |
| AIN7/IEXC/GPIO7 | 16 | Analog input Digital in/out | Analog input 7, optional excitation current output, or general-purpose digital input/output pin 7 |
| AIN2/IEXC/GPIO2 | 17 | Analog input Digital in/out | Analog input 2, optional excitation current output, or general-purpose digital input/output pin 2 |
| AIN3/IEXC/GPIO3 | 18 | Analog input Digital in/out | Analog input 3, optional excitation current output, or general-purpose digital input/output pin 3 |
| IEXC2 | 19 | Analog output | Excitation current output 2 |
| IEXC1 | 20 | Analog output | Excitation current output 1 |
| AVSS | 21 | Analog | Negative analog power supply |
| AVDD | 22 | Analog | Positive analog power supply |
| START | 23 | Digital input | Conversion start. See text for complete description. |
| $\overline{\text{CS}}$ | 24 | Digital input | Chip select (active low) |
| $\overline{\text{DRDY}}$ | 25 | Digital output | Data ready (active low) |
| DOUT/ $\overline{\text{DRDY}}$ | 26 | Digital output | Serial data out output, or data out combined with data ready (active low when DRDY function enabled) |
| DIN | 27 | Digital input | Serial data input |
| SCLK | 28 | Digital input | Serial clock input |

TIMING DIAGRAMS

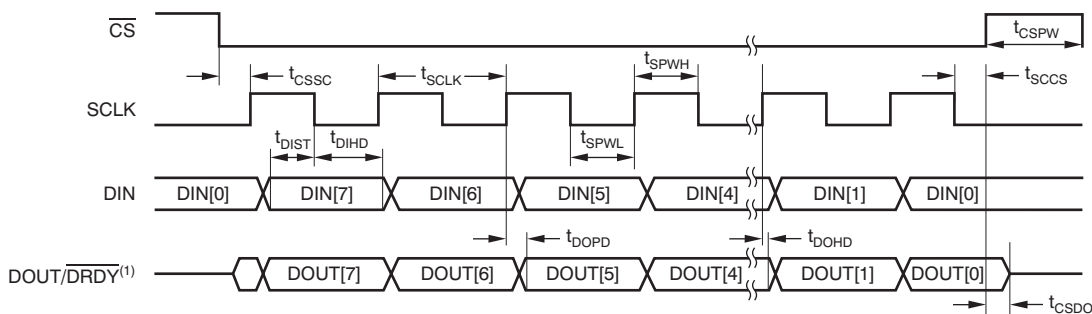


Figure 1. Serial Interface Timing

Timing Characteristics for Figure 1⁽¹⁾

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT |
|------------|--|------|-------------------|--------------------------|
| t_{CSSC} | \overline{CS} low to first SCLK high (set up time) | 10 | | ns |
| t_{SCCS} | SCLK low to \overline{CS} high (hold time) | 7 | | t_{osc} ⁽²⁾ |
| t_{DIST} | DIN set up time | 5 | | ns |
| t_{DIHD} | DIN hold time | 5 | | ns |
| t_{DOPD} | SCLK rising edge to new data valid | | 50 ⁽³⁾ | ns |
| t_{DOHD} | DOUT hold time | 0 | | ns |
| t_{SCLK} | SCLK period | 500 | | ns |
| | | | 64 | conversions |
| t_{SPWH} | SCLK pulse width high | 0.25 | 0.75 | t_{SCLK} |
| t_{SPWL} | SCLK pulse width low | 0.25 | 0.75 | t_{SCLK} |
| t_{CSDO} | \overline{CS} high to DOUT high impedance | | 10 | ns |
| t_{CSPW} | Chip Select high pulse width | 5 | | t_{osc} |

(1) DRDY MODE bit = 0.

(2) $t_{osc} = 1/f_{CLK}$. The default clock frequency $f_{CLK} = 4.096\text{MHz}$.

(3) For $DVDD > 3.6\text{V}$, $t_{DOPD} = 180\text{ns}$.

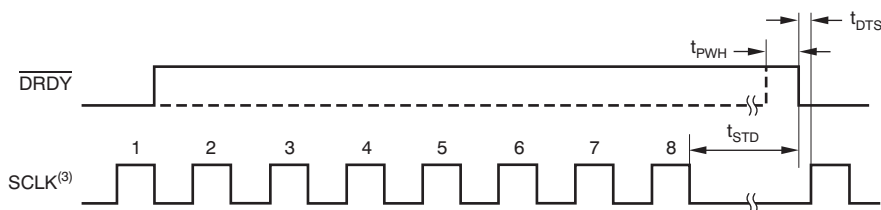


Figure 2. SPI Interface Timing to Allow Conversion Result Loading⁽⁴⁾⁽⁵⁾

Timing Characteristics for Figure 2

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT |
|-----------|--|-------------|-----|-----------|
| t_{PWH} | \overline{DRDY} pulse width high | 3 | | t_{osc} |
| t_{STD} | SCLK low prior to \overline{DRDY} low | 5 | | t_{osc} |
| t_{DTS} | \overline{DRDY} falling edge to SCLK rising edge | $1/f_{CLK}$ | | ns |

(4) This timing diagram is applicable only when the \overline{CS} pin is low. SCLK need not be low during t_{STD} when \overline{CS} is high.

(5) SCLK should only be sent in multiples of eight during partial retrieval of output data.

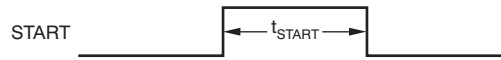


Figure 3. Minimum START Pulse Width

Timing Characteristics for Figure 3

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT |
|-------------|------------------------|-----|-----|-----------|
| t_{START} | START pulse width high | 3 | | t_{osc} |

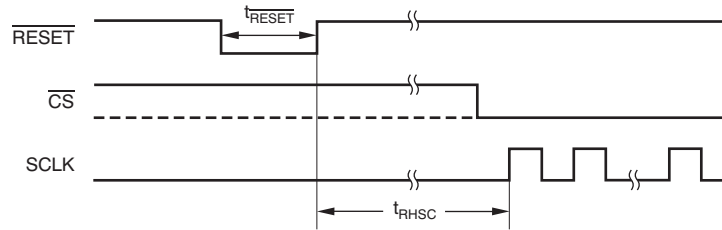


Figure 4. Reset Pulse Width and SPI Communication After Reset

Timing Characteristics for Figure 4

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT |
|-------------|---------------------------------------|--------------------|-----|-----------|
| t_{RESET} | RESET pulse width low | 4 | | t_{osc} |
| t_{RHSC} | RESET high to SPI communication start | 0.6 ⁽¹⁾ | | ms |

(1) For $f_{OSC} = 4.096\text{MHz}$, scales proportionately with f_{OSC} frequency.

NOISE PERFORMANCE

The ADS1146/7/8 noise performance can be optimized by adjusting the data rate and PGA setting. As the averaging is increased by reducing the data rate, the noise drops correspondingly. Increasing the PGA value reduces the input-referred noise, particularly useful when measuring low-level signals. Table 1 and Table 2 summarize noise performance of the ADS1146/7/8. The data are representative of typical noise performance at T = +25°C. The data shown are the result of averaging the readings from multiple devices and were measured with the inputs shorted together.

Table 1 lists the input-referred noise in units μV_{PP} . In many of the settings, especially at lower data rates, the inherent device noise is less than 1LSB. For these cases, the noise is rounded up to 1LSB. Table 2 lists the corresponding data in units of ENOB (effective number of bits) where:

$$\text{ENOB} = \ln(\text{Full-Scale Range}/\text{Noise})/\ln(2) \quad (1)$$

**Table 1. Noise in μV_{PP}
At $V_{\text{REF}} = 2.048\text{V}$, $\text{AVDD} = 5\text{V}$, and $\text{AVSS} = 0\text{V}$**

| DATA RATE (SPS) | PGA SETTING | | | | | | | |
|-----------------|----------------------|----------------------|----------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |
| 5 | 62.50 ⁽¹⁾ | 31.25 ⁽¹⁾ | 15.63 ⁽¹⁾ | 7.81 ⁽¹⁾ | 3.91 ⁽¹⁾ | 1.95 ⁽¹⁾ | 0.98 ⁽¹⁾ | 0.49 ⁽¹⁾ |
| 10 | 62.50 ⁽¹⁾ | 31.25 ⁽¹⁾ | 15.63 ⁽¹⁾ | 7.81 ⁽¹⁾ | 3.91 ⁽¹⁾ | 1.95 ⁽¹⁾ | 0.98 ⁽¹⁾ | 0.49 ⁽¹⁾ |
| 20 | 62.50 ⁽¹⁾ | 31.25 ⁽¹⁾ | 15.63 ⁽¹⁾ | 7.81 ⁽¹⁾ | 3.91 ⁽¹⁾ | 1.95 ⁽¹⁾ | 0.98 ⁽¹⁾ | 0.55 |
| 40 | 62.50 ⁽¹⁾ | 31.25 ⁽¹⁾ | 15.63 ⁽¹⁾ | 7.81 ⁽¹⁾ | 3.91 ⁽¹⁾ | 1.95 ⁽¹⁾ | 0.98 ⁽¹⁾ | 0.75 |
| 80 | 62.50 ⁽¹⁾ | 31.25 ⁽¹⁾ | 15.63 ⁽¹⁾ | 7.81 ⁽¹⁾ | 3.91 ⁽¹⁾ | 1.95 ⁽¹⁾ | 1.09 | 0.98 |
| 160 | 62.50 ⁽¹⁾ | 31.25 ⁽¹⁾ | 15.63 ⁽¹⁾ | 7.81 ⁽¹⁾ | 3.91 ⁽¹⁾ | 1.95 ⁽¹⁾ | 1.88 | 1.57 |
| 320 | 62.50 ⁽¹⁾ | 35.30 | 17.52 | 8.86 | 4.35 | 3.03 | 2.44 | 2.34 |
| 640 | 93.06 | 45.20 | 18.73 | 12.97 | 6.51 | 4.20 | 3.69 | 3.50 |
| 1000 | 284.59 | 129.77 | 61.30 | 33.04 | 16.82 | 9.08 | 5.42 | 4.65 |
| 2000 | 273.39 | 130.68 | 67.13 | 36.16 | 19.22 | 9.87 | 6.93 | 6.48 |

(1) Peak-to-peak noise rounded up to 1LSB.

**Table 2. Effective Number of Bits From Peak-to-Peak Noise
At $V_{\text{REF}} = 2.048\text{V}$, $\text{AVDD} = 5\text{V}$, and $\text{AVSS} = 0\text{V}$**

| DATA RATE (SPS) | PGA SETTING | | | | | | | |
|-----------------|-------------|------|------|------|------|------|------|------|
| | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 |
| 5 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| 10 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| 20 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 15.8 |
| 40 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 15.4 |
| 80 | 16 | 16 | 16 | 16 | 16 | 16 | 15.8 | 15.0 |
| 160 | 16 | 16 | 16 | 16 | 16 | 16 | 15.1 | 14.3 |
| 320 | 16 | 15.8 | 15.8 | 15.8 | 15.8 | 15.4 | 14.7 | 13.7 |
| 640 | 15.4 | 15.5 | 15.7 | 15.3 | 15.3 | 14.9 | 14.1 | 13.2 |
| 1000 | 13.8 | 13.9 | 14.0 | 13.9 | 13.9 | 13.8 | 13.5 | 12.7 |
| 2000 | 13.9 | 13.9 | 13.9 | 13.8 | 13.7 | 13.7 | 13.2 | 12.3 |

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $AVDD = 5\text{V}$, $V_{REF} = 2.5\text{V}$, and $AVSS = 0\text{V}$, unless otherwise noted.

ANALOG CURRENT vs TEMPERATURE

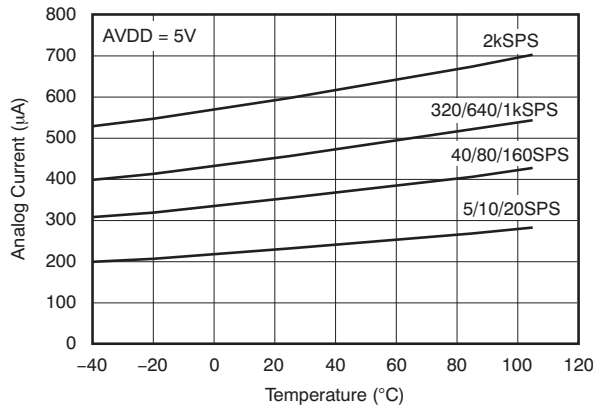


Figure 5.

DIGITAL CURRENT vs TEMPERATURE

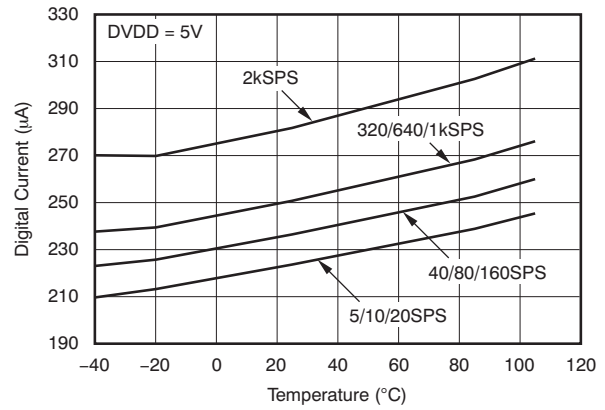


Figure 6.

ANALOG CURRENT vs TEMPERATURE

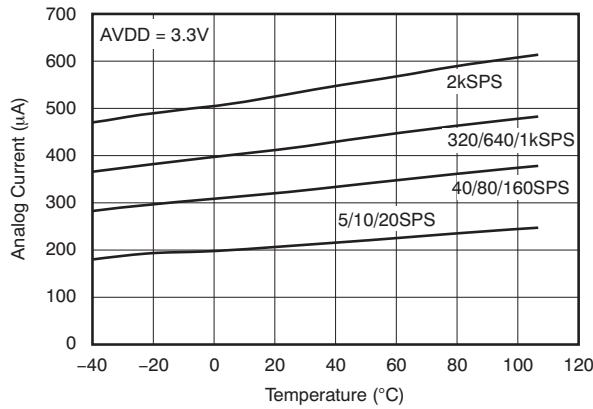


Figure 7.

DIGITAL CURRENT vs TEMPERATURE

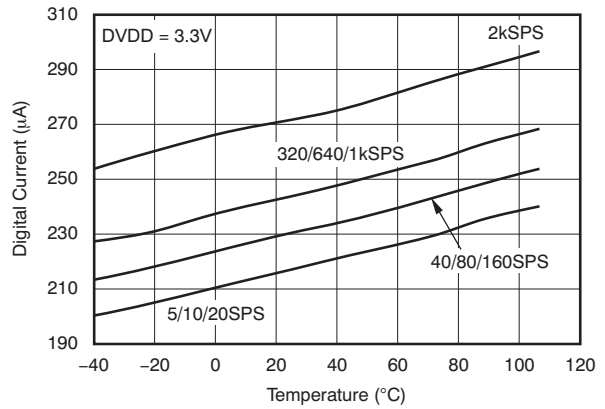


Figure 8.

ANALOG CURRENT vs DATA RATE

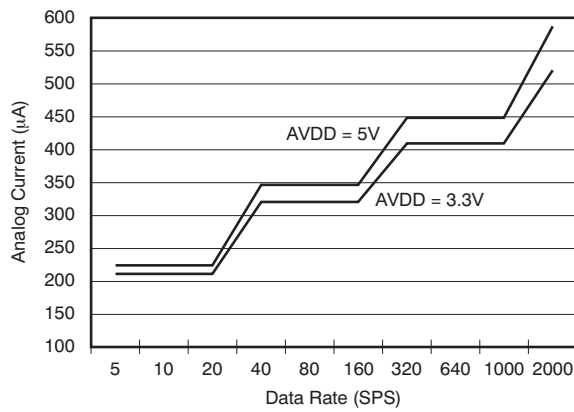


Figure 9.

DIGITAL CURRENT vs DATA RATE

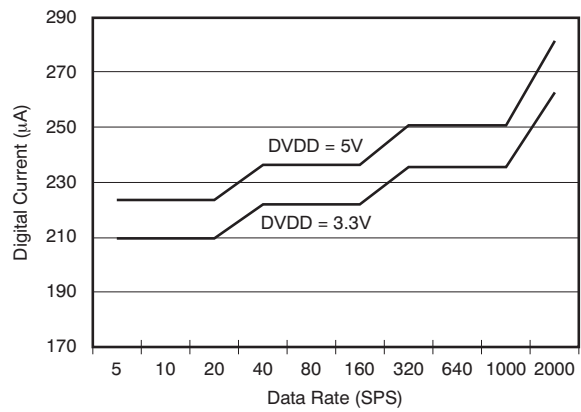


Figure 10.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AV_{DD} = 5\text{V}$, $V_{REF} = 2.5\text{V}$, and $AV_{SS} = 0\text{V}$, unless otherwise noted.

DATA RATE ERROR vs TEMPERATURE

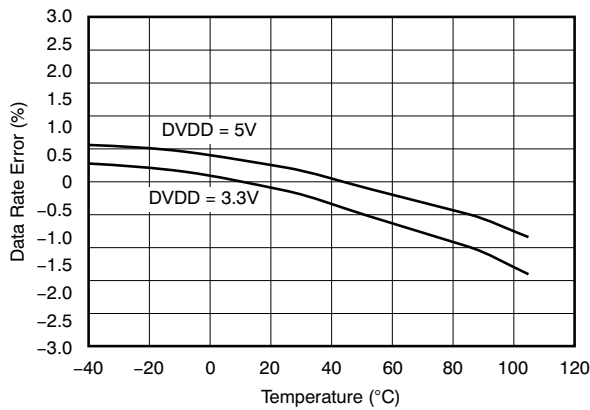


Figure 11.

IDAC LINE REGULATION

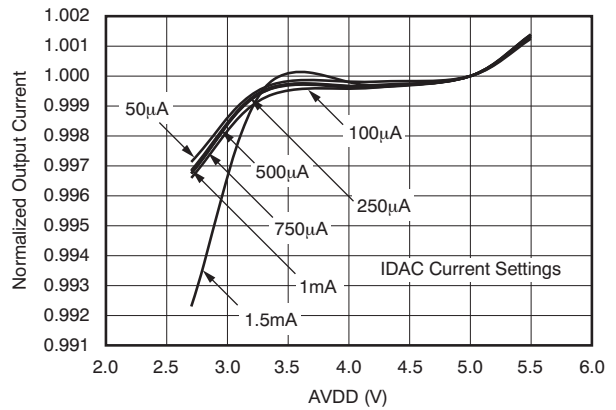


Figure 12.

IDAC DRIFT

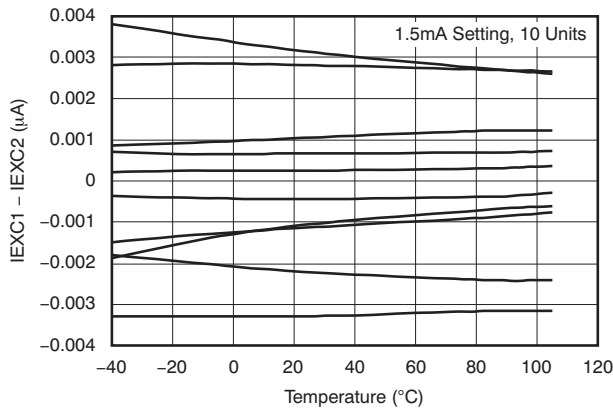


Figure 13.

INTERNAL REFERENCE LONG TERM DRIFT

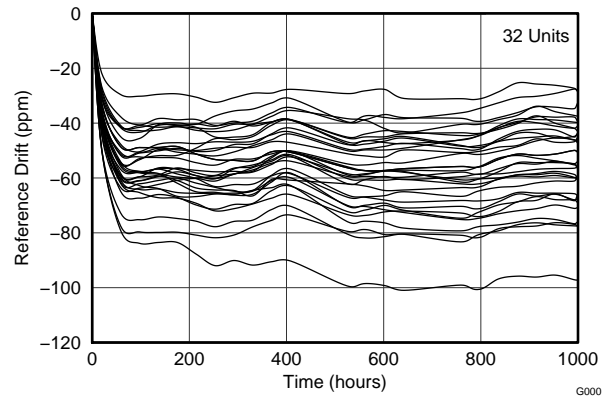


Figure 14.

IDAC VOLTAGE COMPLIANCE

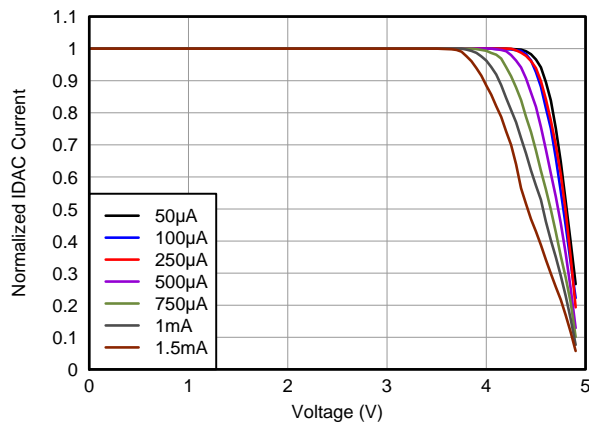


Figure 15.

IDAC VOLTAGE COMPLIANCE

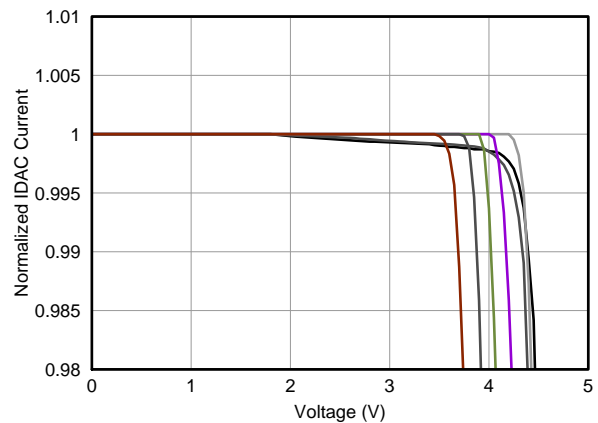


Figure 16.

GENERAL DESCRIPTION

OVERVIEW

The ADS1146, ADS1147 and ADS1148 are highly integrated 24-bit data converters. Each device includes a low-noise, high-impedance programmable gain amplifier (PGA), a delta-sigma ($\Delta\Sigma$) ADC with an adjustable single-cycle settling digital filter, internal oscillator, and a simple but flexible SPI-compatible serial interface.

The ADS1147 and ADS1148 also include a flexible input multiplexer with system monitoring capability and general-purpose I/O settings, a very low-drift voltage reference, and two matched current sources for sensor excitation. Figure 17 and Figure 18 show the various functions incorporated into each device.

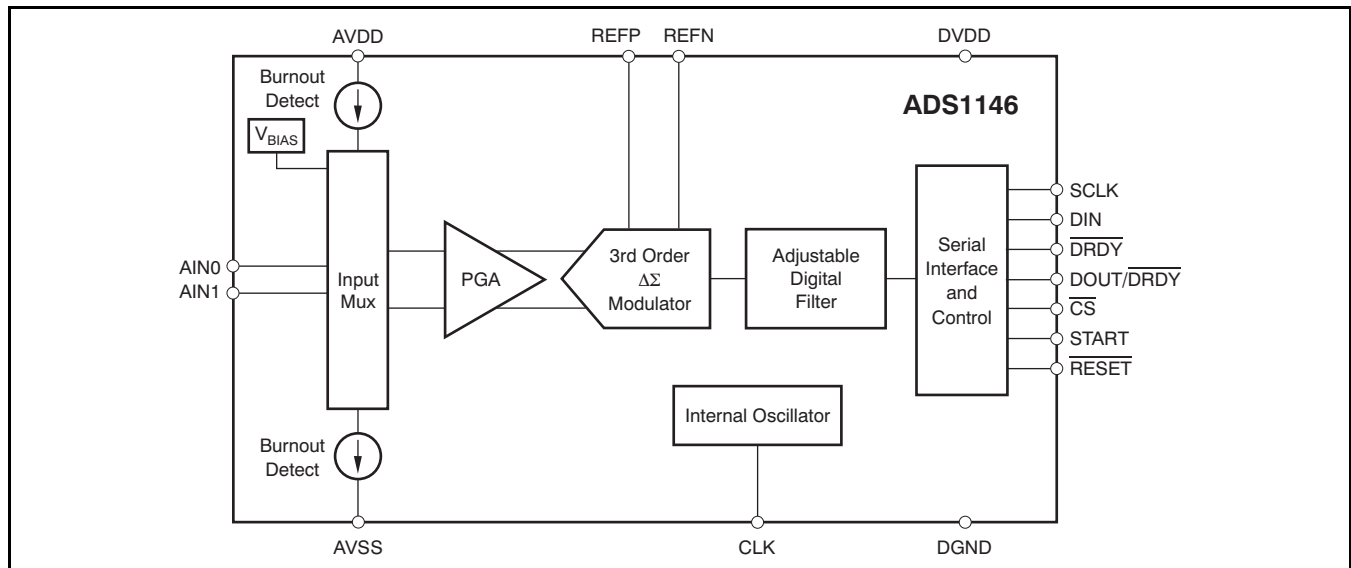


Figure 17. ADS1146 Diagram

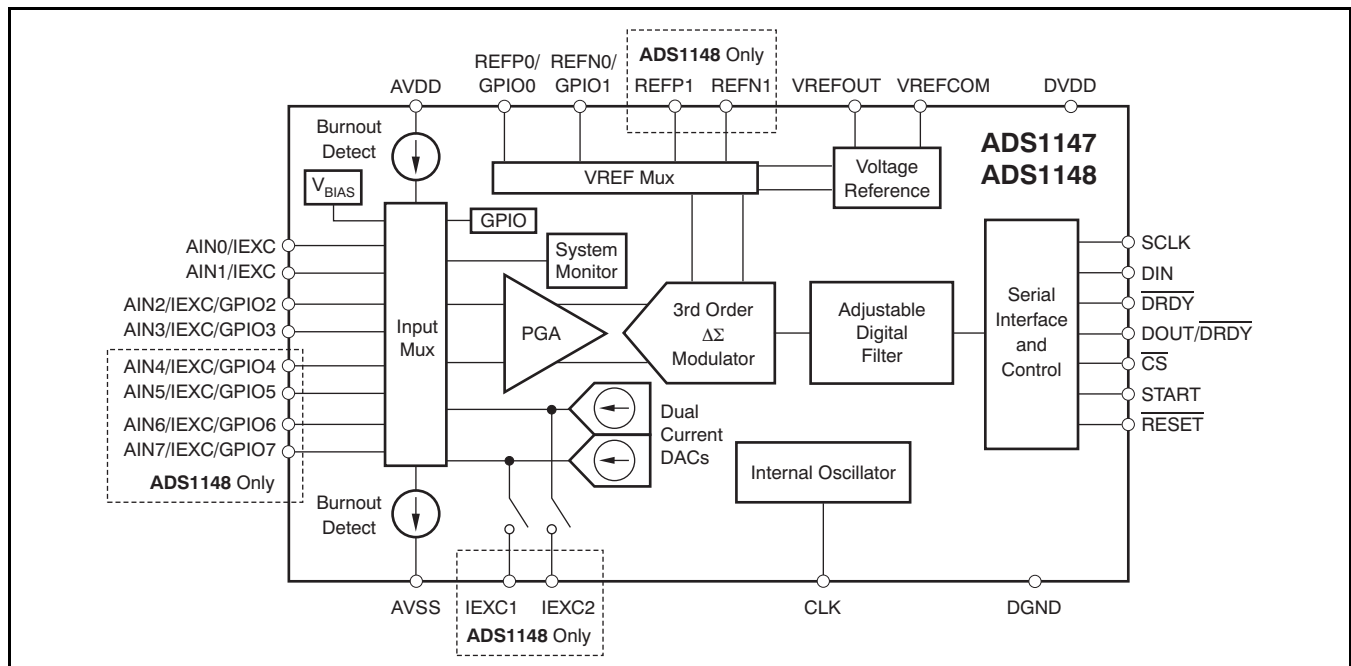


Figure 18. ADS1147, ADS1148 Diagram

ADC INPUT AND MULTIPLEXER

The ADS1146/7/8 ADC measures the input signal through the onboard PGA. All analog inputs are connected to the internal AIN_P or AIN_N analog inputs through the analog multiplexer. A block diagram of the analog input multiplexer is shown in Figure 19.

The input multiplexer connects to eight (ADS1148), four (ADS1147), or two (ADS1146) analog inputs that can be configured as single-ended inputs, differential inputs, or in a combination of single-ended and differential inputs. The multiplexer also allows the on-chip excitation current and/or bias voltage to be selected to a specific channel.

Any analog input pin can be selected as the positive input or negative input through the MUX0 register. The ADS1146/7/8 have a true fully differential mode, meaning that the input signal range can be from $-2.5V$ to $+2.5V$ (when $AVDD = 2.5V$ and $AVSS = -2.5V$).

Through the input multiplexer, the ambient temperature (internal temperature sensor), $AVDD$, $DVDD$, and external reference can all be selected for measurement. Refer to the *System Monitor* section for details.

On the ADS1147 and ADS1148, the analog inputs can also be configured as general-purpose inputs/outputs (GPIOs). See the *General-Purpose Digital I/O* section for more details.

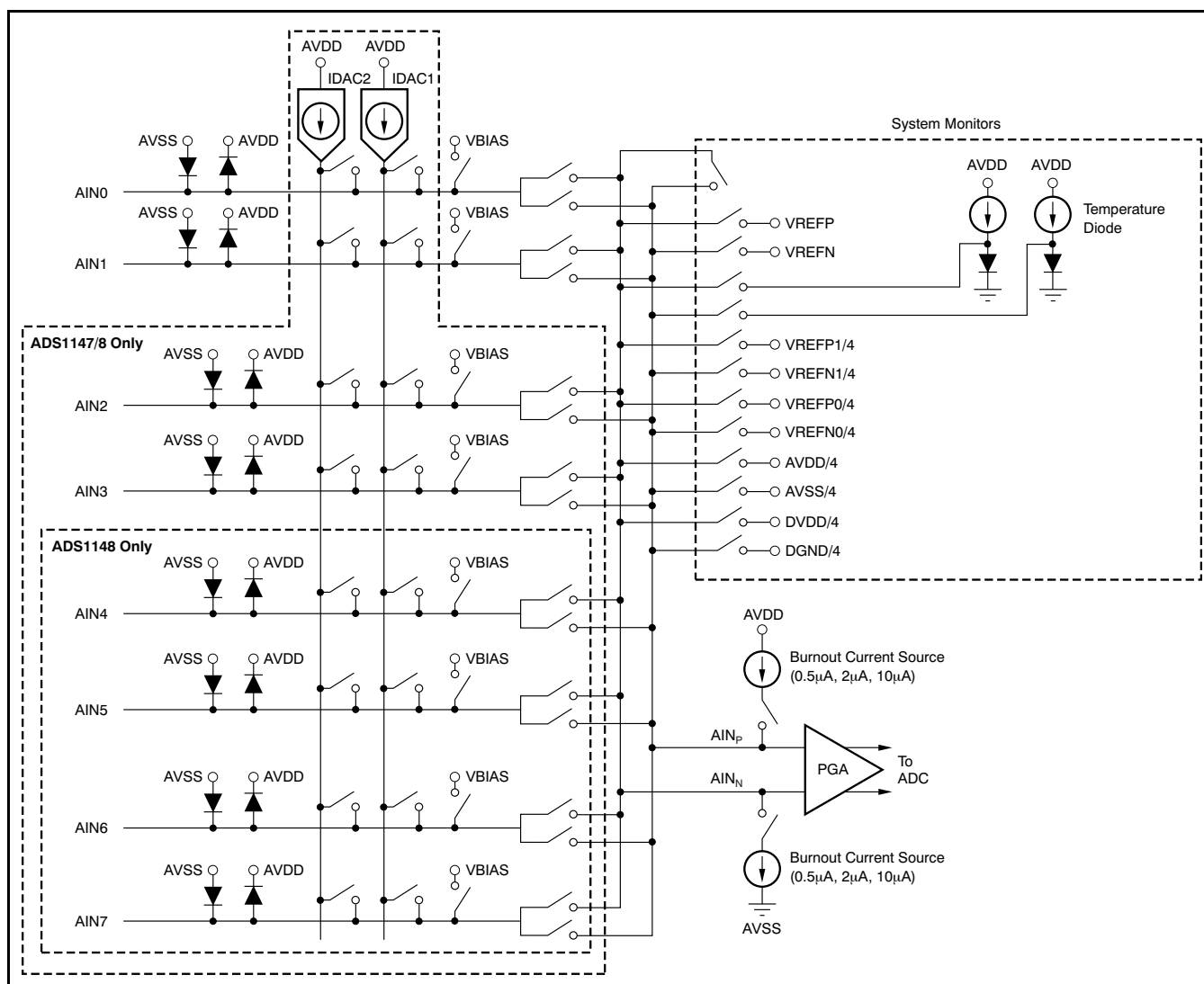


Figure 19. Analog Input Multiplexer Circuit

ESD diodes protect the ADC inputs. To prevent these diodes from turning on, make sure the voltages on the input pins do not go below AVSS by more than 100mV, and do not exceed AVDD by more than 100mV, as shown in Equation 2. Note that the same caution is true if the inputs are configured to be GPIOs.

$$AVSS - 100mV < (AINX) < AVDD + 100mV \quad (2)$$

Settling Time for Channel Multiplexing

The ADS1146/7/8 is a true single-cycle settling $\Delta\Sigma$ converter. The first data available after the start of a conversion are fully settled and valid for use. The time required to settle is roughly equal to the inverse of the data rate. The exact time depends on the specific data rate and the operation that resulted in the start of a conversion; see Table 12 for specific values.

ANALOG INPUT IMPEDANCE

The ADS1146/7/8 inputs are buffered through a high-impedance PGA before they reach the $\Delta\Sigma$ modulator. For the majority of applications, the input current leakage is minimal and can be neglected. However, because the PGA is chopper-stabilized for noise and offset performance, the input impedance is best described as a small absolute input current. The absolute current leakage for selected channels is approximately proportional to the selected modulator clock. Table 3 shows the typical values for these currents with a differential voltage coefficient and the corresponding input impedances over data rate.

VOLTAGE REFERENCE INPUT

The voltage reference for the ADS1146/7/8 is the differential voltage between REFP and REFN:

$$V_{REF} = V_{REFP} - V_{REFN}$$

In the case of the ADS1146, these pins are dedicated inputs. For the ADS1147 and ADS1148, there is a multiplexer that selects the reference inputs, as shown in Figure 20. The reference input uses a buffer to increase the input impedance.

As with the analog inputs, REFP0 and REFN0 can be configured as digital I/Os on the ADS1147 and ADS1148.

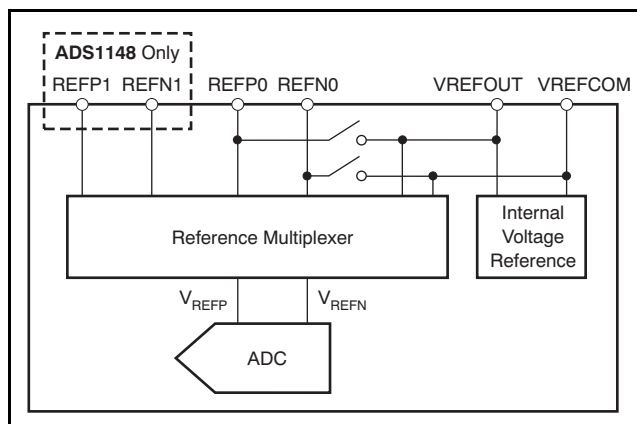


Figure 20. Reference Input Multiplexer

The reference input circuit has ESD diodes to protect the inputs. To prevent the diodes from turning on, make sure the voltage on the reference input pin is not less than AVSS – 100mV, and does not exceed AVDD + 100mV, as shown in Equation 3:

$$AVSS - 100mV < (V_{REFP} \text{ or } V_{REFN}) < AVDD + 100mV \quad (3)$$

Table 3. Typical Values for Analog Input Current Over Data Rate

| CONDITION | ABSOLUTE INPUT CURRENT | EFFECTIVE INPUT IMPEDANCE |
|----------------------------|-------------------------|---------------------------|
| DR = 5SPS, 10SPS, 20SPS | $\pm (0.5nA + 0.1nA/V)$ | 5000M Ω |
| DR = 40SPS, 80SPS, 160SPS | $\pm (2nA + 0.5nA/V)$ | 1200M Ω |
| DR = 320SPS, 640SPS, 1kSPS | $\pm (4nA + 1nA/V)$ | 600M Ω |
| DR = 2kSPS | $\pm (8nA + 2nA/V)$ | 300M Ω |

LOW-NOISE PGA

The ADS1146/7/8 feature a low-drift, low-noise, high input impedance programmable gain amplifier (PGA). The PGA can be set to gain of 1, 2, 4, 8, 16, 32, 64, or 128 by register SYS0. A simplified diagram of the PGA is shown in Figure 21.

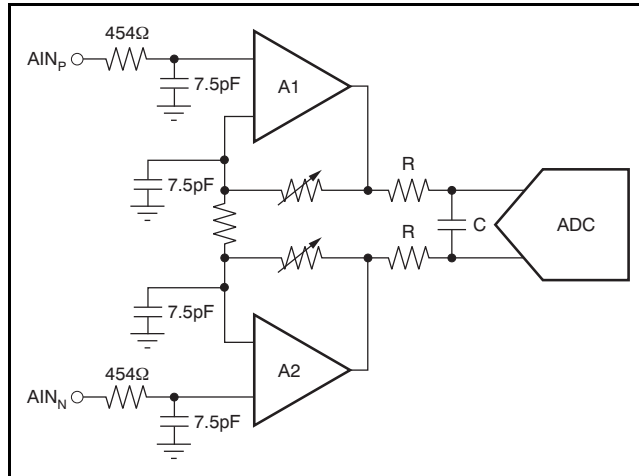


Figure 21. Simplified Diagram of the PGA

The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the gain of the PGA. The PGA input is equipped with an electromagnetic interference (EMI) filter, as shown in Figure 21. Note that as with any PGA, it is necessary to ensure that the input voltage stays within the specified common-mode input range specified in the Electrical Characteristics. The common-mode input (V_{CMI}) must be within the range shown in Equation 4:

$$\left(AVSS + 0.1V + \frac{(V_{IN})(Gain)}{2} \right) \leq V_{CMI} \leq \left(AVDD - 0.1V - \frac{(V_{IN})(Gain)}{2} \right) \quad (4)$$

MODULATOR

A third-order modulator is used in the ADS1146/7/8. The modulator converts the analog input voltage into a pulse code modulated (PCM) data stream. To save power, the modulator clock runs from 32kHz up to 512kHz for different data rates, as shown in Table 4.

DIGITAL FILTER

The ADS1146/7/8 use linear-phase finite impulse response (FIR) digital filters that can be adjusted for different output data rates. The digital filter always settles in a single cycle.

Table 5 shows the exact data rates when an external oscillator equal to 4.096MHz is used. Also shown is the signal $-3dB$ bandwidth, and the 50Hz and 60Hz attenuation. For good 50Hz or 60Hz rejection, use a data rate of 20SPS or slower.

The frequency responses of the digital filter are shown in Figure 22 to Figure 32. Figure 25 shows a detailed view of the filter frequency response from 48Hz to 62Hz for a 20SPS data rate. All filter plots are generated with 4.096MHz external clock.

Table 4. Modulator Clock Frequency for Different Data Rates

| DATA RATE (SPS) | f_{MOD} (kHz) |
|-----------------|-----------------|
| 5, 10, 20 | 32 |
| 40, 80, 160 | 128 |
| 320, 640, 1000 | 256 |
| 2000 | 512 |

Table 5. Digital Filter Specifications⁽¹⁾

| DATA RATE | -3dB BANDWIDTH | ATTENUATION | | | |
|-----------|----------------|---------------------------|---------------------------|-------------------------|-------------------------|
| | | $f_{IN} = 50Hz \pm 0.3Hz$ | $f_{IN} = 60Hz \pm 0.3Hz$ | $f_{IN} = 50Hz \pm 1Hz$ | $f_{IN} = 60Hz \pm 1Hz$ |
| 5SPS | 2.26Hz | -106dB | -74dB | -81dB | -69dB |
| 10SPS | 4.76Hz | -106dB | -74dB | -80dB | -69dB |
| 20SPS | 14.8Hz | -71dB | -74dB | -66dB | -68dB |
| 40SPS | 9.03Hz | | | | |
| 80SPS | 19.8Hz | | | | |
| 160SPS | 118Hz | | | | |
| 320SPS | 154Hz | | | | |
| 640SPS | 495Hz | | | | |
| 1000SPS | 732Hz | | | | |
| 2000SPS | 1465Hz | | | | |

(1) Values shown for $f_{OSC} = 4.096MHz$.

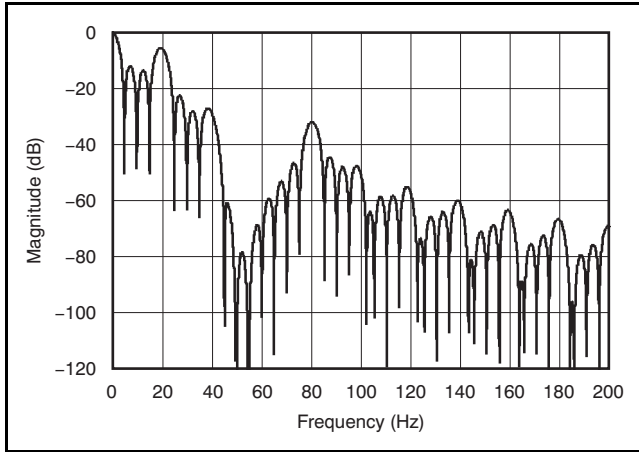


Figure 22. Filter Profile with Data Rate = 5SPS

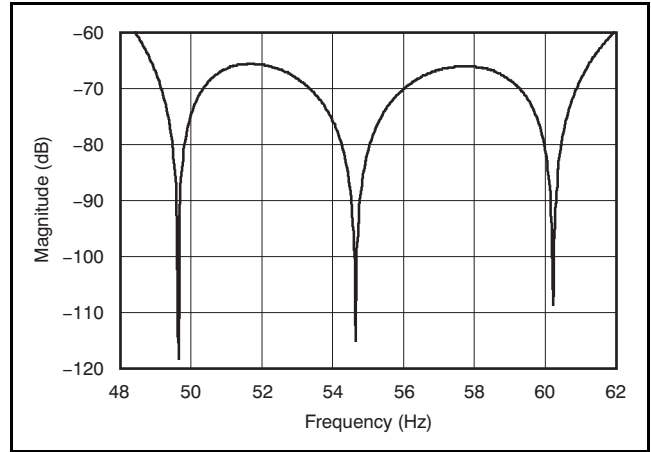


Figure 25. Detailed View of Filter Profile with Data Rate = 20SPS between 48Hz and 62Hz

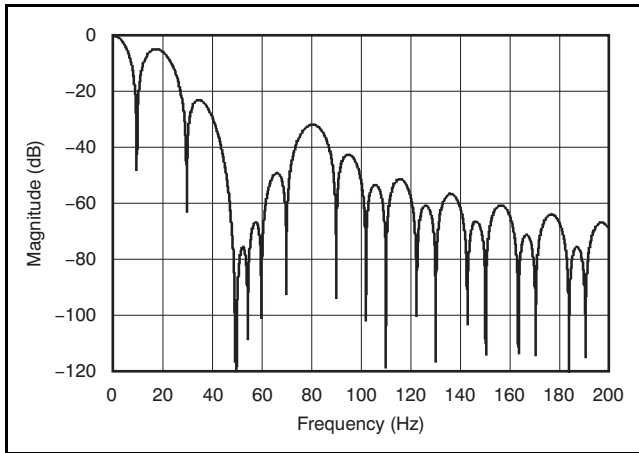


Figure 23. Filter Profile with Data Rate = 10SPS

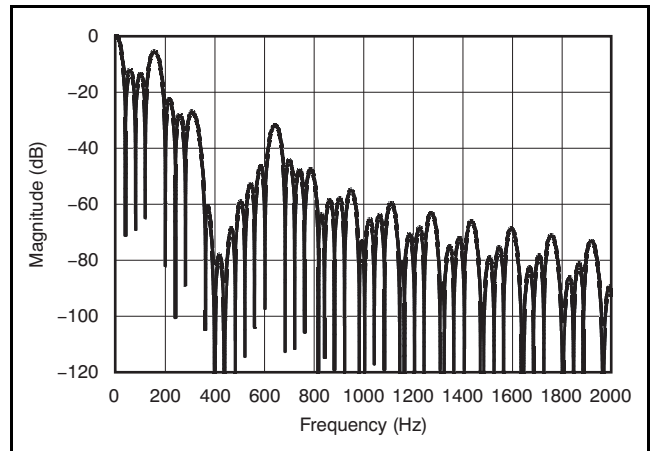


Figure 26. Filter Profile with Data Rate = 40SPS

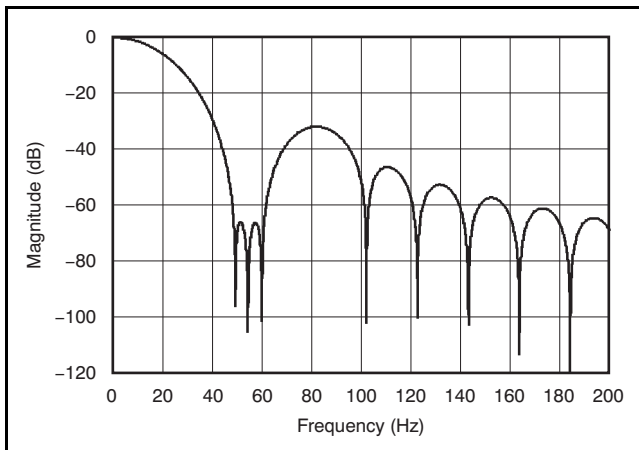


Figure 24. Filter Profile with Data Rate = 20SPS

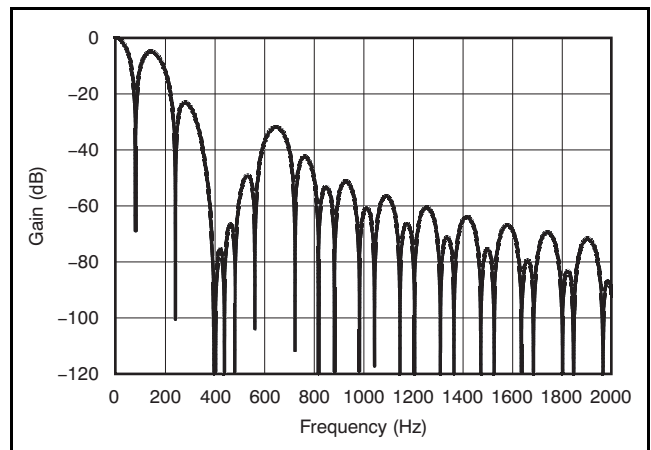


Figure 27. Filter Profile with Data Rate = 80SPS

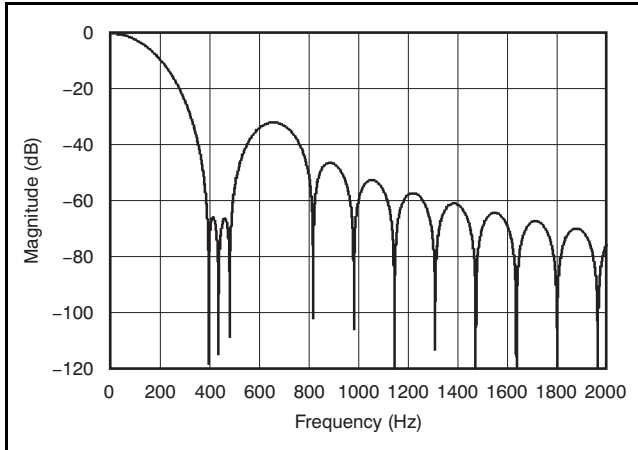


Figure 28. Filter Profile with Data Rate = 160SPS

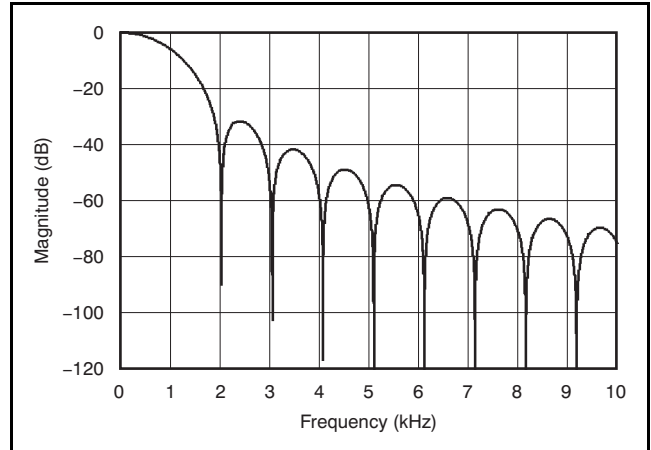


Figure 31. Filter Profile with Data Rate = 1kSPS

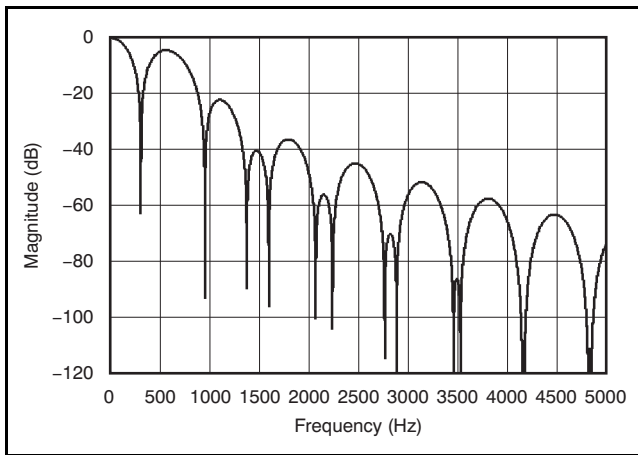


Figure 29. Filter Profile with Data Rate = 320SPS

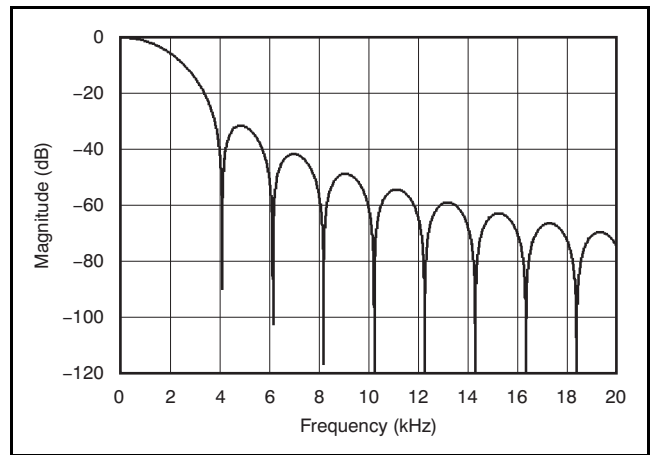


Figure 32. Filter Profile with Data Rate = 2kSPS

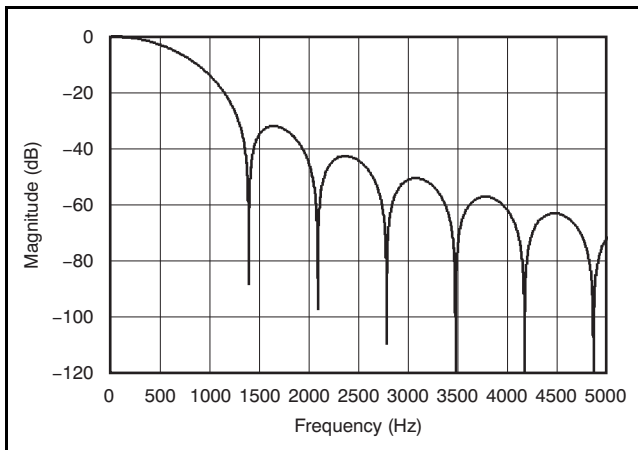


Figure 30. Filter Profile with Data Rate = 640SPS

CLOCK SOURCE

The ADS1146/7/8 can use either the internal oscillator or an external clock. Connect the CLK pin to DGND before power-on or reset to activate the internal oscillator. Connecting an external clock to the CLK pin at any time deactivates the internal oscillator, with the device then operating on the external clock. After the device switches to the external clock, it cannot be switched back to the internal oscillator without cycling the power supplies or resetting the device.

INTERNAL VOLTAGE REFERENCE

The ADS1147 and ADS1148 include an onboard voltage reference with a low temperature coefficient. The output of the voltage reference is 2.048V with the capability of both sourcing and sinking up to 10mA of current.

The voltage reference must have a capacitor connected between VREFOUT and VREFCOM. The value of the capacitance should be in the range of 1 μ F to 47 μ F. Large values provide more filtering of the reference; however, the turn-on time increases with capacitance, as shown in [Table 6](#). For stability reasons, VREFCOM must have a path with an impedance less than 10 Ω to ac ground nodes, such as GND (for a 0V to 5V analog power supply), or AVSS for a \pm 2.5V analog power supply). In case this impedance is higher than 10 Ω , a capacitor of at least 0.1 μ F should be connected between VREFCOM and an ac ground node (for example, GND). Note that because it takes time for the voltage reference to settle to the final voltage, care must be taken when the device is turned off between conversions. Allow adequate time for the internal reference to fully settle.

Table 6. Internal Reference Settling Time

| VREFOUT CAPACITOR | SETTLING ERROR | TIME TO REACH THE SETTLING ERROR |
|-------------------|----------------|----------------------------------|
| 1 μ F | \pm 0.5% | 70 μ s |
| | \pm 0.1% | 110 μ s |
| 4.7 μ F | \pm 0.5% | 290 μ s |
| | \pm 0.1% | 375 μ s |
| 47 μ F | \pm 0.5% | 2.2ms |
| | \pm 0.1% | 2.4ms |

The onboard reference is controlled by the registers; by default, it is off after startup (see the [ADS1147/48 Detailed Register Definitions](#) section for more details). Therefore, the internal reference must first be turned on and then connected via the internal reference multiplexer. Because the onboard reference is used to generate the current reference for the excitation current sources, it must be turned on before the excitation currents become available.

EXCITATION CURRENT SOURCE DACS

The ADS1147 and ADS1148 provide two matched excitation current sources for RTD applications. For three- or four-wire RTD applications, the matched current sources can be used to cancel the errors caused by sensor lead resistance. The output current of the current source DACs can be programmed to 50 μ A, 100 μ A, 250 μ A, 500 μ A, 750 μ A, 1000 μ A, or 1500 μ A.

The two matched current sources can be connected to dedicated current output pins IOUT1 and IOUT2 (ADS1148 only), or to any AIN pin (ADS1147 and ADS1148); refer to the [ADS1147/48 Detailed Register Definitions](#) section for more information. It is possible to connect both current sources to the same pin. Note that the internal reference must be turned on and properly compensated when using the excitation current source DACs.

SENSOR DETECTION

The ADS1146/7/8 provide a selectable current (0.5 μ A, 2 μ A, or 10 μ A) to help detect a possible sensor malfunction.

When enabled, two burnout current sources flow through the selected pair of analog inputs to the sensor. One sources the current to the positive input channel, and the other sinks the same current from the negative input channel.

When the burnout current sources are enabled, a full-scale reading may indicate an open circuit in the front-end sensor, or that the sensor is overloaded. It may also indicate that the reference voltage is absent. A near-zero reading may indicate a short-circuit in the sensor.

BIAS VOLTAGE GENERATION

A selectable bias voltage is provided for use with ungrounded thermocouples. The bias voltage is (AVDD + AVSS)/2 and can be applied to any analog input channel through internal input multiplexer. The bias voltage turn-on times for different sensor capacitances are listed in [Table 7](#).

The internal bias generator when selected on multiple channels causes them to be internally shorted. Because of this, it is important that care be taken to limit the amount of current that may flow through the device. It is recommended that under no circumstances more than 5mA be allowed to flow through this path. This applies when the device is in operation and when it is in shutdown mode.

Table 7. Bias Voltage Settling Time

| SENSOR CAPACITANCE | SETTLING TIME |
|--------------------|---------------|
| 0.1 μ F | 220 μ s |
| 1 μ F | 2.2ms |
| 10 μ F | 22ms |
| 200 μ F | 450ms |

GENERAL-PURPOSE DIGITAL I/O

The ADS1148 has eight pins and the ADS1147 has four pins that serve a dual purpose as either analog inputs or general-purpose digital inputs/outputs (GPIOs).

Figure 33 shows a diagram of how these functions are combined onto a single pin. Note that when the pin is configured as a GPIO, the corresponding logic is powered from AVDD and AVSS. When the ADS1147 and ADS1148 are operated with bipolar analog supplies, the GPIO outputs bipolar voltages. Care must be taken loading the GPIO pins when used as outputs because large currents can cause droop or noise on the analog supplies.

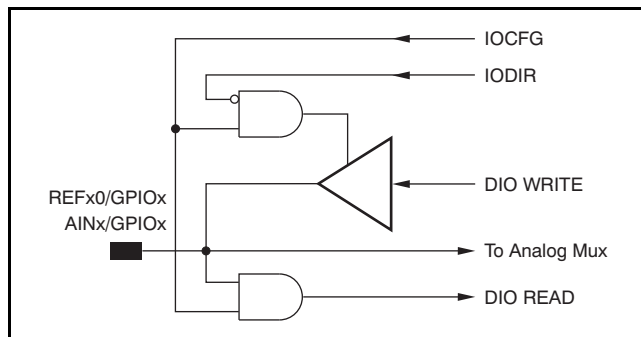


Figure 33. Analog/Data Interface Pin

SYSTEM MONITOR

The ADS1147 and ADS1148 provide a system monitor function. This function can measure the analog power supply, digital power supply, external voltage reference, or ambient temperature. Note that the system monitor function provides a coarse result. When the system monitor is enabled, the analog inputs are disconnected.

Power-Supply Monitor

The system monitor can measure the analog or digital power supply. When measuring the power supply, the resulting conversion is approximately 1/4 of the actual power supply voltage.

$$\text{Conversion Result} = (V_{SP}/4)/V_{REF} \quad (5)$$

Where V_{SP} is the selected supply to be measured.

External Voltage Reference Monitor

The ADS1146/7/8 can be selected to measure the external voltage reference. In this configuration, the monitored external voltage reference is connected to the analog input. The result (conversion code) is approximately 1/4 of the actual reference voltage.

$$\text{Conversion Result} = (V_{REX}/4)/V_{REF} \quad (6)$$

Where V_{REX} is the external reference to be monitored.

NOTE: The internal reference voltage must be enabled when measuring an external voltage reference using the system monitor.

Ambient Temperature Monitor

On-chip diodes provide temperature-sensing capability. When selecting the temperature monitor function, the anodes of two diodes are connected to the ADC. Typically, the difference in diode voltage is 118mV at +25°C with a temperature coefficient of 405 μ V/°C.

Note that when the onboard temperature monitor is selected, the PGA is automatically set to '1'. However, the PGA register bits in are not affected and the PGA returns to its set value when the temperature monitor is turned off.

CALIBRATION

The conversion data are scaled by offset and gain registers before yielding the final output code. As shown in Figure 34, the output of the digital filter is first subtracted by the offset register (OFC) and then multiplied by the full-scale register (FSC). A digital clipping circuit ensures that the output code does not exceed 16 bits. Equation 7 shows the scaling.

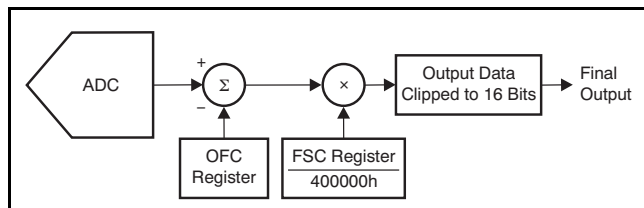


Figure 34. Calibration Block Diagram

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:1]) \times \frac{\text{FSC}[2:0]}{400000\text{h}} \quad (7)$$

The values of the offset and full-scale registers are set by writing to them directly, or they are set automatically by calibration commands.

The gain and offset calibration features are intended for correction of minor system level offset and gain errors. When entering manual values into the calibration registers, care must be taken to avoid scaling down the gain register to values far below a scaling factor of 1.0. Under extreme situations it becomes possible to over-range the ADC. To avoid this, make sure to avoid encountering situations where the analog inputs are connected to voltages greater than the reference/PGA.

Care must also be taken when increasing the digital gain. When implementing custom digital gains less than 20% higher than nominal and offsets less than 40% of full scale, no special care is required. When operating at digital gains greater than 20% higher than nominal and offsets greater than 40% of full scale, make sure that the offset and gain registers follow the conditions of equation 8.

$$\frac{2V}{\text{Gain Scaling}} - 1.251V > |\text{Offset Scaling}| \quad (8)$$

Offset Calibration Register: OFC[2:0]

The offset calibration is a 24-bit word, composed of three 8-bit registers. The upper 16 bits, OFC[2:1], are the most important for calibration and can correct offsets ranging from –FS to +FS, as shown in Table 8. The lower eight bits, OFC[0], provide sub-

LSB correction and are used by the ADS1146/7/8 calibration commands. If an ADS1146/7/8 calibration command is issued and the offset register is then read for storage and re-use later, it is recommended that all 24 bits of the OFC be used. When the calibration commands are not used and the offset is corrected by writing a user-calculated value to the OFC register, it is recommended that only that only OFC[2:1] be used and that OFC[0] be left as all zeros.

Note that while the offset calibration register value can correct offsets ranging from –FS to +FS (as shown in Table 8), make sure to avoid overloading the analog inputs.

Table 8. Final Output Code versus Offset Calibration Register Setting

| OFFSET REGISTER | FINAL OUTPUT CODE WITH $V_{IN} = 0$ |
|-----------------|-------------------------------------|
| 7FFFFFFh | 8000000h |
| 000001h | FFFFFFFh |
| 000000h | 000000h |
| FFFFFFFh | 000000h |
| 8000000h | 7FFFFFFh |

1. Excludes effects of noise and inherent offset errors.

Full-Scale Calibration Register: FSC[2:0]

The full-scale or gain calibration is a 24-bit word composed of three 8-bit registers. The full-scale calibration value is 24-bit, straight binary, normalized to 1.0 at code 400000h. Table 9 summarizes the scaling of the full-scale register. Note that while the full-scale calibration register can correct gain errors > 1 (with gain scaling < 1), make sure to avoid overloading the analog inputs.

Table 9. Gain Correction Factor versus Full-Scale Calibration Register Setting

| FULL-SCALE REGISTER | GAIN SCALING |
|---------------------|--------------|
| 800000h | 2.0 |
| 400000h | 1.0 |
| 200000h | 0.5 |
| 000000h | 0 |

Calibration Commands

The ADS1146/7/8 provide commands for three types of calibration: system gain calibration, system offset calibration and self offset calibration. Where absolute accuracy is needed, it is recommended that calibration be performed after power on, a change in temperature, a change of PGA and in some cases a change in channel. At the completion of calibration, the DRDY signal goes low indicating the calibration is finished. The first data after calibration are always valid. If the START pin is taken low or a SLEEP command is issued after any calibration command, the devices goes to sleep after completing calibration.

It is important to allow a pending system calibration to complete before issuing any other commands. Issuing commands during a calibration can result in corrupted data. If this occurs either resend the calibration command that was aborted or issue a device reset.

System Gain Calibration

System gain calibration corrects for gain error in the signal path. The system gain calibration is initiated by sending the SYSGCAL command while applying a full-scale input to the selected analog inputs. Afterwards the full-scale calibration register (FSC) is updated. When a system gain calibration command is issued, the ADS1146/7/8 stop the current conversion and start the calibration procedure immediately.

System Offset and Self Offset Calibration

System offset calibration corrects both internal and external offset errors. The system offset calibration is initiated by sending the SYSOCAL command while applying a zero differential input ($V_{IN} = 0$) to the selected analog inputs. The self offset calibration is initiated by sending the SELFOCAL command. During self offset calibration, the selected inputs are disconnected from the internal circuitry and a zero differential signal is applied internally. With both offset

calibrations the offset calibration register (OFC) is updated afterwards. When either offset calibration command is issued, the ADS1146/7/8 stop the current conversion and start the calibration procedure immediately.

Calibration Timing

When calibration is initiated, the device performs 16 consecutive data conversions and averages the results to calculate the calibration value. This provides a more accurate calibration value. The time required for calibration is shown in Table 10 and can be calculated using Equation 9:

$$\text{Calibration Time} = \frac{50}{f_{\text{OSC}}} + \frac{32}{f_{\text{MOD}}} + \frac{16}{f_{\text{DATA}}} \quad (9)$$

Table 10. Calibration Time versus Data Rate

| DATA RATE (SPS) | CALIBRATION TIME (ms) |
|-----------------|-----------------------|
| 5 | 3201.01 |
| 10 | 1601.01 |
| 20 | 801.012 |
| 40 | 400.26 |
| 80 | 200.26 |
| 160 | 100.14 |
| 320 | 50.14 |
| 640 | 25.14 |
| 1000 | 16.14 |
| 2000 | 8.07 |

1. For $f_{\text{OSC}} = 4.096\text{MHz}$.

ADC SLEEP MODE

Power consumption can be dramatically reduced by placing the ADS1146/7/8 into sleep mode. There are two ways to put the device into sleep mode: the sleep command (SLEEP) and through the START pin.

During sleep mode, the internal reference status depends on the setting of the VREFCON bits in the MUX1 register; see the [Register Descriptions](#) section for details.

ADC CONTROL

ADC Conversion Control

The START pin provides easy and precise control of conversions. Pulse the START pin high to begin a conversion, as shown in Figure 35 and Table 11. The conversion completion is indicated by the DOUT/DRDY pin going low. When the conversion completes, the ADS1146/7/8 automatically shuts

down to save power. During shutdown, the conversion result can be retrieved; however, START must be taken high before communicating with the configuration registers. The device stays shut down until the START pin is once again taken high to begin a new conversion. When the START pin is taken back high again, the decimation filter is held in a reset state for 32 modulator clock cycles internally to allow the analog circuits to settle.

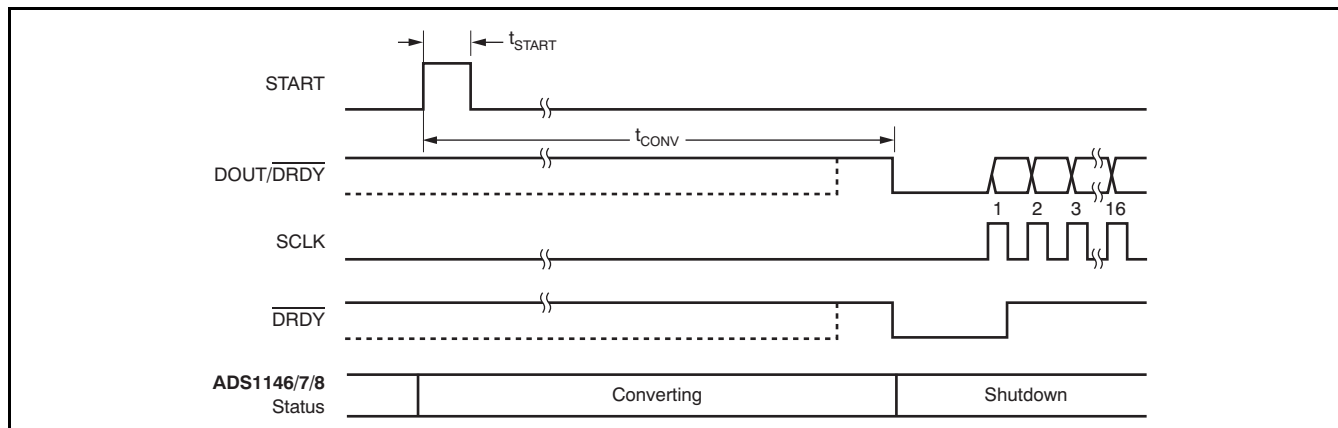


Figure 35. Timing for Single Conversion Using START Pin

Table 11. START Pin Conversion Times for Figure 35

| SYMBOL | DESCRIPTION | DATA RATE (SPS) | VALUE | UNIT |
|------------|--|-----------------|---------|------|
| t_{CONV} | Time from START pulse to \overline{DRDY} and DOUT/DRDY going low | 5 | 200.295 | ms |
| | | 10 | 100.644 | ms |
| | | 20 | 50.825 | ms |
| | | 40 | 25.169 | ms |
| | | 80 | 12.716 | ms |
| | | 160 | 6.489 | ms |
| | | 320 | 3.247 | ms |
| | | 640 | 1.692 | ms |
| | | 1000 | 1.138 | ms |
| | | 2000 | 0.575 | ms |

The ADS1146/7/8 can be configured to convert continuously by holding the START pin high, as shown in Figure 36. With the START pin held high, the ADC converts the selected input channels continuously. This configuration continues until the START pin is taken low.

The START pin can also be used to perform the synchronized measurement for the multi-channel applications by pulsing the START pin.

RESET

When the $\overline{\text{RESET}}$ pin goes low, the device is immediately reset. All the registers are restored to default values. The device stays in reset mode as long as the $\overline{\text{RESET}}$ pin stays low. When it goes high, the ADC comes out of reset mode and is able to convert data. After the $\overline{\text{RESET}}$ pin goes high, and when the system clock frequency is 4.096MHz, the digital filter and the registers are held in a reset state for 0.6ms when $f_{\text{OSC}} = 4.096\text{MHz}$. Therefore, valid SPI communication can only be resumed 0.6ms after the $\overline{\text{RESET}}$ pin goes high; see Figure 4. When the $\overline{\text{RESET}}$ pin goes low, the clock selection is reset to the internal oscillator.

Channel Cycling and Overload Recovery

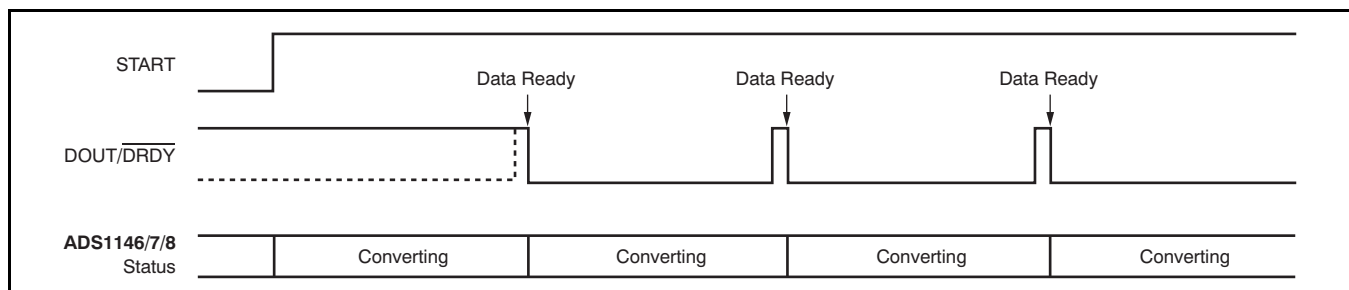
When cycling through channels, care must be taken when configuring the ADS1146/7/8 to ensure that settling occurs within one cycle. For setups that simply cycle through MUX channels, but do not change PGA and data rate settings, simply changing the MUX0 register is sufficient. However, when changing PGA and data rate settings it is important to ensure that an overloaded condition cannot occur during the transmission. When configuration data are

transferred to the ADS1146/7/8, new settings become active at the end of each byte sent. Therefore, a brief overload condition can occur during the transmission of configuration data after the completion of the MUX0 byte and before the completion of the SYS0 byte. This temporary overload can result in intermittent incorrect readings. To ensure that an overload does not occur, it may be necessary to split the communication into two separate communications allowing the change of the SYS0 register before the change of the MUX0 register.

In the event of an overloaded state, care must also be taken to ensure single cycle settling into the next cycle. Because the ADS1146/7/8 implement a chopper-stabilized PGA, changing data rates during an overload state can cause the chopper to become unstable. This instability results in slow settling time. To prevent this slow settling, always change the PGA setting or MUX setting to a non-overloaded state before changing the data rate.

Single-Cycle Settling

The ADS1146/7/8 are capable of single-cycle settling across all gains and data rates. However, to achieve single-cycle settling at 2kSPS, special care must be taken with respect to the interface. When operating at 2kSPS, the SPI data SCLK period must not exceed 520ns, and the time between the beginning of a byte and the beginning of a subsequent byte must not exceed 4.2µs. Additionally, when performing multiple individual write commands to the first four registers, wait at least 64 oscillator clocks before initiating another write command.



NOTE: SCLK held low in this example.

Figure 36. Timing for Conversion with START Pin High

Digital Filter Reset Operation

Apart from the RESET command and the $\overline{\text{RESET}}$ pin, the digital filter is reset automatically when either a write operation to the MUX0, VBIAS, MUX1, or SYS0 registers is performed, when a SYNC command is issued, or the START pin is taken high.

The filter is reset two system clocks after the last bit of the SYNC command is sent. The reset pulse created internally lasts for two multiplier clock cycles. If any write operation takes place in the MUX0 register, the filter is reset regardless of whether the value changed or not. Internally, the filter pulse lasts for two system clock periods. If any write activity

takes place in the VBIAS, MUX1, or SYS0 registers, the filter is reset as well, regardless of whether the value changed or not. The reset pulse lasts for 32 modulator clocks after the write operation. If there are multiple write operations, the resulting reset pulse may be viewed as the ANDed result of the different active low pulses created individually by each action.

Table 12 shows the conversion time after a filter reset. Note that this time depends on the operation initiating the reset. Also, the first conversion after a filter reset has a slightly different time than the second and subsequent conversions.

Table 12. Data Conversion Time

| NOMINAL DATA RATE (SPS) | EXACT DATA RATE (SPS) | FIRST DATA CONVERSION TIME AFTER FILTER RESET | | | | SECOND AND SUBSEQUENT CONVERSION TIME AFTER FILTER RESET | |
|-------------------------|-----------------------|---|----------------------------|--|----------------------------|--|----------------------------|
| | | SYNC COMMAND, MUX0 REGISTER WRITE | | HARDWARE RESET, RESET COMMAND, START PIN HIGH, WAKEUP COMMAND, VBIAS, MUX1, or SYS0 REGISTER WRITE | | | |
| | | (ms) ⁽¹⁾ | NO. OF SYSTEM CLOCK CYCLES | (ms) ⁽¹⁾ | NO. OF SYSTEM CLOCK CYCLES | (ms) | NO. OF SYSTEM CLOCK CYCLES |
| 5 | 5.019 | 199.258 | 816160 | 200.26 | 820265 | 199.250 | 816128 |
| 10 | 10.038 | 99.633 | 408096 | 100.635 | 412201 | 99.625 | 408064 |
| 20 | 20.075 | 49.820 | 204064 | 50.822 | 208169 | 49.812 | 204032 |
| 40 | 40.151 | 24.920 | 102072 | 25.172 | 103106 | 24.906 | 102016 |
| 80 | 80.301 | 12.467 | 51064 | 12.719 | 52098 | 12.453 | 51008 |
| 160 | 160.602 | 6.241 | 25560 | 6.492 | 26594 | 6.226 | 25504 |
| 320 | 321.608 | 3.124 | 12796 | 3.250 | 13314 | 3.109 | 12736 |
| 640 | 643.216 | 1.569 | 6428 | 1.695 | 6946 | 1.554 | 6368 |
| 1000 | 1000.000 | 1.014 | 4156 | 1.141 | 4674 | 1.000 | 4096 |
| 2000 | 2000.000 | 0.514 | 2108 | 0.578 | 2370 | 0.500 | 2048 |

(1) For $f_{\text{OSC}} = 4.096\text{MHz}$.

Data Format

The ADS1146/7/8 output 16 bits of data in binary twos complement format. The least significant bit (LSB) has a weight of $(V_{REF}/PGA)/(2^{15} - 1)$. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals exceeding full-scale. Table 13 summarizes the ideal output codes for different input signals.

Table 13. Ideal Output Code vs Input Signal

| INPUT SIGNAL, V_{IN} ($A_{INP} - A_{INN}$) | IDEAL OUTPUT CODE |
|---|-------------------|
| $\geq +V_{REF}/PGA$ | 7FFFh |
| $(+V_{REF}/PGA)/(2^{15} - 1)$ | 0001h |
| 0 | 0000h |
| $(-V_{REF}/PGA)/(2^{15} - 1)$ | FFFFh |
| $\leq -(V_{REF}/PGA) \times (2^{15}/2^{15} - 1)$ | 8000h |

1. Excludes effects of noise, linearity, offset, and gain errors.

Digital Interface

The ADS1146/7/8 provide a standard SPI serial communication interface plus a data ready signal (\overline{DRDY}). Communication is full-duplex with the exception of a few limitations in regards to the RREG command and the RDATA command. These limitations are explained in detail in the [SPI Commands](#) section of this data sheet. For the basic serial interface timing characteristics, see [Figure 1](#) and [Figure 2](#) of this document.

\overline{CS}

This pin is the chip select pin (active low). The \overline{CS} pin activates SPI communication. \overline{CS} must be low before data transactions and must stay low for the entire SPI communication period. When \overline{CS} is high, the DOUT/ \overline{DRDY} pin enters a high-impedance state. Therefore, reading and writing to the serial interface are ignored and the serial interface is reset. \overline{DRDY} pin operation is independent of \overline{CS} .

Taking \overline{CS} high deactivates only the SPI communication with the device. Data conversion continues and the \overline{DRDY} signal can be monitored to check if a new conversion result is ready. A master device monitoring the \overline{DRDY} signal can select the appropriate slave device by pulling the \overline{CS} pin low.

The ADS1146/7/8 implement a timeout function for all listed commands in the event that data is corrupted and chip select is permanently tied low. However, it is important in systems where chip select is tied low permanently that register writes always be fully completed in 8 bit increments. The SCLK line should also be kept clean and situations should be avoided where noise on the SCLK line could cause the device to interpret the transient as a false SCLK pulse. In systems where such events are likely to occur, it is recommended that chip select be used to frame communications to the device.

SCLK

This signal is the serial clock signal. SCLK provides the clock for serial communication. It is a Schmitt-trigger input, but it is highly recommended that SCLK be kept as clean as possible to prevent glitches from inadvertently shifting the data. Data are shifted into DIN on the falling edge of SCLK and shifted out of DOUT on the rising edge of SCLK.

DIN

This pin is the data input pin. DIN is used along with SCLK to send data to the device. Data on DIN are shifted into the device on the falling edge of SCLK.

The communication of this device is full-duplex in nature. The device monitors commands shifted in even when data are being shifted out. Data that are present in the output shift register are shifted out when sending in a command. Therefore, it is important to make sure that whatever is being sent on the DIN pin is valid when shifting out data. When no command is to be sent to the device when reading out data, the NOP command should be sent on DIN.

\overline{DRDY}

This pin is the data ready pin. The \overline{DRDY} pin goes low to indicate a new conversion is complete, and the conversion result is stored in the conversion result buffer. The SPI clock must be low in a short time frame around the \overline{DRDY} low transition (see [Figure 2](#)) so that the conversion result is loaded into both the result buffer and the output shift register. Therefore, no commands should be issued during this time frame if the conversion result is to be read out later. This constraint applies only when \overline{CS} is asserted. When \overline{CS} is not asserted, SPI communication with other devices on the SPI bus does not affect loading of the conversion result. After the \overline{DRDY} pin goes low, it is forced high on the first falling edge of SCLK (so that the \overline{DRDY} pin can be polled for '0' instead of waiting for a falling edge). If the \overline{DRDY} pin is not taken high after it falls low, a short high pulse is created on it to indicate the next data are ready.

DOUT/ $\overline{\text{DRDY}}$

This pin has two modes: data out (DOUT) only, or data out (DOUT) combined with data ready ($\overline{\text{DRDY}}$). The DRDY MODE bit determines the function of this pin. In either mode, the DOUT/ $\overline{\text{DRDY}}$ pin goes to a high-impedance state when $\overline{\text{CS}}$ is taken high.

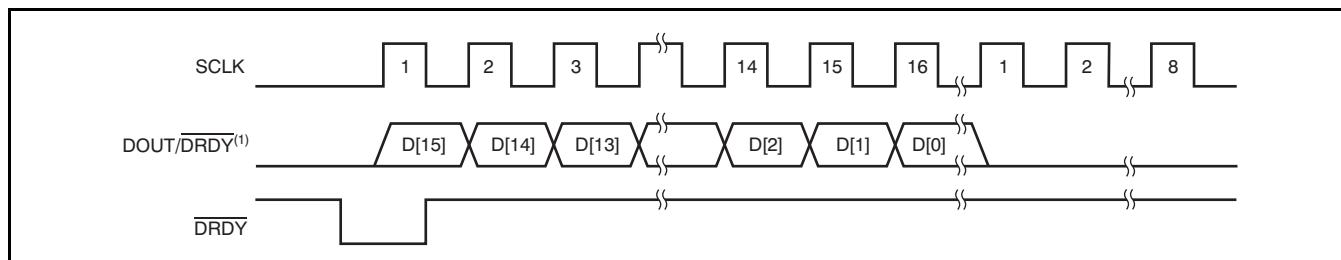
When the DRDY MODE bit is set to '0', this pin functions as DOUT only. Data are clocked out at rising edge of SCLK, MSB first, as shown in Figure 37.

When the DRDY MODE bit is set to '1', this pin functions as both DOUT and $\overline{\text{DRDY}}$. Data are shifted out from this pin, MSB first, at the rising edge of SCLK. This combined pin allows for the same control but with fewer pins.

When the DRDY MODE bit is enabled and a new conversion is complete, DOUT/ $\overline{\text{DRDY}}$ goes low if it is high. If it is already low, then DOUT/ $\overline{\text{DRDY}}$ goes high and then goes low, as shown in Figure 38. Similar to the $\overline{\text{DRDY}}$ pin, a falling edge on the DOUT/ $\overline{\text{DRDY}}$ pin signals that a new conversion result is ready. After DOUT/ $\overline{\text{DRDY}}$ goes low, the data can be clocked out

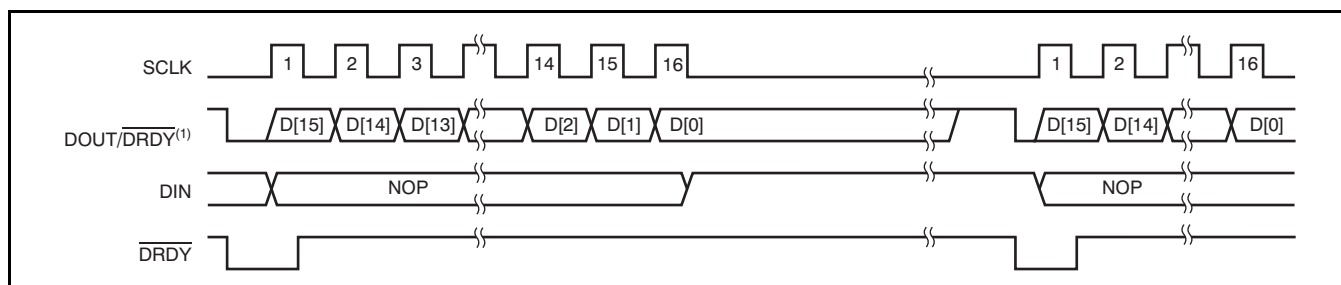
by providing 16 SCLKs. In order to force DOUT/ $\overline{\text{DRDY}}$ high (so that DOUT/ $\overline{\text{DRDY}}$ can be polled for a '0' instead of waiting for a falling edge), a no operation command (NOP) or any other command that does not load the data output register can be sent after reading out the data. Because SCLKs can only be sent in multiples of eight, a NOP can be sent to force DOUT/ $\overline{\text{DRDY}}$ high if no other command is pending. The DOUT/ $\overline{\text{DRDY}}$ pin goes high after the first rising edge of SCLK after reading the conversion result completely (see Figure 39). The same condition also applies after an RREG command. After all the register bits have been read out, the rising edge of SCLK forces DOUT/ $\overline{\text{DRDY}}$ high. Figure 40 illustrates an example where sending four NOP commands after an RREG command forces the DOUT/ $\overline{\text{DRDY}}$ pin high.

The DRDY MODE bit modifies only the DOUT/ $\overline{\text{DRDY}}$ pin functionality. The $\overline{\text{DRDY}}$ pin functionality remains unaffected.



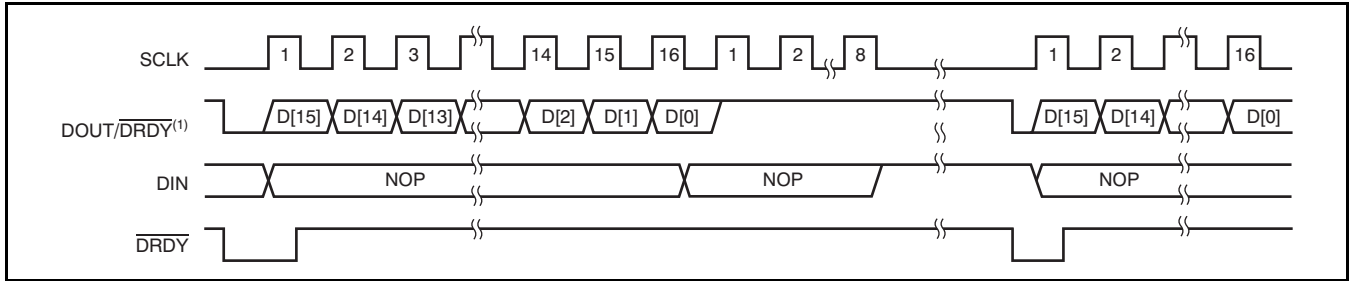
(1) $\overline{\text{CS}}$ tied low.

Figure 37. Data Retrieval with the DRDY MODE Bit = 0 (Disabled)



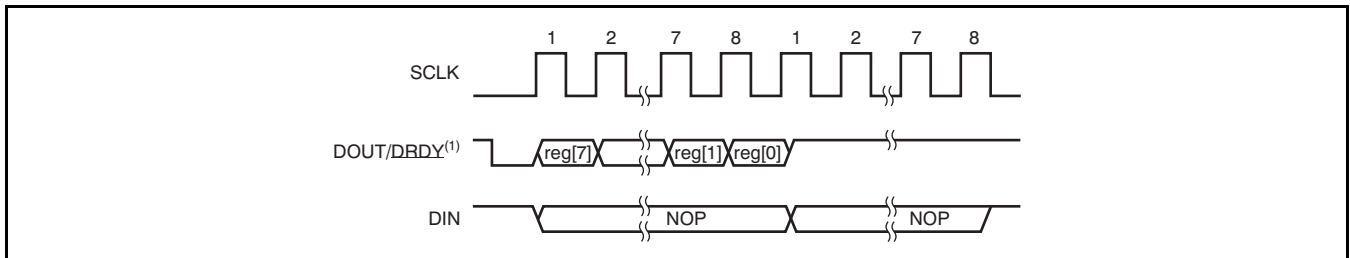
(1) $\overline{\text{CS}}$ tied low.

Figure 38. Data Retrieval with the DRDY MODE Bit = 1 (Enabled)



(1) DRDY MODE bit enabled, \overline{CS} tied low.

Figure 39. DOUT/DRDY Forced High After Retrieving the Conversion Result



(1) DRDY MODE bit enabled, \overline{CS} tied low.

Figure 40. DOUT/DRDY Forced High After Reading Register Data

SPI Reset

SPI communication can be reset in several ways. In order to reset the SPI interface (without resetting the registers or the digital filter), the \overline{CS} pin can be pulled high. Taking the RESET pin low causes the SPI interface to be reset along with all the other digital functions. In this case, the registers and the conversion are reset.

SPI Communication During Sleep Mode

When the START pin is low or the device is in sleep mode, only the RDATA, RDATA_C, SDATA_C, WAKEUP, and NOP commands can be issued. The RDATA command can be used to repeatedly read the last conversion result during sleep mode. Other commands do not function because the internal clock is shut down to save power during sleep mode.

REGISTER DESCRIPTIONS

ADS1146 REGISTER MAP

Table 14. ADS1146 Register Map

| ADDRESS | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------|----------|---------|-------|-------|-------|--------------|---------|---------|---------|
| 00h | BCS | BCS1 | BCS0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 01h | VBIAS | 0 | 0 | 0 | 0 | 0 | 0 | VBIAS1 | VBIAS0 |
| 02h | MUX1 | CLKSTAT | 0 | 0 | 0 | 0 | MUXCAL2 | MUXCAL1 | MUXCAL0 |
| 03h | SYS0 | 0 | PGA2 | PGA1 | PGA0 | DR3 | DR2 | DR1 | DR0 |
| 04h | OFC0 | OFC7 | OFC6 | OFC5 | OFC4 | OFC3 | OFC2 | OFC1 | OFC0 |
| 05h | OFC1 | OFC15 | OFC14 | OFC13 | OFC12 | OFC11 | OFC10 | OFC9 | OFC8 |
| 06h | OFC2 | OFC23 | OFC22 | OFC21 | OFC20 | OFC19 | OFC18 | OFC17 | OFC16 |
| 07h | FSC0 | FSC7 | FSC6 | FSC5 | FSC4 | FSC3 | FSC2 | FSC1 | FSC0 |
| 08h | FSC1 | FSC15 | FSC14 | FSC13 | FSC12 | FSC11 | FSC10 | FSC9 | FSC8 |
| 09h | FSC2 | FSC23 | FSC22 | FSC21 | FSC20 | FSC19 | FSC18 | FSC17 | FSC16 |
| 0Ah | ID | ID3 | ID2 | ID1 | ID0 | DRDY MODE | 0 | 0 | 0 |

ADS1146 DETAILED REGISTER DEFINITIONS

BCS—Burnout Current Source Register. These bits control the settling of the sensor burnout detect current source.

| BCS - ADDRESS 00h | | | | | | | RESET VALUE = 01h | |
|-------------------|-------|-------|-------|-------|-------|-------|-------------------|--|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| BCS1 | BCS0 | 0 | 0 | 0 | 0 | 0 | 1 | |

Bits[7:6] BCS[1:0]

These bits select the magnitude of the sensor burnout detect current source.

00 = Burnout current source off (default)

01 = Burnout current source on, 0.5 μ A

10 = Burnout current source on, 2 μ A

11 = Burnout current source on, 10 μ A

Bits[5:0] These bits must always be set to '000001'.

ADS1146 DETAILED REGISTER DEFINITIONS (continued)

VBIAS—Bias Voltage Register. This register enables a bias voltage on the analog inputs.

| VBIAS - ADDRESS 01h | | | | | | | RESET VALUE = 00h | |
|---------------------|-------|-------|-------|-------|-------|--------|-------------------|--|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | VBIAS1 | VBIAS0 | |

Bits[7:2] These bits must always be set to '000000'.

Bits[1:0] **VBIAS[1:0]**

These bits apply a bias voltage of midsupply $(AVDD + AVSS)/2$ to the selected analog input. Bit 0 is for AIN0, and bit 1 is for AIN1.

0 = Bias voltage not enabled (default)

1 = Bias voltage is applied to the analog input

MUX—Multiplexer Control Register.

| MUX - ADDRESS 02h | | | | | | | RESET VALUE = x0h | |
|-------------------|-------|-------|-------|-------|---------|---------|-------------------|--|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| CLKSTAT | 0 | 0 | 0 | 0 | MUXCAL2 | MUXCAL1 | MUXCAL0 | |

Bit 7 **CLKSTAT**

This bit is read-only and indicates whether the internal or external oscillator is being used.

0 = Internal oscillator in use

1 = External oscillator in use

Bits[6:3] These bits must always be set to '0000'.

Bits[2:0] **MUXCAL[2:0]**

These bits are used to select a system monitor. The MUXCAL selection supercedes selections from the VBIAS register.

000 = Normal operation (default)

001 = Offset calibration. The analog inputs are disconnected and AINP and AINN are internally connected to midsupply $(AVDD + AVSS)/2$.

010 = Gain calibration. The analog inputs are connected to the voltage reference.

011 = Temperature measurement. The inputs are connected to a diode circuit that produces a voltage proportional to the ambient temperature of the device.

Table 15 lists the ADC input connection and PGA settings for each MUXCAL setting. The PGA setting reverts to the original SYS0 register setting when MUXCAL is taken back to normal operation or offset measurement.

Table 15. MUXCAL Settings

| MUXCAL[2:0] | PGA GAIN SETTING | ADC INPUT |
|-------------|----------------------|---|
| 000 | Set by SYS0 register | Normal operation |
| 001 | Set by SYS0 register | Offset calibration: inputs shorted to midsupply $(AVDD + AVSS)/2$ |
| 010 | Forced to 1 | Gain calibration: $V_{REFP} - V_{REFN}$ (full-scale) |
| 011 | Forced to 1 | Temperature measurement diode |

ADS1146 DETAILED REGISTER DEFINITIONS (continued)
SYS0—System Control Register 0.

| SYS0 - ADDRESS 03h | | | | | | | RESET VALUE = 00h |
|--------------------|-------|-------|-------|-------|-------|-------|-------------------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| 0 | PGA2 | PGA1 | PGA0 | DOR3 | DOR2 | DOR1 | DOR0 |

Bit 7 These bits must always be set to '0'.

Bits[6:4] PGA[2:0]

These bits determine the gain of the PGA.

000 = 1 (default)

001 = 2

010 = 4

011 = 8

100 = 16

101 = 32

110 = 64

111 = 128

Bits[3:0] DOR[3:0]

These bits select the output data rate of the ADC. Bits with a value higher than 1001 select the highest data rate of 2000SPS.

0000 = 5SPS (default)

0001 = 10SPS

0010 = 20SPS

0011 = 40SPS

0100 = 80SPS

0101 = 160SPS

0110 = 320SPS

0111 = 640SPS

1000 = 1000SPS

1001 to 1111 = 2000SPS

OFC[23:0]

These bits make up the offset calibration coefficient register of the ADS1148.

OFC0—Offset Calibration Coefficient Register 0

| OFC0 - ADDRESS 04h | | | | | | | RESET VALUE = 00h |
|--------------------|-------|-------|-------|-------|-------|-------|-------------------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| OFC7 | OFC6 | OFC5 | OFC4 | OFC3 | OFC2 | OFC1 | OFC0 |

OFC1—Offset Calibration Coefficient Register 1

| OFC1 - ADDRESS 05h | | | | | | | RESET VALUE = 00h |
|--------------------|-------|-------|-------|-------|-------|-------|-------------------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| OFC15 | OFC14 | OFC13 | OFC12 | OFC11 | OFC10 | OFC9 | OFC8 |

OFC2—Offset Calibration Coefficient Register 2

| OFC2 - ADDRESS 06h | | | | | | | RESET VALUE = 00h |
|--------------------|-------|-------|-------|-------|-------|-------|-------------------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| OFC23 | OFC22 | OFC21 | OFC20 | OFC19 | OFC18 | OFC17 | OFC16 |

ADS1146 DETAILED REGISTER DEFINITIONS (continued)

FSC[23:0]

These bits make up the full-scale calibration coefficient register.

FSC0—Full-Scale Calibration Coefficient Register 0

| FSC0 - ADDRESS 07h | | | | | RESET VALUE IS PGA DEPENDENT ⁽¹⁾ | | |
|--------------------|-------|-------|-------|-------|---|-------|-------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| FSC7 | FSC6 | FSC5 | FSC4 | FSC3 | FSC2 | FSC1 | FSC0 |

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note that the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

FSC1—Full-Scale Calibration Coefficient Register 1

| FSC1 - ADDRESS 08h | | | | | RESET VALUE IS PGA DEPENDENT ⁽¹⁾ | | |
|--------------------|-------|-------|-------|-------|---|-------|-------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| FSC15 | FSC14 | FSC13 | FSC12 | FSC11 | FSC10 | FSC9 | FSC8 |

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note that the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

FSC2—Full-Scale Calibration Coefficient Register 2

| FSC2 - ADDRESS 09h | | | | | RESET VALUE IS PGA DEPENDENT ⁽¹⁾ | | |
|--------------------|-------|-------|-------|-------|---|-------|-------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| FSC23 | FSC22 | FSC21 | FSC20 | FSC19 | FSC18 | FSC17 | FSC16 |

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note that the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

ID—ID Register

| IDAC0 - ADDRESS 0Ah | | | | | RESET VALUE = x0h | | |
|---------------------|-------|-------|-------|-----------|-------------------|-------|-------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| ID3 | ID2 | ID1 | ID0 | DRDY MODE | 0 | 0 | 0 |

Bits 7:4 ID3:0
Read-only, factory-programmed bits; used for revision identification.

Bit 3 DRDY MODE
This bit sets the DOUT/ $\overline{\text{DRDY}}$ pin functionality. In either setting of the DRDY MODE bit, the $\overline{\text{DRDY}}$ pin continues to indicate data ready, active low.
0 = DOUT/ $\overline{\text{DRDY}}$ pin functions only as Data Out (default)
1 = DOUT/ $\overline{\text{DRDY}}$ pin functions both as Data Out and Data Ready, active low

Bits 2:0 These bits must always be set to '000'.

ADS1147 AND ADS1148 REGISTER MAP
Table 16. ADS1147 and ADS1148 Register Map

| ADDRESS | REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---------|----------|---------|----------|----------|----------|--------------|---------|---------|---------|
| 00h | MUX0 | BCS1 | BCS0 | MUX_SP2 | MUX_SP1 | MUX_SP0 | MUX_SN2 | MUX_SN1 | MUX_SN0 |
| 01h | VBIAS | VBIAS7 | VBIAS6 | VBIAS5 | VBIAS4 | VBIAS3 | VBIAS2 | VBIAS1 | VBIAS0 |
| 02h | MUX1 | CLKSTAT | VREFCON1 | VREFCON0 | REFSELT1 | REFSELT0 | MUXCAL2 | MUXCAL1 | MUXCAL0 |
| 03h | SYS0 | 0 | PGA2 | PGA1 | PGA0 | DR3 | DR2 | DR1 | DR0 |
| 04h | OFC0 | OFC7 | OFC6 | OFC5 | OFC4 | OFC3 | OFC2 | OFC1 | OFC0 |
| 05h | OFC1 | OFC15 | OFC14 | OFC13 | OFC12 | OFC11 | OFC10 | OFC9 | OFC8 |
| 06h | OFC2 | OFC23 | OFC22 | OFC21 | OFC20 | OFC19 | OFC18 | OFC17 | OFC16 |
| 07h | FSC0 | FSC7 | FSC6 | FSC5 | FSC4 | FSC3 | FSC2 | FSC1 | FSC0 |
| 08h | FSC1 | FSC15 | FSC14 | FSC13 | FSC12 | FSC11 | FSC10 | FSC9 | FSC8 |
| 09h | FSC2 | FSC23 | FSC22 | FSC21 | FSC20 | FSC19 | FSC18 | FSC17 | FSC16 |
| 0Ah | IDAC0 | ID3 | ID2 | ID1 | ID0 | DRDY MODE | IMAG2 | IMAG1 | IMAG0 |
| 0Bh | IDAC1 | I1DIR3 | I1DIR2 | I1DIR1 | I1DIR0 | I2DIR3 | I2DIR2 | I2DIR1 | I2DIR0 |
| 0Ch | GPIOCFG | IOCFG7 | IOCFG6 | IOCFG5 | IOCFG4 | IOCFG3 | IOCFG2 | IOCFG1 | IOCFG0 |
| 0Dh | GPIODIR | IODIR7 | IODIR6 | IODIR5 | IODIR4 | IODIR3 | IODIR2 | IODIR1 | IODIR0 |
| 0Eh | GPIODAT | IODAT7 | IODAT6 | IODAT5 | IODAT4 | IODAT3 | IODAT2 | IODAT1 | IODAT0 |

ADS1147 AND ADS1148 DETAILED REGISTER DEFINITIONS

MUX0—Multiplexer Control Register 0. This register allows any combination of differential inputs to be selected on any of the input channels. Note that this setting can be superseded by the MUXCAL and VBIAS bits.

| MUX0 - ADDRESS 00h | | | | | | | RESET VALUE = 01h | |
|--------------------|-------|---------|---------|---------|---------|---------|-------------------|--|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| BCS1 | BCS0 | MUX_SP2 | MUX_SP1 | MUX_SP0 | MUX_SN2 | MUX_SN1 | MUX_SN0 | |

Bits[7:6] BCS[1:0]

These bits select the magnitude of the sensor detect current source.

- 00 = Burnout current source off (default)
- 01 = Burnout current source on, 0.5µA
- 10 = Burnout current source on, 2µA
- 11 = Burnout current source on, 10µA

Bits[5:3] MUX_SP[2:0]

Positive input channel selection bits.

- 000 = AIN0 (default)
- 001 = AIN1
- 010 = AIN2
- 011 = AIN3
- 100 = AIN4 (ADS1148 only)
- 101 = AIN5 (ADS1148 only)
- 110 = AIN6 (ADS1148 only)
- 111 = AIN7 (ADS1148 only)

Bits[2:0] MUX_SN[2:0]

Negative input channel selection bits.

- 000 = AIN0
- 001 = AIN1 (default)
- 010 = AIN2
- 011 = AIN3
- 100 = AIN4 (ADS1148 only)
- 101 = AIN5 (ADS1148 only)
- 110 = AIN6 (ADS1148 only)
- 111 = AIN7 (ADS1148 only)

VBIAS—Bias Voltage Register

| VBIAS - ADDRESS 01h | | | | | | | RESET VALUE = 00h | |
|---------------------|--------|--------|--------|--------|--------|--------|-------------------|--------|
| DEVICE | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| ADS1148 | VBIAS7 | VBIAS6 | VBIAS5 | VBIAS4 | VBIAS3 | VBIAS2 | VBIAS1 | VBIAS0 |
| ADS1147 | 0 | 0 | 0 | 0 | VBIAS3 | VBIAS2 | VBIAS1 | VBIAS0 |

Bits[7:0] VBIAS[7:0]

These bits apply a bias voltage of midsupply (AVDD + AVSS)/2 to the selected analog input.

- 0 = Bias voltage not enabled (default)
- 1 = Bias voltage is applied on the corresponding analog input (bit 0 corresponds to AIN0, etc.).

ADS1147 AND ADS1148 DETAILED REGISTER DEFINITIONS (continued)
MUX1—Multiplexer Control Register 1

| MUX1 - ADDRESS 02h | | | | | | | RESET VALUE = 00h |
|--------------------|----------|----------|----------|----------|---------|---------|-------------------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| CLKSTAT | VREFCON1 | VREFCON0 | REFSELT1 | REFSELT0 | MUXCAL2 | MUXCAL1 | MUXCAL0 |

Bit 7 CLKSTAT

This bit is read-only and indicates whether the internal or external oscillator is being used.

0 = Internal oscillator in use

1 = External oscillator in use

Bits[6:5] VREFCON[1:0]

These bits control the internal voltage reference. These bits allow the reference to be turned on or off completely, or allow the reference state to follow the state of the device. Note that the internal reference is required for operation of the IDAC functions.

00 = Internal reference is always off (default)

01 = Internal reference is always on

10 or 11 = Internal reference is on when a conversion is in progress and shuts down when the device receives a shutdown opcode or the START pin is taken low

Bits[4:3] REFSELT[1:0]

These bits select the reference input for the ADC.

00 = REF0 input pair selected (default)

01 = REF1 input pair selected (ADS1148 only)

10 = Onboard reference selected

11 = Onboard reference selected and internally connected to REF0 input pair

Bits[2:0] MUXCAL[2:0]

These bits are used to select a system monitor. The MUXCAL selection supercedes selections from registers MUX0 and MUX1 (MUX_SP, MUX_SN, and VBIAS).

000 = Normal operation (default)

001 = Offset measurement

010 = Gain measurement

011 = Temperature diode

100 = External REF1 measurement (ADS1148 only)

101 = External REF0 measurement

110 = AVDD measurement

111 = DVDD measurement

[Table 17](#) provides the ADC input connection and PGA settings for each MUXCAL setting. The PGA setting reverts to the original SYS0 register setting when MUXCAL is taken back to normal operation or offset measurement.

Table 17. MUXCAL Settings

| MUXCAL[2:0] | PGA GAIN SETTING | ADC INPUT |
|-------------|----------------------|---|
| 000 | Set by SYS0 register | Normal operation |
| 001 | Set by SYS0 register | Inputs shorted to midsupply (AVDD + AVSS)/2 |
| 010 | Forced to 1 | $V_{REFP} - V_{REFN}$ (full-scale) |
| 011 | Forced to 1 | Temperature measurement diode |
| 100 | Forced to 1 | $(V_{REFP1} - V_{REFN1})/4$ |
| 101 | Forced to 1 | $(V_{REFP0} - V_{REFN0})/4$ |
| 110 | Forced to 1 | $(AVDD - AVSS)/4$ |
| 111 | Forced to 1 | $(DVDD - DVSS)/4$ |

ADS1147 AND ADS1148 DETAILED REGISTER DEFINITIONS (continued)

SYS0—System Control Register 0

| SYS0 - ADDRESS 03h | | | | | | | RESET VALUE = 00h |
|--------------------|-------|-------|-------|-------|-------|-------|-------------------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| 0 | PGA2 | PGA1 | PGA0 | DOR3 | DOR2 | DOR1 | DOR0 |

Bit 7 This bit must always be set to '0'

Bits[6:4] PGA[2:0]

These bits determine the gain of the PGA.

000 = 1 (default)

001 = 2

010 = 4

011 = 8

100 = 16

101 = 32

110 = 64

111 = 128

Bits[3:0] DOR[3:0]

These bits select the output data rate of the ADC. Bits with a value higher than 1001 select the highest data rate of 2000SPS.

0000 = 5SPS (default)

0001 = 10SPS

0010 = 20SPS

0011 = 40SPS

0100 = 80SPS

0101 = 160SPS

0110 = 320SPS

0111 = 640SPS

1000 = 1000SPS

1001 to 1111 = 2000SPS

OFC[23:0]

These bits make up the offset calibration coefficient register of the ADS1148.

OFC0—Offset Calibration Coefficient Register 0

| OFC0 - ADDRESS 04h | | | | | | | RESET VALUE = 000000h |
|--------------------|-------|-------|-------|-------|-------|-------|-----------------------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| OFC7 | OFC6 | OFC5 | OFC4 | OFC3 | OFC2 | OFC1 | OFC0 |

OFC1—Offset Calibration Coefficient Register 1

| OFC1 - ADDRESS 05h | | | | | | | RESET VALUE = 000000h |
|--------------------|-------|-------|-------|-------|-------|-------|-----------------------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| OFC15 | OFC14 | OFC13 | OFC12 | OFC11 | OFC10 | OFC9 | OFC8 |

OFC2—Offset Calibration Coefficient Register 2

| OFC2 - ADDRESS 06h | | | | | | | RESET VALUE = 000000h |
|--------------------|-------|-------|-------|-------|-------|-------|-----------------------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| OFC23 | OFC22 | OFC21 | OFC20 | OFC19 | OFC18 | OFC17 | OFC16 |

ADS1147 AND ADS1148 DETAILED REGISTER DEFINITIONS (continued)
FSC[23:0]

These bits make up the full-scale calibration coefficient register.

FSC0—Full-Scale Calibration Coefficient Register 0

| FSC0 - ADDRESS 07h | | | | | RESET VALUE IS PGA DEPENDENT ⁽¹⁾ | | |
|--------------------|-------|-------|-------|-------|---|-------|-------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| FSC7 | FSC6 | FSC5 | FSC4 | FSC3 | FSC2 | FSC1 | FSC0 |

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note that the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

FSC1—Full-Scale Calibration Coefficient Register 1

| FSC1 - ADDRESS 08h | | | | | RESET VALUE IS PGA DEPENDENT ⁽¹⁾ | | |
|--------------------|-------|-------|-------|-------|---|-------|-------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| FSC15 | FSC14 | FSC13 | FSC12 | FSC11 | FSC10 | FSC9 | FSC8 |

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note that the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

FSC2—Full-Scale Calibration Coefficient Register 2

| FSC2 - ADDRESS 09h | | | | | RESET VALUE IS PGA DEPENDENT ⁽¹⁾ | | |
|--------------------|-------|-------|-------|-------|---|-------|-------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| FSC23 | FSC22 | FSC21 | FSC20 | FSC19 | FSC18 | FSC17 | FSC16 |

(1) The reset value for FSC is factory-trimmed for each PGA setting. Note that the factory-trimmed FSC reset value is automatically loaded whenever the PGA setting is changed.

IDAC0—IDAC Control Register 0

| IDAC0 - ADDRESS 0Ah | | | | | RESET VALUE = x0h | | |
|---------------------|-------|-------|-------|-----------|-------------------|-------|-------|
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| ID3 | ID2 | ID1 | ID0 | DRDY MODE | IMAG2 | IMAG1 | IMAG0 |

Bits[7:4] ID[3:0]

Read-only, factory-programmed bits; used for revision identification.

Bit 3 DRDY MODE

This bit sets the DOUT/ $\overline{\text{DRDY}}$ pin functionality. In either setting of the DRDY MODE bit, the $\overline{\text{DRDY}}$ pin continues to indicate data ready, active low.

0 = DOUT/ $\overline{\text{DRDY}}$ pin functions only as Data Out (default)

1 = DOUT/ $\overline{\text{DRDY}}$ pin functions both as Data Out and Data Ready, active low

Bits[2:0] IMAG[2:0]

The ADS1147 and ADS1148 have two programmable current source DACs that can be used for sensor excitation. The IMAG bits control the magnitude of the excitation current. The IDACs require the internal reference to be on.

000 = off (default)

001 = 50 μ A

010 = 100 μ A

011 = 250 μ A

100 = 500 μ A

101 = 750 μ A

110 = 1000 μ A

111 = 1500 μ A

ADS1147 AND ADS1148 DETAILED REGISTER DEFINITIONS (continued)

IDAC1—IDAC Control Register 1

| IDAC1 - ADDRESS 0Bh | | | | | | | RESET VALUE = FFh | |
|---------------------|--------|--------|--------|--------|--------|--------|-------------------|--------|
| DEVICE | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| ADS1148 | I1DIR3 | I1DIR2 | I1DIR1 | I1DIR0 | I2DIR3 | I2DIR2 | I2DIR1 | I2DIR0 |
| ADS1147 | 0 | 0 | I1DIR1 | I1DIR0 | 0 | 0 | I2DIR1 | I2DIR0 |

The two IDACs on the ADS1147 and ADS1148 can be routed to either the IEXC1 and IEXC2 output pins or directly to the analog inputs.

Bits[7:4] I1DIR[3:0]

These bits select the output pin for the first current source DAC.

- 0000 = AIN0
- 0001 = AIN1
- 0010 = AIN2
- 0011 = AIN3
- 0100 = AIN4 (ADS1148 only)
- 0101 = AIN5 (ADS1148 only)
- 0110 = AIN6 (ADS1148 only)
- 0111 = AIN7 (ADS1148 only)
- 10x0 = IEXT1 (ADS1148 only)
- 10x1 = IEXT2 (ADS1148 only)
- 11xx = Disconnected (default)

Bits[3:0] I2DIR[3:0]

These bits select the output pin for the second current source DAC.

- 0000 = AIN0
- 0001 = AIN1
- 0010 = AIN2
- 0011 = AIN3
- 0100 = AIN4 (ADS1148 only)
- 0101 = AIN5 (ADS1148 only)
- 0110 = AIN6 (ADS1148 only)
- 0111 = AIN7 (ADS1148 only)
- 10x0 = IEXT1 (ADS1148 only)
- 10x1 = IEXT2 (ADS1148 only)
- 11xx = Disconnected (default)

ADS1147 AND ADS1148 DETAILED REGISTER DEFINITIONS (continued)

GPIOCFG—GPIO Configuration Register. The GPIO and analog pins are shared as follows:

- GPIO0 shared with REFP0
- GPIO1 shared with REFN0
- GPIO2 shared with AIN2
- GPIO3 shared with AIN3
- GPIO4 shared with AIN4 (ADS1148)
- GPIO5 shared with AIN5 (ADS1148)
- GPIO6 shared with AIN6 (ADS1148)
- GPIO7 shared with AIN7 (ADS1148)

| GPIOCFG - ADDRESS 0Ch | | | | | | | | RESET VALUE = 00h |
|-----------------------|--------|--------|--------|--------|--------|--------|--------|-------------------|
| DEVICE | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| ADS1148 | IOCFG7 | IOCFG6 | IOCFG5 | IOCFG4 | IOCFG3 | IOCFG2 | IOCFG1 | IOCFG0 |
| ADS1147 | 0 | 0 | 0 | 0 | IOCFG3 | IOCFG2 | IOCFG1 | IOCFG0 |

Bits[7:0] IOCFG[7:0]

These bits enable the GPIO because the GPIO pins are shared with the analog pins. Note that the ADS1148 uses all the IOCFG bits, whereas the ADS1147 uses only bits 3:0.

- 0 = The pin is used as an analog input (default)
- 1 = The pin is used as a GPIO pin

GPIODIR—GPIO Direction Register

| GPIODIR - ADDRESS 0Dh | | | | | | | | RESET VALUE = 00h |
|-----------------------|--------|--------|--------|--------|--------|--------|--------|-------------------|
| DEVICE | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| ADS1148 | IODIR7 | IODIR6 | IODIR5 | IODIR4 | IODIR3 | IODIR2 | IODIR1 | IODIR0 |
| ADS1147 | 0 | 0 | 0 | 0 | IODIR3 | IODIR2 | IODIR1 | IODIR0 |

Bits[7:0] IODIR[7:0]

These bits control the direction of the GPIO when enabled by the IOCFG bits. Note that the ADS1148 uses all the IODIR bits, whereas the ADS1147 uses only bits 3:0.

- 0 = The GPIO is an output (default)
- 1 = The GPIO is an input

GPIODAT—GPIO Data Register

| GPIODAT - ADDRESS 0Eh | | | | | | | | RESET VALUE = 00h |
|-----------------------|--------|--------|--------|--------|--------|--------|--------|-------------------|
| DEVICE | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| ADS1148 | IODAT7 | IODAT6 | IODAT5 | IODAT4 | IODAT3 | IODAT2 | IODAT1 | IODAT0 |
| ADS1147 | 0 | 0 | 0 | 0 | IODAT3 | IODAT2 | IODAT1 | IODAT0 |

Bits[7:0] IODAT[7:0]

If a GPIO pin is enabled in the GPIOCFG register and configured as an output in the GPIO Direction register (GPIODIR), the value written to this register appears on the appropriate GPIO pin. If a GPIO pin is configured as an input in GPIODIR, reading this register returns the value of the digital I/O pins. Note that the ADS1148 uses all eight IODAT bits, while the ADS1147 uses only bits 3:0.

SPI COMMANDS

SPI COMMAND DEFINITIONS

The commands shown in [Table 18](#) control the operation of the ADS1146/7/8. Some of the commands are stand-alone commands (for example, RESET), whereas others require additional bytes (for example, WREG requires command, count, and the data bytes).

Operands:

n = number of registers to be read or written (number of bytes – 1)

r = register (0 to 15)

x = don't care

Table 18. SPI Commands

| COMMAND TYPE | COMMAND | DESCRIPTION | 1st COMMAND BYTE | 2nd COMMAND BYTE |
|----------------|----------|--|------------------------|--------------------|
| System Control | WAKEUP | Exit sleep mode | 0000 000x (00h, 01h) | |
| | SLEEP | Enter sleep mode | 0000 001x (02h, 03h) | |
| | SYNC | Synchronize the A/D conversion | 0000 010x (04h, 05h) | 0000-010x (04,05h) |
| | RESET | Reset to power-up values | 0000 011x (06h, 07h) | |
| | NOP | No operation | 1111 1111 (FFh) | |
| Data Read | RDATA | Read data once | 0001 001x (12h, 13h) | |
| | RDATAc | Read data continuously | 0001 010x (14h, 15h) | |
| | SDATAc | Stop reading data continuously | 0001 011x (16h, 17h) | |
| Read Register | RREG | Read from register <i>rrrr</i> | 0010 <i>rrrr</i> (2xh) | 0000_ <i>nnnn</i> |
| Write Register | WREG | Write to register <i>rrrr</i> | 0100 <i>rrrr</i> (4xh) | 0000_ <i>nnnn</i> |
| Calibration | YSOCAL | System offset calibration | 0110 0000 (60h) | |
| | YSGCAL | System gain calibration | 0110 0001 (61h) | |
| | SELFOCAL | Self offset calibration | 0110 0010 (62h) | |
| Restricted | | Restricted command. Should never be sent to device. | 1111 0001 (F1h) | |

SYSTEM CONTROL COMMANDS

WAKEUP—Wake up from sleep mode that is set by the SLEEP command.

Use this command to awaken the device from sleep mode. After execution of the WAKEUP command, the device wakes up on the rising edge of the eighth SCLK.

SLEEP—Set the device to sleep mode; issue the WAKEUP command to deactivate SLEEP mode.

This command places the part into a sleep (power-saving) mode. When the SLEEP command is issued, the device completes the current conversion and then goes into sleep mode. Note that this command does not automatically power-down the internal voltage reference; see the VREFCON bits in the MUX1 register for each device for further details.

To exit sleep mode, issue the WAKEUP command. Single conversions can be performed by issuing a WAKEUP command followed by a SLEEP command.

Both WAKEUP and SLEEP are the software command equivalents of using the START pin to control the device.

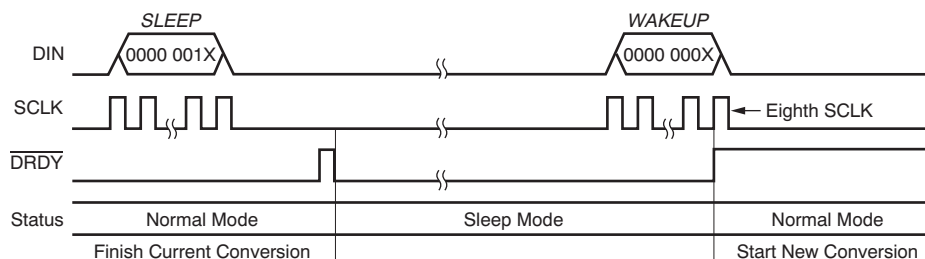


Figure 41. SLEEP and WAKEUP Commands Operation

SYNC—Synchronize $\overline{\text{DRDY}}$.

This command resets the ADC digital filter and starts a new conversion. The $\overline{\text{DRDY}}$ pin from multiple devices connected to the same SPI bus can be synchronized by issuing a SYNC command to all of devices simultaneously.

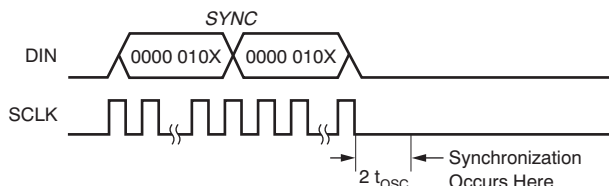


Figure 42. SYNC Command Operation

RESET—Reset the device to power-up state.

This command restores the registers to the respective power-up values. This command also resets the digital filter. RESET is the command equivalent of using the RESET pin to reset the device. However, the RESET command does not reset the SPI interface. If the RESET command is issued when the SPI interface is in the wrong state, the device will not reset. The CS pin can be used to reset SPI interface first, and then a RESET command can be issued to reset the device. The RESET command holds the registers and the decimation filter in a reset state for 0.6ms when the system clock frequency is 4.096MHz, similar to the hardware reset. Therefore, SPI communication can be only be started 0.6ms after the RESET command is issued, as shown in Figure 43.

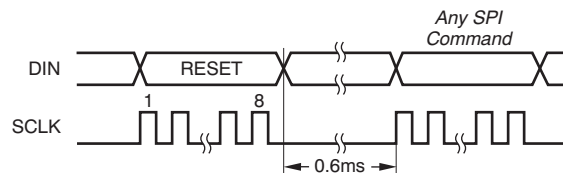


Figure 43. SPI Communication After an SPI Reset

DATA RETRIEVAL COMMANDS

RDATAAC—Read data continuously.

The RDATAAC command enables the automatic loading of a new conversion result into the output data register. In this mode, the conversion result can be received once from the device after the $\overline{\text{DRDY}}$ signal goes low by sending 16 SCLKs. It is not necessary to read back all the bits, as long as the number of bits read out is a multiple of eight. The RDATAAC command must be issued after $\overline{\text{DRDY}}$ goes low, and the command takes effect on the next $\overline{\text{DRDY}}$.

Be sure to complete data retrieval (conversion result or register read-back) before $\overline{\text{DRDY}}$ goes low, or the resulting data will be corrupt. Successful register read operations in RDATAAC mode require the knowledge of when the next $\overline{\text{DRDY}}$ falling edge will occur.

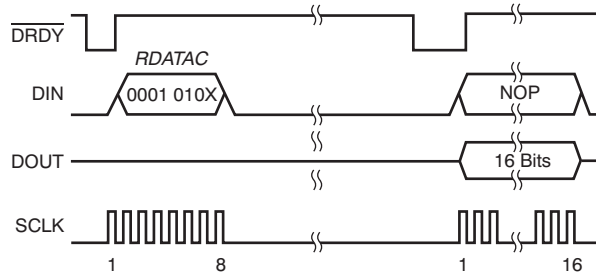


Figure 44. Read Data Continuously

SDATAC—Stop reading data continuously.

The SDATAC command terminates the RDATAAC mode. Afterwards, the conversion result is not automatically loaded into the output shift register when $\overline{\text{DRDY}}$ goes low, and register read operations can be performed without interruption from new conversion results being loaded into the output shift register. Use the RDATA command to retrieve conversion data. The SDATAC command takes effect after the next $\overline{\text{DRDY}}$.

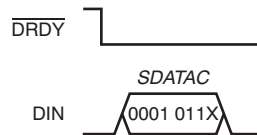


Figure 45. Stop Reading Data Continuously

RDATA—Read data once.

The RDATA command loads the most recent conversion result into the output register. After issuing this command, the conversion result can be read out by sending 16 SCLKs, as shown in Figure 46. This command also works in RDATA mode.

When performing multiple reads of the conversion result, the RDATA command can be sent when the last eight bits of the conversion result are being shifted out during the course of the first read operation by taking advantage of the duplex communication nature of the SPI interface, as shown in Figure 47.

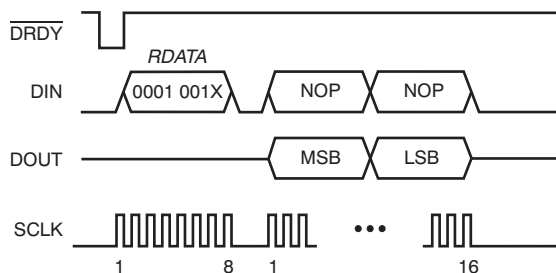


Figure 46. Read Data Once

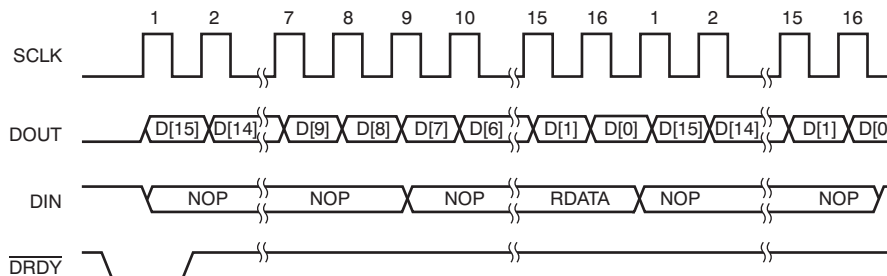


Figure 47. Using RDATA in Full-Duplex Mode

USER REGISTER READ AND WRITE COMMANDS

RREG—Read from registers.

This command outputs the data from up to 16 registers, starting with the register address specified as part of the instruction. The number of registers read is one plus the second byte. If the count exceeds the remaining registers, the addresses wrap back to the beginning.

1st Command Byte: 0010 *rrrr*, where *rrrr* is the address of the first register to read.

2nd Command Byte: 0000 *nnnn*, where *nnnn* is the number of bytes to read – 1.

It is not possible to use the full-duplex nature of the SPI interface when reading out the register data. For example, a SYNC command cannot be issued when reading out the VBIAS and MUX1 data, as shown in [Figure 48](#). Any command sent during the readout of the register data is ignored. Thus, it is advisable to send NOP through the DIN when reading out the register data.

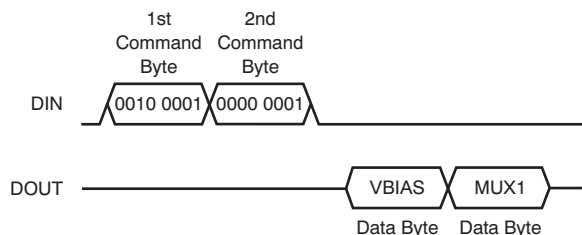


Figure 48. Read from Register

WREG—Write to registers.

This command writes to the registers, starting with the register specified as part of the instruction. The number of registers that are written is one plus the value of the second byte.

1st Command Byte: 0100 *rrrr*, where *rrrr* is the address of the first register to be written.

2nd Command Byte: 0000 *nnnn*, where *nnnn* is the number of bytes to be written – 1.

Data Byte(s): data to be written to the registers.

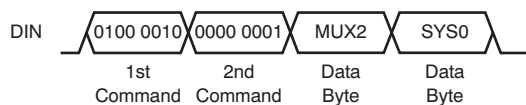


Figure 49. Write to Register

CALIBRATION COMMANDS

The ADS1146/7/8 provide system and offset calibration commands and a system gain calibration command.

SYSOCAL—Offset system calibration.

This command initiates a system offset calibration. For a system offset calibration, the input should be externally set to zero. The OFC register is updated when this operation completes.

SYSGCAL—System gain calibration.

This command initiates the system gain calibration. For a system gain calibration, the input should be set to full-scale. The FSC register is updated after this operation.

SELFOCAL—Self offset calibration.

This command initiates a self-calibration for offset. The device internally shorts the inputs and performs the calibration. The OFC register is updated after this operation.

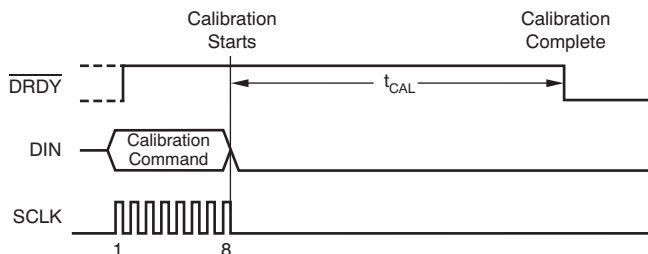


Figure 50. Calibration Command

APPLICATION INFORMATION

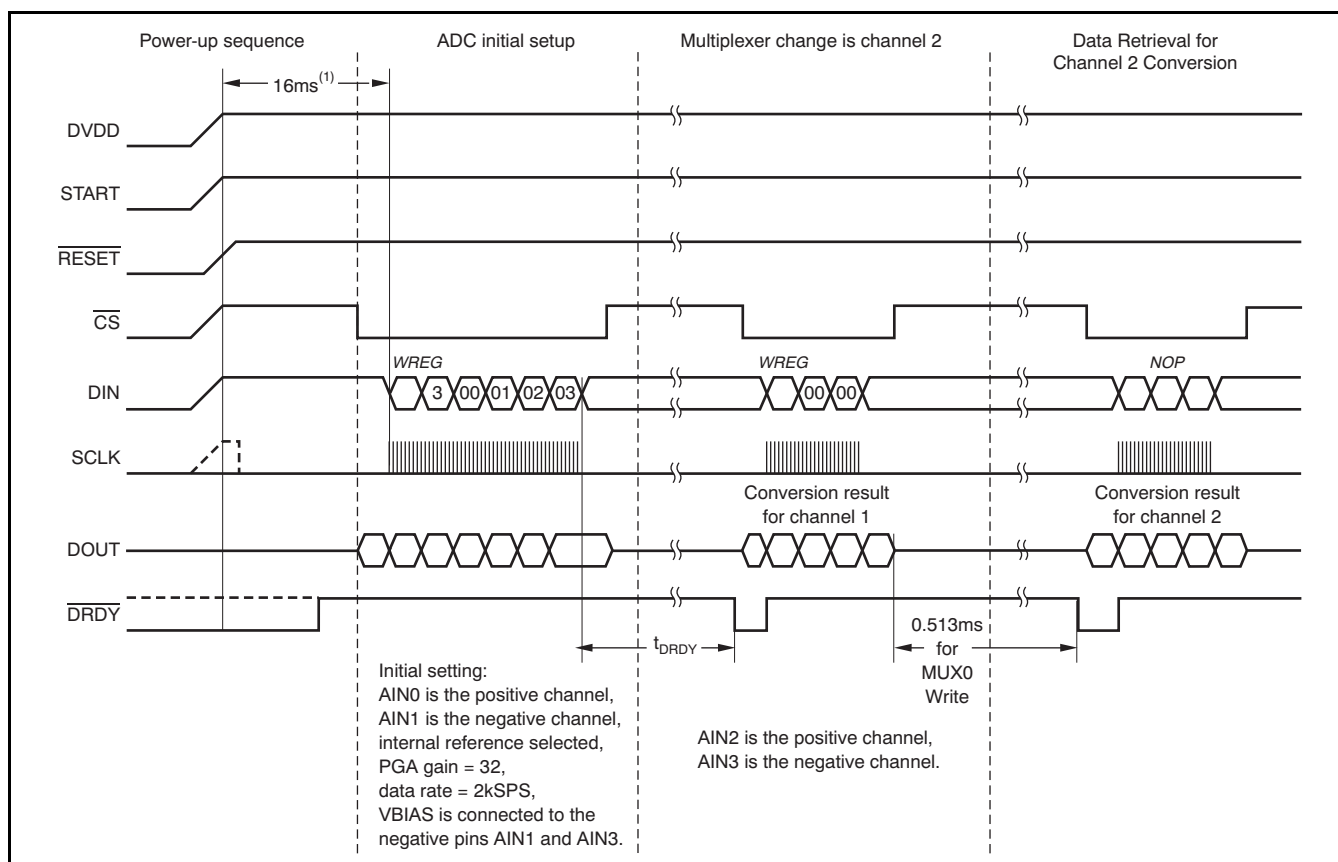
SPI COMMUNICATION EXAMPLES

This section contains several examples of SPI communication with the ADS1146/7/8, including the power-up sequence.

Channel Multiplexing Example

This first example applies only to the ADS1147 and ADS1148. It explains a method to use the device with two sensors connected to two different analog channels. Figure 51 shows the sequence of SPI operations performed on the device. After power-up, 2^{16} system clocks are required before communication may be started. During the first 2^{16} system clock cycles, the devices are internally held in a reset state. In this example, one of the sensors is connected to channels AIN0 and AIN1 and the other sensor is connected to channels AIN2 and AIN3. The ADC is operated at a data rate of 2kSPS. The PGA gain is set to 32 for both sensors. VBIAS is connected to the

negative terminal of both sensors (that is, channels AIN1 and AIN3). All these settings can be changed by performing a block write operation on the first four registers of the device. After the DRDY pin goes low, the conversion result can be immediately retrieved by sending in 16 SPI clock pulses because the device defaults to RDATA mode. As the conversion result is being retrieved, the active input channels can be switched to AIN2 and AIN3 by writing into the MUX0 register in a full-duplex manner, as shown in Figure 51. The write operation is completed with an additional eight SPI clock pulses. The time from the write operation into the MUX0 register to the next DRDY low transition is shown in Figure 51 and is 0.513ms in this case. After DRDY goes low, the conversion result can be retrieved and the active channel can be switched as before.



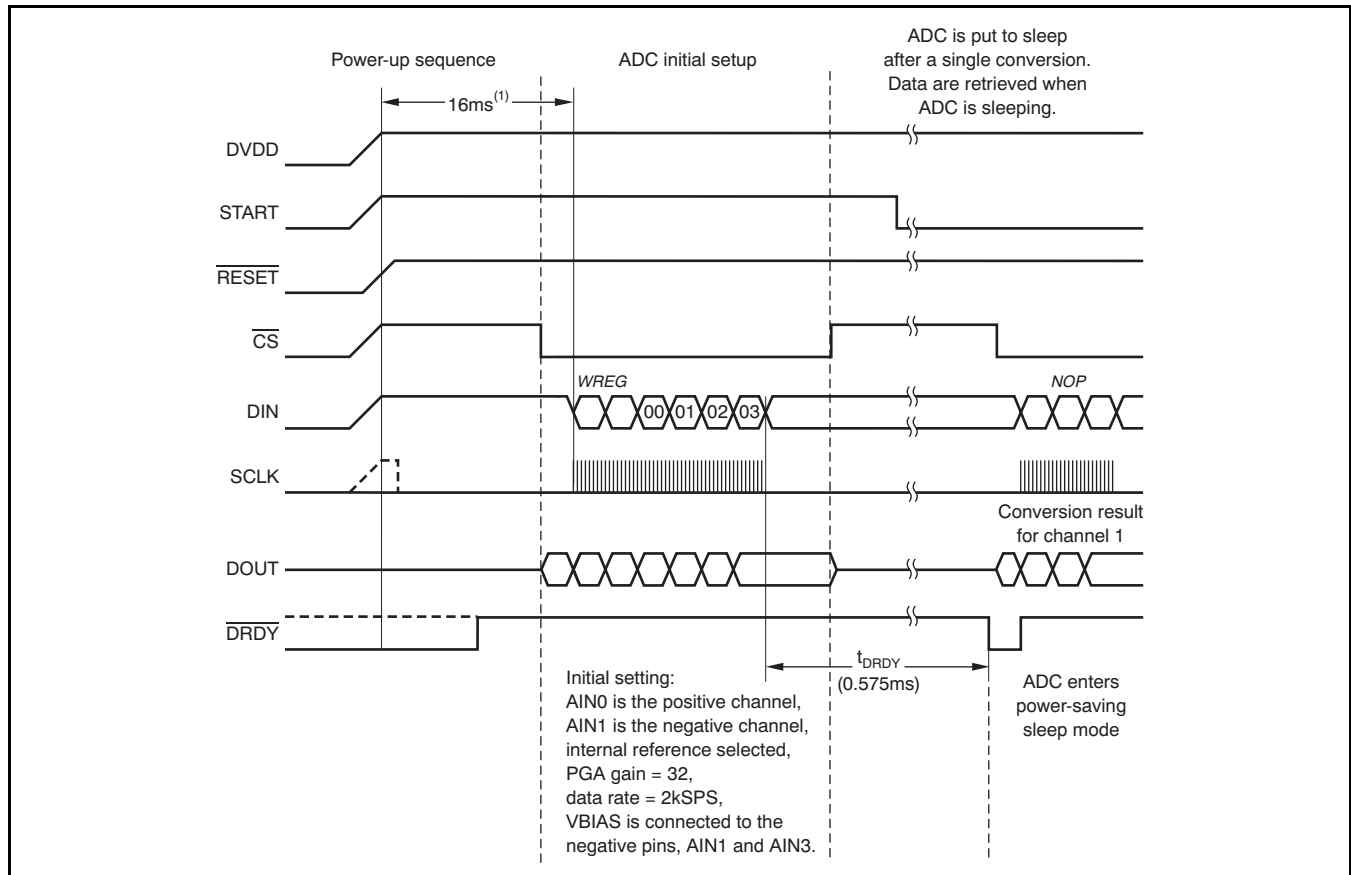
(1) For $f_{OSC} = 4.096\text{MHz}$.

Figure 51. SPI Communication Sequence for Channel Multiplexing

Sleep Mode Example

This second example deals with performing one conversion after power-up and then entering into the power-saving sleep mode. In this example, a sensor is connected to input channels AIN0 and AIN1. Commands to set up the devices must occur at least 2^{16} system clock cycles after powering up the devices. The ADC operates at a data rate of 2kSPS. The PGA gain is set to 32 for both sensors. VBIAS is connected to the negative terminal of both the sensors (that is, channel AIN1). All these settings can

be changed by performing a block write operation on the first four registers of the device. After performing the block write operation, the START pin can be taken low. The device enters the power-saving sleep mode as soon as DRDY goes low 0.575ms after writing into the SYS0 register. The conversion result can be retrieved even after the device enters sleep mode by sending 16 SPI clock pulses.



(1) For $f_{osc} = 4.096\text{MHz}$.

Figure 52. SPI Communication Sequence for Entering Sleep Mode After a Conversion

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (April 2012) to Revision F | Page |
|---|------|
| • Added QFN-32 to listed packages available for the ADS1148 in <i>Description</i> section | 1 |
| • Added ADS1148, QFN-32 row to Package/Ordering Information table | 2 |
| • Corrected ADS1148 Pin Description table name | 11 |

| Changes from Revision D (October 2011) to Revision E | Page |
|--|------|
| • Added RHB pin configuration | 6 |

| Changes from Revision C (April 2001) to Revision D | Page |
|--|------|
| • Added footnote to Analog Inputs, <i>Full-scale input voltage</i> parameter typical specification in Electrical Characteristics table | 3 |
| • Deleted Analog Inputs, <i>Mux leakage current</i> parameter from Electrical Characteristics table | 3 |
| • Updated Figure 1 to show t_{CSPW} timing | 12 |
| • Added t_{CSPW} to Timing Characteristics for Figure 1 | 12 |
| • Changed t_{DTS} minimum specification in Timing Characteristics for Figure 2 | 12 |
| • Added Figure 7 , Figure 8 , Figure 9 , and Figure 10 | 15 |
| • Added Figure 11 , Figure 14 , Figure 15 , and Figure 16 | 16 |
| • Corrected Figure 19 to remove constant short | 18 |
| • Added Table 3 to <i>Analog Input Impedance</i> section | 19 |
| • Corrected Figure 26 and Figure 27 | 21 |
| • Added details to <i>Bias Voltage Generation</i> section | 23 |
| • Added details to <i>Calibration</i> section | 25 |
| • Added Equation 8 to <i>Calibration</i> section | 25 |
| • Added details to <i>Calibration Commands</i> section | 26 |
| • Added <i>Channel Cycling and Overload Recovery</i> section | 28 |
| • Corrected Table 12 | 29 |
| • Added details to <i>Digital Interface</i> section | 30 |
| • Added Restricted command to Table 18 | 44 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| ADS1146IPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ADS1146 | Samples |
| ADS1146IPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ADS1146 | Samples |
| ADS1147IPW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | ADS1147 | Samples |
| ADS1147IPWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | ADS1147 | Samples |
| ADS1148IPW | ACTIVE | TSSOP | PW | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | ADS1148 | Samples |
| ADS1148IPWR | ACTIVE | TSSOP | PW | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | ADS1148 | Samples |
| ADS1148IRHBR | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | ADS 1148 | Samples |
| ADS1148IRHBT | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | ADS 1148 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADS1146IPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ADS1147IPWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| ADS1148IRHBR | QFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| ADS1148IRHBT | QFN | RHB | 32 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADS1146IPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| ADS1147IPWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| ADS1148IRHBR | QFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| ADS1148IRHBT | QFN | RHB | 32 | 250 | 210.0 | 185.0 | 35.0 |

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

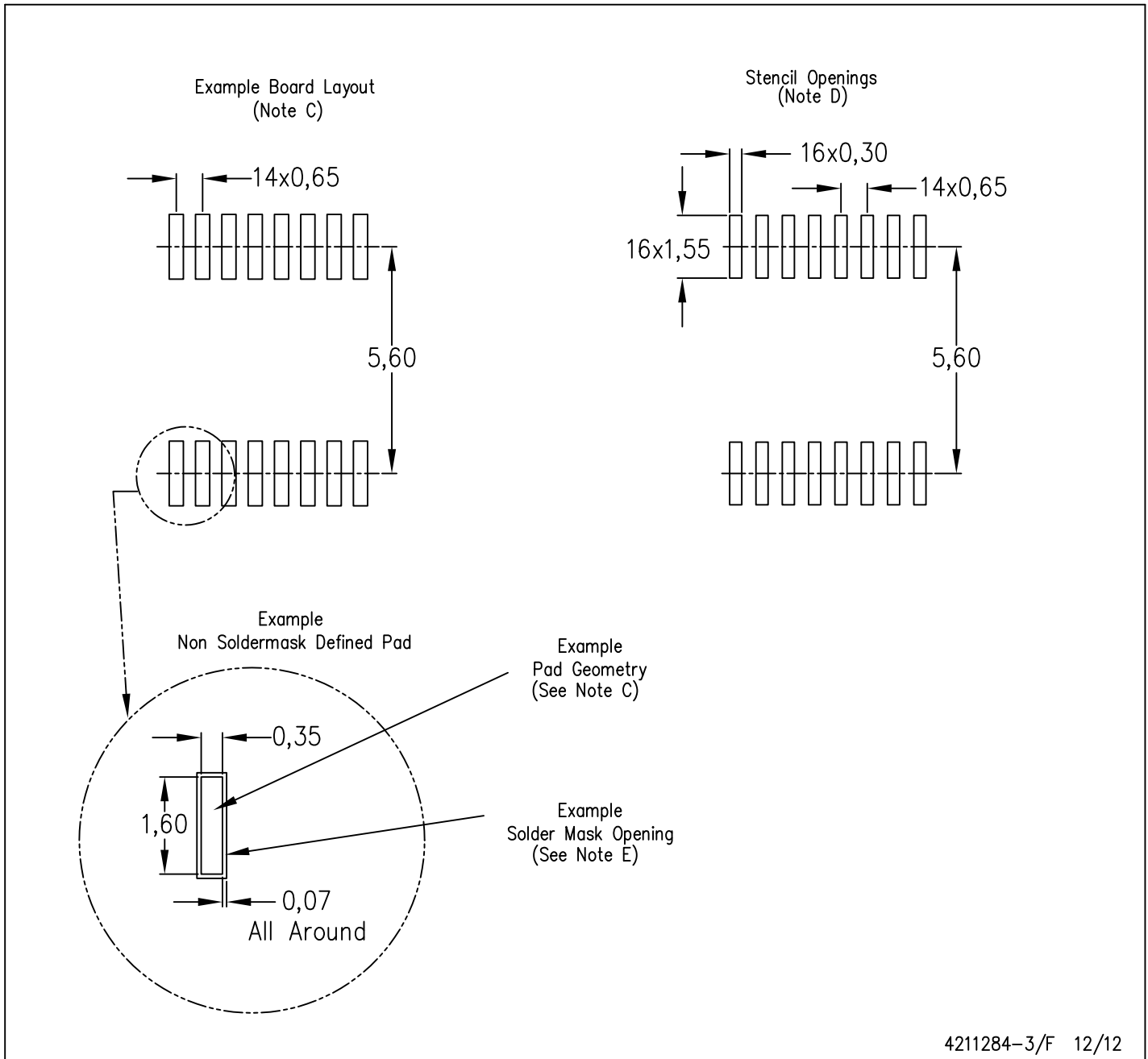


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
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 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

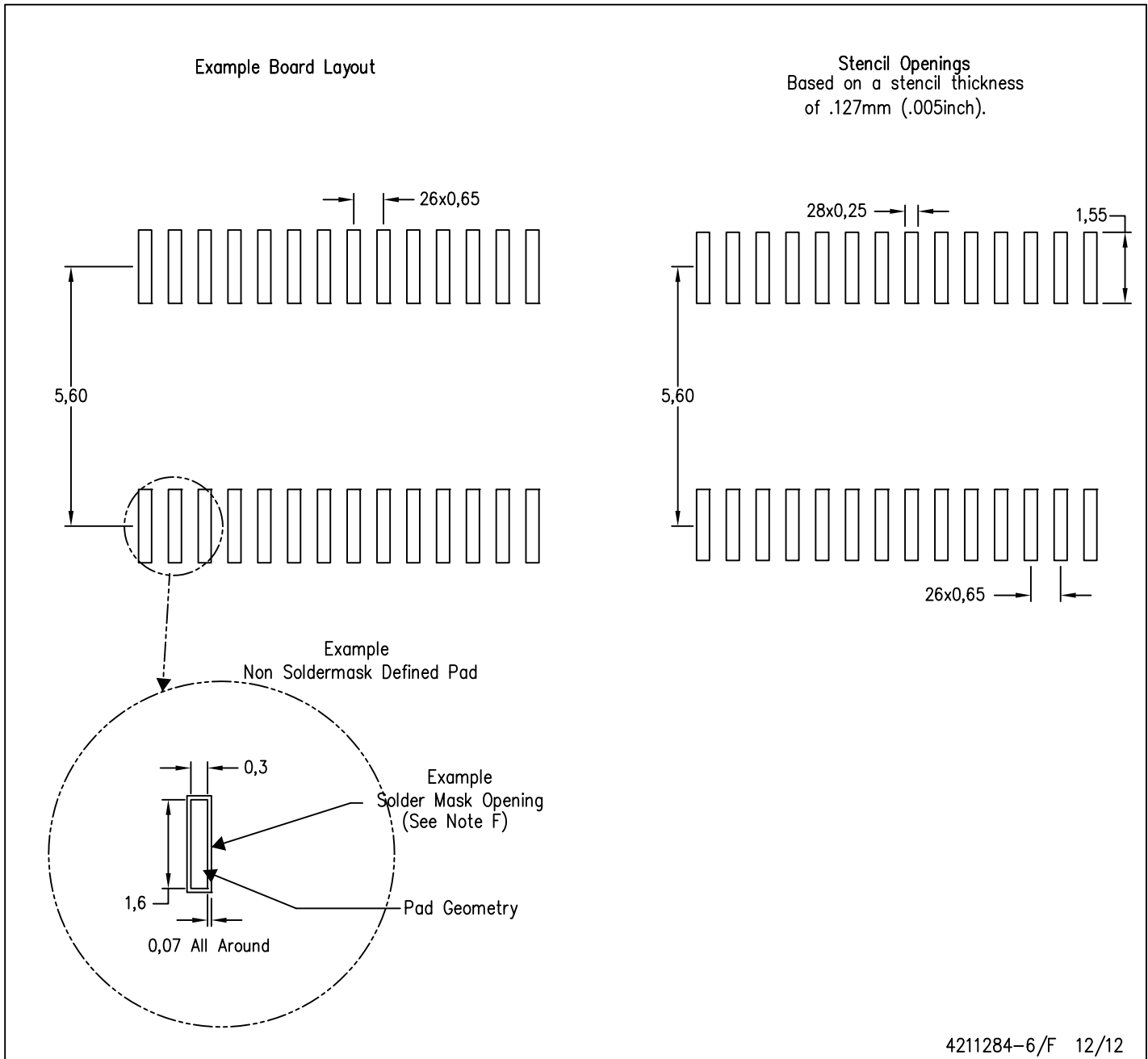


4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

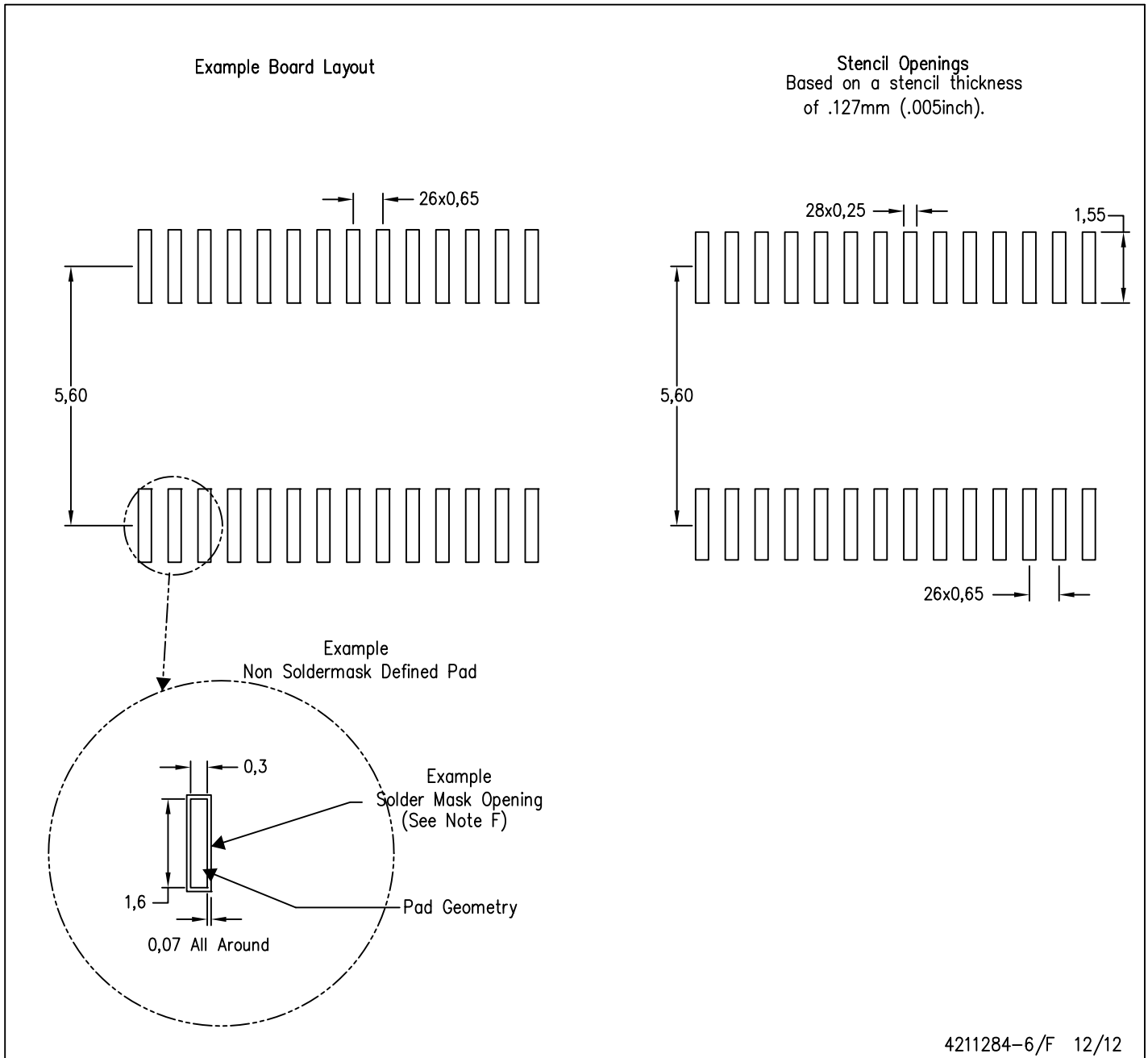
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

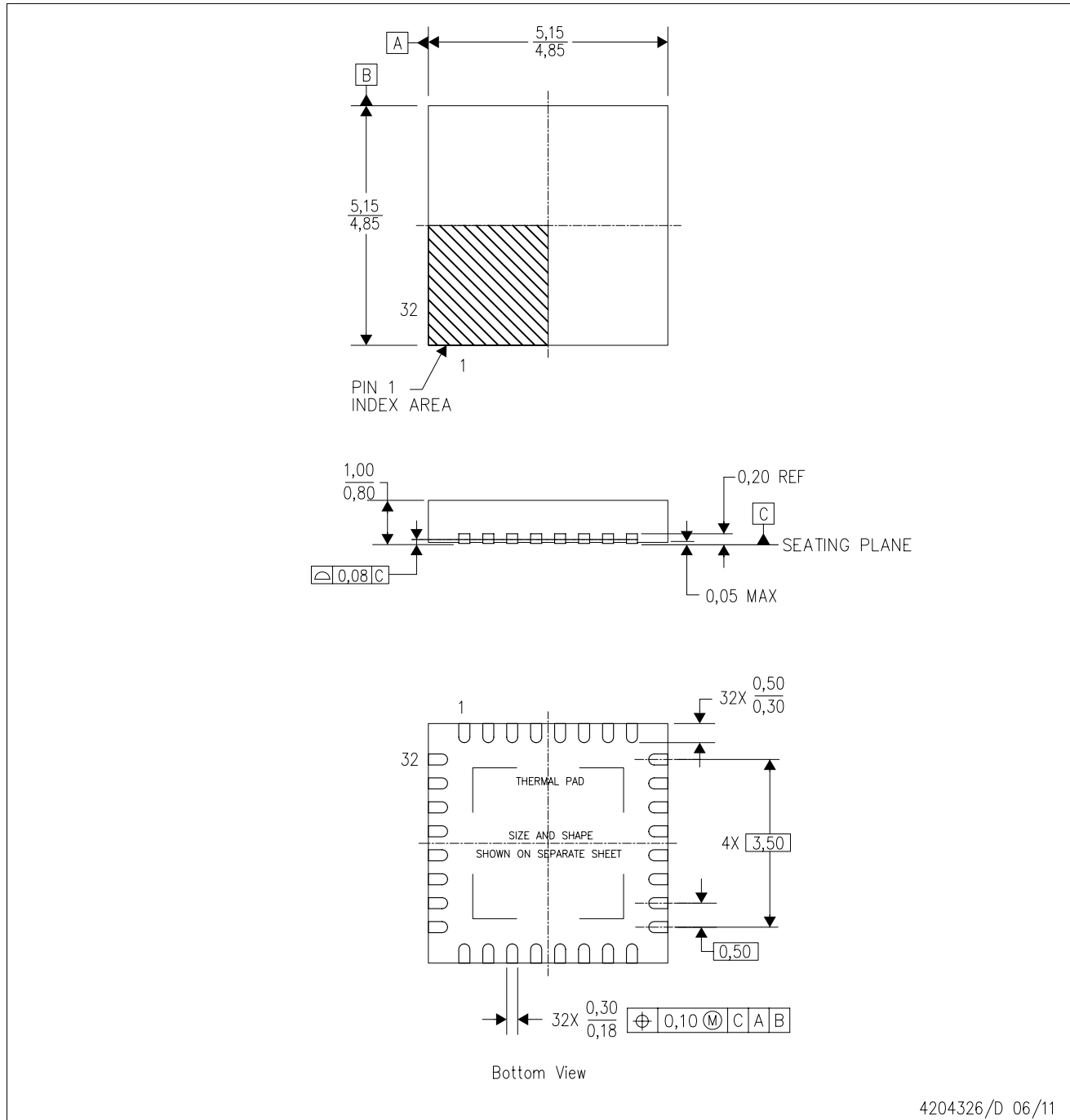


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4204326/D 06/11

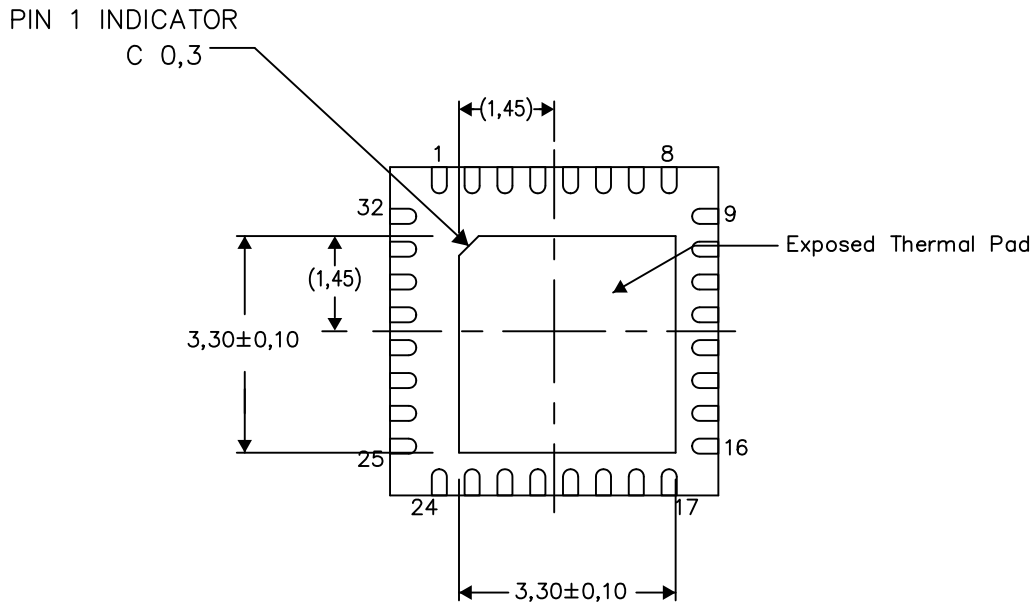
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206356-8/X 12/12

NOTE: A. All linear dimensions are in millimeters

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