Dual-Channel, 14-Bit, 250-MSPS Ultralow-Power ADC with Analog Input Buffer

Check for Samples: ADS42B49

FEATURES

- **Maximum Sample Rate: 250 MSPS**
- **Ultralow Power:**
  - **850-mW Total Power at 250 MSPS**
- **Integrated Analog Input Buffer:**
  - **Input Capacitance: 2.2 pF at 170 MHz**
  - **Input Resistance: 1.1 kΩ at 170 MHz**
- **High Dynamic Performance:**
  - **85-dBc SFDR at 170 MHz**
  - **70.7-dBFS SNR at 170 MHz**
- **Crosstalk: > 85 dB at 185 MHz**
- **Programmable Gain Up to 6 dB for SNR and SFDR Trade-off**
- **DC Offset Correction**
- **Output Interface Options:**
  - **1.8-V Parallel CMOS Interface**
  - **Double Data Rate (DDR) LVDS with Programmable Swing:**
    - **Standard Swing: 350 mV**
    - **Low Swing: 200 mV**
- **Supports Low Input Clock Amplitude Down to 200 mV_{PP}**
- **Package: 9-mm × 9-mm, 64-Pin Quad Flat No-Lead (QFN) Package**

APPLICATIONS

- **Wireless Communications Infrastructure**
- **Software Defined Radio**
- **Power Amplifier Linearization**

DESCRIPTION

The ADS42B49 is an ultralow-power dual-channel, 14-bit analog-to-digital converter (ADC) featuring integrated analog input buffers. It uses innovative design techniques to achieve high dynamic performance, while consuming extremely low power. The presence of analog input buffers makes this device easy to drive and helps achieve high performance over a wide frequency range. The ADS42B49 is well-suited for multi-carrier, wide bandwidth communications applications.

The ADS42B49 has gain options that can be used to improve SFDR performance at lower full-scale input ranges. This device also includes a dc offset correction loop that can be used to cancel the ADC offset. Both DDR LVDS and parallel CMOS digital output interfaces are available in a compact QFN-64 PowerPAD™ package.

The device includes internal references while the traditional reference pins and associated decoupling capacitors have been eliminated. The ADS42B49 is specified over the industrial temperature range (–40°C to +85°C).

ADS424x and ADS422x Family Comparison(1)

	65 MSPS	125 MSPS	160 MSPS	250 MSPS
ADS422x 12-bit family	ADS4222	ADS4225	ADS4226	ADS4229
ADS424x 14-bit family	ADS4242	ADS4245	ADS4246	ADS4249, ADS42B49 (with analog input buffers)

(1) See Table 1 for details on migrating from the ADS62P49 family.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN(2)	LEAD AND BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
ADS42B49	QFN-64	RGC	–40°C to +85°C	GREEN (RoHS, no Sb/Br)	Cu/NiPdAu	AZ42B49	ADS42B49IRGCT	Tape and Reel
							ADS42B49IRGCR	Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Eco Plan is the planned eco-friendly classification. Green (RoHS, no Sb/Br): TI defines *Green* to mean Pb-Free (RoHS compatible) and free of Bromine- (Br) and Antimony- (Sb) based flame retardants. Refer to the Quality and Lead-Free (Pb-Free) Data web site for more information.

The ADS42B49 is pin-compatible with the previous generation ADS62P49 data converter; this similar architecture enables easy migration. However, there are some important differences between the two device generations, summarized in Table 1.

Table 1. Migrating from the ADS62P49 and ADS4249

ADS62P49	ADS4249	ADS42B49
PINS		
Pin 22 is NC (not connected). Must float.	Pin 22 is AVDD (1.8 V)	Pin 22 is AVDD (1.9 V)
Pin 34 is AVDD (3.3 V)	Pin 34 is AVDD (1.8 V)	Pin 34 is AVDD_BUF (3.3 V)
Pin 38 is DRVDD (1.8 V)	Pin 38 is NC. Must float.	Pin 38 is DRVDD (1.8 V)
Pin 39 is DRGND	Pin 39 is NC. Must float.	Pin 39 is DRGND
Pin 58 is DRVDD (1.8 V)	Pin 58 is NC. Must float.	Pin 58 is DRVDD (1.8 V)
Pin 59 is DRGND	Pin 59 is NC. Must float.	Pin 59 is DRGND
SUPPLY		
AVDD is 3.3 V	AVDD is 1.8 V	AVDD is 1.9 V
DRVDD is 1.8 V	DRVDD is 1.8 V	DRVDD is 1.8 V
		AVDD_BUF is 3.3 V
INPUT COMMON-MODE VOLTAGE		
CM is 1.5 V	CM is 0.95 V	CM is 1.9 V
BIASING FOR INPUT PINS (INP, INM)		
INP and INM must be externally biased at 1.5 V	NP and INM must be externally biased at 0.95 V	INP and INM do not require external biasing. Device internally biases these pins to 1.9 V.
EXTERNAL REFERENCE		
Supported	Not supported	Not supported
PARALLEL CONFIGURATION		
SCLK pin controls internal and external reference mode	SCLK pin enables low-speed mode	SCLK pin enables low-speed mode

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE		UNIT
		MIN	MAX	
Supply voltage range	AVDD	–0.3	2.1	V
	AVDD_BUF	–0.3	3.6	V
	DRVDD	–0.3	2.1	V
Voltage between:	AGND and DRGND	–0.3	0.3	V
	AVDD to DRVDD (when AVDD leads DRVDD)	–2.4	2.4	V
	DRVDD to AVDD (when DRVDD leads AVDD)	–2.4	2.4	V
	AVDD_BUF to DRVDD and AVDD	–3.9	3.9	V
Voltage applied to	INP, INM	–0.3	Minimum (3, AVDD_BUF + 0.3)	V
	CLKP, CLKM(2)	–0.3	AVDD + 0.3	V
	RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3	–0.3	3.9	V
Temperature range	Operating free-air, T_A	–40	+85	°C
	Operating junction, T_J		+125	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic discharge (ESD) rating	Human body model (HBM)		2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) When AVDD is turned off, TI recommends switching off the input clock (or ensuring the voltage on CLKP, CLKM is less than |0.3 V|). This configuration prevents the ESD protection diodes at the clock input pins from turning on.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS42B49 RGC 64 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	23.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	10.9	
θ_{JB}	Junction-to-board thermal resistance	4.3	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	4.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.8	1.9	2	V
AVDD_BUF	Analog buffer supply voltage		3.15	3.3	3.45	V
DRVDD	Digital supply voltage		1.7	1.8	2	V
ANALOG INPUTS						
V_{ID}	Differential input voltage range			2		V_{PP}
V_{ICR}	Input common-mode voltage			VCM ± 0.05		V
	Maximum analog input frequency with 2-V_{PP} input amplitude[(1)]			400		MHz
	Maximum analog input frequency with 1.6-V_{PP} input amplitude[(1)]			500		MHz
CLOCK INPUT						
Input clock sample rate						
	Low-speed mode enabled[(2)]		1		80	MSPS
	Low-speed mode disabled[(2)] (by default after reset)		80		250	MSPS
	Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.2	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		1.5		V
Input clock duty cycle						
	Low-speed mode disabled		45	50	55	%
	Low-speed mode enabled		40	50	60	%
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			3.3		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)			100		Ω
T_A	Operating free-air temperature		–40		+85	°C

(1) See the *Analog Input* section in the *Application Information*.
(2) See the *Serial Interface Configuration* section for details on programming the low-speed mode.

HIGH-PERFORMANCE MODES[(1)(2)]

PARAMETER	DESCRIPTION
High-performance modes	Set the HIGH PERF MODE[0] to improve SNR in CMOS mode by approximately 0.5 dB at 170 MHz. Register Address = 03h, data = 02h Set the HIGH PERF MODE[1:11] bits to obtain best performance across input signal frequencies. Register Address = 06h, data = 06h Register Address = BAh, data = 08h Register Address = D5h, data = 20h Register Address = D9h, data = 22h Register Address = DBh, data = E0h Register Address = DCh, data = 22h

(1) TI recommends using these modes to obtain best performance.
(2) See the *Serial Interface Configuration* section for details on register programming.

ELECTRICAL CHARACTERISTICS: ADS42B49 (250 MSPS)

Typical values are at +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range:
T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution				14	Bits
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		71.3		dBFS
		f_{IN} = 70 MHz		71.2		dBFS
		f_{IN} = 100 MHz		71.1		dBFS
		f_{IN} = 170 MHz, 0-dB gain	68	70.7		dBFS
		f_{IN} = 170 MHz, 3-dB gain		67.8		dBFS
		f_{IN} = 300 MHz		69.5		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		71		dBFS
		f_{IN} = 70 MHz		71		dBFS
		f_{IN} = 100 MHz		70.9		dBFS
		f_{IN} = 170 MHz, 0-dB gain	67	70.4		dBFS
		f_{IN} = 170 MHz, 3-dB gain		67.7		dBFS
		f_{IN} = 300 MHz		67.7		dBFS
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		83		dBc
		f_{IN} = 70 MHz		87		dBc
		f_{IN} = 100 MHz		86		dBc
		f_{IN} = 170 MHz, 0-dB gain	73	85		dBc
		f_{IN} = 170 MHz, 3-dB gain		89		dBc
		f_{IN} = 300 MHz		73		dBc
THD	Total harmonic distortion	f_{IN} = 10 MHz		82		dBc
		f_{IN} = 70 MHz		84		dBc
		f_{IN} = 100 MHz		85		dBc
		f_{IN} = 170 MHz, 0-dB gain	70	83		dBc
		f_{IN} = 170 MHz, 3-dB gain		86		dBc
		f_{IN} = 300 MHz		72		dBc
HD2	Second-harmonic distortion	f_{IN} = 10 MHz		95		dBc
		f_{IN} = 70 MHz		93		dBc
		f_{IN} = 100 MHz		98		dBc
		f_{IN} = 170 MHz, 0-dB gain	73	89		dBc
		f_{IN} = 170 MHz, 3-dB gain		94		dBc
		f_{IN} = 300 MHz		80		dBc
HD3	Third-harmonic distortion	f_{IN} = 10 MHz		83		dBc
		f_{IN} = 70 MHz		87		dBc
		f_{IN} = 100 MHz		86		dBc
		f_{IN} = 170 MHz, 0-dB gain	73	85		dBc
		f_{IN} = 170 MHz, 3-dB gain		89		dBc
		f_{IN} = 300 MHz		73		dBc
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		100		dBc
		f_{IN} = 70 MHz		100		dBc
		f_{IN} = 100 MHz		100		dBc
		f_{IN} = 170 MHz, 0-dB gain	84	95		dBc
		f_{IN} = 170 MHz, 3-dB gain		97		dBc
		f_{IN} = 300 MHz		94		dBc
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		88		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		83		dBFS

ELECTRICAL CHARACTERISTICS: ADS42B49 (250 MSPS) (continued)

Typical values are at +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, LVDS interface, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range:
T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crosstalk	10-MHz full-scale signal on channel under observation; 170-MHz full-scale signal on other channel		> 85		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1		Clock cycle
PSRR	AC power-supply rejection ratio	For 50-mV_{PP} signal on AVDD supply		30		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.4		LSBs

ELECTRICAL CHARACTERISTICS: GENERAL

Typical values are at +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, and –1-dBFS differential analog input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V.

PARAMETER			MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{ID}	Differential input voltage range			2		V_{PP}
	Differential input resistance (at 170 MHz)			1.2		kΩ
	Differential input capacitance (at 170 MHz)			2.2		pF
	Analog input bandwidth (with 50-Ω source impedance, and 50-Ω termination)			700		MHz
VCM	Common-mode output voltage			1.9(1)		V
	VCM output current capability			10		mA
DC ACCURACY						
	Offset error		–20	3	20	mV
E_{GREF}	Gain error as a result of internal reference inaccuracy alone		–2		2	%FS
E_{GCHAN}	Gain error of channel alone			–5		%FS
	Temperature coefficient of E_{GCHAN}			0.005		Δ%/°C
POWER SUPPLY						
IAVDD	Analog supply current			186	225	mA
IAVDD_BUF	Analog buffer supply current			67	90	mA
IDRVDD	Output buffer supply current	LVDS interface, 350-mV swing with 100-Ω external termination, f_{IN} = 2.5 MHz		151	180	mA
		CMOS interface, 8-pF external load capacitance, f_{IN} = 2.5 MHz(2)		128		mA
	Analog power			353		mW
	Analog buffer power			224		mW
	Digital power, LVDS interface, 350-mV swing with 100-Ω external termination, f_{IN} = 2.5 MHz			272		mW
	Digital power, CMOS interface, 8-pF external load capacitance,(2) f_{IN} = 2.5 MHz			230		mW
	Total power, LVDS interface, 350-mV swing with 100-Ω external termination, f_{IN} = 2.5 MHz			850	925	mW
	Global power-down				20	mW

(1) After the HIGH PERF MODE[10:0] bits are set.
(2) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see the *CMOS Interface Power Dissipation* section in the *Application Information*).

DIGITAL CHARACTERISTICS

At AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V, unless otherwise noted. DC specifications refer to the condition where the digital outputs do not switch, but are permanently at a valid logic level '0' or '1'.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, CTRL1, CTRL2, CTRL3)(1)							
V_{IH}	High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V_{IL}	Low-level input voltage					0.4	V
I_{IH}	High-level input current	SDATA, SCLK(2)	V_{HIGH} = 1.8 V		10		µA
		SEN(3)	V_{HIGH} = 1.8 V		0		µA
I_{IL}	Low-level input current	SDATA, SCLK	V_{LOW} = 0 V		0		µA
		SEN	V_{LOW} = 0 V		10		µA
DIGITAL OUTPUTS, CMOS INTERFACE (DA[13:0], DB[13:0], CLKOUT, SDOUT)							
V_{OH}	High-level output voltage			DRVDD – 0.1	DRVDD		V
V_{OL}	Low-level output voltage				0	0.1	V
C_O	Output capacitance (internal to device)						pF
DIGITAL OUTPUTS, LVDS INTERFACE							
V_{ODH}	High-level output differential voltage		With an external 100-Ω termination	275	350	425	mV
V_{ODL}	Low-level output differential voltage		With an external 100-Ω termination	–425	–350	–275	mV
V_{OCM}	Output common-mode voltage			0.9	1.05	1.25	V

(1) SCLK, SDATA, and SEN function as digital input pins in serial configuration mode.
(2) SDATA and SCLK have an internal 150-kΩ pull-down resistor.
(3) SEN has an internal 150-kΩ pull-up resistor to AVDD. Because the pull-up resistor is weak, SEN can also be driven by 1.8-V or 3.3-V CMOS buffers.

TIMING REQUIREMENTS: LVDS and CMOS Modes

Typical values are at +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 3.3 pF, and R_{LOAD} = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.7 V to 2 V.

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
t_A	Aperture delay		0.5	0.8	1.1	ns
	Aperture delay matching	Between two channels of the same device		±70		ps
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±150		ps
t_J	Aperture jitter			120		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		50		µs
		Time to valid data after coming out of GLOBAL power-down mode		100		µs
	ADC latency(1)	Default latency after reset		11		Clock cycles
		Digital functions enabled (EN DIGITAL = 1)		19		Clock cycles
DDR LVDS MODE(2)(3)						
t_{SU_RISE}	Data setup time on rising edge of CLKOUTP	Data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM)(4)	0.32	0.68		ns
t_{HO_RISE}	Data hold time on rising edge of CLKOUTP	Zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid(4)	0.5	0.82		ns
t_{SU_FALL}	Data setup time on falling edge of CLKOUTP	Data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM)(4)	0.63	1.04		ns
t_{HO_FALL}	Data hold time on falling edge of CLKOUTP	Zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid(4)	0.18	0.58		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock (CLKOUTP – CLKOUTM) rising edge cross-over	7.6	8.9	10.2	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock (CLKOUTP – CLKOUTM)		57		%
t_{FALL}, t_{RISE}	Data fall time, Data rise time	Rise time measured from –100 mV to +100 mV *1 MSPS ≤ Sampling frequency ≤ 250 MSPS*		0.13		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100 mV to +100 mV *1 MSPS ≤ Sampling frequency ≤ 250 MSPS*		0.13		ns
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD 1 MSPS ≤ Sampling frequency ≤ 250 MSPS		0.13		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD 1 MSPS ≤ Sampling frequency ≤ 250 MSPS		0.13		ns
PARALLEL CMOS MODE						
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over	5.9	8.3	10.6	ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*		50		%
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*		0.7		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *1 MSPS ≤ Sampling frequency ≤ 200 MSPS*		0.7		ns

(1) Overall latency = ADC latency + t_{PDI}. At 250 MSPS, t_{PDI} is greater than two clock periods. Therefore, overall latency at 250 MSPS = ADC latency + 2 clock cycles.
(2) Measurements are done with a transmission line of a 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(3) Setup and hold values in DDR LVDS mode are taken with a delayed output clock by writing register 42h, value 30h.
(4) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.

Table 2. LVDS Timings at Lower Sampling Frequencies(1)

SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)						HOLD TIME (ns)						CLOCK PROPAGATION DELAY (ns)		
	t_{SU_RISE}			t_{SU_FALL}			t_{HO_RISE}			t_{HO_FALL}			t_{PDI}		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
100	0.36	0.72		0.67	1.10		3.37	3.80		3.02	3.48		10.4	11.8	13.1
125	0.35	0.72		0.66	1.08		2.43	2.82		2.09	2.51		9.4	10.8	12.1
150	0.35	0.70		0.66	1.07		1.77	2.15		1.47	1.86		8.8	10.1	11.5
175	0.35	0.70		0.63	1.07		1.32	1.67		1.00	1.40		8.3	9.7	11.0
200	0.38	0.70		0.68	1.08		0.93	1.29		0.66	1.04		8.0	9.4	10.8
230	0.33	0.69		0.67	1.06		0.63	0.97		0.35	0.74		7.7	9.1	10.5

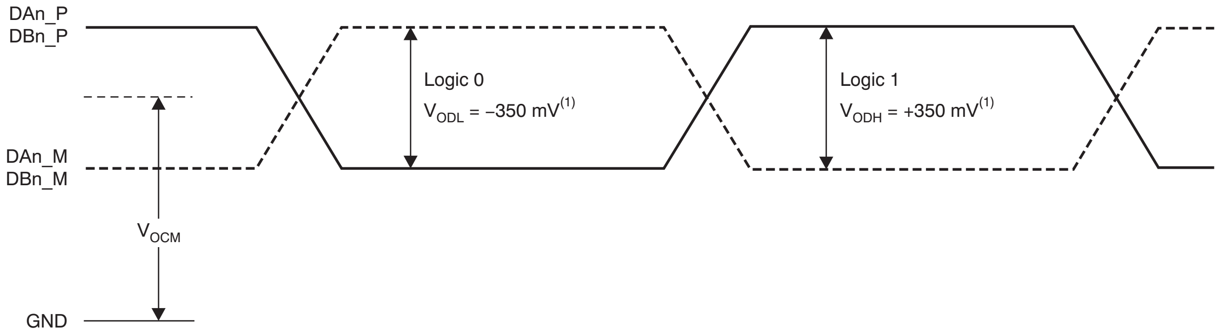
(1) Setup and hold values in DDR LVDS mode belong to delayed output clock by writing register 42h, value 30h.

Table 3. CMOS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	SETUP TIME(1) (t_{SU}, ns)			HOLD TIME(1) (t_{HO}, ns)			CLOCK PROPAGATION DELAY (t_{PDI}, ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
100	3.91	4.40		3.68	4.18		9.5	11.5	13.3
125	2.81	3.40		2.73	3.14		8.5	10.5	12.3
150	2.00	2.64		2.09	2.52		7.9	9.9	11.7
175	1.43	2.14		1.67	2.06		7.6	9.4	11.4
200	1.01	1.76		1.25	1.68		6.4	8.9	11.1

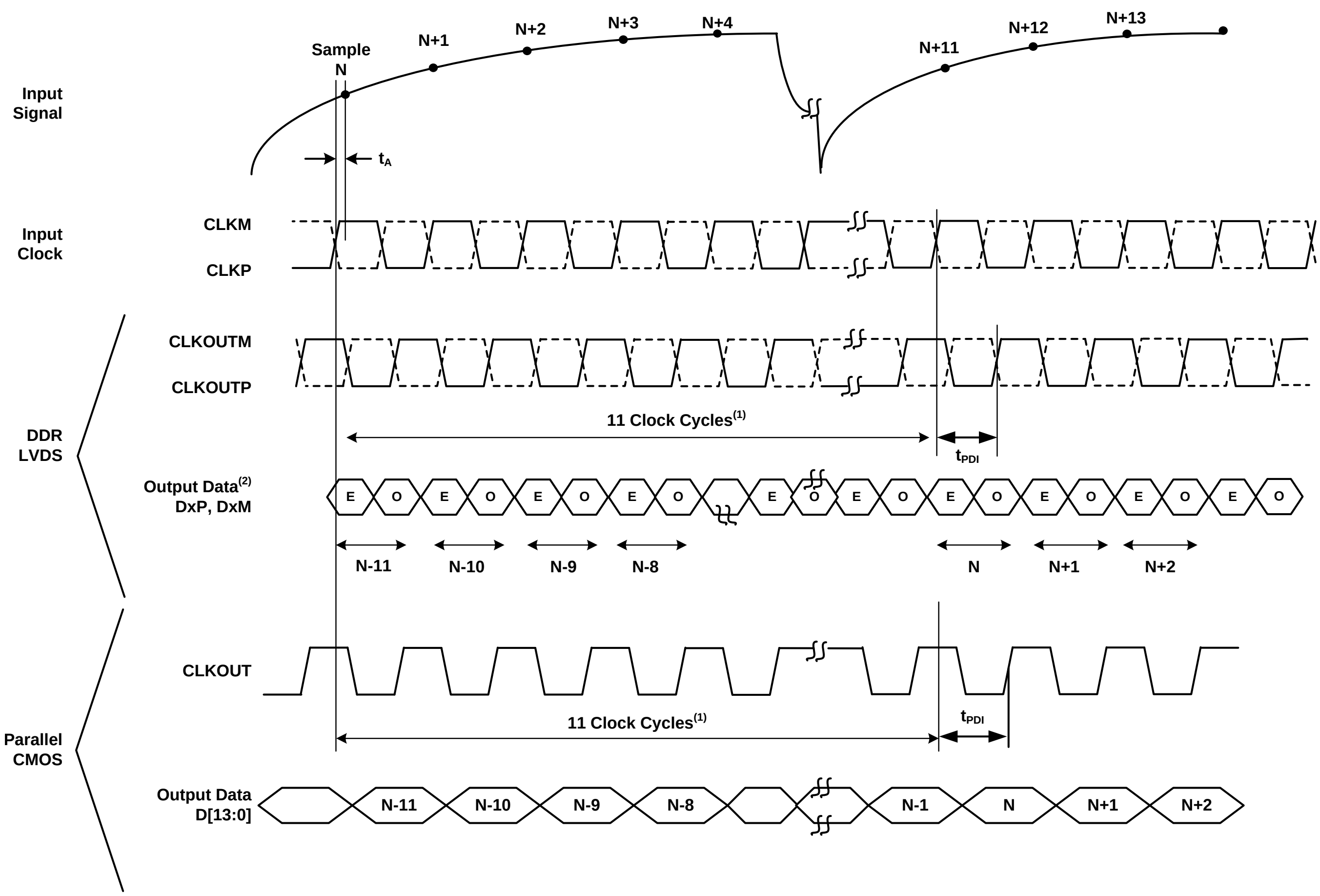
(1) In CMOS mode, setup time is measured from the beginning of data valid to the mid-point of the CLKOUT rising edge, whereas hold time is measured from the mid-point of the CLKOUT rising edge to data becoming invalid.

PARAMETER MEASUREMENT INFORMATION



(1) With an external 100-Ω termination.

Figure 1. LVDS Output Voltage Levels

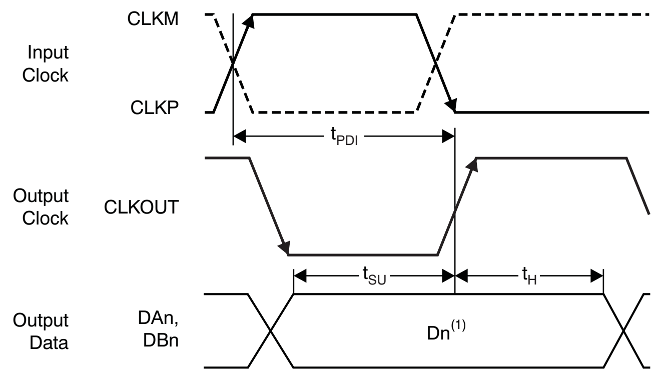


(1) The ADC latency after reset is 11 clock cycles. Overall latency = ADC latency + t_{PDI}.

(2) E = even bits (D0, D2, D4, and so forth); O = odd bits (D1, D3, D5, and so forth).

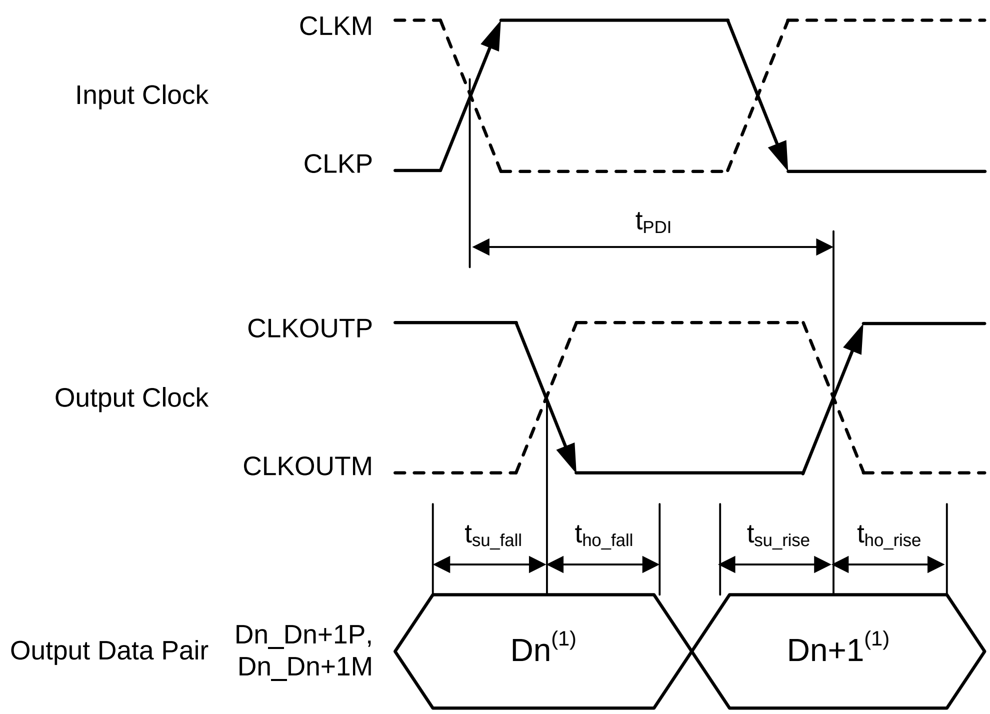
Figure 2. Latency Timing Diagram

PARAMETER MEASUREMENT INFORMATION (continued)



(1) D*n* = bits D0, D1, D2, and so forth of channels A and B.

Figure 3. CMOS Interface Timing Diagram



(1) D*n* = D0, D2, D4, and so forth. D*n*+1 = D1, D3, D5, and so forth.

Figure 4. LVDS Interface Timing Diagram

PARAMETER MEASUREMENT INFORMATION (continued)

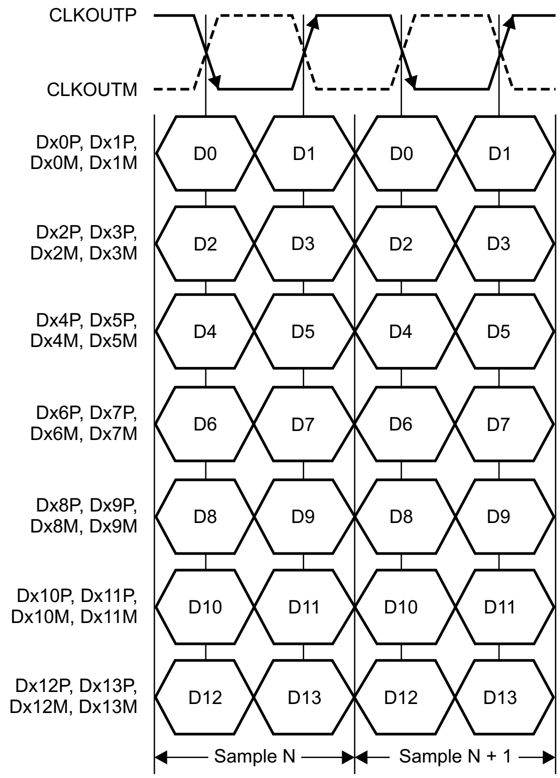
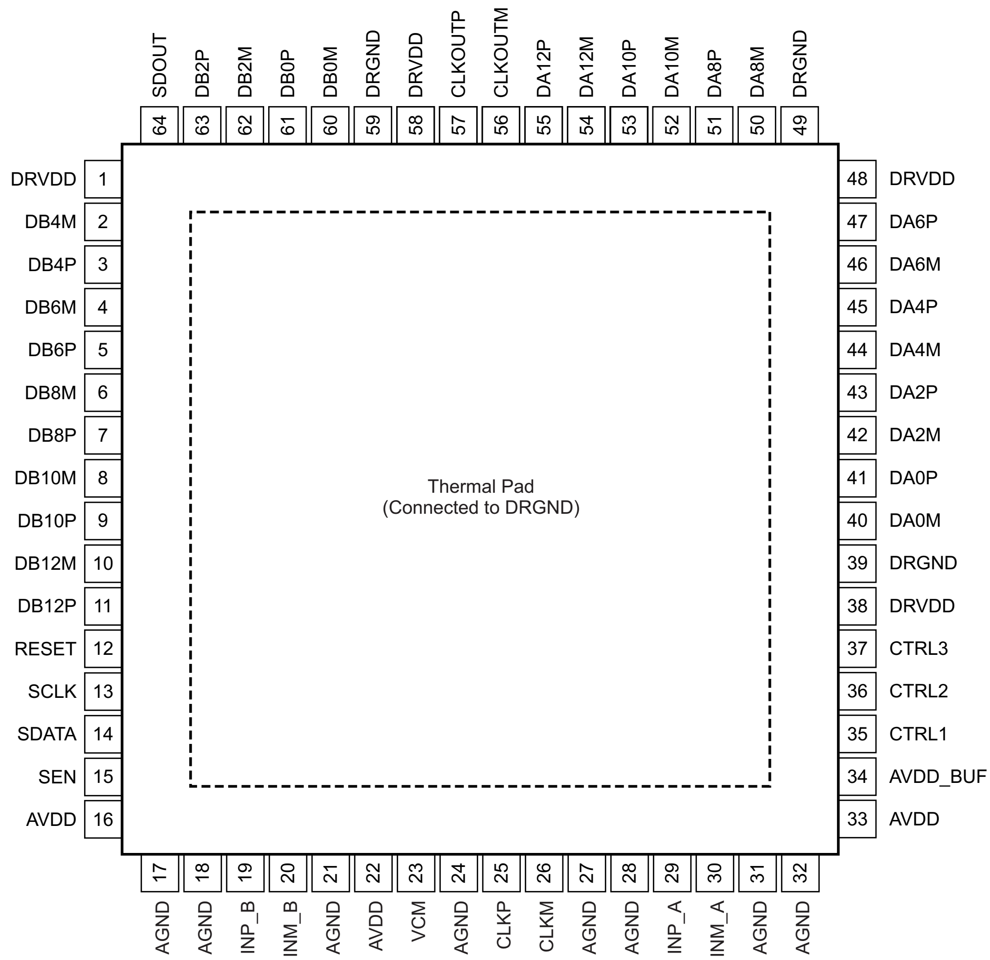


Figure 5. LVDS Bit Order

PIN CONFIGURATION: LVDS MODE

RGC PACKAGE(1)
QFN-64
(TOP VIEW)



(1) The PowerPAD is connected to DRGND.

Figure 6. LVDS Mode

PIN DESCRIPTIONS: LVDS Mode

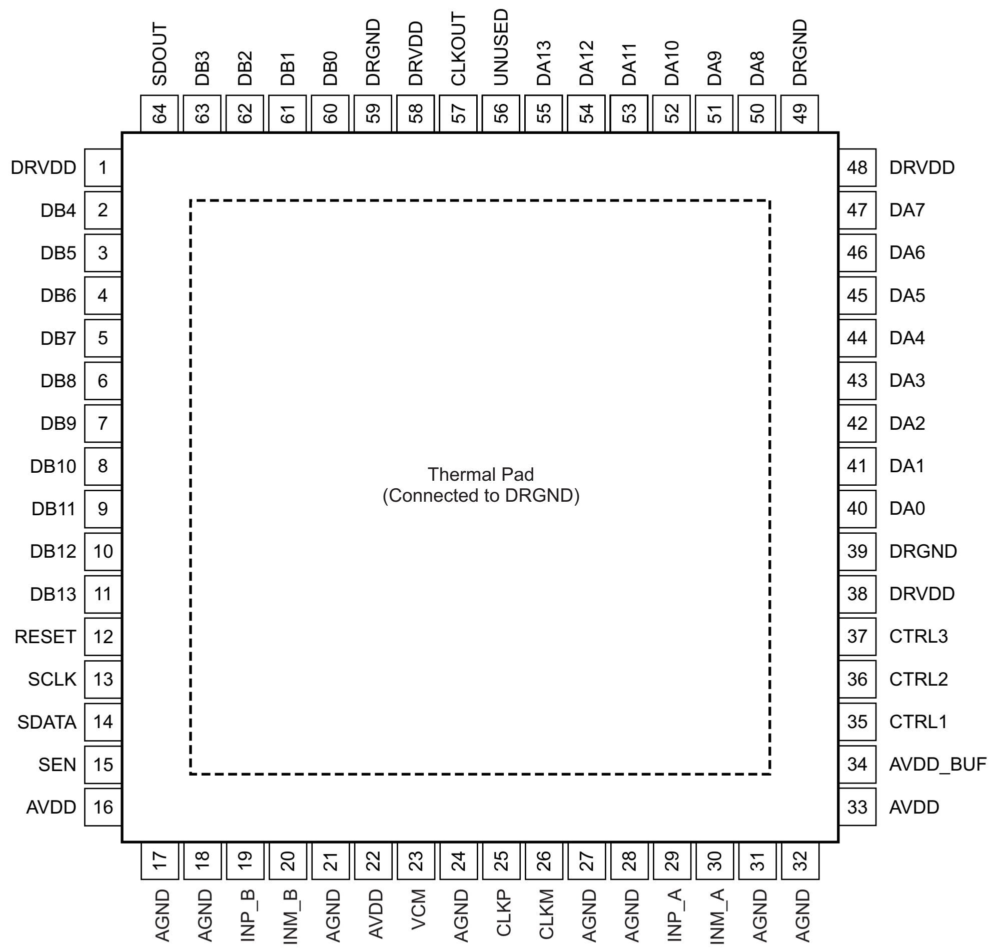
PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
AGND	17, 18, 21, 24, 27, 28, 31, 32	8	Input	Analog ground
AVDD	16, 22, 33	3	Input	Analog power supply
AVDD_BUF	34	1	Input	Analog buffer supply
CLKM	26	1	Input	Differential clock negative input
CLKP	25	1	Input	Differential clock positive input
CLKOUTM	56	1	Output	Differential output clock, complement
CLKOUTP	57	1	Output	Differential output clock, true
CTRL1	35	1	Input	Digital control input pins. Together, these pins control the various power-down modes.
CTRL2	36	1	Input	Digital control input pins. Together, these pins control the various power-down modes.
CTRL3	37	1	Input	Digital control input pins. Together, these pins control the various power-down modes.

PIN DESCRIPTIONS: LVDS Mode (continued)

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
DA0P, DA0M	Refer to Figure 6	2	Output	Channel A differential output data pair, D0 and D1 multiplexed
DA2P, DA2M	Refer to Figure 6	2	Output	Channel A differential output data D2 and D3 multiplexed
DA4P, DA4M	Refer to Figure 6	2	Output	Channel A differential output data D4 and D5 multiplexed
DA6P, DA6M	Refer to Figure 6	2	Output	Channel A differential output data D6 and D7 multiplexed
DA8P, DA8M	Refer to Figure 6	2	Output	Channel A differential output data D8 and D9 multiplexed
DA10P, DA10M	Refer to Figure 6	2	Output	Channel A differential output data D10 and D11 multiplexed
DA12P, DA12M	Refer to Figure 6	2	Output	Channel A differential output data D12 and D13 multiplexed
DB0P, DB0M	Refer to Figure 6	2	Output	Channel B differential output data pair, D0 and D1 multiplexed
DB2P, DB2M	Refer to Figure 6	2	Output	Channel B differential output data D2 and D3 multiplexed
DB4P, DB4M	Refer to Figure 6	2	Output	Channel B differential output data D4 and D5 multiplexed
DB6P, DB6M	Refer to Figure 6	2	Output	Channel B differential output data D6 and D7 multiplexed
DB8P, DB8M	Refer to Figure 6	2	Output	Channel B differential output data D8 and D9 multiplexed
DB10P, DB10M	Refer to Figure 6	2	Output	Channel B differential output data D10 and D11 multiplexed
DB12P, DB12M	Refer to Figure 6	2	Output	Channel B differential output data D12 and D13 multiplexed
DRGND	39, 49, 59, PAD	4	Input	Output buffer ground, should be shorted on-board to analog ground.
DRVDD	1, 38, 48, 58	4	Input	Output buffer supply
INM_A	30	1	Input	Differential analog negative input, channel A
INP_A	29	1	Input	Differential analog positive input, channel A
INM_B	20	1	Input	Differential analog negative input, channel B
INP_B	19	1	Input	Differential analog positive input, channel B
RESET	12	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section. In parallel interface mode, the RESET pin must be permanently tied high. SCLK and SEN are used as parallel control pins in this mode. This pin has an internal 150-kΩ pull-down resistor.
SCLK	13	1	Input	This pin functions as a serial interface clock input when RESET is low. SCLK controls the low-speed mode selection when RESET is tied high; see Table 5 for detailed information. This pin has an internal 150-kΩ pull-down resistor.
SDATA	14	1	Input	Serial interface data input; this pin has an internal 150-kΩ pull-down resistor.
SDOUT	64	1	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is in high-impedance state.
SEN	15	1	Input	This pin functions as a serial interface enable input when RESET is low. SEN controls the output interface and data format selection when RESET is tied high; see Table 6 for detailed information. This pin has an internal 150-kΩ pull-up resistor to AVDD.
VCM	23	1	Output	This pin outputs the common-mode voltage (1.9 V) that can be used externally to bias the analog input pins

PIN CONFIGURATION: CMOS MODE

RGC PACKAGE(2)
QFN-64
(TOP VIEW)



(2) The PowerPAD is connected to DRGND.

Figure 7. CMOS Mode

PIN DESCRIPTIONS: CMOS Mode

PIN NAME	PIN NUMBER	# OF PINS	FUNCTION	DESCRIPTION
AGND	17, 18, 21, 24, 27, 28, 31, 32	8	Input	Analog ground
AVDD	16, 22, 33	3	Input	Analog power supply
AVDD_BUF	34	1	Input	Analog buffer supply
CLKM	26	1	Input	Differential clock negative input
CLKP	25	1	Input	Differential clock positive input
CLKOUT	57	1	Output	CMOS output clock
CTRL1	35	1	Input	Digital control input pins. Together, these pins control various power-down modes.
CTRL2	36	1	Input	Digital control input pins. Together, these pins control various power-down modes.
CTRL3	37	1	Input	Digital control input pins. Together, these pins control various power-down modes.
DA0 to DA13	Refer to Figure 7	14	Output	Channel A ADC output data bits, CMOS levels
DB0 to DB13	Refer to Figure 7	14	Output	Channel B ADC output data bits, CMOS levels
DRGND	39, 49, 59, PAD	4	Input	Output buffer ground, should be shorted on-board to analog ground.
DRVDD	1, 38, 48, 58	4	Input	Output buffer supply
INM_A	30	1	Input	Differential analog negative input, channel A
INP_A	29	1	Input	Differential analog positive input, channel A
INM_B	20	1	Input	Differential analog negative input, channel B
INP_B	19	1	Input	Differential analog positive input, channel B
RESET	12	1	Input	Serial interface RESET input. When using the serial interface mode, the internal registers must be initialized through a hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface Configuration* section. In parallel interface mode, the RESET pin must be permanently tied high. SDATA and SEN are used as parallel control pins in this mode. This pin has an internal 150-kΩ pull-down resistor.
SCLK	13	1	Input	This pin functions as a serial interface clock input when RESET is low. SCLK controls the low-speed mode when RESET is tied high; see Table 5 for detailed information. This pin has an internal 150-kΩ pull-down resistor.
SDATA	14	1	Input	Serial interface data input; this pin has an internal 150-kΩ pull-down resistor.
SDOUT	64	1	Output	This pin functions as a serial interface register readout when the READOUT bit is enabled. When READOUT = 0, this pin is in high-impedance state.
SEN	15	1	Input	This pin functions as a serial interface enable input when RESET is low. SEN controls the output interface and data format selection when RESET is tied high; see Table 6 for detailed information. This pin has an internal 150-kΩ pull-up resistor to AVDD.
UNUSED	56	1	—	This pin is not used in the CMOS interface
VCM	23	1	Output	This pin outputs the common-mode voltage (1.9 V) that can be used externally to bias the analog input pins

FUNCTIONAL BLOCK DIAGRAM

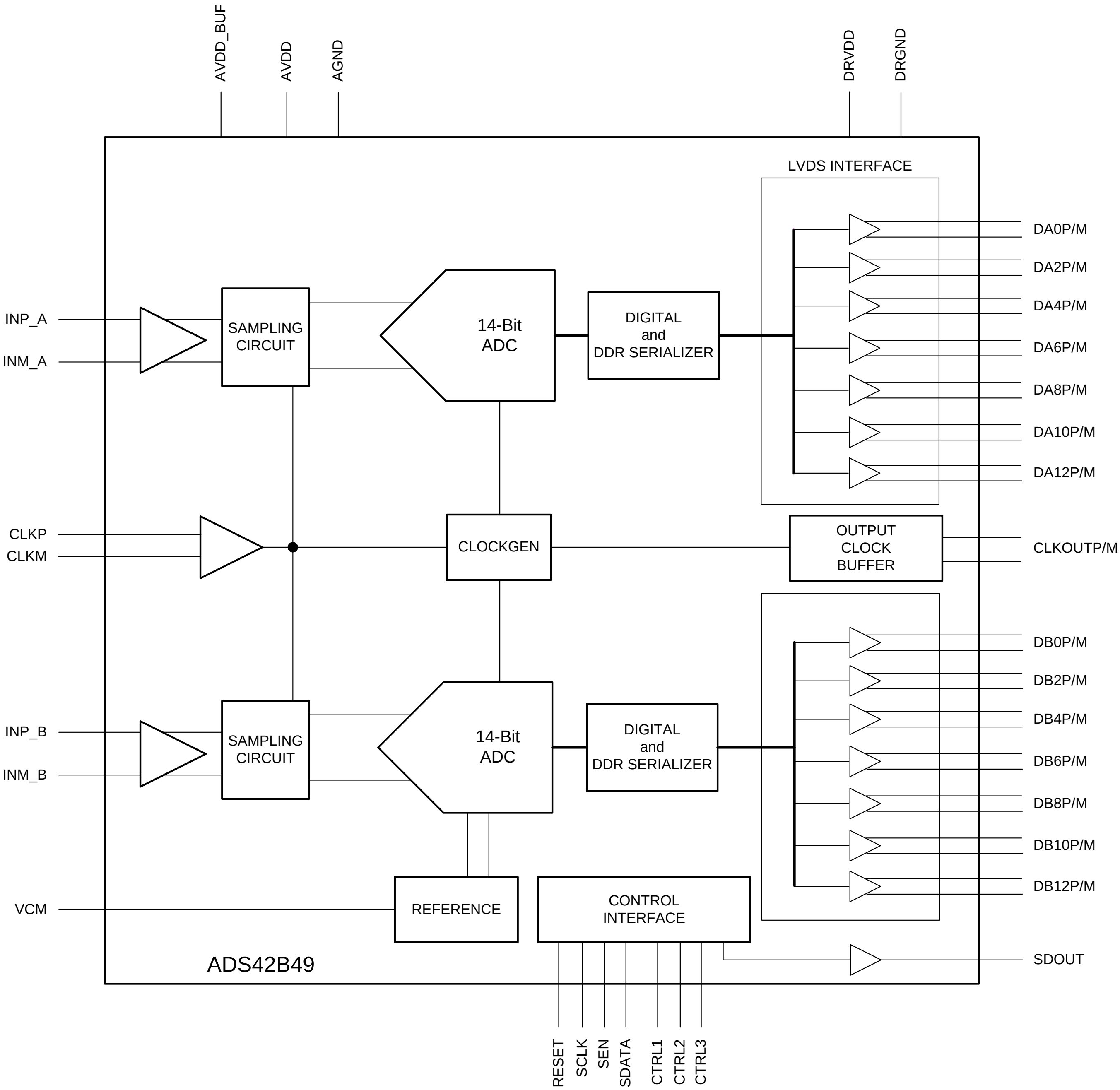


Figure 8. Block Diagram

DEVICE CONFIGURATION

The ADS42B49 can be configured independently using either parallel interface control or serial interface programming.

PARALLEL CONFIGURATION ONLY

To put the device into parallel configuration mode, keep RESET tied high (AVDD). Then, use the SEN, SCLK, CTRL1, CTRL2, and CTRL3 pins to directly control certain modes of the ADC. The device can be easily configured by connecting the parallel pins to the correct voltage levels (as described in Table 4 to Table 7). There is no need to apply a reset and SDATA can be connected to ground.

In this mode, SEN and SCLK function as parallel interface control pins. Some frequently-used functions can be controlled using these pins. Table 4 describes the modes controlled by the parallel pins.

Table 4. Parallel Pin Definition

PIN	CONTROL MODE
SCLK	Low-speed mode selection
SEN	Output data format and output interface selection
CTRL1	Together, these pins control the power-down modes and multiplexed-mode selection (in CMOS interface)
CTRL2	
CTRL3	

SERIAL INTERFACE CONFIGURATION ONLY

To enable this mode, the serial registers must first be reset to the default values and the RESET pin must be kept low. SEN, SDATA, and SCLK function as serial interface pins in this mode and can be used to access the internal registers of the ADC. The registers can be reset either by applying a pulse on the RESET pin or by setting the RESET bit high. The *Serial Register Map* section describes the register programming and the register reset process in more detail.

USING BOTH SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To enable this option, keep RESET low. The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device is automatically configured according to the voltage settings on these pins (see Table 7). SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of the ADC. The registers must first be reset to the default values either by applying a pulse on the RESET pin or by setting the RESET bit to '1'. After reset, the RESET pin must be kept low. The *Serial Register Map* section describes register programming and the register reset process in more detail.

PARALLEL CONFIGURATION DETAILS

The functions controlled by each parallel pin are described in Table 5, Table 6, and Table 7. A simple way of configuring the parallel pins is shown in Figure 9.

Table 5. SCLK Control Pin

VOLTAGE APPLIED ON SCLK	DESCRIPTION
Low	Low-speed mode is disabled
High	Low-speed mode is enabled

Table 6. SEN Control Pin

VOLTAGE APPLIED ON SEN	DESCRIPTION
0 (+50 mV / 0 mV)	Twos complement and parallel CMOS output
(3 / 8) AVDD (±50 mV)	Offset binary and parallel CMOS output
(5 / 8) AVDD (±50 mV)	Offset binary and DDR LVDS output
AVDD (0 mV / –50 mV)	Twos complement and DDR LVDS output

Table 7. CTRL1, CTRL2, and CTRL3 Pins

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Normal operation
Low	Low	High	Not available
Low	High	Low	Not available
Low	High	High	Not available
High	Low	Low	Partial power-down
High	Low	High	Channel A is powered down, channel B is active
High	High	Low	Not available
High	High	High	MUX mode of operation, channel A and B data are multiplexed and output on the DB[13:0] pins.

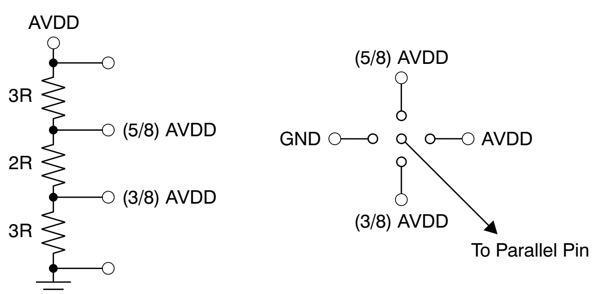


Figure 9. Simple Scheme to Configure the Parallel Pins

SERIAL INTERFACE DETAILS

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK falling edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to the default values. Initialization can be accomplished in one of two ways:

1. Through a hardware reset by applying a high pulse on the RESET pin (of width greater than 10 ns), as shown in Figure 10 and Table 8; or
2. By applying a software reset. When using the serial interface, set the RESET bit high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low. See Figure 11 and Table 9 for reset timing.

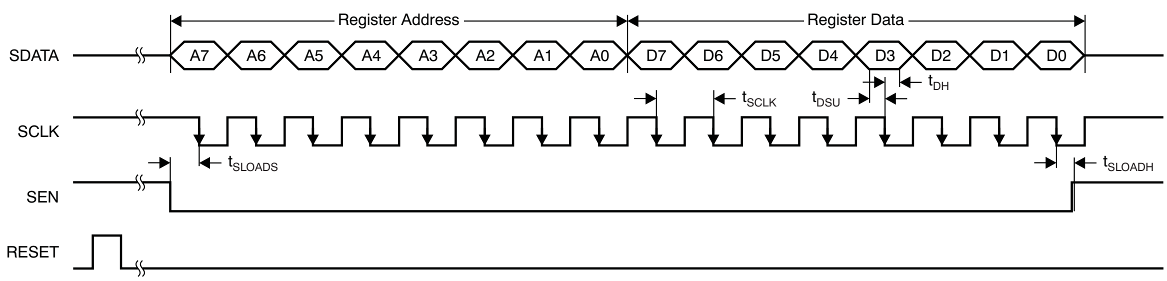
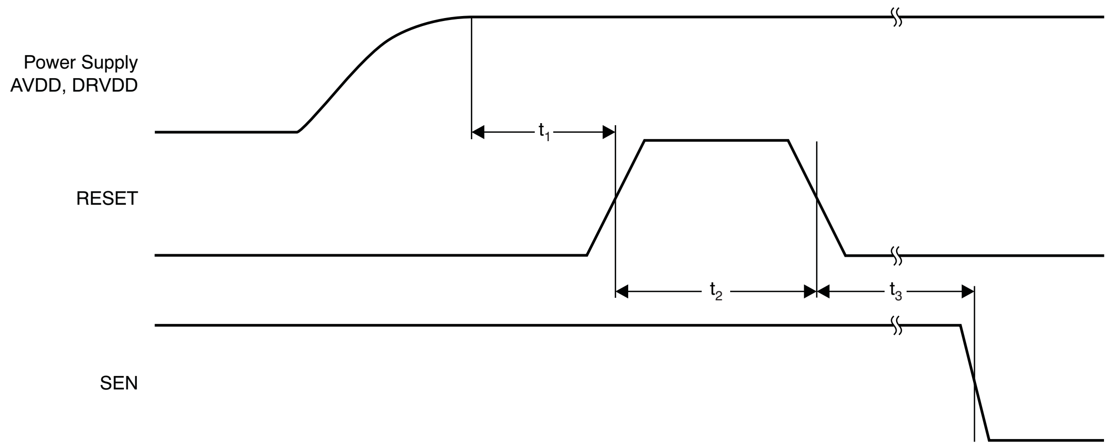


Figure 10. Serial Interface Timing

Table 8. Serial Interface Timing Characteristics(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, and DRVDD = 1.8 V, unless otherwise noted.



NOTE: A high pulse on the RESET pin is required in the serial interface mode when initialized through a hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 11. Reset Timing Diagram

Table 9. Reset Timing (Only when Serial Interface is Used)(1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
t_2	Reset pulse width	Active RESET signal pulse width	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.

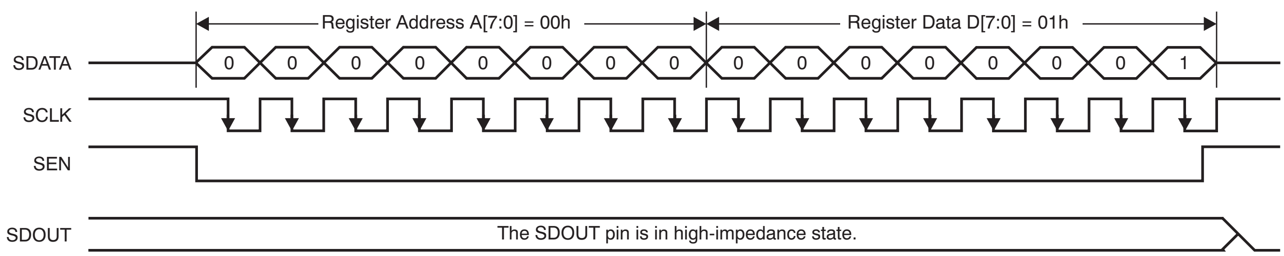
Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. To use readback mode, follow this procedure:

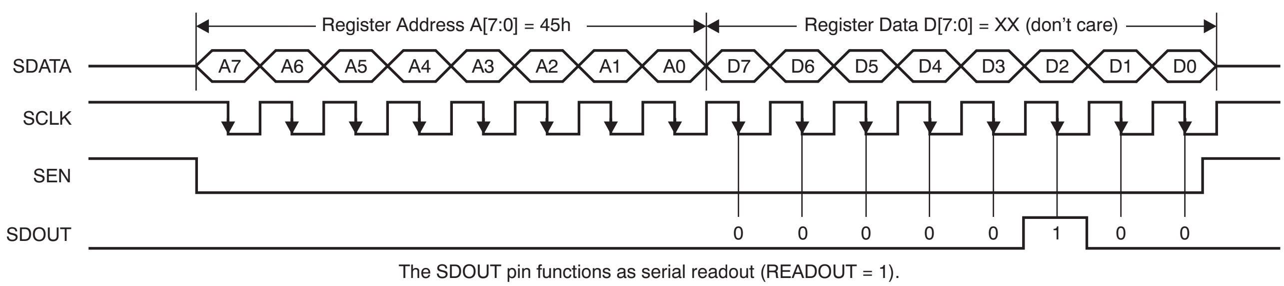
1. Set the READOUT register bit to '1'. This setting disables any further writes to the registers.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin (pin 64).
4. The external controller can latch the contents at the SCLK falling edge.
5. To enable register writes, reset the READOUT register bit to '0'.

The serial register readout works with both CMOS and LVDS interfaces on pin 64. A serial readout timing diagram is shown in Figure 12.

Note that the contents of register 00h cannot be read back because the register contains RESET and READOUT bits. When READOUT is disabled, the SDOUT pin is in a high-impedance state.



a) Enable serial readout (READOUT = 1)



b) Read contents of Register 45h. This register has been initialized with 04h (device is put into global power-down mode.)

Figure 12. Serial Readout Timing Diagram

TYPICAL CHARACTERISTICS: ADS42B49

At T_A = +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

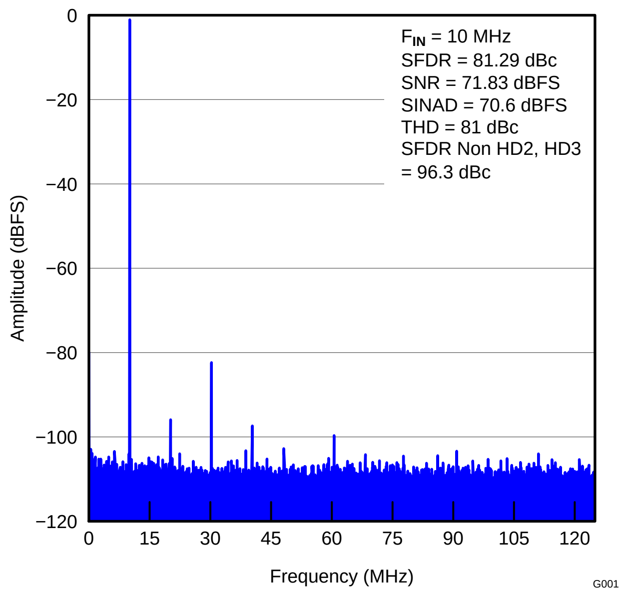


Figure 13. INPUT SIGNAL (10 MHz)

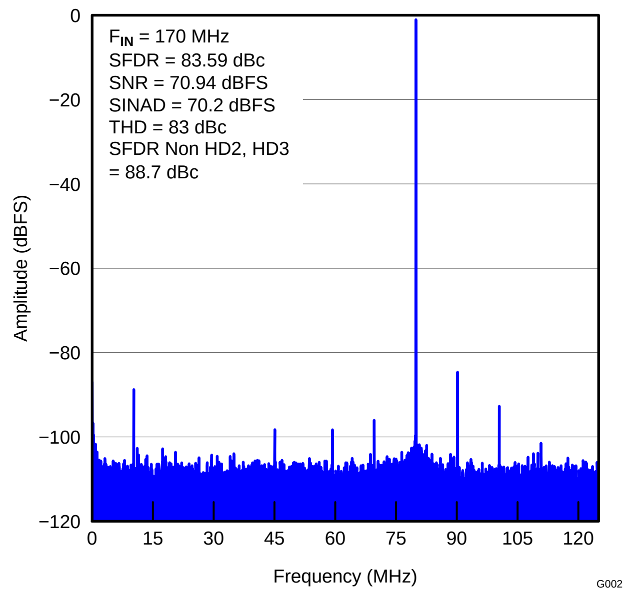


Figure 14. INPUT SIGNAL (170 MHz)

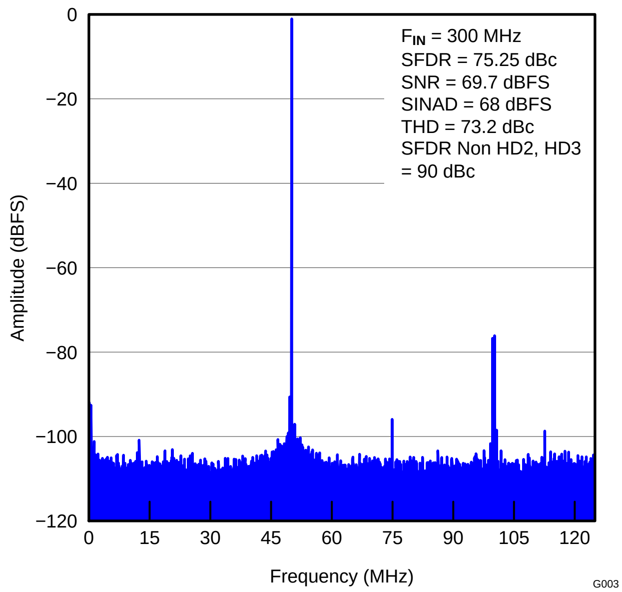


Figure 15. INPUT SIGNAL (300 MHz)

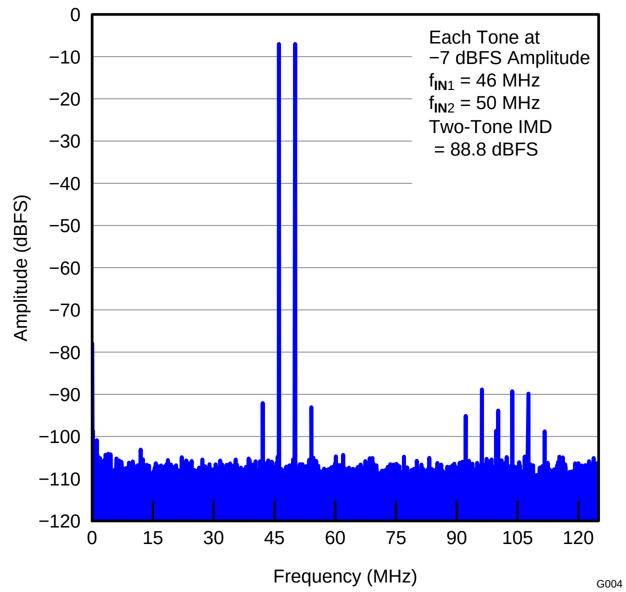


Figure 16. TWO-TONE INPUT SIGNAL

TYPICAL CHARACTERISTICS: ADS42B49 (continued)

At T_A = +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

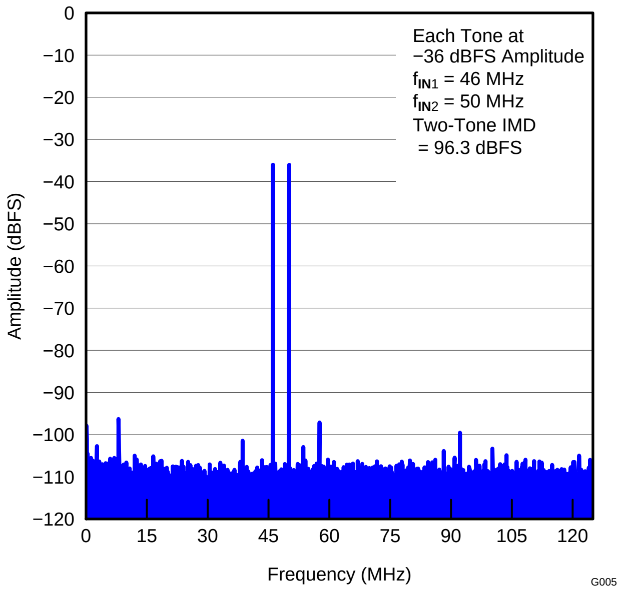


Figure 17. TWO-TONE INPUT SIGNAL

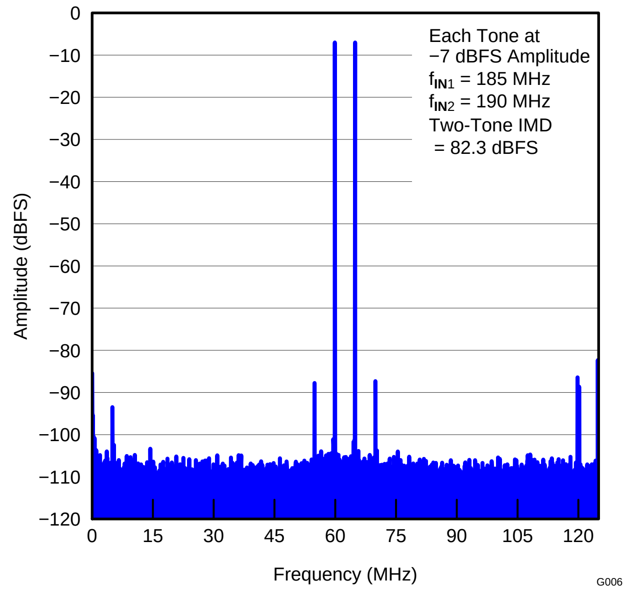


Figure 18. TWO-TONE INPUT SIGNAL

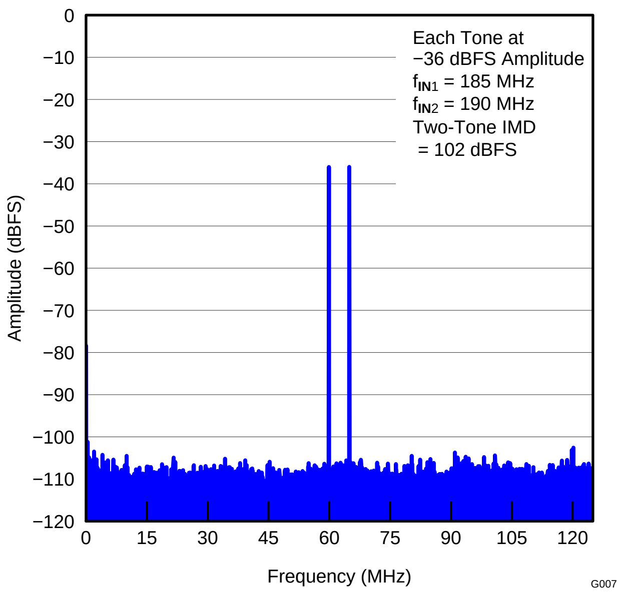


Figure 19. TWO-TONE INPUT SIGNAL

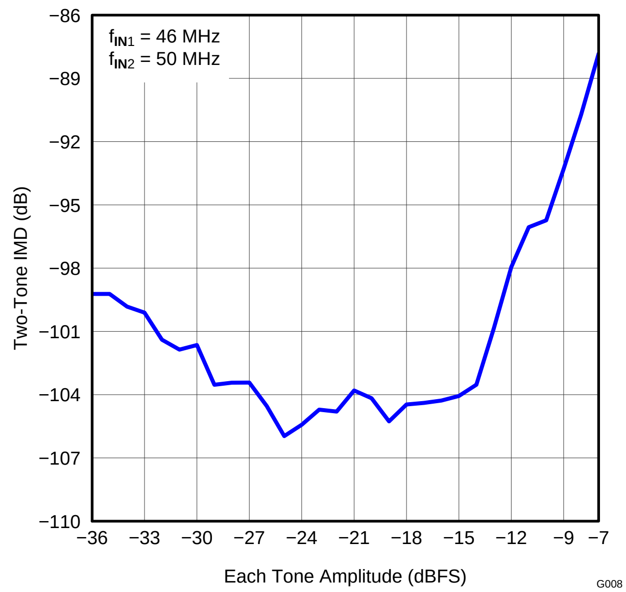


Figure 20. TWO-TONE IMD3 vs INPUT AMPLITUDE

TYPICAL CHARACTERISTICS: ADS42B49 (continued)

At T_A = +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

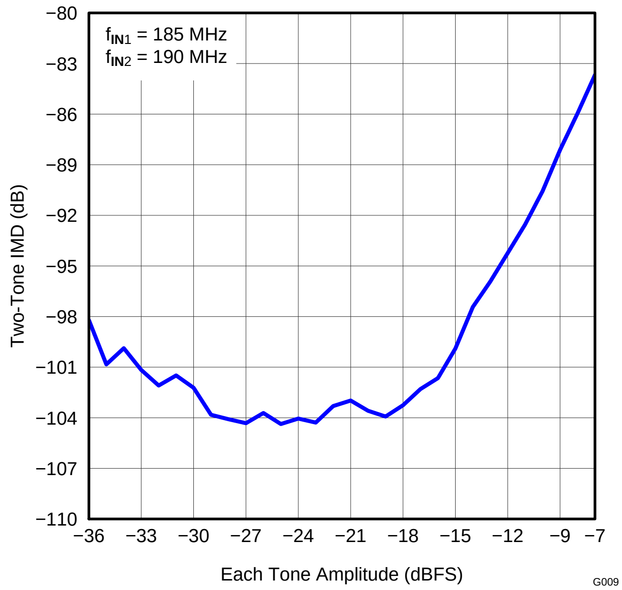


Figure 21. TWO-TONE IMD3 vs INPUT AMPLITUDE

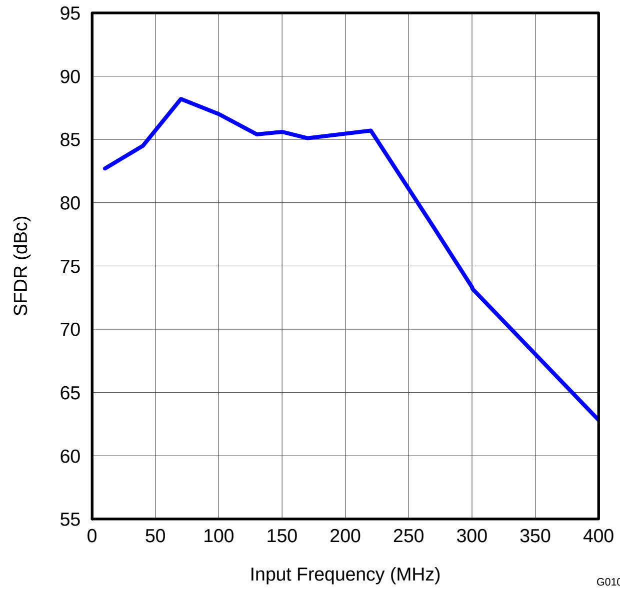


Figure 22. SPURIOUS-FREE DYNAMIC RANGE vs INPUT FREQUENCY

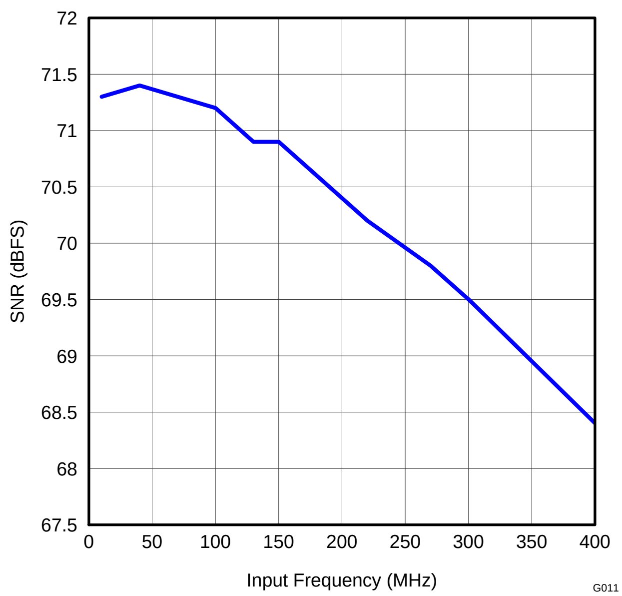


Figure 23. SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

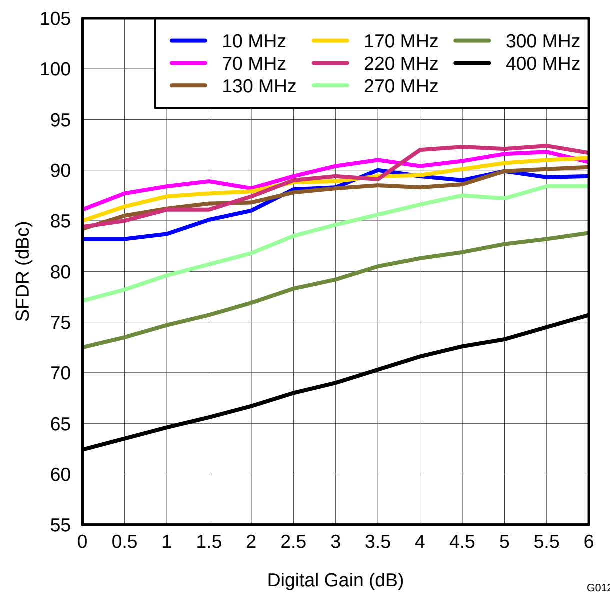


Figure 24. SPURIOUS-FREE DYNAMIC RANGE vs GAIN AND INPUT FREQUENCY

TYPICAL CHARACTERISTICS: ADS42B49 (continued)

At T_A = +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

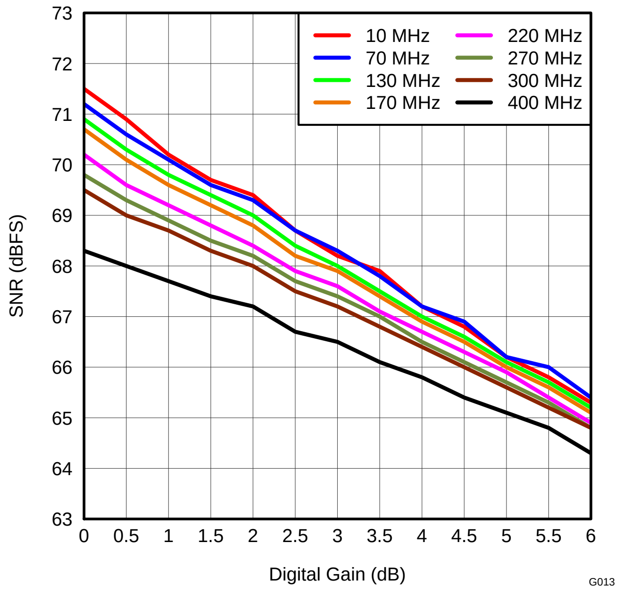


Figure 25. SIGNAL-TO-NOISE RATIO vs GAIN AND INPUT FREQUENCY

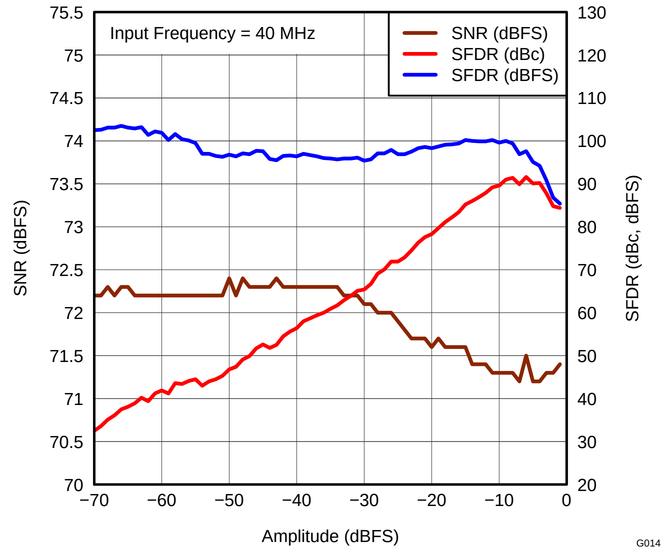


Figure 26. PERFORMANCE vs INPUT AMPLITUDE

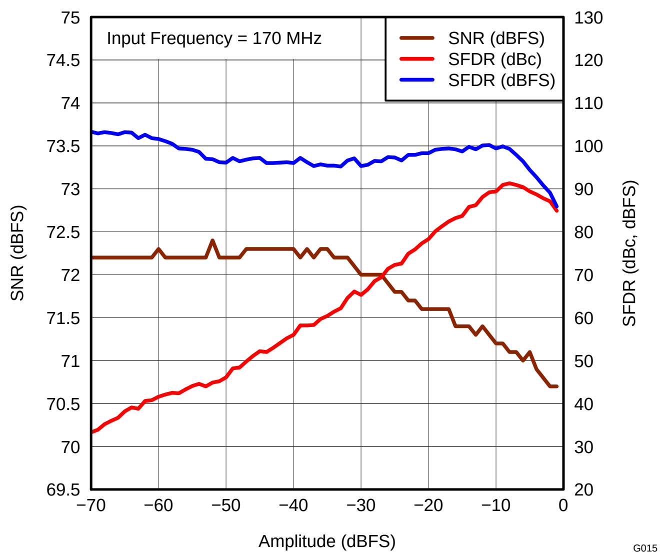


Figure 27. PERFORMANCE vs INPUT AMPLITUDE

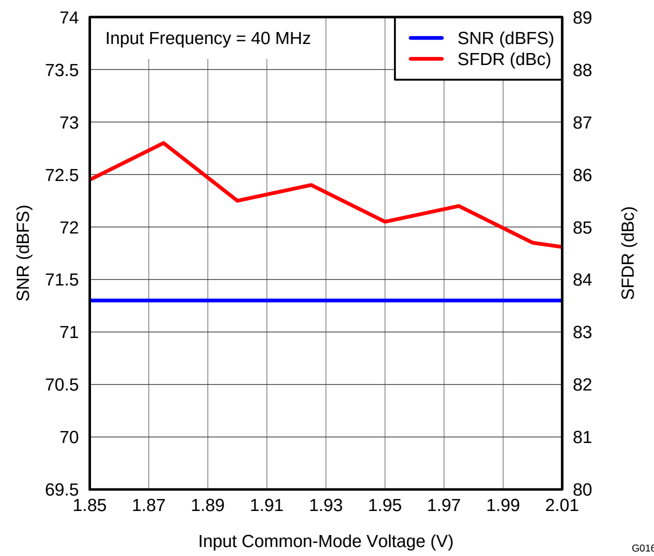


Figure 28. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

TYPICAL CHARACTERISTICS: ADS42B49 (continued)

At T_A = +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

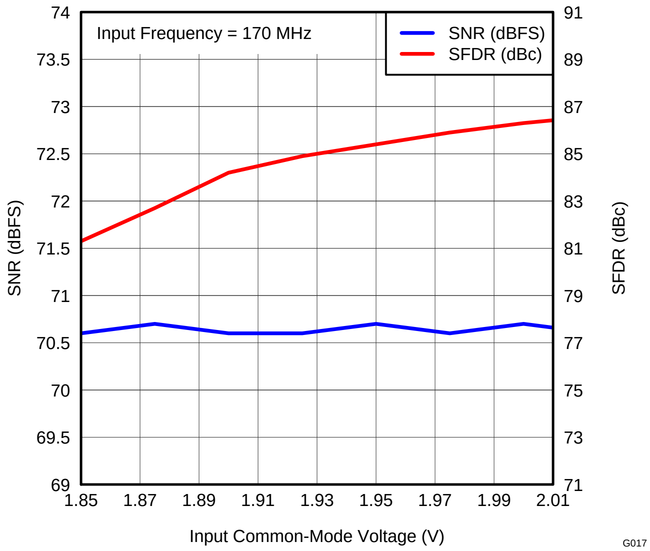


Figure 29. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE

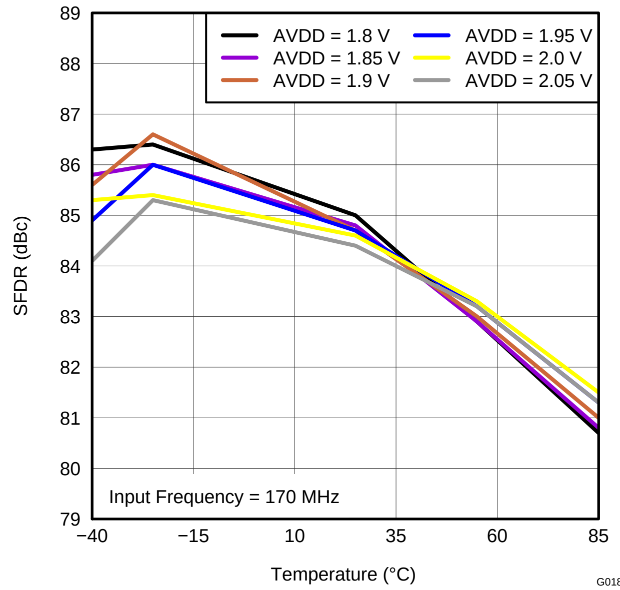


Figure 30. SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE AND AVDD SUPPLY

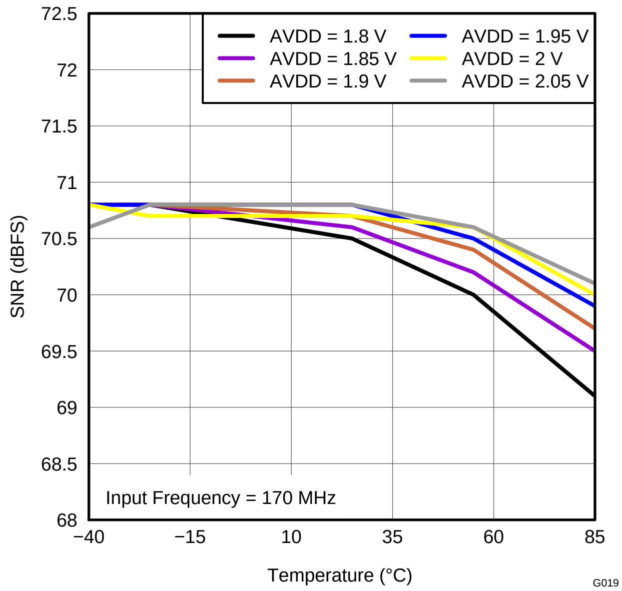


Figure 31. SIGNAL-TO-NOISE RATIO vs TEMPERATURE AND AVDD SUPPLY

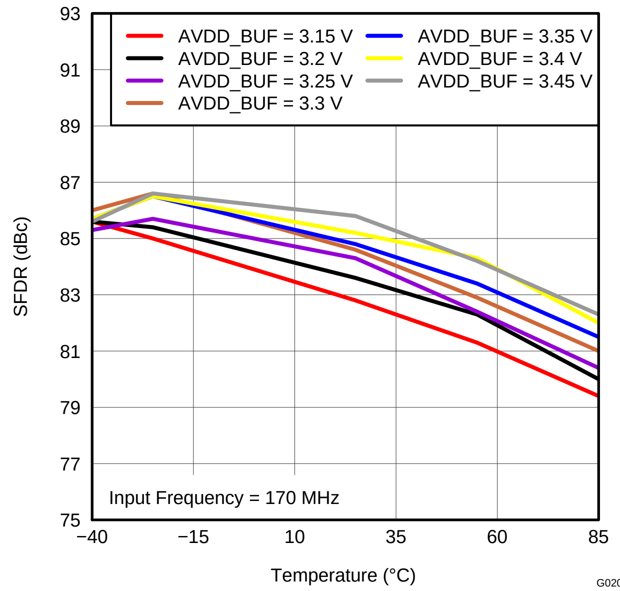


Figure 32. SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE AND AVDD_BUF SUPPLY

TYPICAL CHARACTERISTICS: ADS42B49 (continued)

At T_A = +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

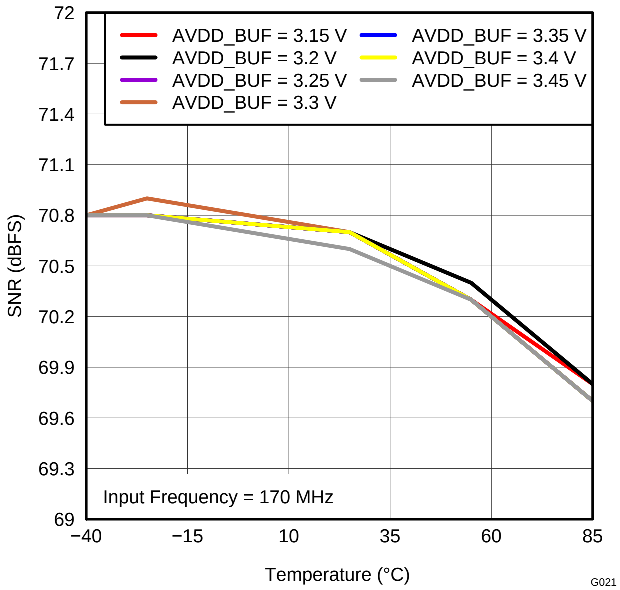


Figure 33. SIGNAL-TO-NOISE RATIO vs TEMPERATURE AND AVDD_BUF SUPPLY

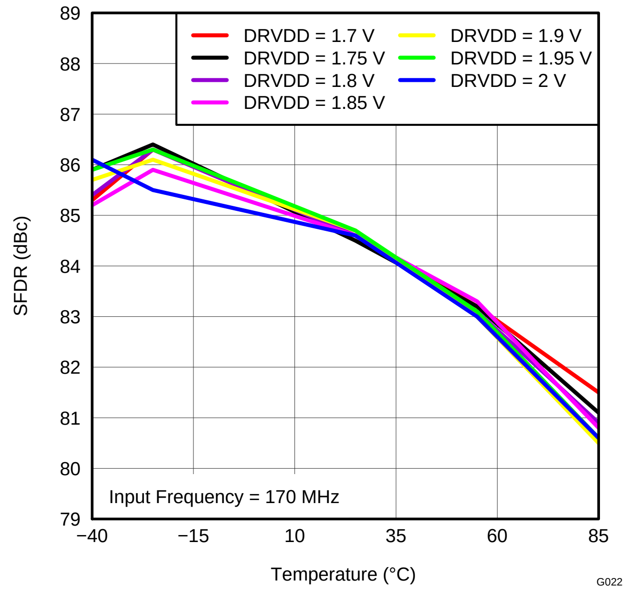


Figure 34. SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE AND DRVDD SUPPLY VOLTAGE

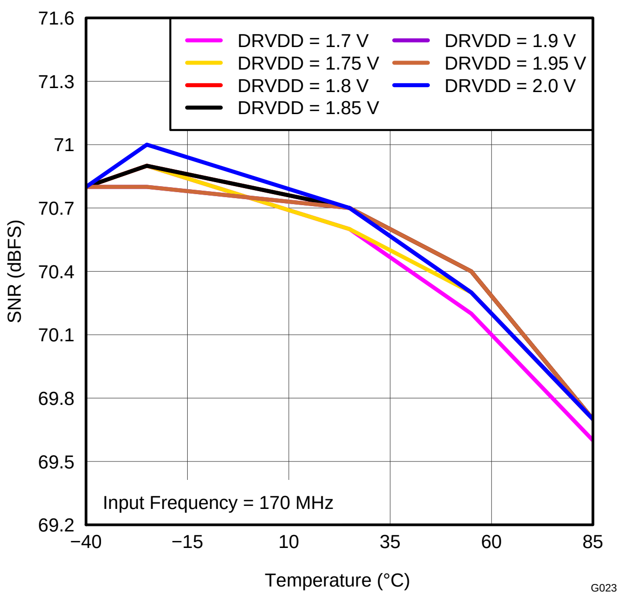


Figure 35. SIGNAL-TO-NOISE RATIO vs TEMPERATURE AND DRVDD SUPPLY VOLTAGE

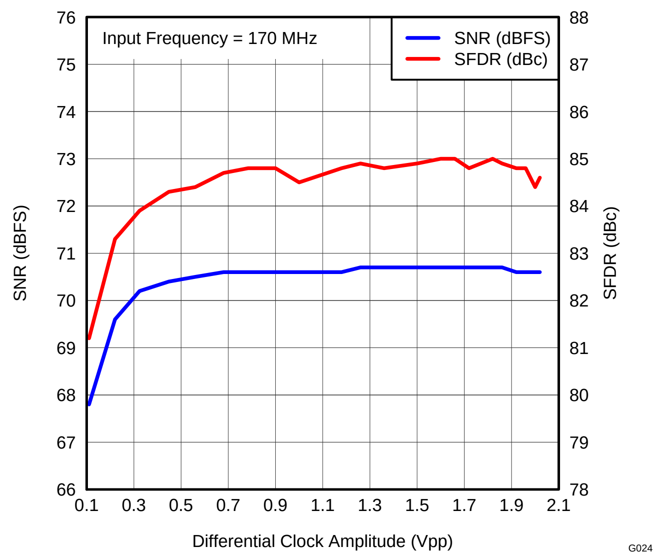


Figure 36. PERFORMANCE vs INPUT CLOCK AMPLITUDE

TYPICAL CHARACTERISTICS: ADS42B49 (continued)

At T_A = +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

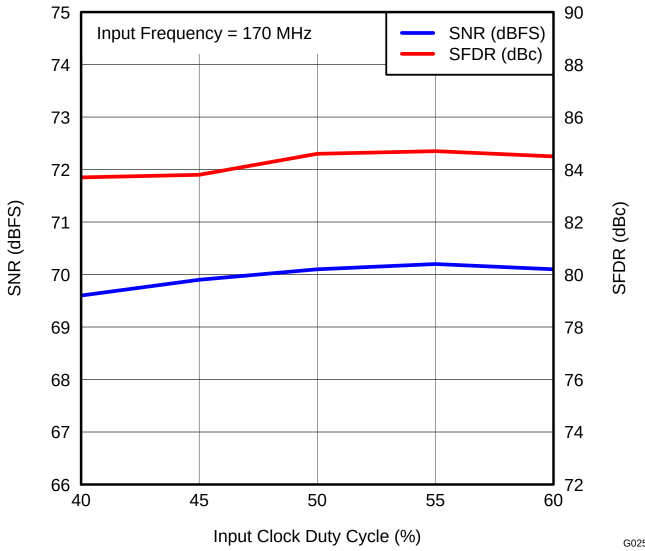


Figure 37. PERFORMANCE vs INPUT CLOCK DUTY CYCLE

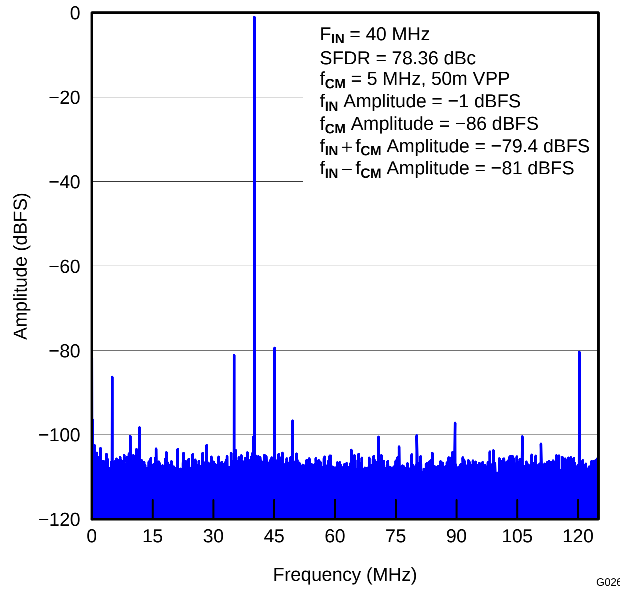


Figure 38. COMMON-MODE REJECTION RATIO PLOT

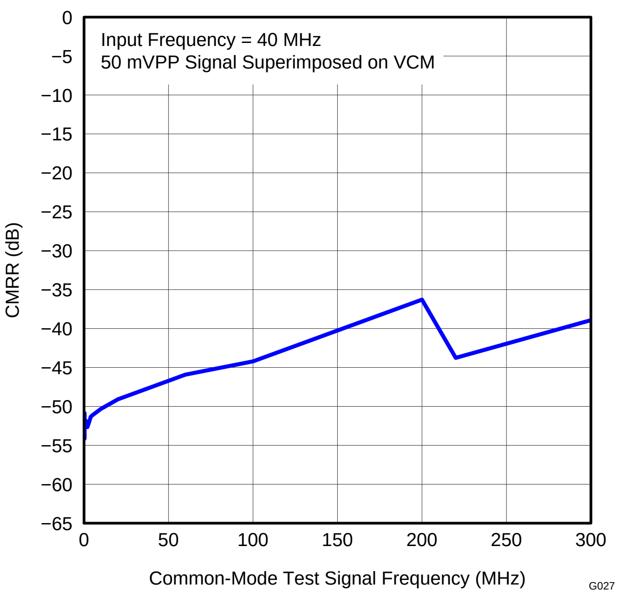


Figure 39. COMMON-MODE REJECTION RATIO vs TEST SIGNAL FREQUENCY

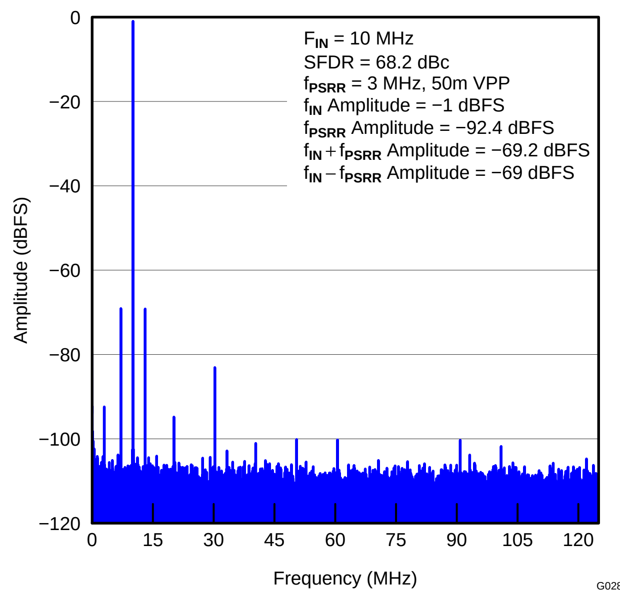


Figure 40. POWER-SUPPLY REJECTION RATIO PLOT

TYPICAL CHARACTERISTICS: ADS42B49 (continued)

At T_A = +25°C, AVDD = 1.9 V, AVDD_BUF = 3.3 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

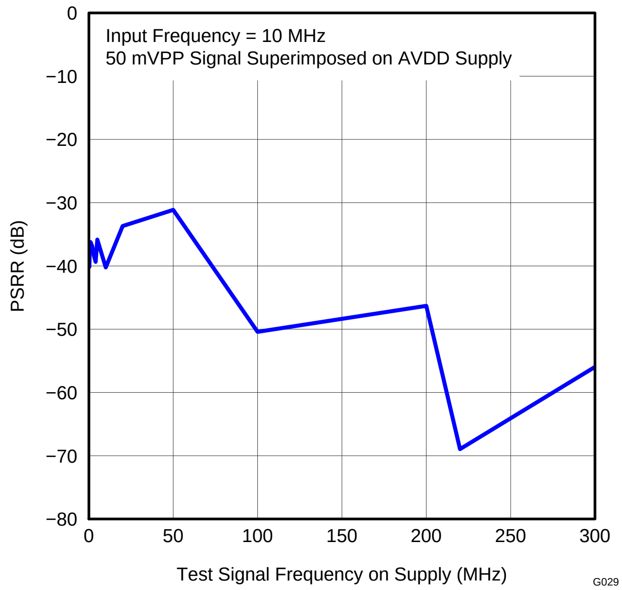


Figure 41. POWER-SUPPLY REJECTION RATIO vs TEST SIGNAL FREQUENCY

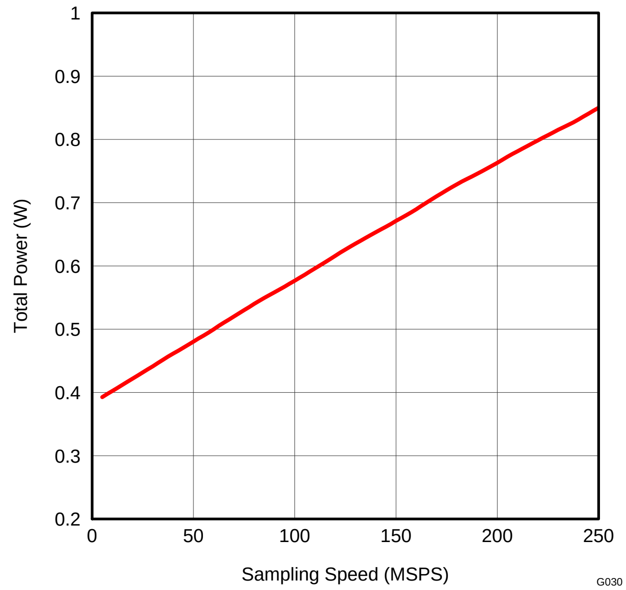


Figure 42. TOTAL POWER vs SAMPLING FREQUENCY

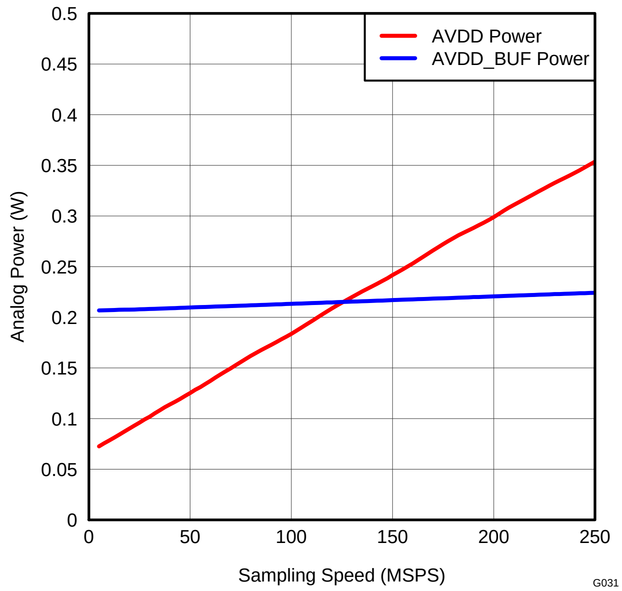


Figure 43. ANALOG POWER vs SAMPLING FREQUENCY

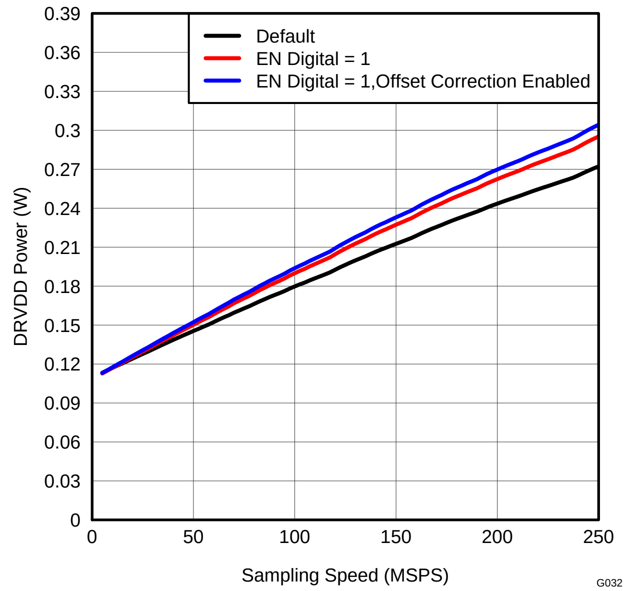


Figure 44. DIGITAL POWER vs SAMPLING FREQUENCY

TYPICAL CHARACTERISTICS: Contour

All graphs are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

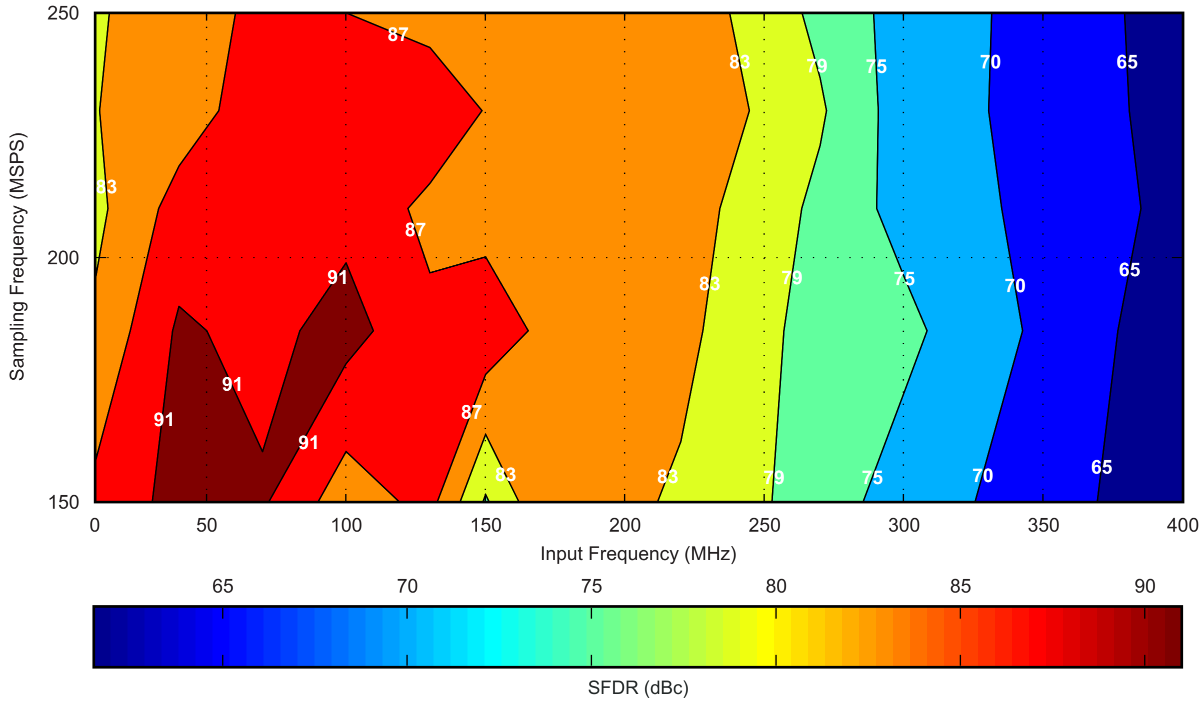


Figure 45. SPURIOUS-FREE DYNAMIC RANGE (0-dB Gain)

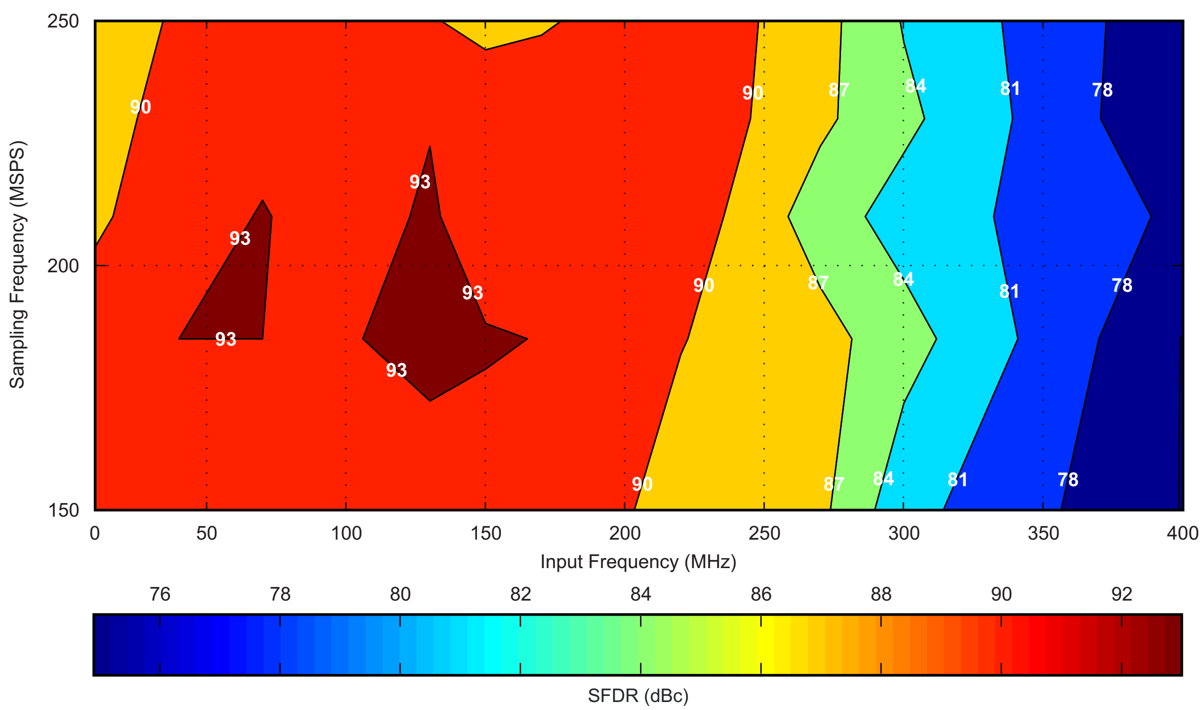


Figure 46. SPURIOUS-FREE DYNAMIC RANGE (6-dB Gain)

TYPICAL CHARACTERISTICS: Contour (continued)

All graphs are at +25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock. 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, high-performance mode disabled, 0-dB gain, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

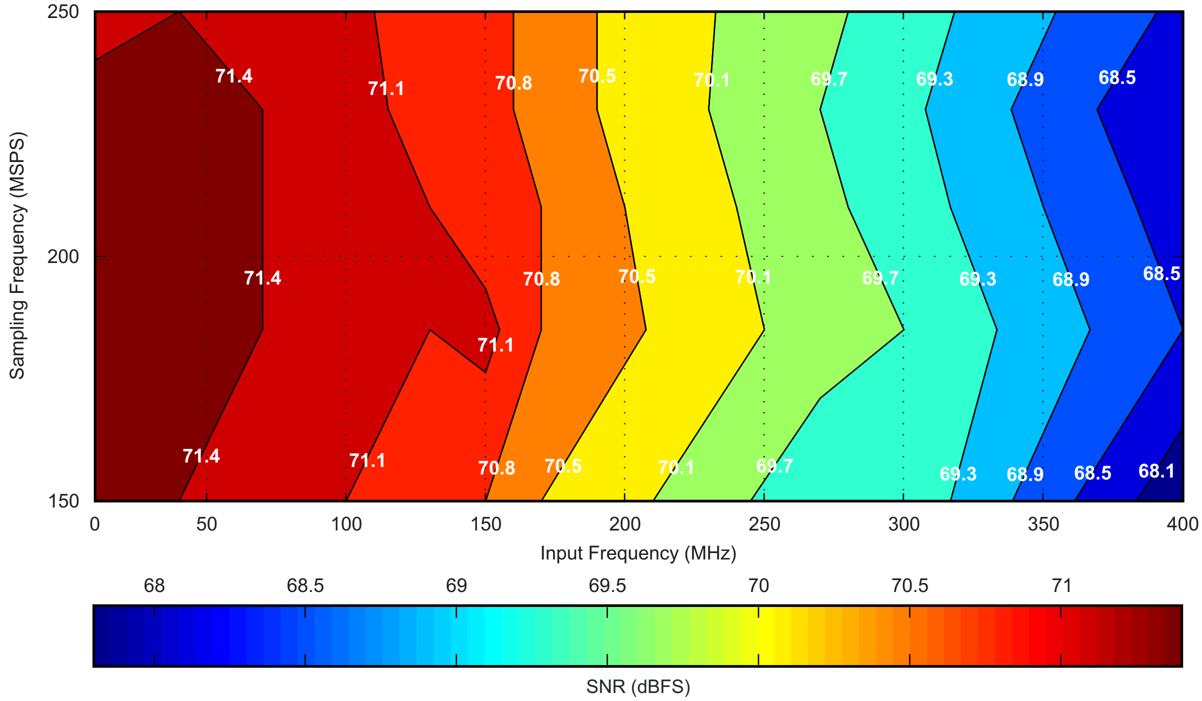


Figure 47. SIGNAL-TO-NOISE RATIO (0-dB Gain)

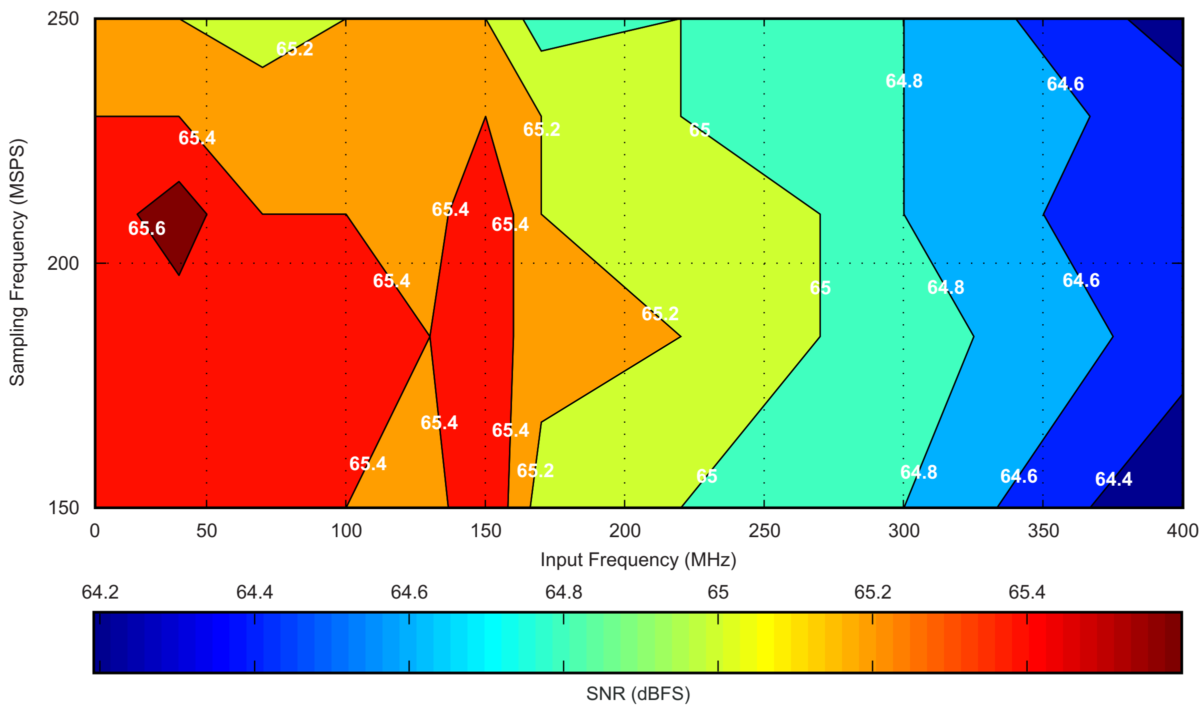


Figure 48. SIGNAL-TO-NOISE RATIO (6-dB Gain)

DEVICE CONFIGURATION

SERIAL REGISTER MAP

Table 10 summarizes the functions supported by the serial interface.

Table 10. Serial Interface Register Map(1)

<table>
<tr><th>REGISTER ADDRESS</th><th colspan="8">REGISTER DATA</th></tr>
<tr><th>A[7:0] (Hex)</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>00</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>RESET</td><td>READOUT</td></tr>
<tr><td>01</td><td colspan="6">LVDS SWING</td><td>0</td><td>0</td></tr>
<tr><td>03</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>HP[0]</td><td>0</td></tr>
<tr><td>06</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>HP[2]</td><td>HP[1]</td><td>0</td></tr>
<tr><td>25</td><td colspan="4">CH A GAIN</td><td>0</td><td colspan="3">CH A TEST PATTERNS</td></tr>
<tr><td>29</td><td>0</td><td>0</td><td>0</td><td colspan="2">DATA FORMAT</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>2B</td><td colspan="4">CH B GAIN</td><td>0</td><td colspan="3">CH B TEST PATTERNS</td></tr>
<tr><td>3D</td><td>0</td><td>0</td><td>ENABLE OFFSET CORR</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>3F</td><td>0</td><td>0</td><td colspan="6">CUSTOM PATTERN D[13:8]</td></tr>
<tr><td>40</td><td colspan="8">CUSTOM PATTERN D[7:0]</td></tr>
<tr><td>41</td><td colspan="2">LVDS CMOS</td><td colspan="2">CMOS CLKOUT STRENGTH</td><td>0</td><td>0</td><td colspan="2">DIS OBUF</td></tr>
<tr><td>42</td><td colspan="4">CLKOUT DELAY PROG</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>44</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>EN DIGITAL</td></tr>
<tr><td>45</td><td>STBY</td><td>LVDS CLKOUT STRENGTH</td><td>LVDS DATA STRENGTH</td><td>0</td><td>0</td><td>PDN GLOBAL</td><td>0</td><td>0</td></tr>
<tr><td>BA</td><td>0</td><td>0</td><td>0</td><td>0</td><td>HP[3]</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>BF</td><td colspan="4">CH A OFFSET PEDESTAL</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>C1</td><td colspan="4">CH B OFFSET PEDESTAL</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>CF</td><td>FREEZE OFFSET CORR</td><td>0</td><td colspan="4">OFFSET CORR TIME CONSTANT</td><td>0</td><td>0</td></tr>
<tr><td>D5</td><td>0</td><td>0</td><td>HP[4}</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>D9</td><td>0</td><td>0</td><td>HP[6]</td><td>0</td><td>0</td><td>0</td><td>HP[5]</td><td>0</td></tr>
<tr><td>DB</td><td>HP[9]</td><td>HP[8]</td><td>HP[7]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>LOW SPEED MODE CH B</td></tr>
<tr><td>DC</td><td>0</td><td>0</td><td>HP[11]</td><td>0</td><td>0</td><td>0</td><td>HP[10]</td><td>0</td></tr>
<tr><td>EF</td><td>0</td><td>0</td><td>0</td><td>EN LOW SPEED MODE</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>F1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="2">EN LVDS SWING</td></tr>
<tr><td>F2</td><td>0</td><td>0</td><td>0</td><td>0</td><td>LOW SPEED MODE CH A</td><td>0</td><td>0</td><td>0</td></tr>
</table>

(1) Multiple functions in a register can be programmed in a single write operation. All registers default to '0' after reset.

DESCRIPTION OF SERIAL REGISTERS

Register Address 00h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	RESET	READOUT

Bits D[7:2] **Always write '0'**

Bit D1 **RESET: Software reset applied**

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit D0 **READOUT: Serial readout**

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the SDOUT pin is placed in a high-impedance state.
1 = Serial readout enabled; the SDOUT pin functions as a serial data readout with CMOS logic levels running from the DRVDD supply. See the *Serial Register Readout* section.

Register Address 01h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
LVDS SWING						0	0

Bits D[7:2] **LVDS SWING: LVDS swing programmability**

These bits program the LVDS swing. Set the EN LVDS SWING bit to '1' before programming swing.
000000 = Default LVDS swing; ±350 mV with external 100-Ω termination
011011 = LVDS swing ±410 mV
110010 = LVDS swing ±465 mV
010100 = LVDS swing ±570 mV
111110 = LVDS swing ±200 mV
001111 = LVDS swing ±125 mV

Bits D[1:0] **Always write '0'**

Register Address 03h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	HP[0]	0

Bits D[7:2] **Always write '0'**

Bit D1 **HP[0]**

This bit improves SNR in CMOS mode, increases AVDD supply current by approximately 3 mA.

0 = Default after reset

1 = HP[0] is enabled

Bit 0 **Always write '0'**

Register Address 06h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	HP[2]	HP[1]	0

Bits D[7:3] **Always write '0'**

Bits D[2:1] **HP[2:1]**

Set bits HP[11:1] for best performance.

00 = Default after reset

11 = HP[2:1] are enabled

Bit D0 **Always write '0'**

Register Address 25h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
CH A GAIN				0	CH A TEST PATTERNS		

Bits D[7:4] **CH A GAIN: Channel A gain programmability**

These bits set the gain programmability in 0.5-dB steps for channel A.

0000 = 0-dB gain (default after reset)
0001 = 0.5-dB gain
0010 = 1-dB gain
0011 = 1.5-dB gain
0100 = 2-dB gain
0101 = 2.5-dB gain
0110 = 3-dB gain
0111 = 3.5-dB gain
1000 = 4-dB gain
1001 = 4.5-dB gain
1010 = 5-dB gain
1011 = 5.5-dB gain
1100 = 6-dB gain

Bit D3 **Always write '0'**

Bits D[2:0] **CH A TEST PATTERNS: Channel A data capture**

These bits verify data capture for channel A.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern.
The output data D[13:0] are an alternating sequence of *10101010101010* and *01010101010101*.
100 = Outputs digital ramp.
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

Register Address 29h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	DATA FORMAT		0	0	0

Bits D[7:5] **Always write '0'**

Bits D[4:3] **DATA FORMAT: Data format selection**

00 = Twos complement
01 = Twos complement
10 = Twos complement
11 = Offset binary

Bits D[2:0] **Always write '0'**

Register Address 2Bh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
CH B GAIN				0	CH B TEST PATTERNS		

Bits D[7:4] **CH B GAIN: Channel B gain programmability**

These bits set the gain programmability in 0.5-dB steps for channel B.

0000 = 0-dB gain (default after reset)
0001 = 0.5-dB gain
0010 = 1-dB gain
0011 = 1.5-dB gain
0100 = 2-dB gain
0101 = 2.5-dB gain
0110 = 3-dB gain
0111 = 3.5-dB gain
1000 = 4-dB gain
1001 = 4.5-dB gain
1010 = 5-dB gain
1011 = 5.5-dB gain
1100 = 6-dB gain

Bit D3 **Always write '0'**

Bits D[2:0] **CH B TEST PATTERNS: Channel B data capture**

These bits verify data capture for channel B.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern.
The output data D[11:0] are an alternating sequence of *10101010101010* and *01010101010101*.
100 = Outputs digital ramp.
101 = Outputs custom pattern; use registers 3Fh and 40h to set the custom pattern
110 = Unused
111 = Unused

Register Address 3Dh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	ENABLE OFFSET CORR	0	0	0	0	0

Bits D[7:6] **Always write '0'**

Bit D5 **ENABLE OFFSET CORR: Offset correction setting**

This bit enables the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

Bits D[4:0] **Always write '0'**

Register Address 3Fh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	CUSTOM PATTERN D13	CUSTOM PATTERN D12	CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8

Bits D[7:6] **Always write '0'**

Bits D[5:0] **CUSTOM PATTERN D[13:8]**

These are the six upper bits of the custom pattern available at the output instead of ADC data.
The ADS42B49 custom pattern is 14-bit.

Register Address 40h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
CUSTOM PATTERN D7	CUSTOM PATTERN D6	CUSTOM PATTERN D5	CUSTOM PATTERN D4	CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0

Bits D[7:0] **CUSTOM PATTERN D[7:0]**

These are the eight lower bits of the custom pattern available at the output instead of ADC data.
The ADS42B49 custom pattern is 14-bit; use the CUSTOM PATTERN D[13:0] register bits.

Register Address 41h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
LVDS CMOS		CMOS CLKOUT STRENGTH		0	0	DIS OBUF	

Bits D[7:6] **LVDS CMOS: Interface selection**

These bits select the interface.
00 = DDR LVDS interface
01 = DDR LVDS interface
10 = DDR LVDS interface
11 = Parallel CMOS interface

Bits D[5:4] **CMOS CLKOUT STRENGTH**

These bits control the strength of the CMOS output clock.
00 = Maximum strength (recommended)
01 = Medium strength
10 = Low strength
11 = Very low strength

Bits D[3:2] **Always write '0'**

Bits D[1:0] **DIS OBUF**

These bits power down data and clock output buffers for both the CMOS and LVDS output interface. When powered down, the output buffers are in 3-state.
00 = Default
01 = Power-down data output buffers for channel B
10 = Power-down data output buffers for channel A
11 = Power-down data output buffers for both channels as well as the clock output buffer

Register Address 42h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
CLKOUT DELAY PROG				0	0	0	0

Bits D[7:4] **CLKOUT DELAY PROG**

These bits are useful to delay output clock in LVDS mode to optimize setup and hold time. Typical delay in output clock obtained by these bits in LVDS mode is given below:
0000 = Default
0001 = 190 ps
0010 = 350 ps
0011 = 700 ps
0111 = 1000 ps
1011 = 1250 ps
1111 = 1450 ps
Others = Do not use

Bits D[3:0] **Always write '0'**

Register Address 44h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	EN DIGITAL

Bits D[7:1] **Always write '0'**

Bit D0 **EN DIGITAL: Digital function enable**

0 = Default

1 = Digital functions including test pattern are enabled

Register Address 45h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
STBY	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH	0	0	PDN GLOBAL	0	0

Bit D7 **STBY: Standby setting**

0 = Normal operation
1 = Both channels are put in standby; wake-up time from this mode is fast (typically 50 µs).

Bit D6 **LVDS CLKOUT STRENGTH: LVDS output clock buffer strength setting**

0 = LVDS output clock buffer at default strength to be used with 100-Ω external termination
1 = LVDS output clock buffer has double strength to be used with 50-Ω external termination

Bit D5 **LVDS DATA STRENGTH**

0 = All LVDS data buffers at default strength to be used with 100-Ω external termination
1 = All LVDS data buffers have double strength to be used with 50-Ω external termination

Bits D[4:3] **Always write '0'**

Bit D2 **PDN GLOBAL**

0 = Normal operation
1 = Total power down; all ADC channels, internal references, and output buffers are powered down. Wake-up time from this mode is slow (typically 100 µs).

Bits D[1:0] **Always write '0'**

Register Address BAh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	HP[3]	0	0	0

Bits D[7:4] **Always write '0'**

Bit D3 **HP[3]**

Set bits HP[11:1] for best performance.

0 = Default after reset

1 = HP[3] is enabled

Bits D[2:0] **Always write '0'**

Register Address BFh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
CH A OFFSET PEDESTAL						0	0

Bits D[7:4] **CH A OFFSET PEDESTAL: Channel A offset pedestal selection**

When the offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits. See the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.
The pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+31 by adding pedestal D[7:2].

Program bits D[7:2]

011111 = Midcode+31
011110 = Midcode+30
011101 = Midcode+29
…
000010 = Midcode+2
000001 = Midcode+1
000000 = Midcode
111111 = Midcode-1
111110 = Midcode-2
…
100000 = Midcode-32

Bits D[3:0] **Always write '0'**

Register Address C1h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
CH B OFFSET PEDESTAL						0	0

Bits D[7:4] **CH B OFFSET PEDESTAL: Channel B offset pedestal selection**

When offset correction is enabled, the final converged value after the offset is corrected is the ADC midcode value. A pedestal can be added to the final converged value by programming these bits; see the *Offset Correction* section. Channels can be independently programmed for different offset pedestals by choosing the relevant register address.
The pedestal ranges from –32 to +31, so the output code can vary from midcode-32 to midcode+31 by adding pedestal D7-D2.

Program Bits D[7:2]

011111 = Midcode+31
011110 = Midcode+30
011101 = Midcode+29
…
000010 = Midcode+2
000001 = Midcode+1
000000 = Midcode
111111 = Midcode-1
111110 = Midcode-2
…
100000 = Midcode-32

Bits D[3:0] **Always write '0'**

Register Address CFh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0

Bit D7 **FREEZE OFFSET CORR: Freeze offset correction setting**

This bit sets the freeze offset correction estimation.
0 = Estimation of offset correction is not frozen (the EN OFFSET CORR bit must be set)
1 = Estimation of offset correction is frozen (the EN OFFSET CORR bit must be set); when frozen, the last estimated value is used for offset correction of every clock cycle. See the *Offset Correction* section.

Bit D6 **Always write '0'**

Bits D[5:2] **OFFSET CORR TIME CONSTANT**

The offset correction loop time constant in number of clock cycles. Refer to the *Offset Correction* section.

Bits D[1:0] **Always write '0'**

Register Address D5h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	HP[4]	0	0	0	0	0

Bits D[7:6] **Always write '0'**

Bit D5 **HP[4]**

Set bits HP[11:1] for best performance.

0 = Default after Reset

1 = HP[4] is enabled

Bits D[4:0] **Always write '0'**

Register Address D9h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	HP[6]	0	0	0	HP[5]	0

Bits D[7:6] **Always write '0'**

Bit D5 **HP[6]**

Set bits HP[11:1] for best performance.

0 = Default after reset

1 = HP[6] is enabled

Bits D[4:2] **Always write '0'**

Bit D1 **HP[5]**

Set bits HP[11:1] for best performance.

0 = Default after reset

1 = HP[5] is enabled

Bit D0 **Always write '0'**

Register Address DBh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
HP[9]	HP[8]	HP[7]	0	0	0	0	LOW SPEED MODE CH B

Bits D[7:5] **HP[9:7]**

Bit D5 **HP[6]**

Set bits HP[11:1] for best performance.

000 = Default after reset

111 = HP[9:7] are enabled

Bits D[4:1] **Always write '0'**

Bit D0 **LOW SPEED MODE CH B: Channel B low-speed mode enable**

This bit enables the low-speed mode for channel B. Set the EN LOW SPEED MODE bit to '1' before using this bit.
0 = Low-speed mode is disabled for channel B
1 = Low-speed mode is enabled for channel B

Register Address DCh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	HP[11]	0	0	0	HP[10]	0

Bits D[7:6] **Always write '0'**

Bit D5 **HP[11]**

Set bits HP[11:1] for best performance.

0 = Default after reset

1 = HP[11] is enabled

Bits D[4:2] **Always write '0'**

Bit D1 **HP[10]**

Set bits HP[11:1] for best performance.

0 = Default after reset

1 = HP[10] is enabled

Bit D0 **Always write '0'**

Register Address EFh (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	EN LOW SPEED MODE	0	0	0	0

Bits D[7:5] **Always write '0'**

Bit D4 **EN LOW SPEED MODE: Enable control of low-speed mode through serial register bits**

This bit enables the control of the low-speed mode using the LOW SPEED MODE CH B and LOW SPEED MODE CH A register bits.
0 = Low-speed mode is disabled
1 = Low-speed mode is controlled by serial register bits

Bits D[3:0] **Always write '0'**

Register Address F1h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	EN LVDS SWING	

Bits D[7:2] **Always write '0'**

Bits D[1:0] **EN LVDS SWING: LVDS swing enable**

These bits enable LVDS swing control using the LVDS SWING register bits.
00 = LVDS swing control using the LVDS SWING register bits is disabled
01 = Do not use
10 = Do not use
11 = LVDS swing control using the LVDS SWING register bits is enabled

Register Address F2h (Default = 00h)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	LOW SPEED MODE CH A	0	0	0

Bits D[7:4] **Always write '0'**

Bit D3 **LOW SPEED MODE CH A: Channel A low-speed mode enable**

This bit enables the low-speed mode for channel A. Set the EN LOW SPEED MODE bit to '1' before using this bit.
0 = Low-speed mode is disabled for channel A
1 = Low-speed mode is enabled for channel A

Bits D[2:0] **Always write '0'**

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS42B49 belongs to a family of buffered analog input and ultralow-power analog-to-digital converters (ADCs) with maximum sampling rates up to 250 MSPS. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 11 clock cycles. The output is available as 14-bit data, in DDR LVDS mode or CMOS mode, and coded in either straight offset binary or binary twos complement format.

ANALOG INPUT

The analog input pins have analog buffers (running off the AVDD_BUF supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (10-kΩ dc resistance and 2.5-pF input capacitance). The buffer helps to isolate the external driving source from the switching currents of the sampling circuit. This buffering makes driving the buffered inputs easier than when compared to an ADC without the buffer.

The input common-mode is set internally using a 5-kΩ resistor from each input pin to VCM so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing.

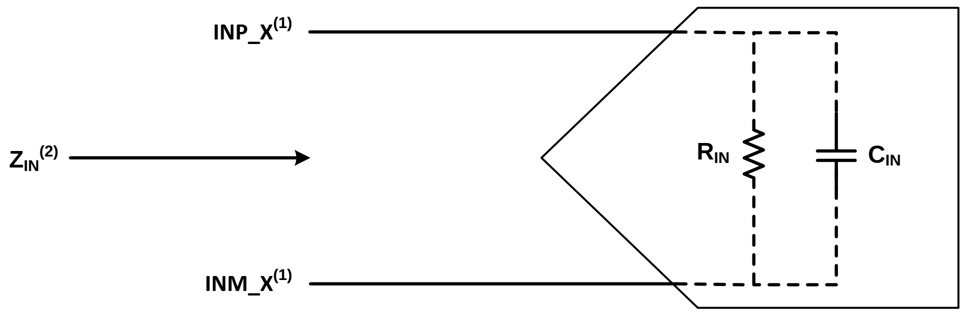
The input sampling circuit has a high 3-dB bandwidth that extends up to 700 MHz (measured with 50-Ω source driving 50-Ω termination between INP and INM).

The dynamic offset of the first-stage sub-ADC limits the maximum analog input frequency to approximately 400 MHz (with 2-V_{PP} amplitude) and to approximately 500 MHz (with 1.6-V_{PP} amplitude) before the performance degrades. This offset is separate from the full-power analog bandwidth of 700 MHz, which is only an indicator of signal amplitude versus frequency.

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (5 Ω to 10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 49, Figure 50, and Figure 51 show the differential impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) at the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1 GHz.



(1) X = A or B.

(2) $Z_{IN} = R_{IN} \parallel (1/j\omega C_{IN})$.

Figure 49. ADC Equivalent Input Impedance

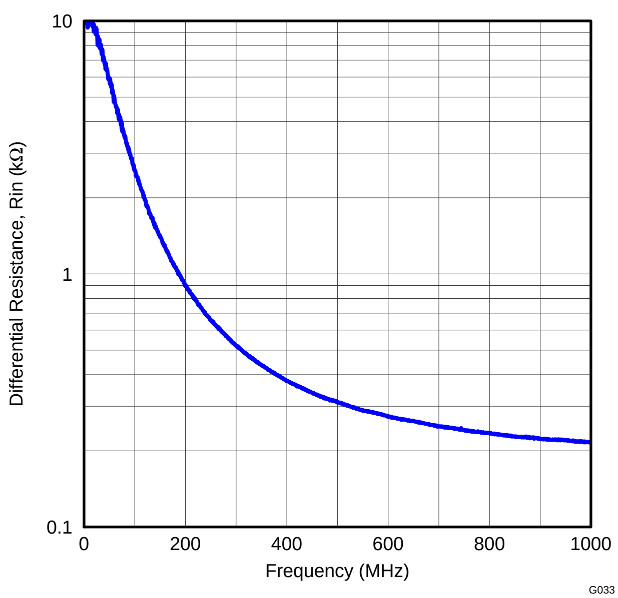


Figure 50. ADC Analog Input Resistance (R_{IN}) Across Frequency

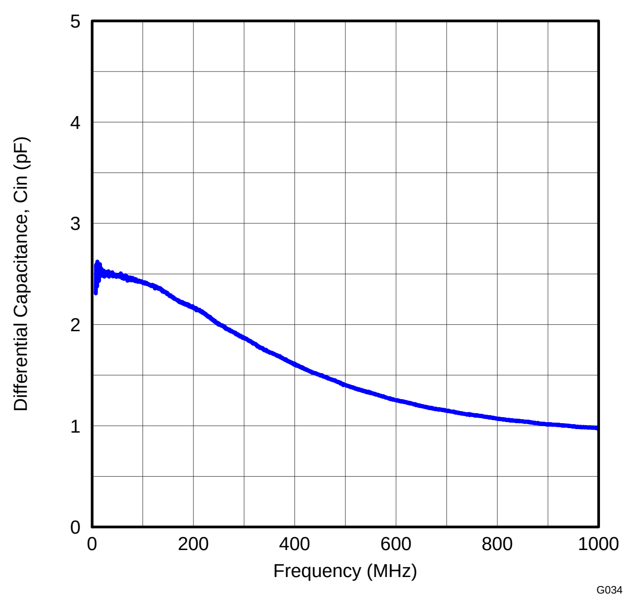


Figure 51. ADC Analog Input Capacitance (C_{IN}) Across Frequency

Driving Circuit

Example driving circuit configuration is shown in Figure 52. Notice that the board circuitry is simplified compared to the non-buffered ADS4249.

To optimize even-harmonic performance at high input frequencies (greater than the first Nyquist), the use of back-to-back transformers is recommended, as shown in Figure 52. Note that the drive circuit is terminated by 50 Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage.

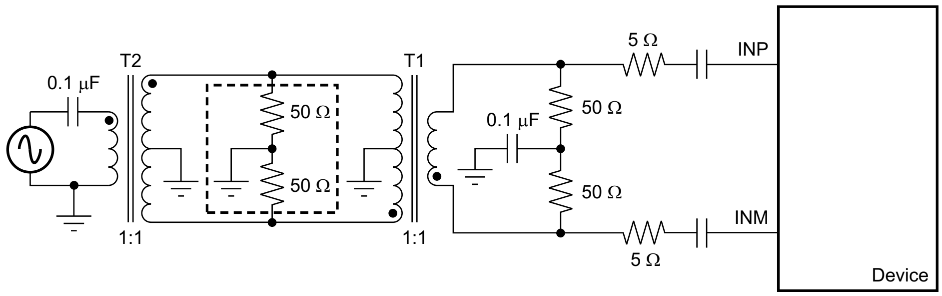


Figure 52. Drive Circuit for High Input Frequencies

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 52. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50-Ω source impedance).

CLOCK INPUT

The ADS42B49 clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources are shown in Figure 53, Figure 54 and Figure 55. See Figure 56 details the internal clock buffer.

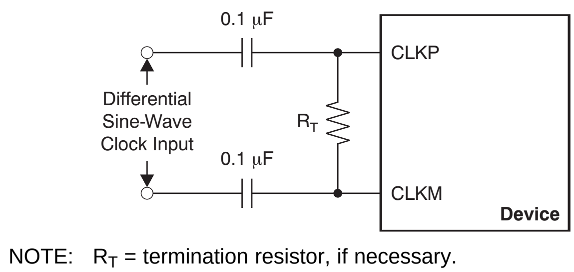


Figure 53. Differential Sine-Wave Clock Driving Circuit

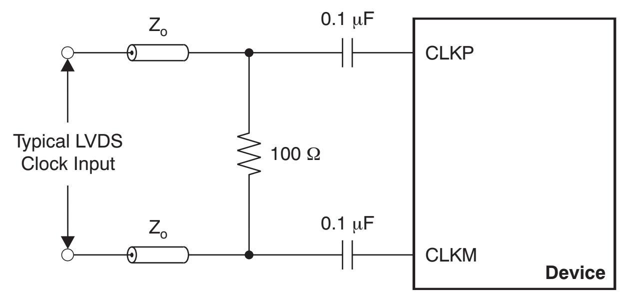


Figure 54. LVDS Clock Driving Circuit

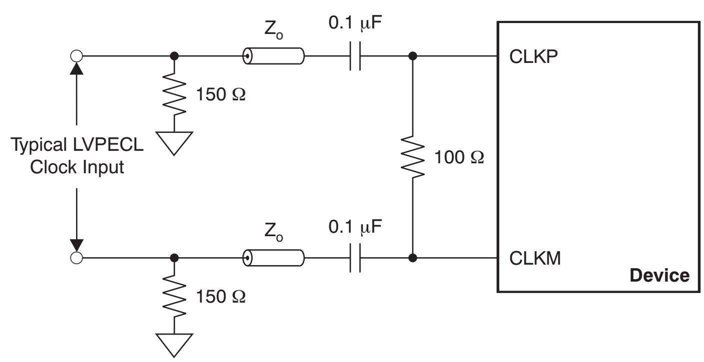
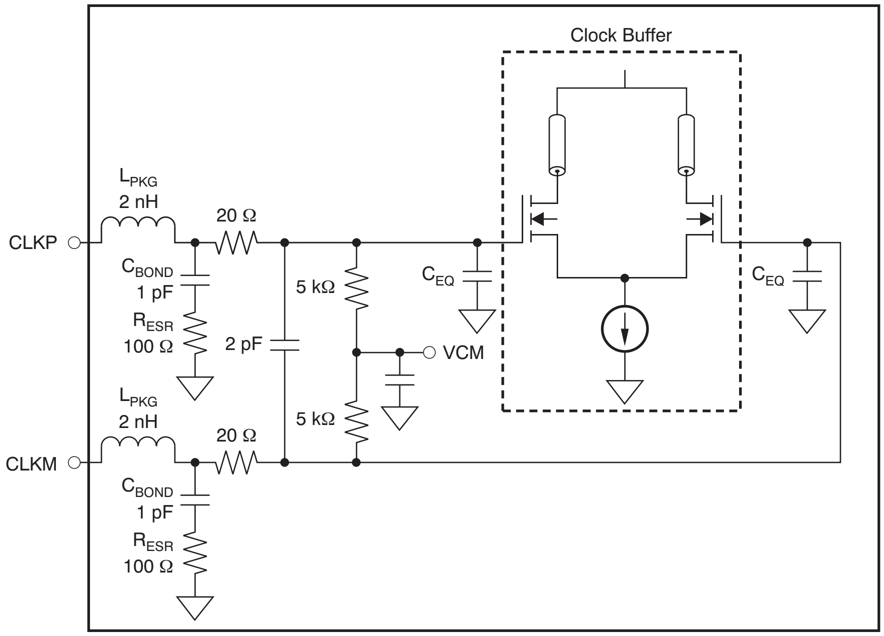


Figure 55. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 56. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-μF capacitor, as shown in Figure 57. For best performance, the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

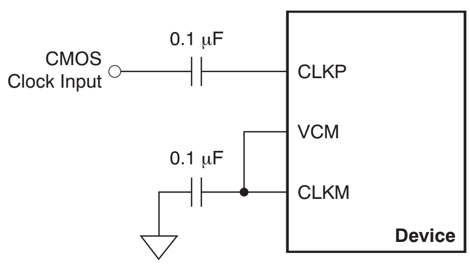


Figure 57. Single-Ended Clock Driving Circuit

DIGITAL FUNCTIONS

The device has several useful digital functions (such as test patterns, gain, and offset correction). These functions require extra clock cycles for operation and increase the overall latency and power of the device. These digital functions are disabled by default after reset and the raw ADC output is routed to the output data pins with a latency of 16 clock cycles. Figure 58 shows more details of the processing after the ADC. In order to use any of the digital functions, the EN DIGITAL bit must be set to '1'. After this, the respective register bits must be programmed as described in the following sections and in the *Serial Register Map* section.

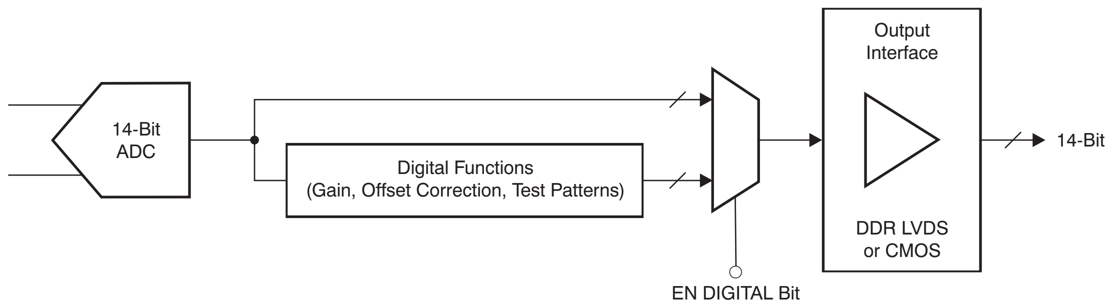


Figure 58. Digital Processing Block

GAIN FOR SFDR AND SNR TRADE-OFF

The ADS42B49 includes gain settings that can be used to get improved SFDR performance (compared to no gain). The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 11.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5 dB and 1 dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB.

Table 11. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V_{PP})
0	Default after reset	1.9
1	Fine, programmable	1.69
2	Fine, programmable	1.51
3	Fine, programmable	1.35
4	Fine, programmable	1.2
5	Fine, programmable	1.07
6	Fine, programmable	0.95

OFFSET CORRECTION

The ADS42B49 has an internal offset correction algorithm that estimates and corrects dc offset up to ±10 mV. The correction can be enabled using the ENABLE OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 12.

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 0. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by default after reset.

Table 12. Time Constant of Offset Correction Algorithm

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1 / f_S$ (ms)(1)
0000	1 M	4
0001	2 M	8
0010	4 M	16.7
0011	8 M	33.5
0100	16 M	67
0101	32 M	134
0110	64 M	268
0111	128 M	537
1000	256 M	1010
1001	512 M	2150
1010	1 G	4300
1011	2 G	8600
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

(1) Sampling frequency, f_S = 250 MSPS.

POWER-DOWN

The ADS42B49 has two power-down modes: global power-down and channel standby. These modes can be set using either the serial register bits or using the control pins CTRL1 to CTRL3 (as shown in Table 13).

Table 13. Power-Down Settings

CTRL1	CTRL2	CTRL3	DESCRIPTION
Low	Low	Low	Default
Low	Low	High	Not available
Low	High	Low	Not available
Low	High	High	Not available
High	Low	Low	Partial power-down
High	Low	High	Channel A powered down, channel B is active
High	High	Low	Not available
High	High	High	MUX mode of operation, channel A and B data is multiplexed and output on DB[10:0] pins

Global Power-Down

In this mode, the entire chip (including ADCs, internal reference, and output buffers) are powered down, resulting in reduced total power dissipation of typically less than 10 mW when the PDN GLOBAL serial register bit is used. The output buffers are in high-impedance state. The wake-up time from global power-down to data becoming valid in normal mode is typically 100 µs.

Channel Standby

In this mode, each ADC channel is powered down. The internal references are active, resulting in a quick wake-up time of 50 µs. The total power dissipation in standby is approximately 240 mW at 250 MSPS.

Input Clock Stop

In addition to the previous modes, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is approximately 190 mW.

DIGITAL OUTPUT INFORMATION

The ADS42B49 provides 14-bit digital data for each channel and an output clock synchronized with the data.

Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the serial interface register bit or by setting the proper voltage on the SEN pin in parallel configuration mode.

DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 59.

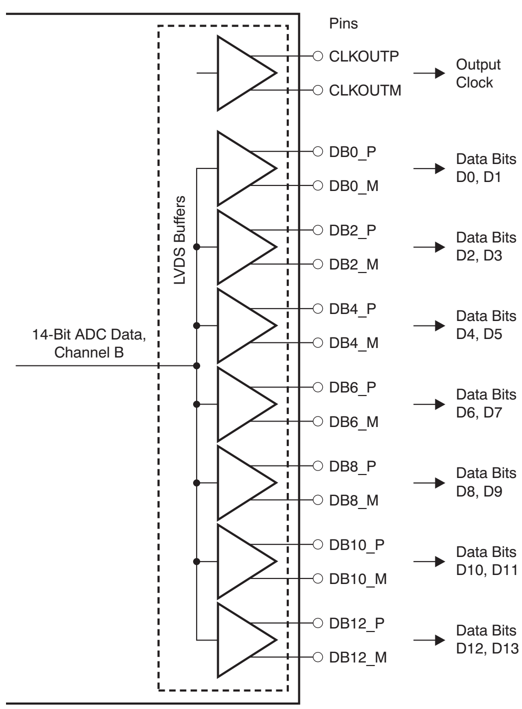


Figure 59. LVDS Interface

Even data bits (D0, D2, D4, and so forth) are output at the CLKOUTP rising edge and the odd data bits (D1, D3, D5, and so forth) are output at the CLKOUTP falling edge. Both the CLKOUTP rising and falling edges must be used to capture all the data bits, as shown in Figure 60.

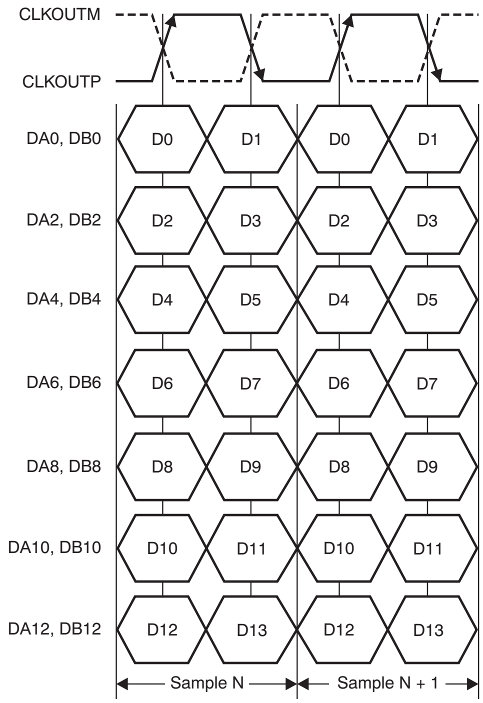
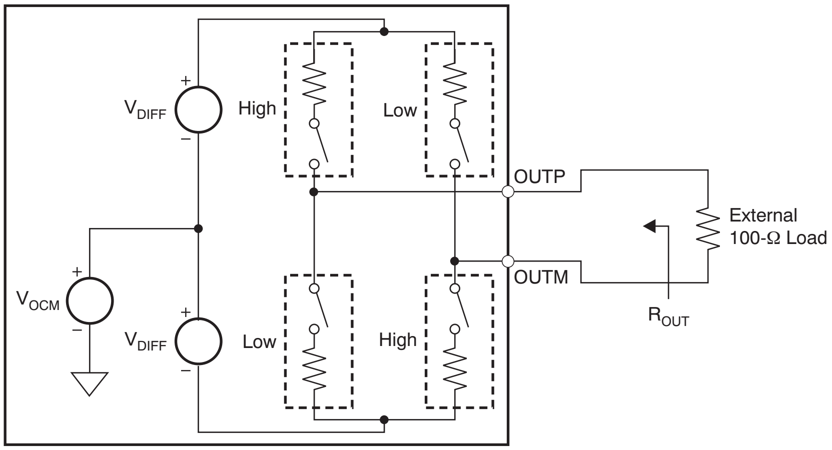


Figure 60. DDR LVDS Interface Timing

LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 61. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100-Ω termination.



NOTE: Default swing across 100-Ω load is ±350 mV. Use the LVDS SWING bits to change the swing.

Figure 61. LVDS Buffer Equivalent Circuit

The V_{DIFF} voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100-Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±125 mV to ±570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50-Ω differential termination, as shown in Figure 62. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100-Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.

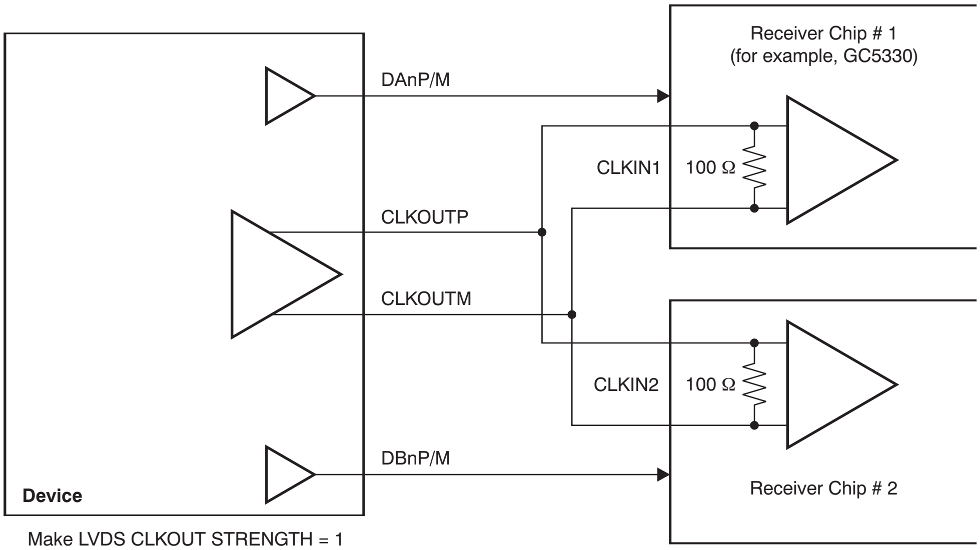


Figure 62. LVDS Buffer Differential Termination

Parallel CMOS Interface

In the CMOS mode, each data bit is output on separate pins as CMOS voltage level, every clock cycle, as Figure 63 shows. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. TI recommends minimizing the load capacitance of the data and clock output pins by using short traces to the receiver. Furthermore, match the output data and clock traces to minimize the skew between them.

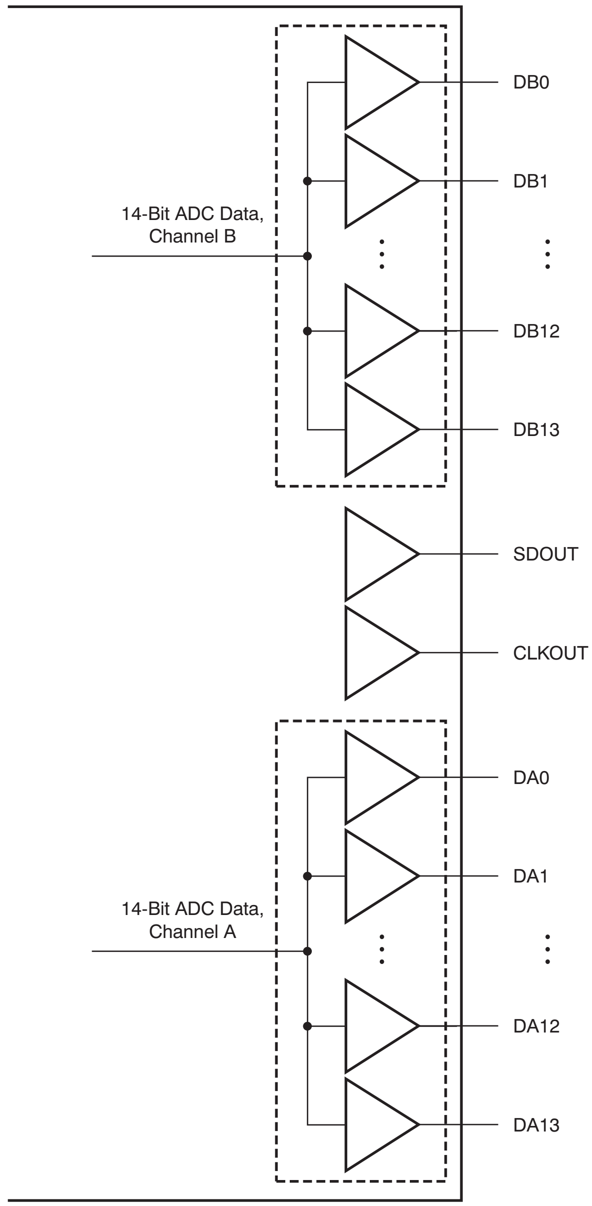


Figure 63. CMOS Outputs

CMOS Interface Power Dissipation

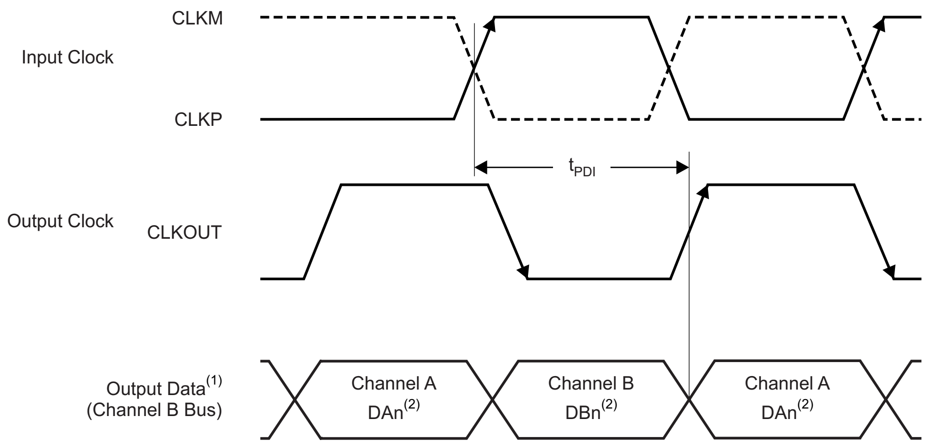
With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between '0' and '1' every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal. This relationship is shown by the formula:

Digital current as a result of CMOS output switching = $C_L \times DRVDD \times (N \times F_{AVG})$,

where C_L = load capacitance, $N \times F_{AVG}$ = average number of output bits switching.

Multiplexed Mode of Operation

In this mode, the digital outputs of both channels are multiplexed and output on a single bus (DB[11:0] pins), as shown in Figure 64. The channel A output pins (DA[11:0]) are in 3-state. Because the output data rate on the DB bus is effectively doubled, this mode is recommended only for low sampling frequencies (less than 125 MSPS). This mode can be enabled by the CTRL[3:1] parallel pins.



(1) In multiplexed mode, the output of both channels comes on the channel B output pins.

(2) Dn = bits D0, D1, D2, and so forth

Figure 64. Multiplexed Mode Timing Diagram

Output Data Format

Two output data formats are supported: twos complement and offset binary. The format can be selected using the DATA FORMAT serial interface register bit.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 3FFFh for the ADS42B49 in offset binary output format; the output code is 1FFFh for the ADS42B49 in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 2000h for the ADS42B49 in twos complement output format.

DEFINITION OF SPECIFICATIONS

Analog Bandwidth: The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay: The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs. This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter): The sample-to-sample variation in aperture delay.

Clock Pulse Width and Duty Cycle: The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate: The maximum sampling rate at which specified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate: The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL): An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

Integral Nonlinearity (INL): The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error: Gain error is the deviation of the ADC actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy (E_{GREF}) and error as a result of the channel (E_{GCHAN}). Both errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from (1 – 0.5 / 100) x FS_{ideal} to (1 + 0.5 / 100) x FS_{ideal}.

Offset Error: The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into millivolts.

Temperature Drift: The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}. Temperature drift is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} - T_{MIN}$.

Signal-to-Noise Ratio (SNR): SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$\text{SNR} = 10\text{Log}^{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD): SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$\text{SINAD} = 10\text{Log}^{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB): ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (3)$$

Total Harmonic Distortion (THD): THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$\text{THD} = 10\text{Log}^{10}\ \frac{P_S}{P_N} \quad (4)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR): The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion (IMD3): IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR): DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR): AC PSRR is the measure of rejection of variations in the supply voltage by the ADC. If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$\text{PSRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \ \text{(Expressed in dBc)} \quad (5)$$

Voltage Overload Recovery: The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs. This is tested by separately applying a sine wave signal with 6 dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR): CMRR is the measure of rejection of variation in the analog input common-mode by the ADC. If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

$$\text{CMRR} = 20\text{Log}^{10}\ \frac{\Delta V_{OUT}}{\Delta V_{CM}} \ \text{(Expressed in dBc)} \quad (6)$$

Crosstalk (only for multichannel ADCs): Crosstalk is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. Crosstalk is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel). Crosstalk is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. Crosstalk is typically expressed in dBc.

BOARD DESIGN CONSIDERATIONS

Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the *ADS4226 Evaluation Module* (SLAU333) for details on layout and grounding.

Supply Decoupling

Because the ADS42B49 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

Exposed Pad

In addition to providing a path for heat dissipation, the PowerPAD is also electrically connected internally to the digital ground. Therefore, the exposed pad must be soldered to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines* (SLOA122) and *QFN/SON PCB Attachment* (SLUA271).

Routing Analog Inputs

TI advises routing differential analog input pairs (INP_x and INM_x) close to each other. To minimize the possibility of coupling from a channel analog input to the sampling clock, the analog input pairs of both channels should be routed perpendicular to the sampling clock; see the *ADS4226 Evaluation Module* (SLAU333) for reference routing. Figure 65 shows a snapshot of the PCB layout from the ADS42xxEVM.

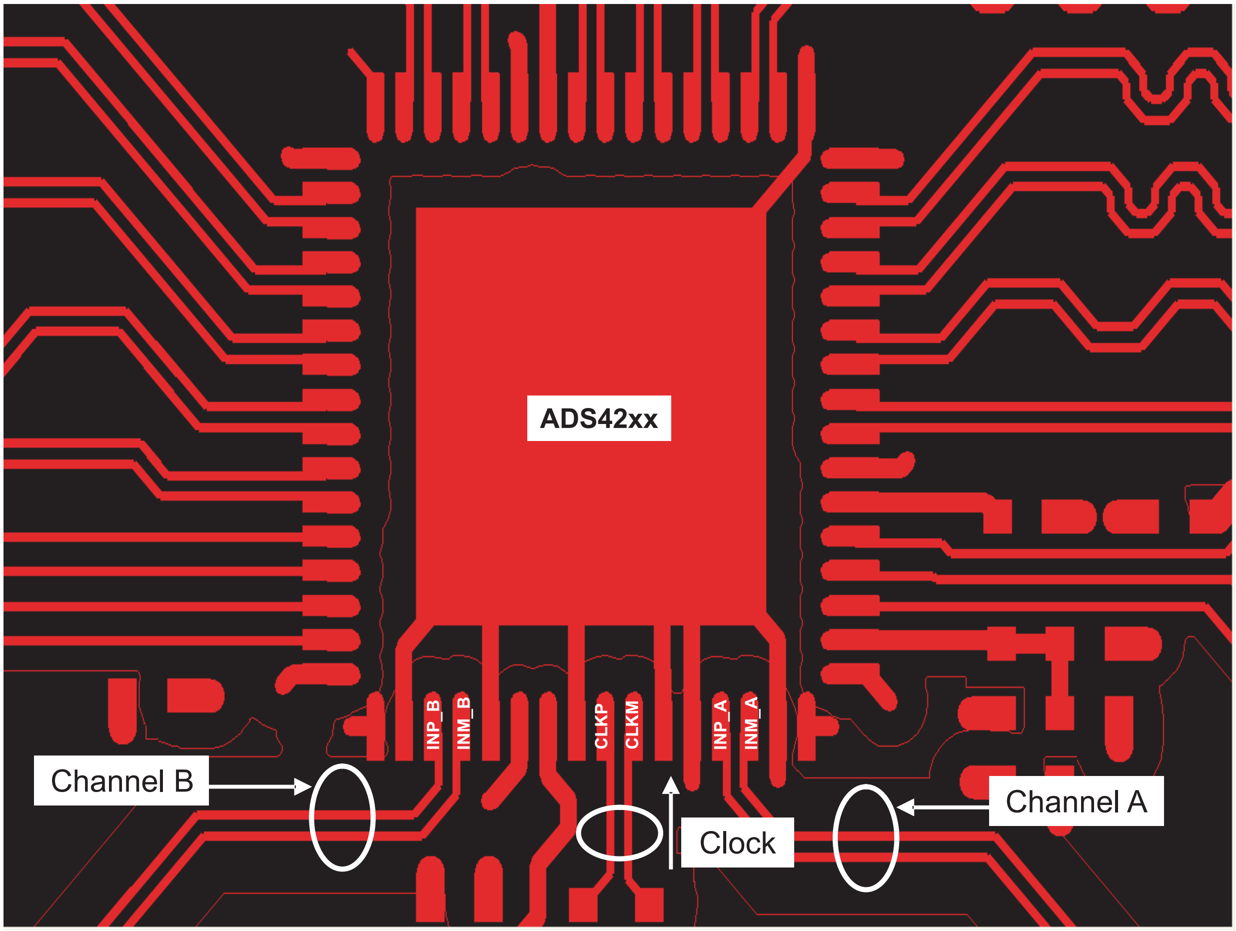


Figure 65. ADS42xxEVM PCB Layout

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2012) to Revision B **Page**

- Changed first two sentences in Description of High-Performance Modes table 4
- Changed footnote for Table 3 9
- Changed D2 and D1 bit names in address 03h of Table 10 33
- Changed Register Address 03h 34

Changes from Original (December 2012) to Revision A **Page**

- Changed product status from Product Preview to Production Data 1
- Changed Analog Inputs, V_{ID} parameter nominal specification in Recommended Operating Conditions table 4
- Changed Analog Inputs, *Maximum analog input frequency* parameter rows in Recommended Operating conditions table 4
- Changed footnote 1 in Recommended Operating Conditions table 4
- Changed *PSRR* parameter test conditions in Electrical Characteristics: ADS42B49 table 6
- Deleted DNL and INL rows from Electrical Characteristics: ADS42B49 table 6
- Changed Analog Inputs, V_{ID} parameter typical specification in Electrical Characteristics: General table 6
- Deleted Analog Inputs, *Analog input common-mode current* row from Electrical Characteristics: General table 6
- Changed DC Accuracy, *Offset error* parameter typical specification in Electrical Characteristics: General table 6
- Changed Power Supply, *IDRVDD* parameter CMOS interface row in Electrical Characteristics: General table 6
- Changed Power Supply, *Digital power, CMOS interface* parameter typical specification in Electrical Characteristics: General table 6
- Changed t_J parameter typical specification in Timing Requirements table 8
- Deleted Wakeup time maximum specifications in Timing Requirements table 8
- Changed footnote 1 in Timing Requirements table 8
- Changed ADC latency, default after reset typical specification in Timing Requirements table 8
- Changed *ADC latency* parameter typical specification in Timing Requirements table 8
- Added t_{PDI} specifications to Timing Requirements table 8
- Updated Figure 4 11
- Updated Figure 5 12
- Changed CTRL1, CTRL2, and CTRL3 control mode description in Table 4 18
- Changed first column of (5 / 8) AVDD row in Table 6 19
- Changed sixth row in Table 7 19
- Changed third paragraph in the *Serial Register Readout* section 22
- Changed Register Address 06h in *Description of Serial Registers* section 35
- Filled in TBD in *Theory of Operation* section 45
- Added *Analog Input* section 45
- Added Figure 49 to *Drive Circuit Requirements* section 46
- Changed description of *Driving Circuit* section 47
- Changed description of *Multiplexed Mode of Operation* section 56

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS42B49IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85		Samples
ADS42B49IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	AZ42B49I	Samples
ADS42B49IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR	-40 to 85	AZ42B49I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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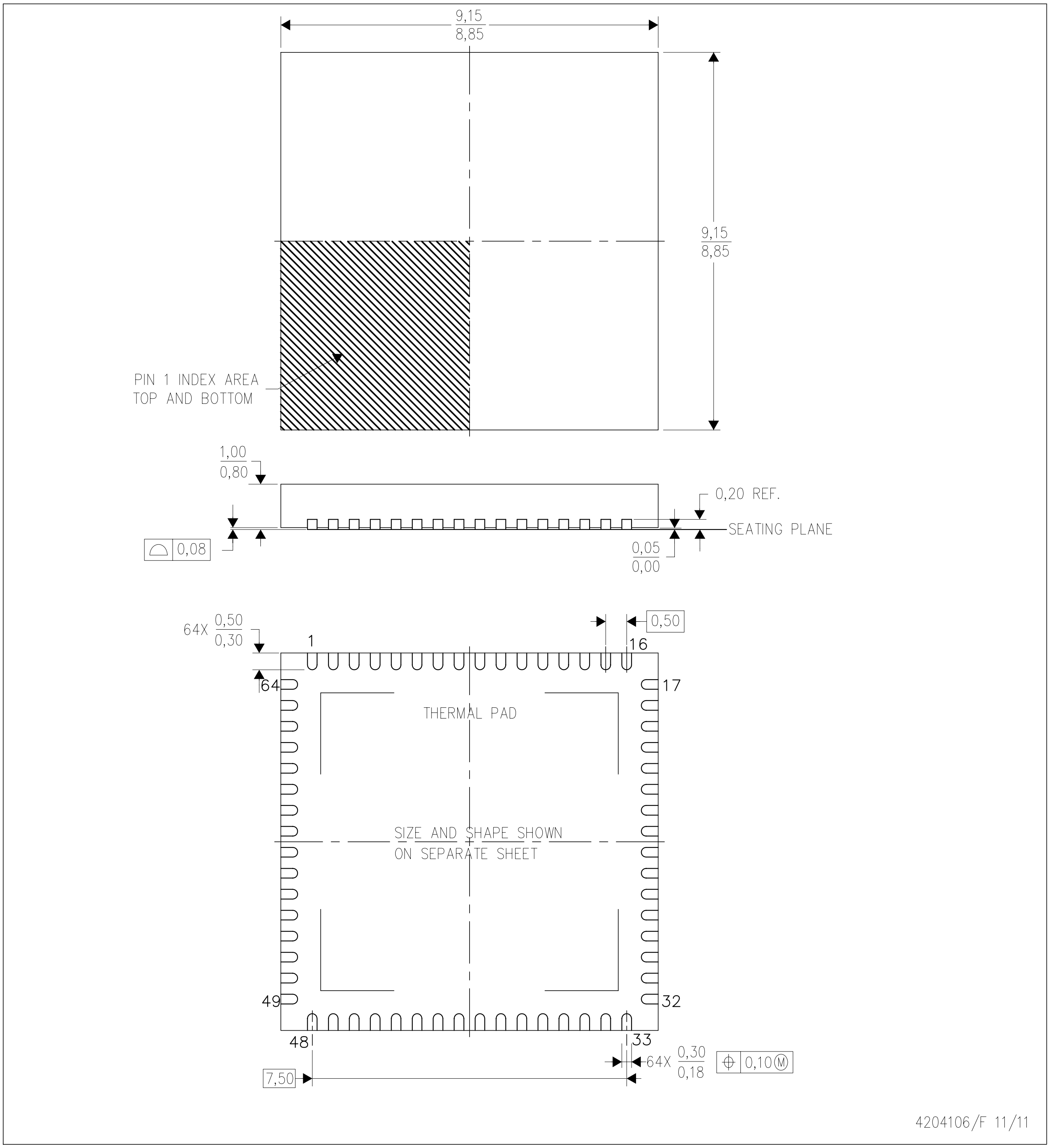
RGC(S-PVQFN-N64)   CUSTOM DEVICE   PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

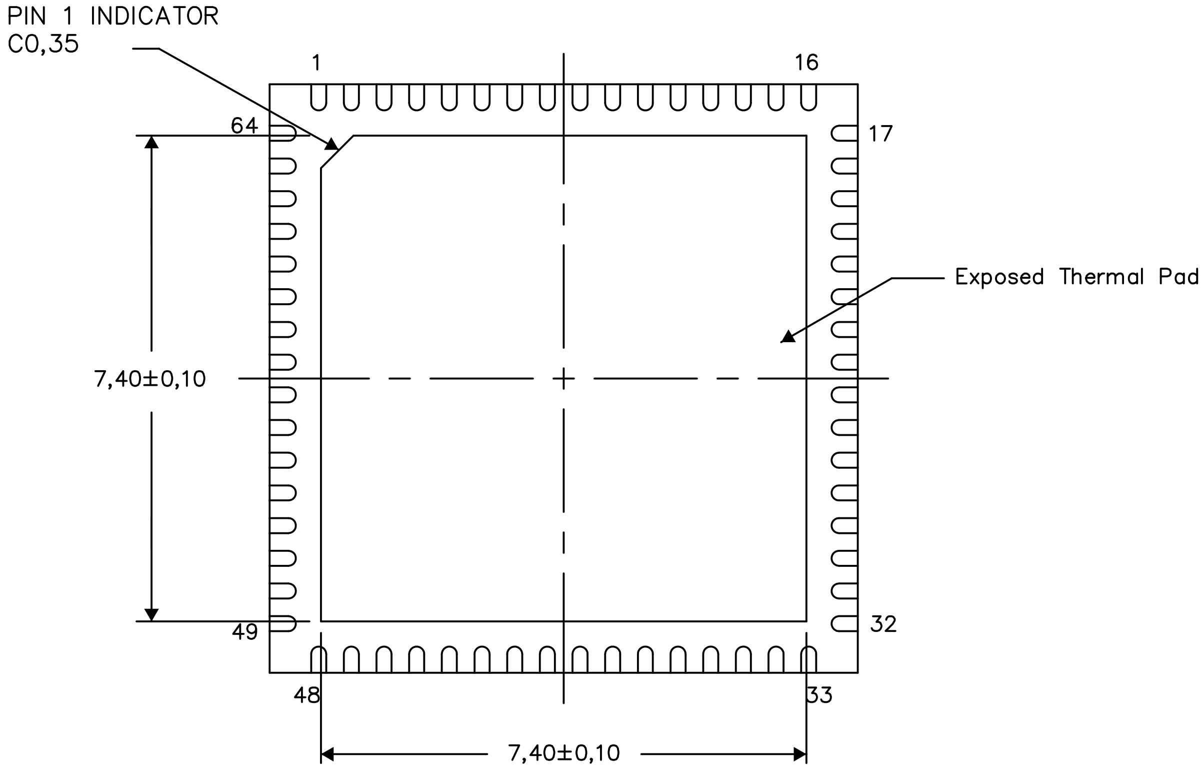
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



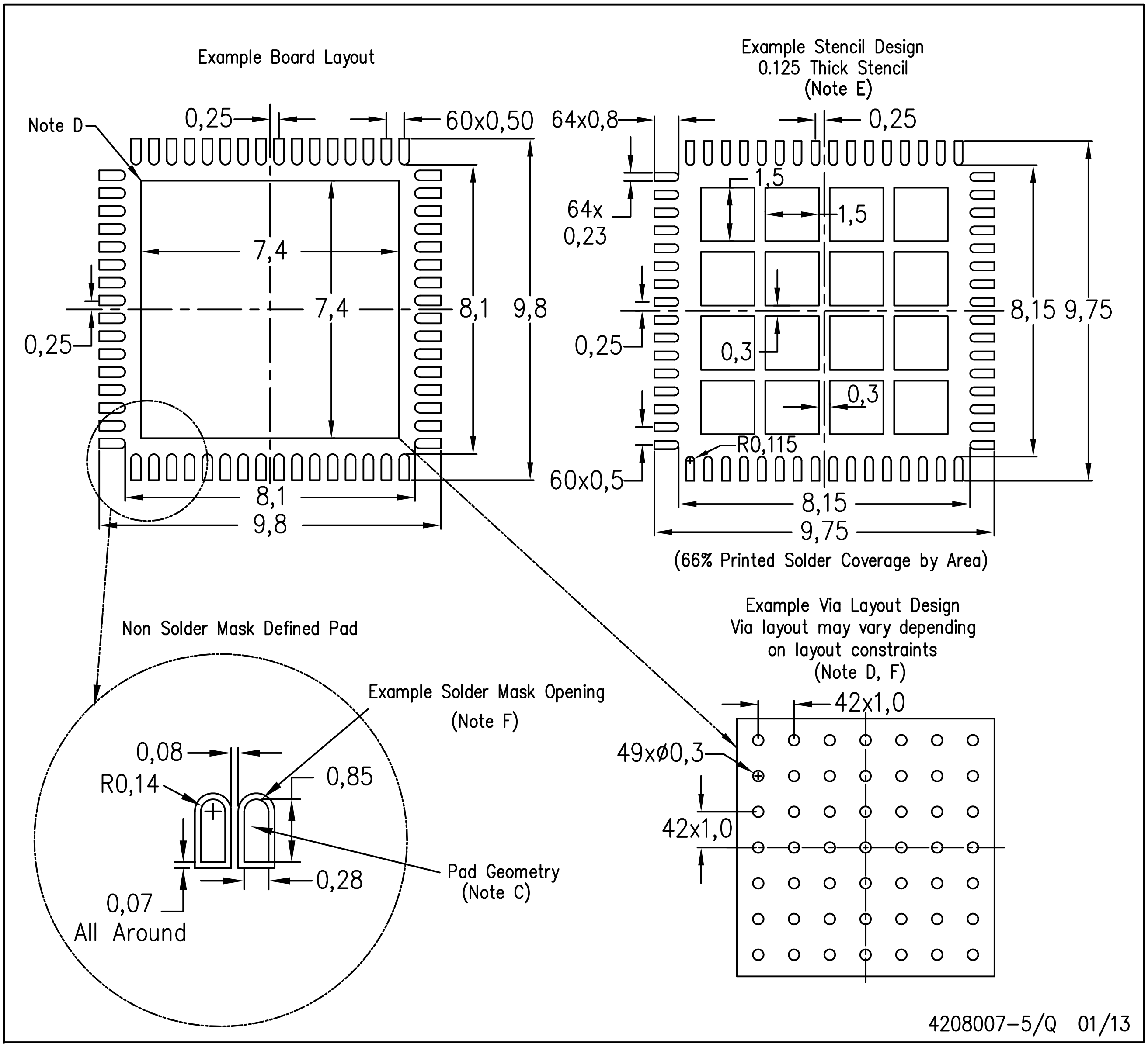
Bottom View

Exposed Thermal Pad Dimensions

4206192–4/W 01/13

NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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