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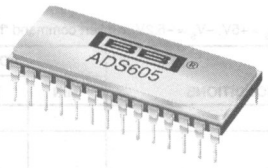
BURR-BROWN®



ADS605

DEMO BOARD AVAILABLE
See Appendix A for more information.

12-Bit 10MSPS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- COMPLETE, SELF-CONTAINED DESIGN
- HIGH SPURIOUS-FREE DYNAMIC RANGE: 76dBc at Nyquist
- LOW DNL ERROR: 0.5 LSB
- HIGH SNR: 65dB at Nyquist
- SINGLE-ENDED TRACK/HOLD
- WIDEBAND TRACK/HOLD: 32MHz Full Power Bandwidth
- LOW DRIFT REFERENCE: 20ppm/°C
- LOW POWER: 1.4W
- COMPACT 28-PIN DIP PACKAGE

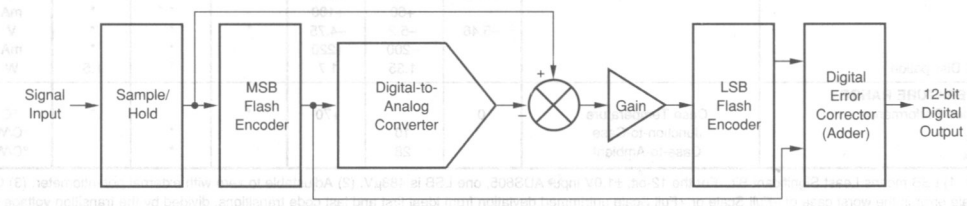
APPLICATIONS

- MEDICAL IMAGING
- CCD IMAGING
- COMMUNICATIONS
- RADAR
- TEST INSTRUMENTATION
- HIGH SPEED DATA ACQUISITION
- PHOTOGRAPHIC IMAGING
- IR IMAGING
- SPECTRUM ANALYSIS

DESCRIPTION

The ADS605 is a high performance sampling analog-to-digital converter complete with a track/hold, low drift reference and internal timing. The wideband track/hold has a user-friendly single-ended input. Its robust, no compromise, design yields EXCELLENT NYQUIST PERFORMANCE for key specifications like spurious free dynamic range, SNR and differential linearity. Both DC and dynamic specifications are guaranteed.

The ADS605 is packaged in a 28-pin hermetic DIP package. The logic interface is TTL. The DEM-ADS605 demonstration board is available to quickly evaluate this high performance device.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

FULL TEMPERATURE SPECIFICATIONS

ELECTRICAL

T = 0°C to +70°C case temperature, f_S = 10MHz, $+V_S$ = +5V, $-V_S$ = –5.2V, convert command "high" pulse width = 42ns, unless otherwise specified.

PARAMETER	CONDITIONS	ADS605H MIN	ADS605H TYP	ADS605H MAX	ADS605HB MIN	ADS605HB TYP	ADS605HB MAX	UNITS
RESOLUTION				12			*	Bits
ANALOG INPUT								
Voltage Range			±1.0			*		V
Impedance			1.5			*		MΩ
Capacitance			5			*		pF
CONVERSION CHARACTERISTICS								
Sample Rate Range		DC		10	*		*	MHz
Throughput Rate		10			*			MHz
Pipeline Delay			One Convert Command Period					
Start Up Time to Rated Accuracy			1				*	minute
DC ACCURACY								
Integral Linearity Error	f_{IN} = 100kHz		±2.0			±1.7	±2.5	LSB[1]
Differential Linearity Error	f_{IN} = 100kHz		±0.6	–0.99, +1.5		±0.5	–0.99, +1.0	LSB
No Missing Codes	f_{IN} = 100kHz		Guaranteed			Guaranteed		
Gain Error[2, 3]	DC		0.9	±1.25		0.7	±1.0	%FSR
Bipolar Zero Error[2]	DC		0.2	±0.75		0.1	±0.3	%
Power Supply Sensitivity								
$+V_S$	+4.75V < $+V_S$ < +5.25V		±0.002	±0.05		±0.001	±0.05	%FSR
$-V_S$	–4.75V < $-V_S$ < –5.46V		±0.002	±0.05		±0.001	±0.05	%FSR
AC ACCURACY	Input Signal within 1dB of Full Scale							
Spurious-Free Dynamic Range	f_{IN} = 100kHz	73	78		78	82		dBFS[4]
	f_{IN} = 5MHz	67	73		71	76		dBFS
Total Harmonic Distortion	f_{IN} = 100kHz		–75	–70		–80	–75	dBFS
	f_{IN} = 5MHz		–70	–67		–74	–70	dBFS
Signal-to-(Noise+Distortion) Ratio	f_{IN} = 100kHz	61	65		64	67		dBc
	f_{IN} = 5MHz	60	63		62	65		dBc
Signal-to-Noise Ratio	f_{IN} = 100kHz	62	64		65	67		dB
	f_{IN} = 5MHz	61	63		63	64		dB
Differential Linearity Error	f_{IN} = 5MHz		±0.8	–0.99, +1.5		±0.6	±0.85	LSB
No Missing Codes	f_{IN} = 5MHz		Guaranteed			Guaranteed		
Full-Power Bandwidth[5]			32			*		MHz
SAMPLING DYNAMICS								
Aperture Delay			1.0			*		ns
Aperture Jitter			3			*		ps rms
Overvoltage Recovery[6]			96	200		*	*	ns
CONVERT INPUT								
Pulse Width		30		42	*		*	ns
Logic Levels								
V_{IL}		–0.15		+0.8	*		*	V
V_{IH}		+2.0		V_D + 0.15	*		*	V
I_{IL}				±750			*	µA
I_{IH}				±750			*	µA
DIGITAL OUTPUTS			Parallel 12-bits					
Data Format			Binary Two's Complement					
Data Coding								
V_{OL}	I_{SINK} = 1.6mA			+0.5			*	V
V_{OH}	I_{SOURCE} = 80µA	+2.4			*			V
POWER SUPPLIES								
Specified Performance								
$+V_S$		+4.75	+5	+5.25	*	*	*	V
$+I_S$			+60	+100		*	*	mA
$-V_S$		–5.46	–5.2	–4.75	*	*	*	V
$-I_S$			–200	+220		*	*	mA
Power Dissipation			1.35	1.7		*	1.5	W
TEMPERATURE RANGE								
Specified Performance	Case Temperature	0		+70	*		*	°C
θ_{JC}	Junction-to-Case		10			*		°C/W
θ_{CA}	Case-to-Ambient		28			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±1.0V input ADS605, one LSB is 488µV. (2) Adjustable to zero with external potentiometer. (3) Gain error scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (4) dBFS is dB relative to a full-scale ±1.0V input. (5) Full-Power Bandwidth defined as the –3dB frequency of the Track/Hold referred to as Full Scale. (6) Recovers to specified performance after 2 x FS input overvoltage.

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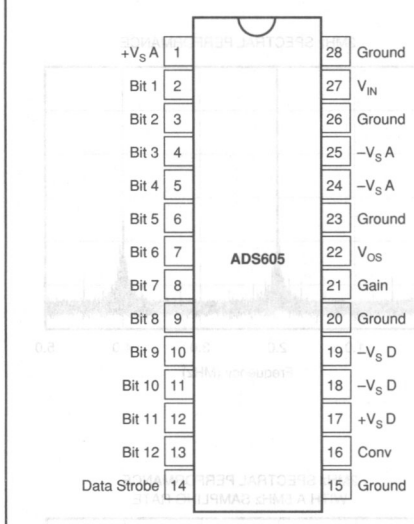
PIN CONFIGURATION

Top View DIP



PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1	Analog +V	+5V
2	Bit 1	Most Significant Bit
3	Bit 2	
4	Bit 3	
5	Bit 4	
6	Bit 5	
7	Bit 6	
8	Bit 7	
9	Bit 8	
10	Bit 9	
11	Bit 10	
12	Bit 11	
13	Bit 12	Least Significant Bit
14	Data Strobe	Rising edge can be used to latch data into external latches.
15	Ground	
16	Conv	Convert Command. A rising edge on this input initiates conversion.
17	Digital $+V_S$	+5V
18	Digital $-V_S$	–5.2V
19	Digital $-V_S$	
20	Ground	
21	Gain	Gain Adjust Input
22	V_{OS}	Offset Adjust Input
23	Ground	
24	Analog $-V_S$	–5.2V
25	Analog $-V_S$	–5.2V
26	Ground	
27	V_{IN}	Analog Input. Full scale range is ±1.0V
28	Ground	

ABSOLUTE MAXIMUM RATINGS

$+V_S$	+7V
$-V_S$	–7V
Analog Input	±2.5V
Logic Input	–0.5V to $+V_S$
Case Temperature	+100°C
Junction Temperature	+165°C
Storage Temperature	–65°C to +125°C

NOTE: (1) Stresses above these ratings may permanently damage the device.

PACKAGE INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS605H	28-Pin Ceramic DIP	237
ADS605HB	28-Pin Ceramic DIP	237

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ORDERING INFORMATION

ADS605 H ( )

Basic Model Number

Package Code
H: Metal and Ceramic

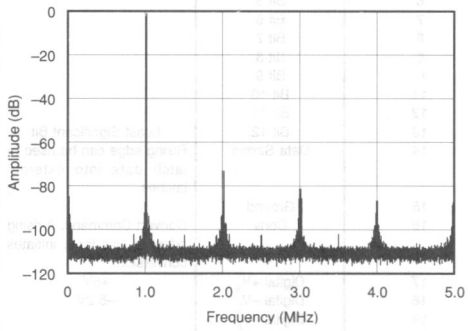
Performance Grade Code
No letter or "B": 0°C to +70°C Case Temperature

For Immediate Assistance, Contact Your Local Salesperson

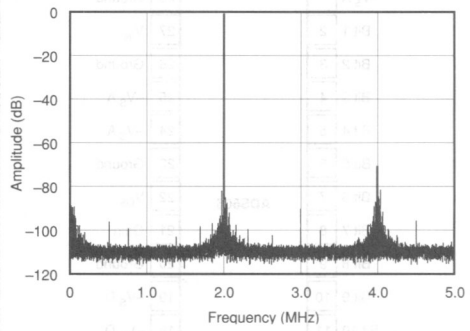
TYPICAL PERFORMANCE CURVES

T = 0°C to +70°C case temperature, f_S = 10MHz, $+V_S$ = +5V, $-V_S$ = –5.2V, convert command "high" pulse width = 42ns, unless otherwise specified.

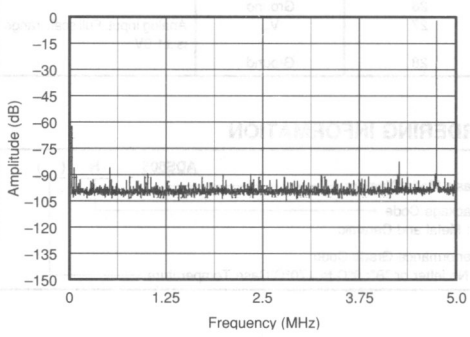
1MHz SPECTRAL PERFORMANCE



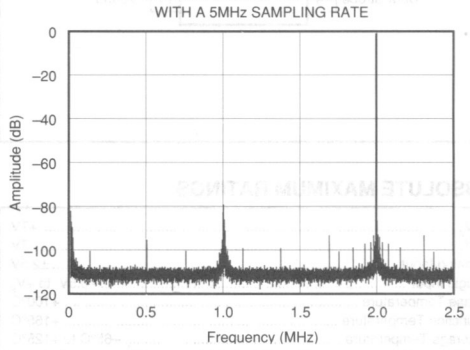
2MHz SPECTRAL PERFORMANCE



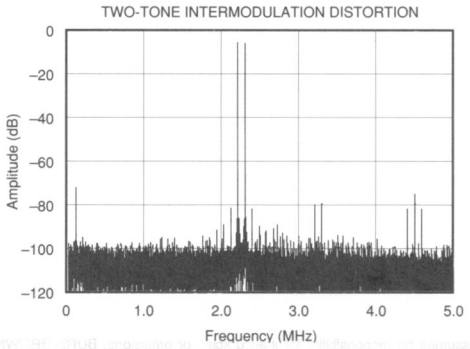
4.7MHz SPECTRAL PERFORMANCE



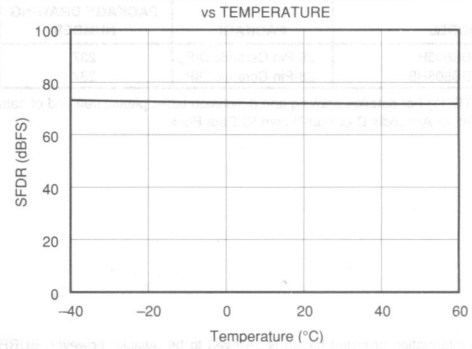
2MHz SPECTRAL PERFORMANCE
WITH A 5MHz SAMPLING RATE



TWO-TONE INTERMODULATION DISTORTION



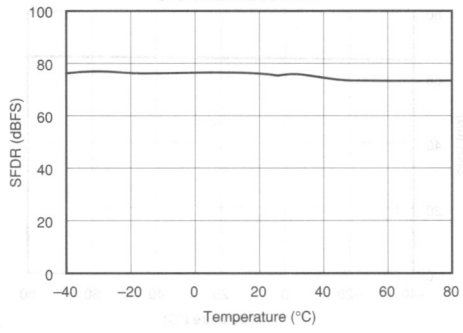
2MHz SPURIOUS FREE DYNAMIC RANGE
vs TEMPERATURE



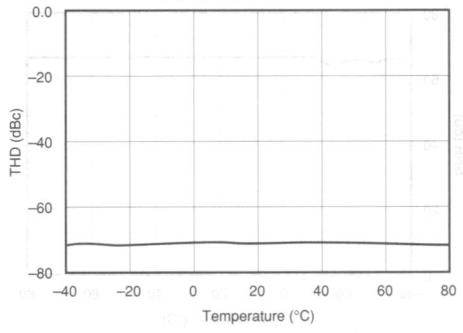
TYPICAL PERFORMANCE CURVES (CONT)

T = 0°C to +70°C case temperature, f_S = 10MHz, $+V_S$ = +5V, $-V_S$ = –5.2V, convert command "high" pulse width = 42ns, unless otherwise specified.

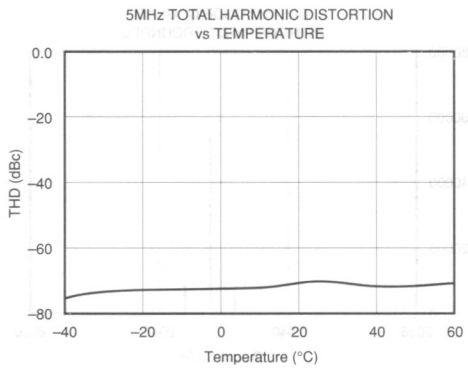
5MHz SPURIOUS FREE DYNAMIC RANGE vs TEMPERATURE



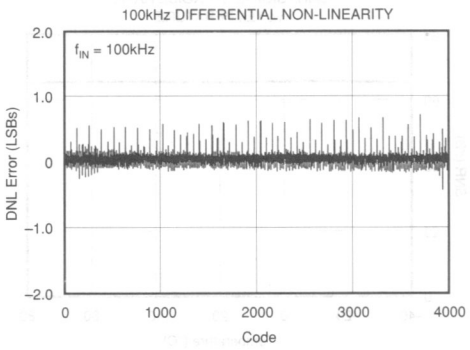
2MHz TOTAL HARMONIC DISTORTION vs TEMPERATURE



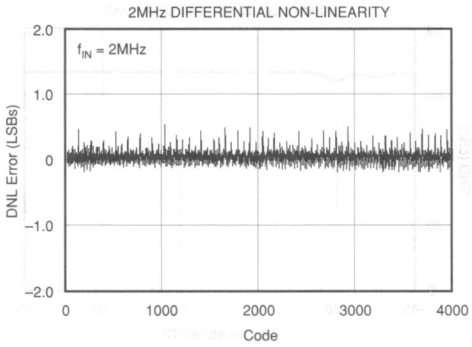
5MHz TOTAL HARMONIC DISTORTION vs TEMPERATURE



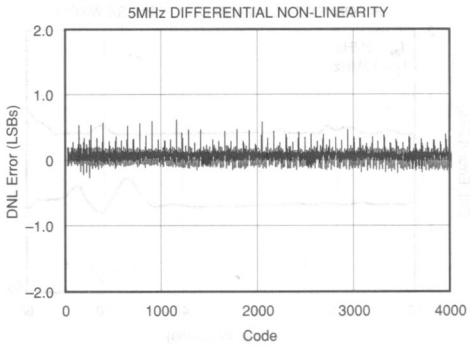
100kHz DIFFERENTIAL NON-LINEARITY



2MHz DIFFERENTIAL NON-LINEARITY



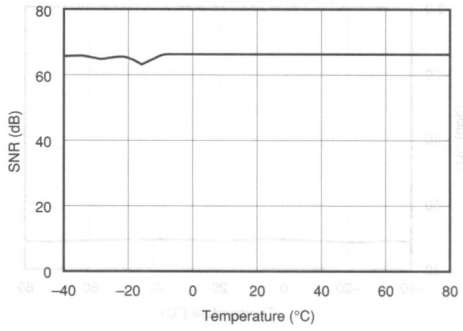
5MHz DIFFERENTIAL NON-LINEARITY



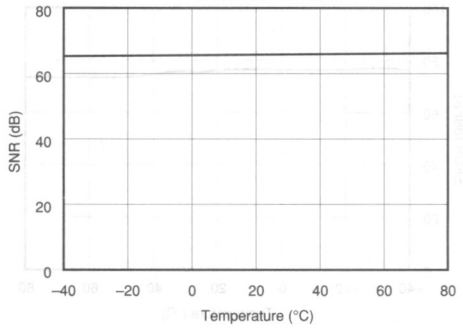
TYPICAL PERFORMANCE CURVES (CONT)

T = 0°C to +70°C case temperature, f_S = 10MHz, $+V_S$ = +5V, $-V_S$ = –5.2V, convert command "high" pulse width = 42ns, unless otherwise specified.

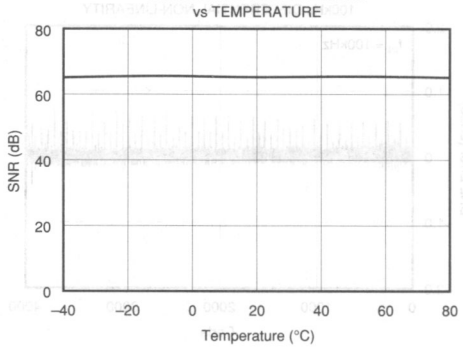
100kHz SIGNAL-TO-NOISE RATIO vs TEMPERATURE



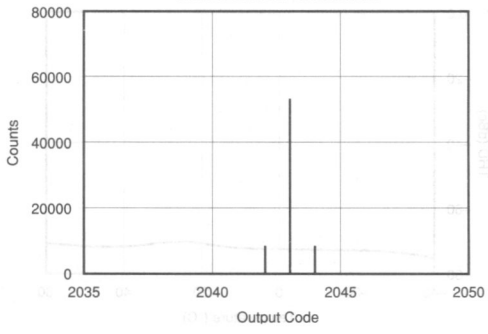
2MHz SIGNAL-TO-NOISE RATIO vs TEMPERATURE



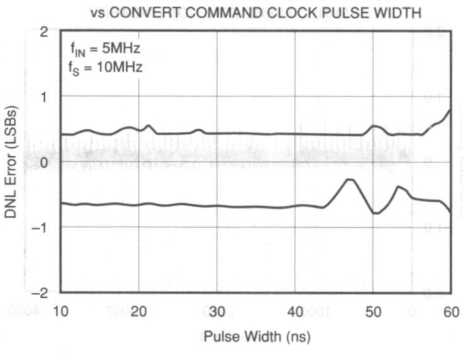
5MHz SIGNAL-TO-NOISE RATIO vs TEMPERATURE



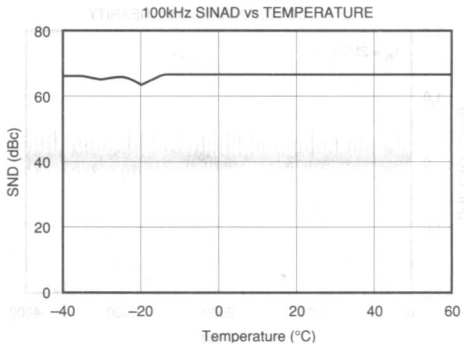
OUTPUT CODE COUNTS WITH THE INPUT GROUNDED



DIFFERENTIAL NON-LINEARITY ERROR vs CONVERT COMMAND CLOCK PULSE WIDTH



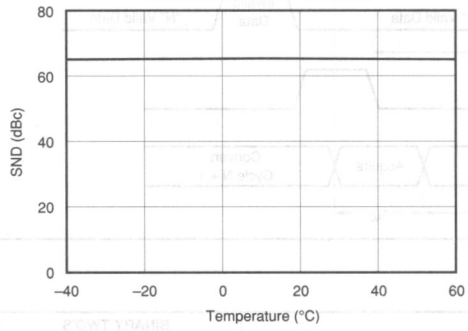
100kHz SINAD vs TEMPERATURE



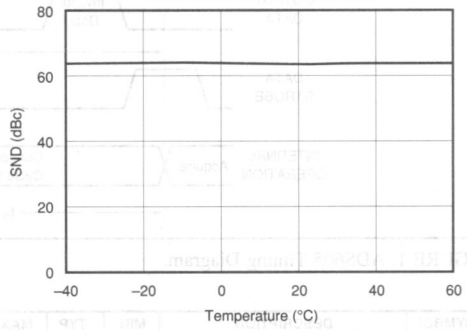
TYPICAL PERFORMANCE CURVES (CONT)

T = 0°C to +70°C case temperature, f_S = 10MHz, $+V_S$ = +5V, $-V_S$ = –5.2V, convert command "high" pulse width = 42ns, unless otherwise specified.

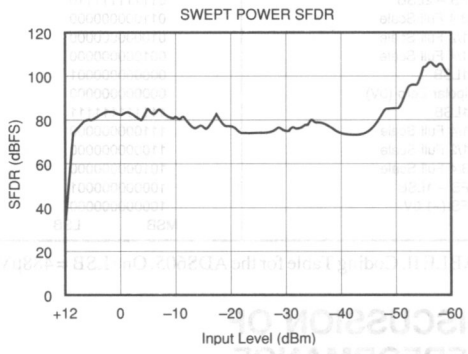
2MHz SINAD vs TEMPERATURE



5MHz SINAD vs TEMPERATURE



SWEPT POWER SFDR



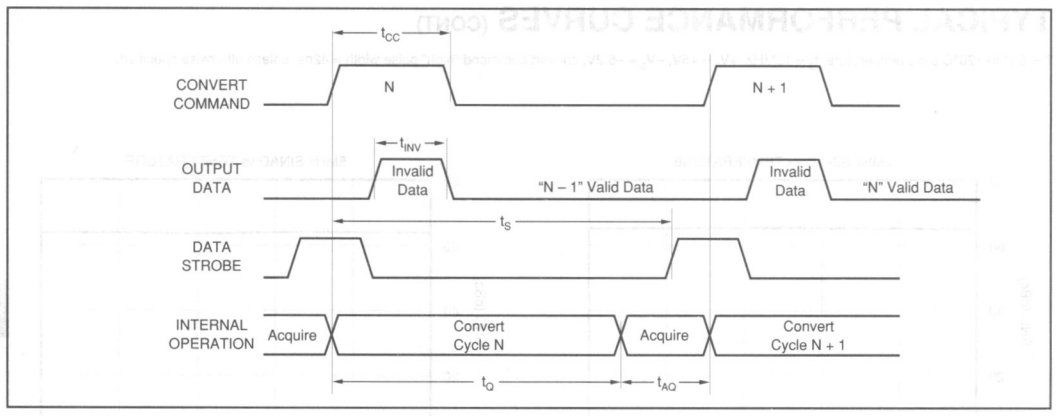


FIGURE 1. ADS605 Timing Diagram.

SYMBOL	DESCRIPTION	MIN	TYP	MAX
t_{CC}	Convert Command Pulse Width	30ns		42ns
t_{INV}	Data Invalid Period	10ns		35ns
t_S	Data Strobe Rising Edge	65ns	75ns	85ns
t_{AQ}	Acquisition Time		30ns	
t_Q	Quantizer Time		70ns	

TABLE I. Timing Specifications.

THEORY OF OPERATION

The ADS605 is a two-step subranging analog-to-digital converter. Conceptually, the subranging technique is simple: sample and hold the input signal, convert to digital with a coarse ADC, convert back to analog with a coarse-resolution (but high accuracy) DAC, subtract this voltage from the T/H output, amplify this "remainder," convert to digital with second coarse ADC, and combine the digital output from the first ADC with the digital output from the second ADC. In practice, however achieving high conversion speed without sacrificing accuracy is a difficult task.

The analog input signal is sampled by a high-speed track/hold amplifier with low distortion, fast acquisition time and very low aperture uncertainty (jitter).

Internal timing circuits (ECL logic is used internally) supply all the critical timing signals necessary for proper operation of the ADS605. Timing signals are laser-trimmed for both pulse width and delay. ECL logic is used internally for its speed, low noise characteristics and timing delay stability over a wide range of temperatures and power supply voltages.

The ADS605 timing technique generates a variable width T/H gate pulse which is determined by the conversion command pulse period minus a fixed 70ns ADC conversion time. ADS605 conversion rates are therefore possible somewhat above the 10MSPS specification but acquisition time is sacrificed and accuracy is rapidly degraded.

INPUT VOLTAGE (Exact Center of Code)	BINARY TWO'S COMPLEMENT (BTC) OUTPUT CODING
+FS (+1.0V)	011111111111
+FS – 1LSB	011111111111
+FS – 2LSB	011111111110
+3/4 Full Scale	011000000000
+1/2 Full Scale	010000000000
+1/4 Full Scale	001000000000
+1LSB	000000000001
Bipolar Zero (0V)	000000000000
–1LSB	111111111111
–1/4 Full Scale	111000000000
–1/2 Full Scale	110000000000
–3/4 Full Scale	101000000000
–FS – 1LSB	100000000001
–FS (–1.0V)	100000000000
	MSB LSB

TABLE II. Coding Table for the ADS605. One LSB = 488µV.

DISCUSSION OF PERFORMANCE

DYNAMIC PERFORMANCE TESTING

The ADS605 is a very high performance converter and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a fast Fourier transform (FFT) to the ADC digital output will provide data on all important dynamic performance parameters: spurious free dynamic range (SFDR), signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SINAD), and intermodulation distortion (IMD).

Highly accurate phase-locked signal sources allow high resolution coherent FFT measurements to be made without using window functions. By choosing appropriate signal frequencies and sample rates, an odd integral number of signal frequency periods can be sampled. Because no spectral leakage results, a rectangular window (no window function) can be used. This was used to generate the typical FFT performance curves.

If generators cannot be phase-locked and set to extreme accuracy, every low side-lobe window must be applied to the digital data before executing an FFT. A commonly used window such as the Hanning window is not appropriate for testing high performance converters; a minimum four-sample Blackman-Harris window is strongly recommended. To assure that the majority of codes are exercised in the ADS605, a minimum 4096 point FFT should be taken.

APPLICATIONS

The following points must be followed carefully in order to accurately test the precision ADS605:

1. The ADC analog input must not be overdriven. Using a signal amplitude slightly lower than FSR will allow a small amount of "headroom" so that noise or DC offset voltage will not overrange the AC+DC and "hard limit" on signal peaks.
2. Two-tone tests can produce signal envelopes that exceed FSR. Set each test signal to slightly less than –6dB to prevent "hard limiting" on peaks.
3. Two-tone testing will require isolation between test signal generators to prevent IMD generation in the test generator output circuits. An active summing amplifier using an OPA642 is shown in Figure 2. This circuit will provide excellent performance from DC to 10MHz with harmonic and intermodulation components typically better than –85dBc. A passive (hybrid transformer) signal combiner can also be used (Figures 3 and 4) over a range of about 0.1MHz to 30MHz. This combiner's port-to-port isolation will be approximately 45dB between signal generators and its input-output insertion loss will be about 6dB. Distortion will be better than –85dBc for the powdered-iron core specified.

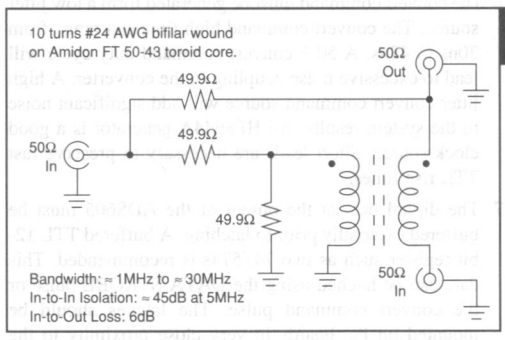


FIGURE 3. Passive Signal Divider.

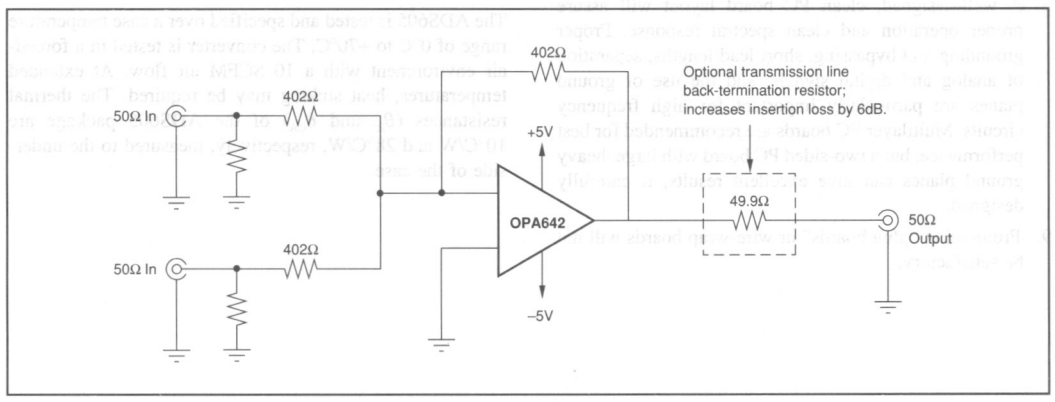


FIGURE 2. Active Signal Combiner.

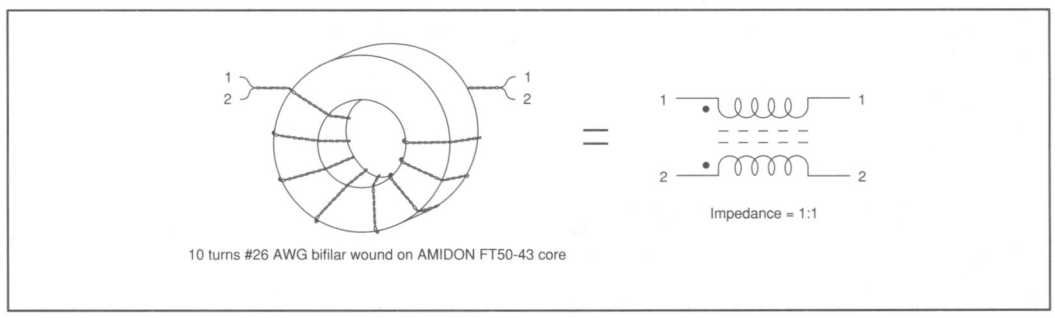


FIGURE 4. Transformer Details.

4. The signal source must be filtered to provide a clean, harmonic-free input to the ADS605. This signal source must have exceptional noise performance to achieve accurate SNR measurements.
5. The analog input of the ADS605 should be terminated directly at the input pin sockets with the correct filter terminating impedance (50Ω or 75Ω), or it should be driven by a low output impedance buffer such as an OPA642. Short leads are necessary to prevent digital noise pickup.
6. The convert command must be generated form a low jitter source. The convert command high time can range from 30ns to 42ns. A 50% convert command duty cycle will lead to excessive noise coupling in the converter. A high jitter convert command source will add significant noise to the system results. An HP8644A generator is a good clock source. Short leads are necessary to preserve fast TTL rise times.
7. The digital data at the output of the ADS605 must be buffered externally prior to latching. A buffered TTL 12-bit register such as two 74F574s is recommended. This data can be latched using the DATA STROBE pulse or the convert command pulse. The latches should be mounted on PC boards in very close proximity to the ADS605. Avoid long leads.
8. A well-designed, clean PC board layout will assure proper operation and clean spectral response. Proper grounding and bypassing, short lead lengths, separation of analog and digital signals, and the use of ground planes are particularly important for high frequency circuits. Multilayer PC boards are recommended for best performance, but a two-sided PC board with large, heavy ground planes can give excellent results, if carefully designed.
9. Prototyping "plug boards" or wire-wrap boards will not be satisfactory.
10. Connect analog and digital ground pins of the ADS605 directly to the ground plane. In our experience, connecting these pins to a common ground plane gives the best results. Analog and digital power supply commons should be tied together at the ground plane.
11. Power supplies should be bypassed with 0.1µF and 2.2µF capacitors. The 0.1µF monoblock capacitors should be placed on the topside of the PC board as close to the pin as your manufacturing process allows.
12. If using a cable to drive the input of the ADS605, avoid reflections down the cable that could degrade dynamic performance by placing a 3dB attenuator at the end of the cable. The input amplitude may be doubled to maintain signal amplitude.

OFFSET AND GAIN ADJUSTMENT

The ADS605 is carefully laser-trimmed to achieve its rated accuracy without external adjustments. If desired, both gain error and input offset voltage error may be trimmed to zero with external potentiometers by using the application circuits in Figure 5. Trim range is typically ±2.0% for gain and ±2.0% for offset. If gain and offset trim is not used, pins 21 and 22 should be grounded.

THERMAL REQUIREMENTS

The ADS605 is tested and specified over a case temperature range of 0°C to +70°C. The converter is tested in a forced-air environment with a 10 SCFM air flow. At extended temperatures, heat sinking may be required. The thermal resistances (θ_{JC} and θ_{CA}) of the ADS605 package are 10°C/W and 28°C/W, respectively, measured to the underside of the case.

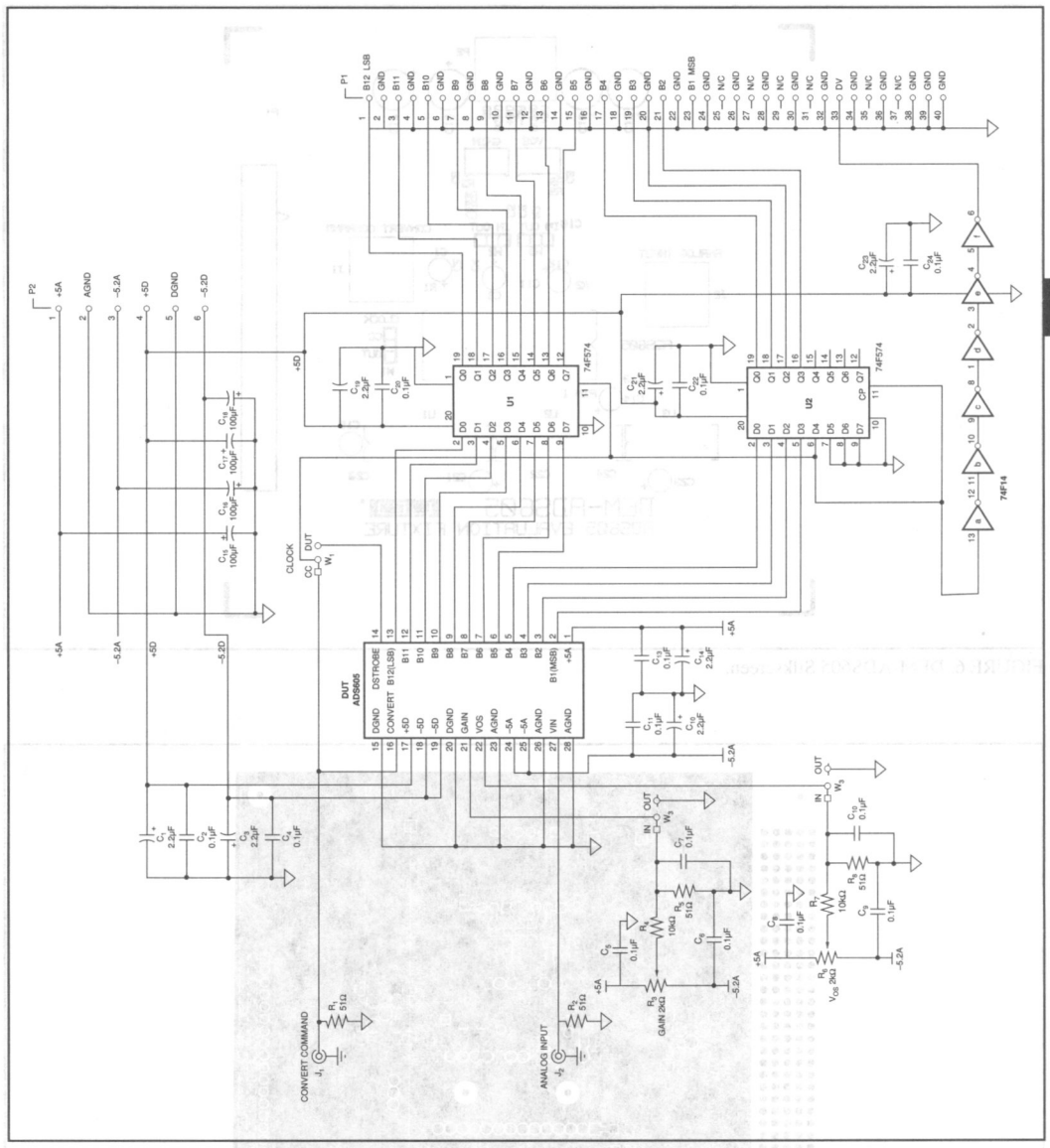


FIGURE 5. Application Diagram for the DEM-ADS605 Evaluation Board.

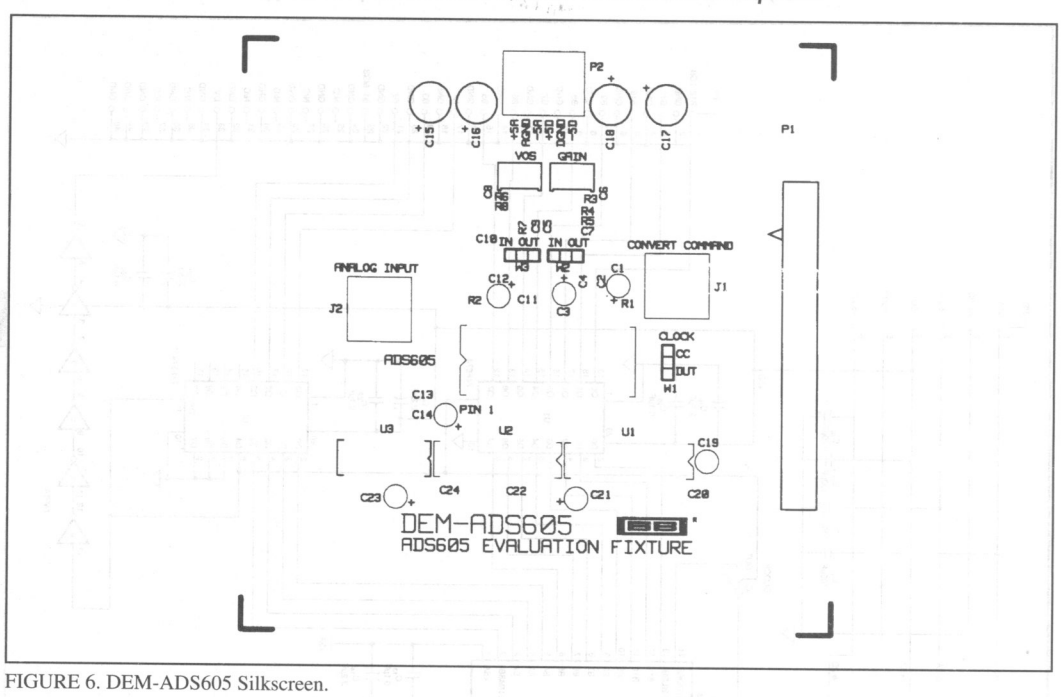


FIGURE 6. DEM-ADS605 Silkscreen.

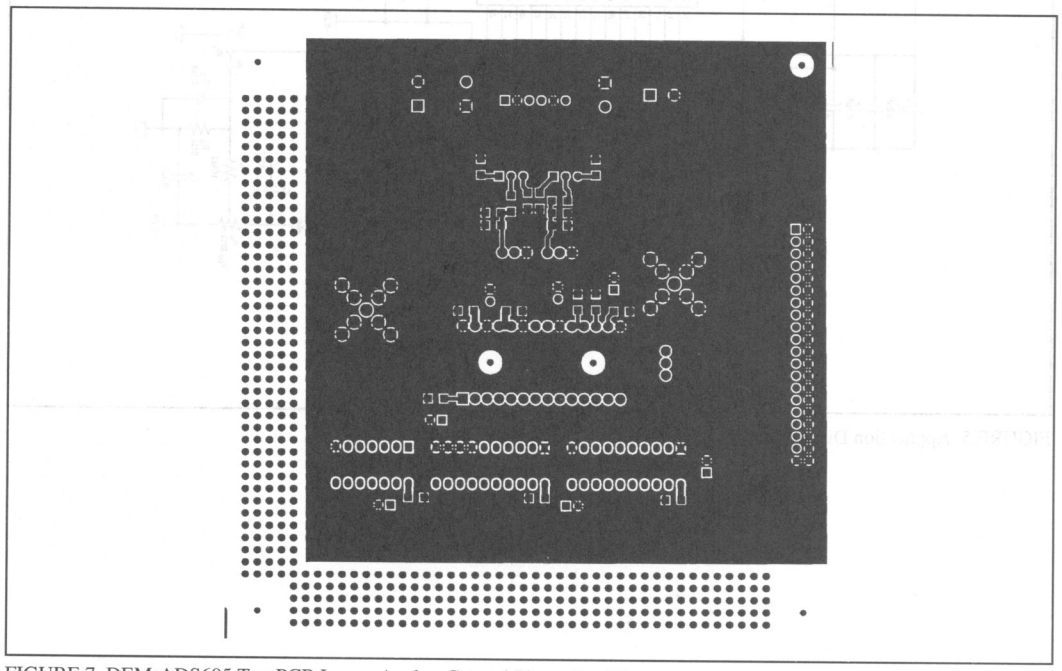


FIGURE 7. DEM-ADS605 Top PCB Layer. Analog Ground Plane, Top View.

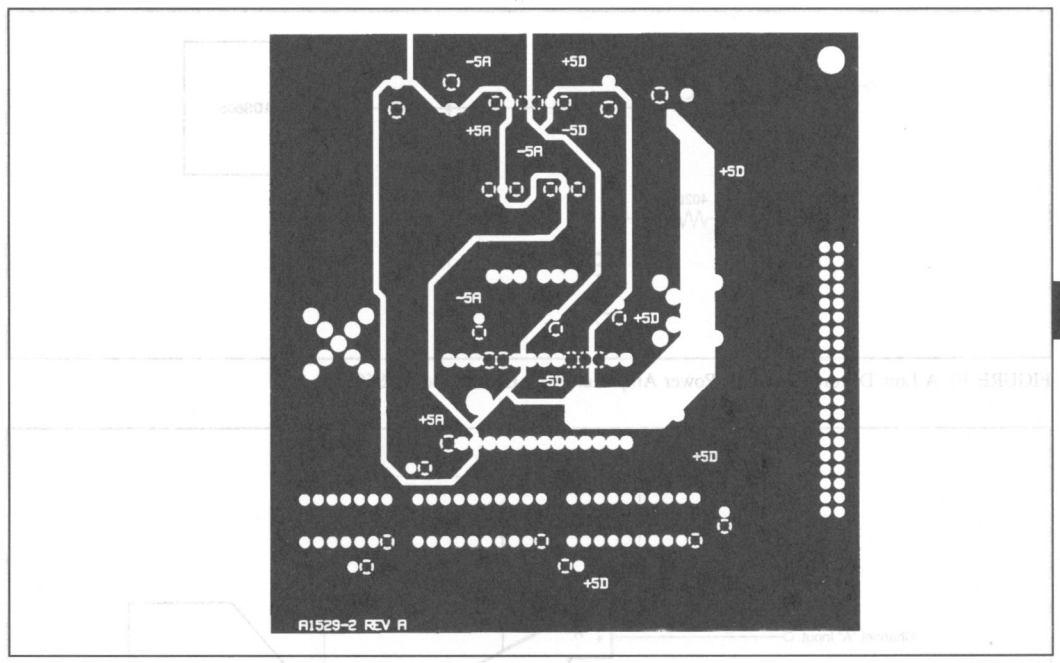


FIGURE 8. DEM-ADS605 Middle PCB Layer. Power Plane, Top View.

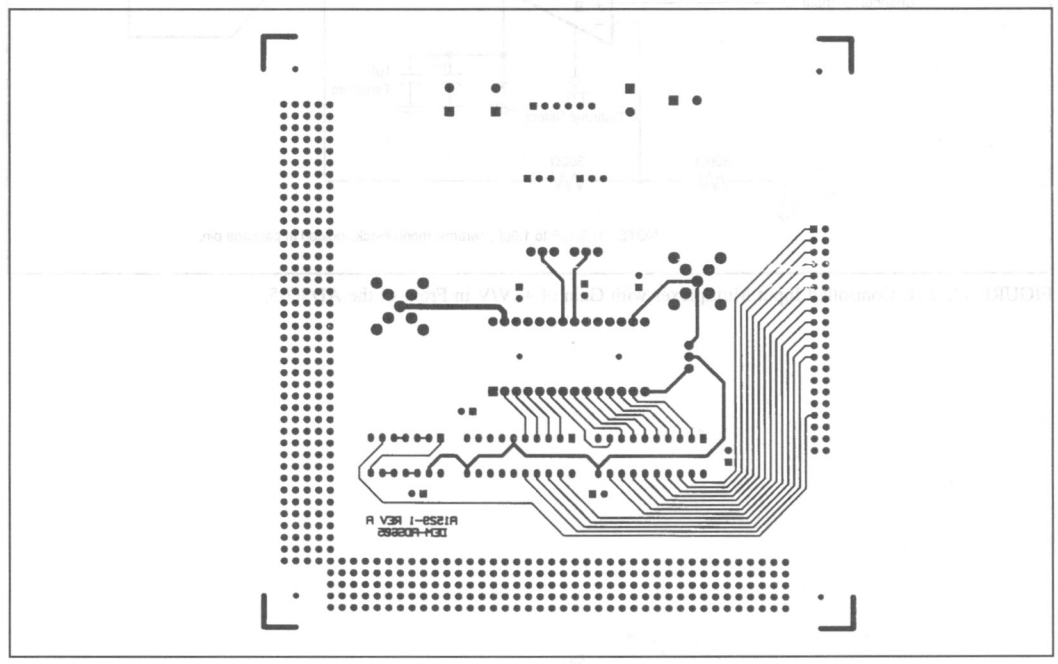


FIGURE 9. DEM-ADS605 Bottom PCB Layer. Interconnect, Top View.

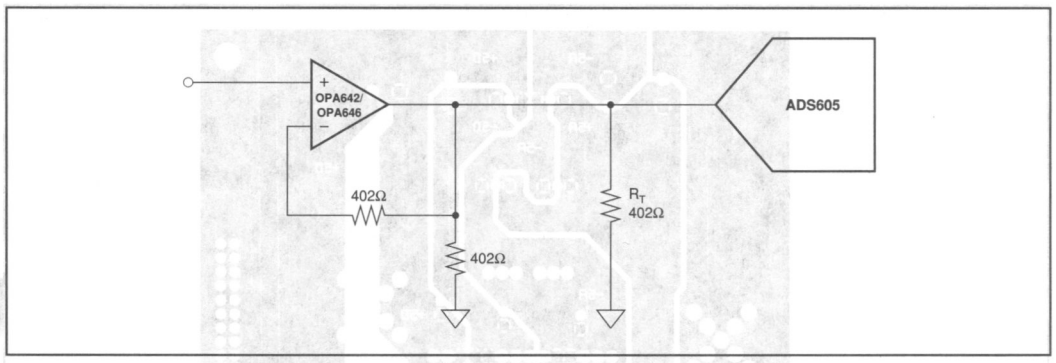


FIGURE 10. A Low Distortion or Low Power Amplifier Front End for the ADS605.

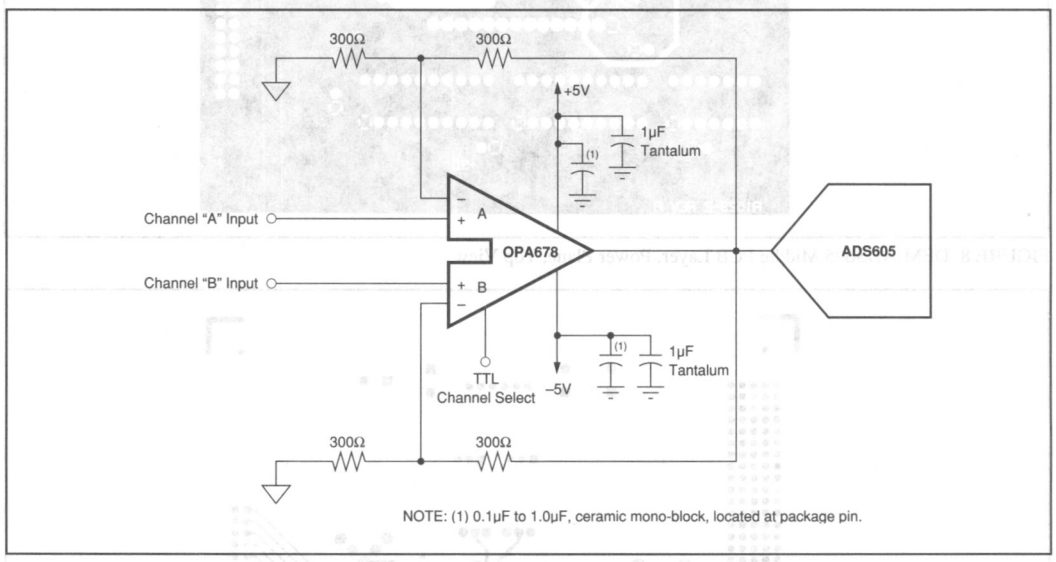


FIGURE 11. TTL-Controlled Input Multiplexer with Gain of +2V/V in Front of the ADS605.

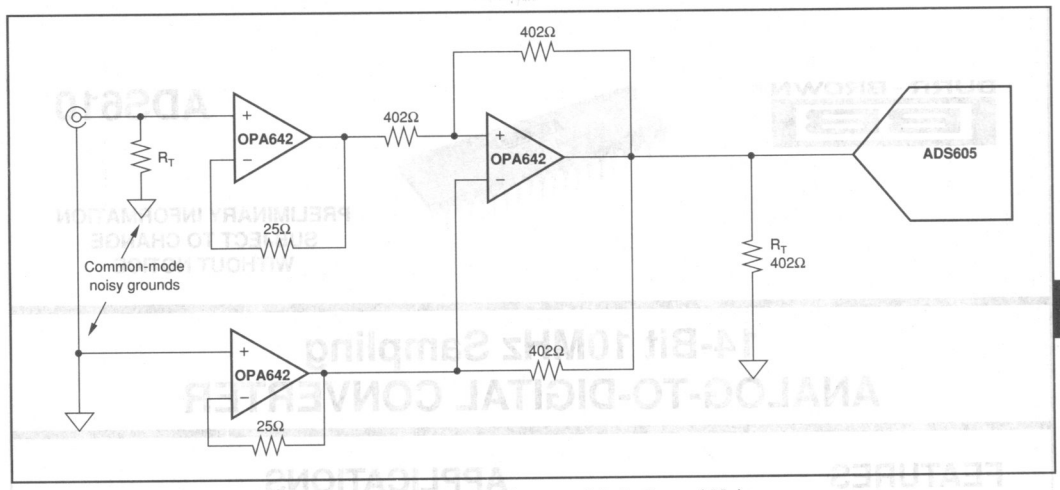


FIGURE 12. A Differential Amplifier Input for Rejecting Common-Mode Ground Noise.