12-, 14-, 16-Bit, Eight-Channel, Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTERS

Check for Samples: ADS8528, ADS8548, ADS8568

FEATURES

- **Family of 12-, 14-, 16-Bit, Pin- and Software-Compatible ADCs**
- **Maximum Data Rate Per Channel:**
  - **ADS8528: 650kSPS (PAR) or 480kSPS (SER)**
  - **ADS8548: 600kSPS (PAR) or 450kSPS (SER)**
  - **ADS8568: 510kSPS (PAR) or 400kSPS (SER)**
- **Excellent AC Performance:**
  - **Signal-to-Noise Ratio:**
    ADS8528: 73.9dB
    ADS8548: 85dB
    ADS8568: 91.5dB
  - **Total Harmonic Distortion:**
    ADS8528: –89dB
    ADS8548: –91dB
    ADS8568: –94dB
- **Programmable and Buffered Internal Reference: 0.5V to 2.5V or 0.5V to 3.0V Supports Input Voltage Ranges of Up to ±12V**
- **Selectable Parallel or Serial Interface**
- **Scalable Low-Power Operation Using Auto-Sleep Mode: Only 32mW at 10kSPS**
- **Fully Specified Over the Extended Industrial Temperature Range**

APPLICATIONS

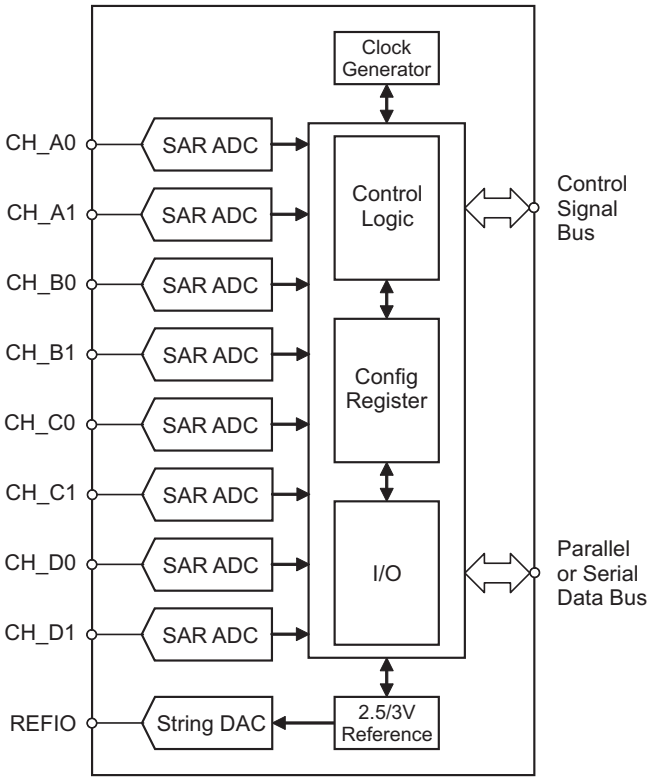
- **Protection Relays**
- **Power Quality Measurement**
- **Multi-Axis Motor Control**
- **Programmable Logic Controllers**
- **Industrial Data Acquisition**

DESCRIPTION

The ADS8528/48/68 contain eight low-power, 12-, 14-, or 16-bit, successive approximation register (SAR)-based analog-to-digital converters (ADCs) with true bipolar inputs. These channels are grouped in four pairs, thus allowing simultaneous high-speed signal acquisition of up to 650kSPS.

The devices support selectable parallel or serial interface with daisy-chain capability. The programmable reference allows handling of analog input signals with amplitudes up to ±12V.

The ADS8528/48/68 family supports an auto-sleep mode for minimum power dissipation and is available in both QFN-64 and LQFP-64 packages. The entire family is specified over a temperature range of –40°C to +125°C.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FAMILY/ORDERING INFORMATION(1)

PRODUCT	RESOLUTION (Bits)	MAXIMUM DATA RATE: PAR/SER (kSPS/ch)	SNR (dB, typ)	THD (dB, typ)
ADS8528	12	650/480	73.9	–89
ADS8548	14	600/450	85	–91
ADS8568	16	510/400	91.5	–94

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
Supply voltage	HVDD to AGND	–0.3 to 18	V
	HVSS to AGND	–18 to 0.3	V
	AVDD to AGND	–0.3 to 6	V
	DVDD to DGND	–0.3 to 6	V
Analog input voltage		HVSS – 0.3 to HVDD + 0.3	V
Reference input voltage with respect to AGND		AGND – 0.3 to AVDD + 0.3	V
Digital input voltage with respect to DGND		DGND – 0.3 to DVDD + 0.3	V
Ground voltage difference AGND to DGND		±0.3	V
Input current to all pins except supply		±10	mA
Maximum virtual junction temperature, T_J		+150	°C
ESD ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±2500	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		ADS8528/48/68		UNITS
		RGC	PM	
		64 PINS	64 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	22	48.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	9.0	9.4	
θ_{JB}	Junction-to-board thermal resistance	3.6	21.9	
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.3	
ψ_{JB}	Junction-to-board characterization parameter	2.9	21.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.3	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS: ADS8528

All minimum/maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V.

PARAMETER		CONDITIONS	ADS8528 MIN	ADS8528 TYP	ADS8528 MAX	UNIT
SAMPLING DYNAMICS						
Conversion time		Internal conversion clock			1.33	µs
Throughput rate	f_{DATA}	Serial interface, all four SDOx active			480	kSPS
		Parallel interface			650	kSPS
DC ACCURACY						
Resolution				12		Bits
No missing codes			12			Bits
Integral linearity error(1)	INL		–0.75	±0.2	0.75	LSB
Differential linearity error	DNL		–0.5	±0.2	0.5	LSB
Offset error			–1.5	±0.5	1.5	mV
Offset error matching			–0.65		0.65	mV
Offset error drift				±3.5		µV/°C
Gain error		Referenced to voltage at REFIO	–0.5	±0.25	0.5	%
Gain error matching		Between channels of any pair	–0.2		0.2	%
		Between any two channels	–0.4		0.4	%
Gain error drift		Referenced to voltage at REFIO		±6		ppm/°C
AC ACCURACY						
Signal-to-noise ratio	SNR	At f_{IN} = 10kHz	73	73.9		dB
Signal-to-noise ratio + distortion	SINAD	At f_{IN} = 10kHz	73	73.8		dB
Total harmonic distortion(2)	THD	At f_{IN} = 10kHz		–89	–84	dB
Spurious-free dynamic range	SFDR	At f_{IN} = 10kHz	84	92		dB
Channel-to-channel isolation		At f_{IN} = 10kHz		120		dB
–3dB small-signal bandwidth	BW	In 4VREF mode		48		MHz
		In 2VREF mode		24		MHz

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as the number of LSBs or percentage of the specified full-scale range.
(2) Calculated on the first nine harmonics of the input frequency.

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ELECTRICAL CHARACTERISTICS: ADS8548

All minimum/maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V.

PARAMETER		CONDITIONS	ADS8548 MIN	ADS8548 TYP	ADS8548 MAX	UNIT
SAMPLING DYNAMICS						
Conversion time		Internal conversion clock			1.45	µs
Throughput rate	f_{DATA}	Serial interface, all four SDOx active			450	kSPS
		Parallel interface			600	kSPS
DC ACCURACY						
Resolution				14		Bits
No missing codes			14			Bits
Integral linearity error(1)	INL		–1	±0.5	1	LSB
Differential linearity error	DNL		–1	±0.25	1	LSB
Offset error			–1.5	±0.5	1.5	mV
Offset error matching			–0.65		0.65	mV
Offset error drift				±3.5		µV/°C
Gain error		Referenced to voltage at REFIO	–0.5	±0.25	0.5	%
Gain error matching		Between channels of any pair	–0.2		0.2	%
		Between any two channels	–0.4		0.4	%
Gain error drift		Referenced to voltage at REFIO		±6		ppm/°C
AC ACCURACY						
Signal-to-noise ratio	SNR	At f_{IN} = 10kHz	84	85		dB
Signal-to-noise ratio + distortion	SINAD	At f_{IN} = 10kHz	83	84		dB
Total harmonic distortion(2)	THD	At f_{IN} = 10kHz		–91	–86	dB
Spurious-free dynamic range	SFDR	At f_{IN} = 10kHz	86	92		dB
Channel-to-channel isolation		At f_{IN} = 10kHz		120		dB
–3dB small-signal bandwidth	BW	In 4VREF mode		48		MHz
		In 2VREF mode		24		MHz

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as the number of LSBs or percentage of the specified full-scale range.
(2) Calculated on the first nine harmonics of the input frequency.

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ELECTRICAL CHARACTERISTICS: ADS8568

All minimum/maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V.

PARAMETER		CONDITIONS	ADS8568 MIN	ADS8568 TYP	ADS8568 MAX	UNIT
SAMPLING DYNAMICS						
Conversion time		Internal conversion clock			1.7	µs
Throughput rate	f_{DATA}	Serial interface, all four SDOx active			400	kSPS
		Parallel interface			510	kSPS
DC ACCURACY						
Resolution				16		Bits
No missing codes			16			Bits
Integral linearity error(1)	INL	At T_A = –40°C to +85°C, QFN package (RGC)	–3	±1.5	3	LSB
		At T_A = –40°C to +125°C, QFN package (RGC)	–4	±1.5	4	LSB
		At T_A = –40°C to +85°C, LQFP package (PM)	–4	±1.5	4	LSB
		At T_A = –40°C to +125°C, LQFP package (PM)	–4.5	±1.5	4.5	LSB
Differential linearity error	DNL	At T_A = –40°C to +85°C	–1	±0.75	1.75	LSB
		At T_A = –40°C to +125°C	–1	±0.75	2	LSB
Offset error			–1.5	±0.5	1.5	mV
Offset error matching			–0.65		0.65	mV
Offset error drift				±3.5		µV/°C
Gain error		Referenced to voltage at REFIO	–0.5	±0.25	0.5	%
Gain error matching		Between channels of any pair	–0.2		0.2	%
		Between any two channels	–0.4		0.4	%
Gain error drift		Referenced to voltage at REFIO		±6		ppm/°C
AC ACCURACY						
Signal-to-noise ratio	SNR	At f_{IN} = 10kHz, T_A = –40°C to +85°C	90	91.5		dB
		At f_{IN} = 10kHz, T_A = –40°C to +125°C	89	91.5		dB
Signal-to-noise ratio + distortion	SINAD	At f_{IN} = 10kHz, T_A = –40°C to +85°C	87	90		dB
		At f_{IN} = 10kHz, T_A = –40°C to +125°C	86.5	90		dB
Total harmonic distortion(2)	THD	At f_{IN} = 10kHz, T_A = –40°C to +85°C		–94	–90	dB
		At f_{IN} = 10kHz, T_A = –40°C to +125°C		–94	–89.5	dB
Spurious-free dynamic range	SFDR	At f_{IN} = 10kHz, T_A = –40°C to +85°C	90	95		dB
		At f_{IN} = 10kHz, T_A = –40°C to +125°C	89.5	95		dB
Channel-to-channel isolation		At f_{IN} = 10kHz		120		dB
–3dB small-signal bandwidth	BW	In 4VREF mode		48		MHz
		In 2VREF mode		24		MHz

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as the number of LSBs or percentage of the specified full-scale range.
(2) Calculated on the first nine harmonics of the input frequency.

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ELECTRICAL CHARACTERISTICS: GENERAL

All minimum/maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V.

PARAMETER		CONDITIONS	ADS8528, ADS8548, ADS8568			UNIT
			MIN	TYP	MAX	
ANALOG INPUT						
Bipolar full-scale range	CHXX	RANGE pin/RANGE bit = 0	–4VREF		4VREF	V
		RANGE pin/RANGE bit = 1	–2VREF		2VREF	V
Input capacitance		Input range = ±4VREF		10		pF
		Input range = ±2VREF		20		pF
Input leakage current		No ongoing conversion	–1		1	µA
Aperture delay				5		ns
Aperture delay matching		Common CONVST for all channels		100		ps
Aperture jitter				50		ps
Power-supply rejection ratio	PSRR	At output code FFFFh, related to HVDD and HVSS		–78		dB
REFERENCE VOLTAGE OUTPUT (REF_{OUT})						
Reference voltage	VREF	2.5V operation, REFDAC = 3FFh	2.485	2.5	2.515	V
		2.5V operation, REFDAC = 3FFh at +25°C	2.496	2.5	2.504	V
		3.0V operation, REFDAC = 3FFh	2.985	3.0	3.015	V
		3.0V operation, REFDAC = 3FFh at +25°C	2.995	3.0	3.005	V
Reference voltage drift	dVREF/dT			±10		ppm/°C
Power-supply rejection ratio	PSRR	At output code FFFFh, related to AVDD		–77		dB
Output current	$IREF_{OUT}$	DC current	–2		2	mA
Short-circuit current[1]	I_{REFSC}			50		mA
Turn-on settling time	t_{REFON}			10		ms
External load capacitance		At REF_xP/N pins	4.7	10		µF
		At REFIO pin	100	470		nF
Tuning range	REFDAC	Internal reference output voltage range	0.2 VREF		VREF	V
REFDAC resolution			10			Bits
REFDAC differential nonlinearity	DNL_{DAC}		–1	±0.1	1	LSB
REFDAC integral nonlinearity	INL_{DAC}		–2	±0.1	2	LSB
REFDAC offset error	V_{OSDAC}	VREF = 0.5V (DAC = 0CDh)	–4	±0.65	4	LSB
REFERENCE VOLTAGE INPUT (REF_{IN})						
Reference input voltage	$VREF_{IN}$		0.5	2.5	3.025	V
Input resistance				100		MΩ
Input capacitance				5		pF
Reference input current					1	µA

(1) Reference output current is not limited internally.

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ELECTRICAL CHARACTERISTICS: GENERAL (continued)

All minimum/maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V.

PARAMETER		CONDITIONS	ADS8528, ADS8548, ADS8568 MIN	TYP	MAX	UNIT
DIGITAL INPUTS(2)						
Logic family				CMOS with Schmitt-Trigger		
High-level input voltage			0.7 DVDD		DVDD + 0.3	V
Low-level input voltage			DGND – 0.3		0.3 DVDD	V
Input current		V_I = DVDD to DGND	–50		50	nA
Input capacitance				5		pF
DIGITAL OUTPUTS(2)						
Output capacitance				5		pF
Load capacitance					30	pF
High-impedance-state output current			–50		50	nA
Logic family				CMOS		
High-level output voltage	V_{OH}	I_{OH} = 100µA	DVDD – 0.6			V
Low-level output voltage	V_{OL}	I_{OH} = –100µA			DGND + 0.4	V
POWER-SUPPLY REQUIREMENTS						
Analog supply voltage	AVDD		4.5	5.0	5.5	V
Buffer I/O supply voltage	DVDD		2.7	3.3	5.5	V
Input positive supply voltage	HVDD		5.0	15.0	16.5	V
Input negative supply voltage	HVSS		–16.5	–15.0	–5.0	V
Analog supply current	IAVDD	ADS8528, f_{DATA} = maximum		37.9	50.1	mA
		ADS8548, f_{DATA} = maximum		37.3	49.3	mA
		ADS8568, f_{DATA} = maximum		36.6	48.4	mA
		f_{DATA} = 250kSPS, auto-sleep mode		20.3	30.0	mA
		f_{DATA} = 200kSPS, auto-sleep mode		17		mA
		f_{DATA} = 10kSPS, normal operation		30		mA
		f_{DATA} = 10kSPS, auto-sleep mode		4.6		mA
		Auto-sleep mode, no ongoing conversion, internal conversion clock			7.0	mA
		Power-down mode			0.03	mA
Buffer I/O supply current	IDVDD	f_{DATA} = maximum		0.5	2.0	mA
		f_{DATA} = 250kSPS		0.5	1.4	mA
		f_{DATA} = 200kSPS		0.5		mA
		f_{DATA} = 10kSPS		0.4		mA
		Auto-sleep mode, no ongoing conversion, internal conversion clock			0.35	mA
		Power-down mode			0.01	mA
Input positive supply current	IHVDD	ADS8528, f_{DATA} = maximum		3.0	4.2	mA
		ADS8548, f_{DATA} = maximum		2.8	3.9	mA
		ADS8568, f_{DATA} = maximum		2.3	3.2	mA
		f_{DATA} = 250kSPS		1.8	2.4	mA
		f_{DATA} = 200kSPS		1.5		mA
		f_{DATA} = 10kSPS		0.4		mA
		Auto-sleep mode, no ongoing conversion, internal conversion clock			0.45	mA
		Power-down mode			0.01	mA

(2) Specified by design.

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ELECTRICAL CHARACTERISTICS: GENERAL (continued)

All minimum/maximum specifications are at T_A = –40°C to +125°C, specified supply voltage range, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = max, unless otherwise noted. Typical values are at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V.

PARAMETER		CONDITIONS	ADS8528, ADS8548, ADS8568			UNIT
			MIN	TYP	MAX	
POWER-SUPPLY REQUIREMENTS (continued)						
Input negative supply current	IHVSS	ADS8528, f_{DATA} = maximum		3.4	4.5	mA
		ADS8548, f_{DATA} = maximum		3.3	4.4	mA
		ADS8568, f_{DATA} = maximum		2.7	3.6	mA
		f_{DATA} = 250kSPS		2.1	2.6	mA
		f_{DATA} = 200kSPS		1.7		mA
		f_{DATA} = 10kSPS		0.4		mA
		Auto-sleep mode, no ongoing conversion, internal conversion clock			0.35	mA
		Power-down mode			0.01	mA
Power dissipation(3)		ADS8528, f_{DATA} = maximum		287.1	430.1	mW
		ADS8548, f_{DATA} = maximum		279.7	419.1	mW
		ADS8568, f_{DATA} = maximum		259.7	389.4	mW
		f_{DATA} = 250kSPS, auto-sleep mode		161.7	255.2	mW
		f_{DATA} = 200kSPS, auto-sleep mode		151.2		mW
		f_{DATA} = 10kSPS, normal operation		163.3		mW
		f_{DATA} = 10kSPS, auto-sleep mode		36.3		mW
		Auto-sleep mode, no ongoing conversion, internal conversion clock			53.6	mW
		Power-down mode			0.6	mW
Operating ambient temperature range	T_A		–40	25	+125	°C

(3) Maximum power dissipation values are specified with HVDD = 15V and HVSS = –15V.

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PARAMETER MEASUREMENT INFORMATION

TIMING CHARACTERISTICS

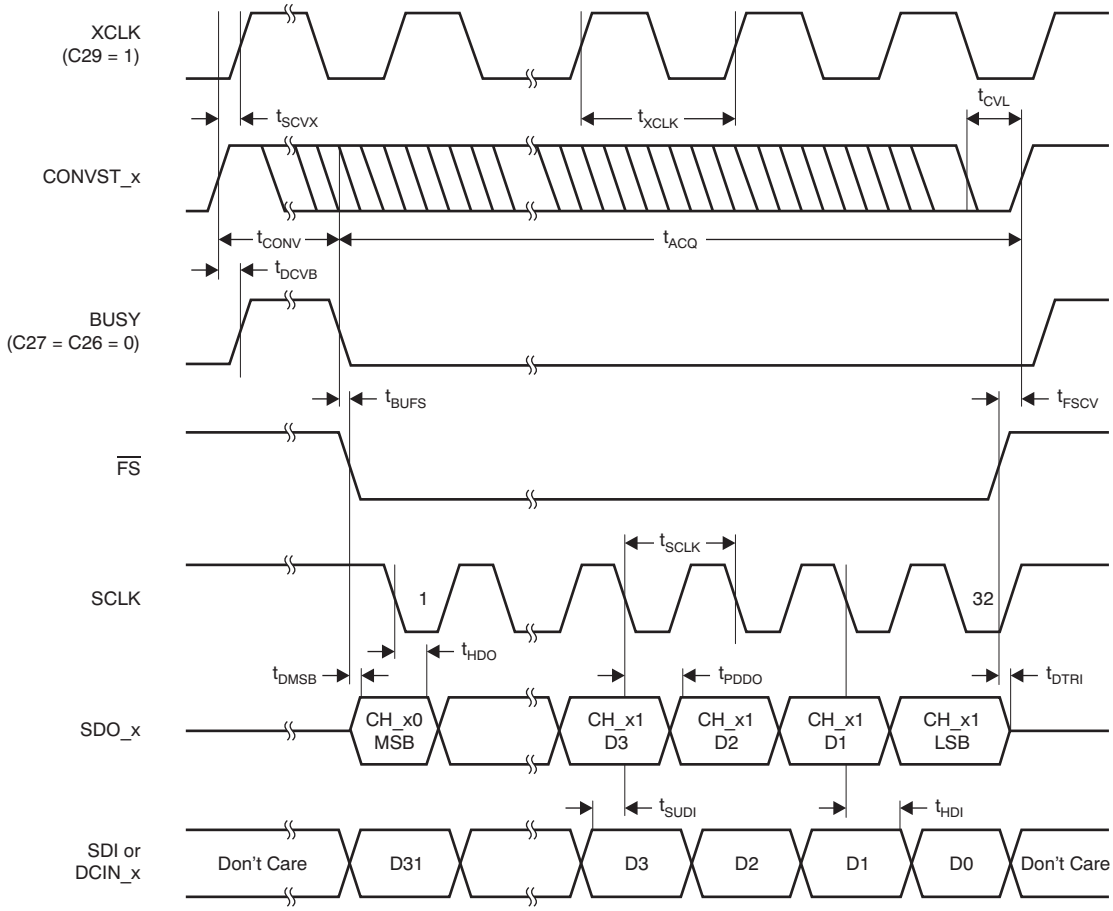

Figure 1. Serial Operation Timing Diagram (All Four SDO_x Active)

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PARAMETER MEASUREMENT INFORMATION (continued)

Table 1. Serial Interface Timing Requirements(1)(2)

PARAMETER		TEST CONDITION	ADS8528, ADS8548, ADS8568			UNIT
			MIN	TYP	MAX	
t_{SCVX}	CONVST_x high to XCLK rising edge setup time	CLKSEL = 1	6			ns
t_{XCLK}	External conversion clock period	ADS8528	66.67			ns
		ADS8548	72.46			ns
		ADS8568	85.11			ns
	External conversion clock frequency	ADS8528	1		15.0	MHz
		ADS8548	1		13.8	MHz
		ADS8568	1		11.75	MHz
	External conversion clock duty cycle		40		60	%
t_{CVL}	CONVST_x low time		20			ns
t_{ACQ}	Acquisition time		280			ns
t_{CONV}	Conversion time		19		20	t_{CCLK} or t_{XCLK}
		ADS8528, CLKSEL = 0			1.33	µs
		ADS8548, CLKSEL = 0			1.45	µs
		ADS8568, CLKSEL = 0			1.7	µs
t_{DCVB}	CONVST_x high to BUSY high delay				25	ns
t_{BUFS}	BUSY low to $\overline{FS}$ low time		0			ns
t_{FSCV}	Bus access finished to next conversion start time	ADS8528	0			ns
		ADS8548	20			ns
		ADS8568	40			ns
t_{SCLK}	Serial clock period		0.022		10	µs
	Serial clock frequency		0.1		45	MHz
	Serial clock duty cycle		40		60	%
t_{DMSB}	$\overline{FS}$ low to MSB valid delay				12	ns
t_{HDO}	Output data to SCLK falling edge hold time		5			ns
t_{PDDO}	SCLK falling edge to new data valid propagation delay				17	ns
t_{DTRI}	$\overline{FS}$ high to SDO_x three-state delay				10	ns
t_{SUDI}	Input data to SCLK falling edge setup time		3			ns
t_{HDI}	Input data to SCLK falling edge hold time		5			ns

(1) Over recommended operating free-air temperature range T_A, AVDD = 5V, and DVDD = 2.7V to 5.5V, unless otherwise noted.
(2) All input signals are specified with $t_R = t_F$ = 1.5ns (10% to 90% of DVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

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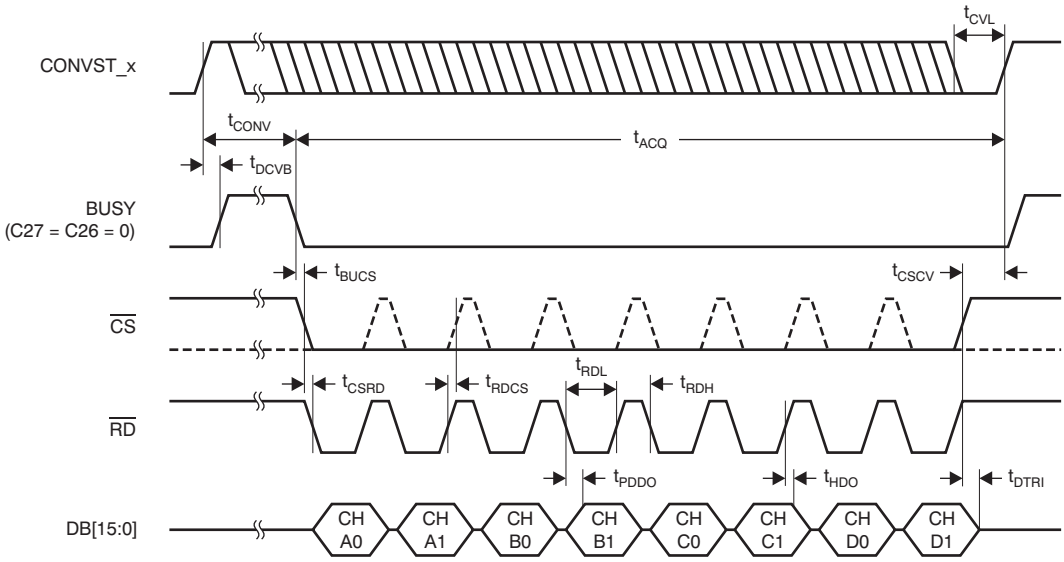

Figure 2. Parallel Read Access Timing Diagram

Table 2. Parallel Interface Timing Requirements (Read Access)(1)(2)

PARAMETER		TEST CONDITION	ADS8528, ADS8548, ADS8568			UNIT
			MIN	TYP	MAX	
t_{CVL}	CONVST_x low time		20			ns
t_{ACQ}	Acquisition time		280			ns
t_{CONV}	Conversion time		19		20	t_{CCLK} or t_{XCLK}
		ADS8528, CLKSEL = 0			1.33	µs
		ADS8548, CLKSEL = 0			1.45	µs
		ADS8568, CLKSEL = 0			1.7	µs
t_{DCVB}	CONVST_x high to BUSY high delay				25	ns
t_{BUCS}	BUSY low to $\overline{CS}$ low time		0			ns
t_{CSCV}	Bus access finished to next conversion start time(3)	ADS8528	0			ns
		ADS8548	20			ns
		ADS8568	40			ns
t_{CSRD}	$\overline{CS}$ low to $\overline{RD}$ low time		0			ns
t_{RDCS}	$\overline{RD}$ high to $\overline{CS}$ high time		0			ns
t_{RDL}	$\overline{RD}$ pulse width		20			ns
t_{RDH}	Minimum time between two read accesses		2			ns
t_{PDDO}	$\overline{RD}$ or $\overline{CS}$ falling edge to data valid propagation delay				15	ns
t_{HDO}	Output data to $\overline{RD}$ or $\overline{CS}$ rising edge hold time		5			ns
t_{DTRI}	$\overline{CS}$ high to DB[15:0] three-state delay				10	ns

(1) Over recommended operating free-air temperature range T_A, AVDD = 5V, and DVDD = 2.7V to 5.5V, unless otherwise noted.
(2) All input signals are specified with $t_R = t_F$ = 1.5ns (10% to 90% of DVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(3) Refer to $\overline{CS}$ signal or $\overline{RD}$, whichever occurs first.

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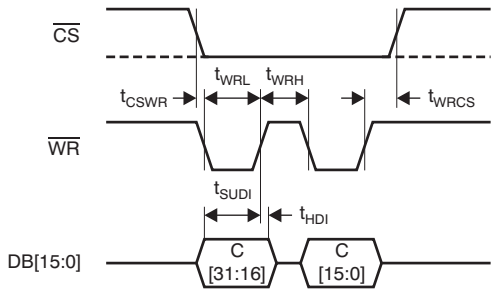

Figure 3. Parallel Write Access Timing Diagram

Table 3. Parallel Interface Timing Requirements (Write Access)(1)(2)

PARAMETER		ADS8528, ADS8548, ADS8568			UNIT
		MIN	TYP	MAX	
t_{CSWR}	$\overline{CS}$ low to $\overline{WR}$ low time	0			ns
t_{WRL}	$\overline{WR}$ low pulse width	15			ns
t_{WRH}	Minimum time between two write accesses	10			ns
t_{WRCS}	$\overline{WR}$ high to $\overline{CS}$ high time	0			ns
t_{SUDI}	Output data to $\overline{WR}$ rising edge setup time	5			ns
t_{HDI}	Data output to $\overline{WR}$ rising edge hold time	5			ns

(1) Over recommended ambient temperature range T_A, AVDD = 5V, and DVDD = 2.7V to 5.5V, unless otherwise noted.
(2) All input signals are specified with $t_R = t_F$ = 1.5ns (10% to 90% of DVDD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

EQUIVALENT CIRCUITS

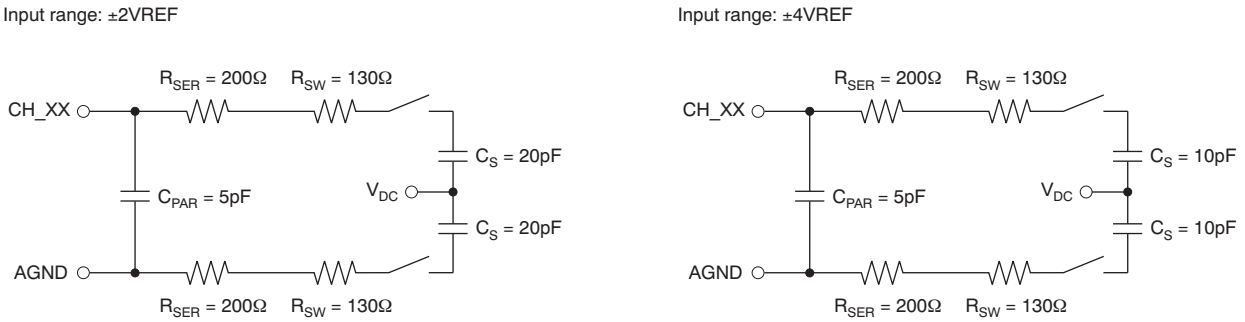

Figure 4. Equivalent Input Circuits

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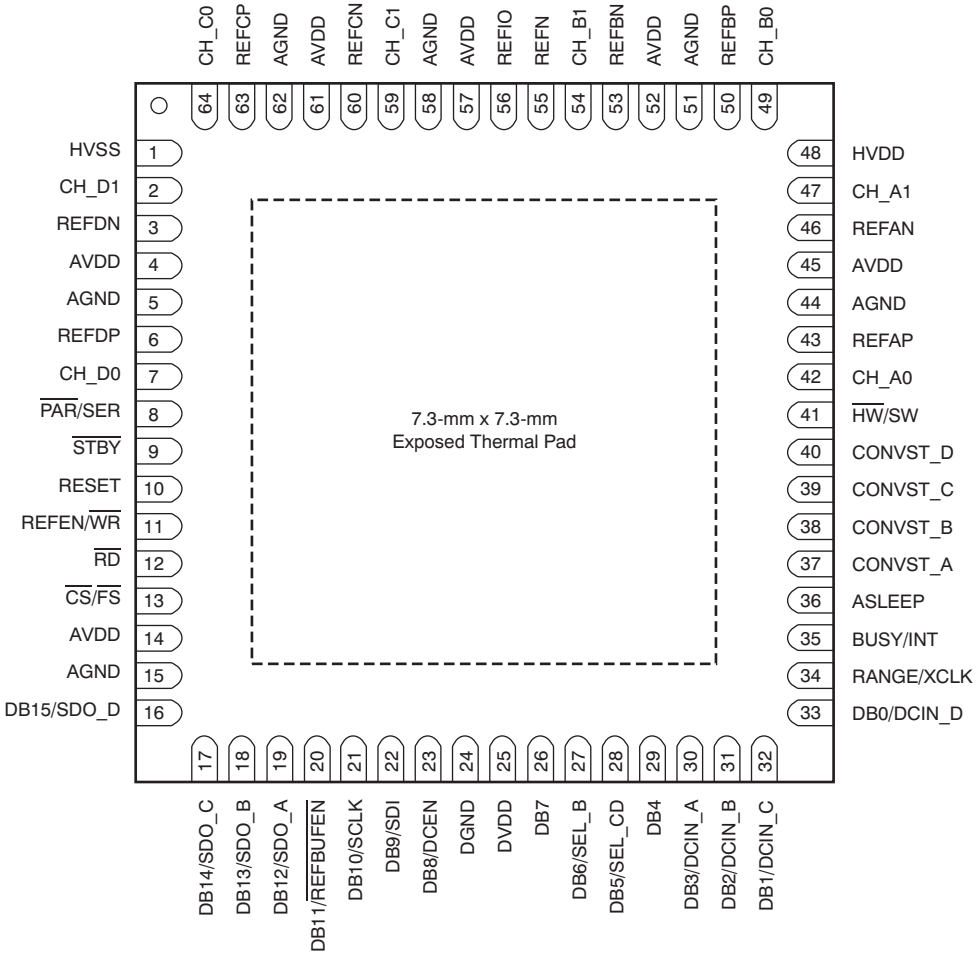
PIN CONFIGURATIONS

RGC PACKAGE
QFN-64
(TOP VIEW)



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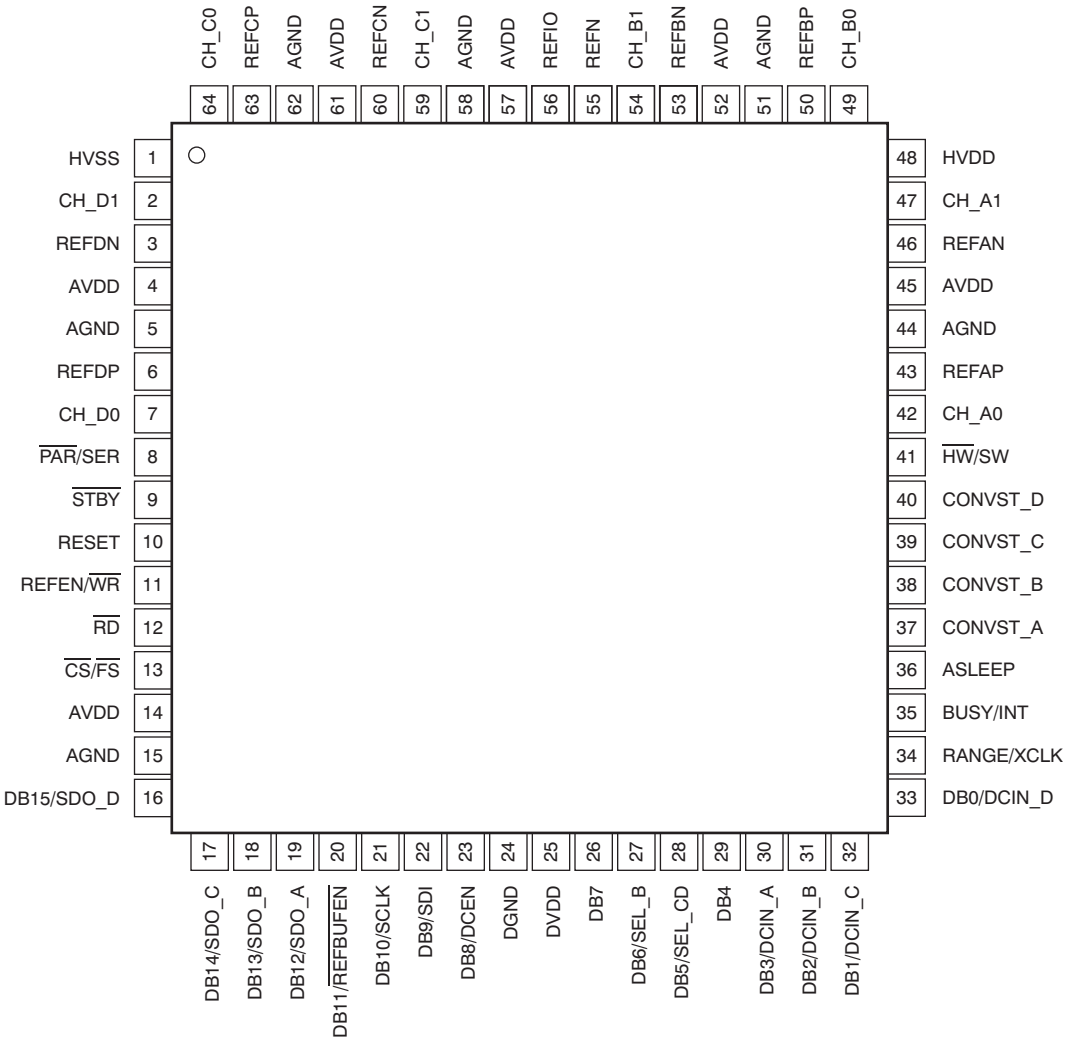
PM PACKAGE
LQFP-64
(TOP VIEW)



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PIN DESCRIPTIONS

PIN #	NAME	TYPE[1]	DESCRIPTION	
			PARALLEL INTERFACE ($\overline{PAR}$/SER = 0)	SERIAL INTERFACE ($\overline{PAR}$/SER = 1)
1	HVSS	P	Negative supply voltage for the analog inputs. Decouple according to the *Power Supply* section.	
2	CH_D1	AI	Analog input of channel D1. The input voltage range is controlled by the RANGE pin in hardware mode or by the Configuration Register (CONFIG) bit C19 (RANGE_D) in software mode. This pin can be powered down using CONFIG bit C18 (PD_D) in software mode.	
3	REFDN	AI	Decoupling capacitor input for reference of channel pair D. Connect to the decoupling capacitor and AGND according to the *Power Supply* section.	
4, 14, 45, 52, 57, 61	AVDD	P	Analog power supply. Decouple according to the *Power Supply* section.	
5, 15, 44, 51, 58, 62	AGND	P	Analog ground; connect to the analog ground plane.	
6	REFDP	AI	Decoupling capacitor input for the channel pair D reference. Connect to the decoupling capacitor according to the *Power Supply* section.	
7	CH_D0	AI	Analog input of channel D0. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C19 (RANGE_D) in software mode. This pin can be powered down using CONFIG bit C18 (PD_D) in software mode.	
8	$\overline{PAR}$/SER	DI	Interface mode selection input. When low, the parallel interface is selected. When high, the serial interface is enabled.	
9	$\overline{STBY}$	DI	Hardware mode ($\overline{HW}$/SW = 0): standby mode input. When low, the entire device is powered down (including the internal conversion clock source and reference). When high, the device operates in normal mode. Software mode ($\overline{HW}$/SW = 1): connect to DGND or DVDD. The standby mode can be activated using CONFIG bit C25 ($\overline{STBY}$).	
10	RESET	DI	Reset input, active high. This pin aborts any ongoing conversions and resets the internal Configuration Register (CONFIG) to 000003FFh. A valid reset pulse should be at least 50 ns long.	
11	REFEN/$\overline{WR}$	DI/DI	Hardware mode ($\overline{HW}$/SW = 0): internal reference enable input. When high, the internal reference is enabled (the reference buffers are also enabled). When low, the internal reference is disabled and an external reference is applied at REFIO. Software mode ($\overline{HW}$/SW = 1): write input. The parallel data input is enabled when $\overline{CS}$ and $\overline{WR}$ are low. The internal reference is enabled by CONFIG bit C15 (REFEN).	Hardware mode ($\overline{HW}$/SW = 0): internal reference enable input. When high, the internal reference is enabled (the reference buffers are also enabled). When low, the internal reference is disabled and an external reference is applied at REFIO. Software mode ($\overline{HW}$/SW = 1): connect to DGND or DVDD. The internal reference is enabled by CONFIG bit C15 (REFEN).
12	$\overline{RD}$	DI/DI	Read data input. When low, the parallel data output is enabled (if $\overline{CS}$ = 0). When high, the data output is disabled.	Must be connected to DGND.
13	$\overline{CS}$/$\overline{FS}$	DI/DI	Chip select input. When low, the parallel interface is enabled. When high, the interface is disabled.	Frame synchronization. The $\overline{FS}$ falling edge controls the frame transfer.
16	DB15/SDO_D	DIO/DO	Data bit 15 (MSB) input/output. Output is sign extension for the ADS8528/48.	When SEL_CD = 1, this pin is the data output for channel pair D. When SEL_CD = 0, this pin should be tied to DGND.
17	DB14/SDO_C	DIO/DO	Data bit 14 input/output. Output is sign extension for the ADS8528/48.	When SEL_CD = 1, this pin is the data output for channel pair C. When SEL_CD = 0, this pin should be tied to DGND.
18	DB13/SDO_B	DIO/DO	Data bit 13 input/output. Output is sign extension for the ADS8528 and MSB for the ADS8548.	When SEL_B = 1, this pin is the data output for channel pair B. When SEL_B = 0, this pin should be tied to DGND. When SEL_CD = 0, data from channel pair D are also available on this output.
19	DB12/SDO_A	DIO/DO	Data bit 12 input/output. Output is sign extension for the ADS8528.	Data output for channel pair A. When SEL_CD = 0, data from channel pair C are also available on this output. When SEL_CD = 0 and SEL_B = 0, SDO_A acts as single data output for all eight channels.

(1) AI = analog input; AIO = analog input/output; DI = digital input; DO = digital output; DIO = digital input/output; and P = power supply.

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PIN DESCRIPTIONS (continued)

PIN #	NAME	TYPE[1]	DESCRIPTION	
			PARALLEL INTERFACE ($\overline{PAR}$/SER = 0)	SERIAL INTERFACE ($\overline{PAR}$/SER = 1)
20	DB11/$\overline{REFBUFEN}$	DIO/DI	Data bit 11 input/output. Output is MSB for the ADS8528.	Hardware mode ($\overline{HW}$/SW = 0): reference buffer enable input. When low, all internal reference buffers are enabled (mandatory if internal reference is used). When high, all reference buffers are disabled.
				Software mode ($\overline{HW}$/SW = 1): connect to DGND or DVDD. The internal reference buffers are controlled by bit C14 ($\overline{REFBUFEN}$) in the Configuration Register (CONFIG).
21	DB10/SCLK	DIO/DI	Data bit 10 input/output	Serial interface clock input.
22	DB9/SDI	DIO/DI	Data bit 9 input/output	Hardware mode ($\overline{HW}$/SW = 0): connect to DGND.
				Software mode ($\overline{HW}$/SW = 1): serial data input.
23	DB8/DCEN	DIO/DI	Data bit 8 input/output	Daisy-chain enable input. When high, DB[3:0] serve as daisy-chain inputs DCIN_[A:D]. If daisy-chain mode is not used, connect to DGND.
24	DGND	P	Buffer I/O ground, connect to digital ground plane	
25	DVDD	P	Buffer I/O supply, connect to digital supply. Decouple according to the *Power Supply* section.	
26	DB7	DIO	Data bit 7 input/output	Must be connected to DGND
27	DB6/SEL_B	DIO/DI	Data bit 6 input/output	Select SDO_B input. When low, SDO_B is disabled and data from all eight channels are only available through SDO_A. When high and SEL_CD = 0, data from channel pairs B and D are available on SDO_B. When SEL_CD = 1, data from channel pair B are available on SDO_B.
28	DB5/SEL_CD	DIO/DI	Data bit 5 input/output	Select SDO_C and SDO_D input. When high, data from channel pair C are available on SDO_C while data from channel pair D are available on SDO_D. When low and SEL_B = 1, data from channel pairs A and C are available on SDO_A while data from channel pairs B and D are available on SDO_B. When low and SEL_B = 0, data from all eight channels are avaiable on SDO_A.
29	DB4	DIO	Data bit 4 input/output	Connect to DGND
30	DB3/DCIN_A	DIO/DI	Data bit 3 input/output	When DCEN = 1, this pin is the daisy-chain data input for SDO_A of the previous device in the chain. When DCEN = 0, connect to DGND.
31	DB2/DCIN_B	DIO/DI	Data bit 2 input/output	When DCEN = 1 and SEL_B = 1, this pin is the daisy-chain data input for SDO_B of the previous device in the chain. When DCEN = 0, connect to DGND.
32	DB1/DCIN_C	DIO/DI	Data bit 1 input/output	When DCEN = 1 and SEL_CD = 1, this pin is the daisy-chain data input for SDO_C of the previous device in the chain. When DCEN = 0, connect to DGND.
33	DB0/DCIN_D	DIO/DI	Data bit 0 (LSB) input/output	When DCEN = 1 and SEL_CD = 1, this pin is the daisy-chain data input for SDO_D of the previous device in the chain. When DCEN = 0, connect to DGND.
34	RANGE/XCLK	DI/DI/DO	Hardware mode ($\overline{HW}$/SW = 0): analog input voltage range select input. When low, the analog input voltage range is ±4VREF. When high, the analog input voltage range is ±2VREF.	
			Sofware mode ($\overline{HW}$/SW = 1): this pin is an external conversion clock input if CONFIG bit C29 = 1 (CLKSEL); or an internal conversion clock output if CONFIG bit C28 = 1 (CLKOUT_EN). If this pin is not used, connect to DGND.	
35	BUSY/INT	DO	When CONFIG bit C27 = 0 (BUSY/INT) this pin is a converter busy status output. This pin transitions high when a conversion has been started and transitions low for a single conversion clock cycle (t_{CCLK}) whenever a channel pair conversion is completed and stays low when the conversion of the last channel pair has completed. When bit C27 = 1 (BUSY/INT in CONFIG), this pin is an interrupt output. This pin transitions high after a conversion has been completed and remains high until the next read access. This mode can only be used if all eight channels are sampled simultaneously (all CONVST_x tied together). The polarity of the BUSY/INT output can be changed using bit C26 (BUSY L/H) in the Configuration Register.	

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PIN DESCRIPTIONS (continued)

PIN #	NAME	TYPE[1]	DESCRIPTION	
			PARALLEL INTERFACE ($\overline{PAR}$/SER = 0)	SERIAL INTERFACE ($\overline{PAR}$/SER = 1)
36	ASLEEP	DI	Auto-sleep enable input. When low, the device operates in normal mode. When high, the device works in auto-sleep mode where the hold mode and the actual conversion is activated 6 conversion clock (t_{CCLK}) cycles after issuing a conversion start using a CONVST_x. This mode is recommended to save power if the device runs at a lower data rate; see the *Reset and Power-Down Modes* section for more details.	
37	CONVST_A	DI	Conversion start of channel pair A. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_A[1:0]. This signal resets the internal channel state machine that causes the data output to start with conversion results of channel A0 with the next read access.	
38	CONVST_B	DI	Conversion start of channel pair B. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_B[1:0].	
39	CONVST_C	DI	Conversion start of channel pair C. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_C[1:0].	
40	CONVST_D	DI	Conversion start of channel pair D. The rising edge of this signal initiates simultaneous conversion of analog signals at inputs CH_D[1:0].	
41	$\overline{HW}$/SW	DI	Mode selection input. When low, the hardware mode is selected and the device functions according to the settings of the external pins. When high, the software mode is selected in which the device is configured by writing to the Configuration Register (CONFIG).	
42	CH_A0	AI	Analog input of channel A0; channel A is the master channel pair that is always active. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C24 (RANGE_A) in software mode. In cases where channel pairs of the device are used at different data rates, channel pair A should always run at the highest data rate.	
43	REFAP	AI	Decoupling capacitor input for reference of channel pair A. Connect to the decoupling capacitor according to the *Power Supply* section.	
46	REFAN	AI	Decoupling capacitor input for reference of channel pair A. Connect to the decoupling capacitor and AGND according to the *Power Supply* section.	
47	CH_A1	AI	Analog input of channel A1; channel A is the master channel pair that is always active. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C24 (RANGE_A) in software mode. In cases where channel pairs of the device are used at different data rates, channel pair A should always run at the highest data rate.	
48	HVDD	P	Positive supply voltage for the analog inputs. Decouple according to the *Power Supply* section.	
49	CH_B0	AI	Analog input of channel B0. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C23 (RANGE_B) in software mode.	
50	REFBP	AI	Decoupling capacitor input for reference of channel pair B. Connect to the decoupling capacitor according to the *Power Supply* section.	
53	REFBN	AI	Decoupling capacitor input for reference of channel pair B. Connect to the decoupling capacitor and AGND according to the *Power Supply* section.	
54	CH_B1	AI	Analog input of channel B1. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C23 (RANGE_B) in software mode.	
55	REFN	AI	Negative reference input/output pin. Connect to a decoupling capacitor and AGND according to the *Power Supply* section.	
56	REFIO	AIO	Reference voltage input/output. The internal reference is enabled by the REFEN/$\overline{WR}$ pin in hardware mode or by CONFIG bit C15 (REFEN) in software mode. The output value is controlled by the internal DAC (CONFIG bits C[9:0]). Connect to a decoupling capacitor according to the *Power Supply* section.	
59	CH_C1	AI	Analog input of channel C1. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C21 (RANGE_C) in software mode.	
60	REFCN	AI	Decoupling capacitor input for reference of channel pair C. Connect to the decoupling capacitor and AGND according to the *Power Supply* section.	
63	REFCP	AI	Decoupling capacitor input for reference of channel pair C. Connect to the decoupling capacitor according to the *Power Supply* section.	
64	CH_C0	AI	Analog input of channel C0. The input voltage range is controlled by the RANGE pin in hardware mode or by CONFIG bit C21 (RANGE_C) in software mode.	

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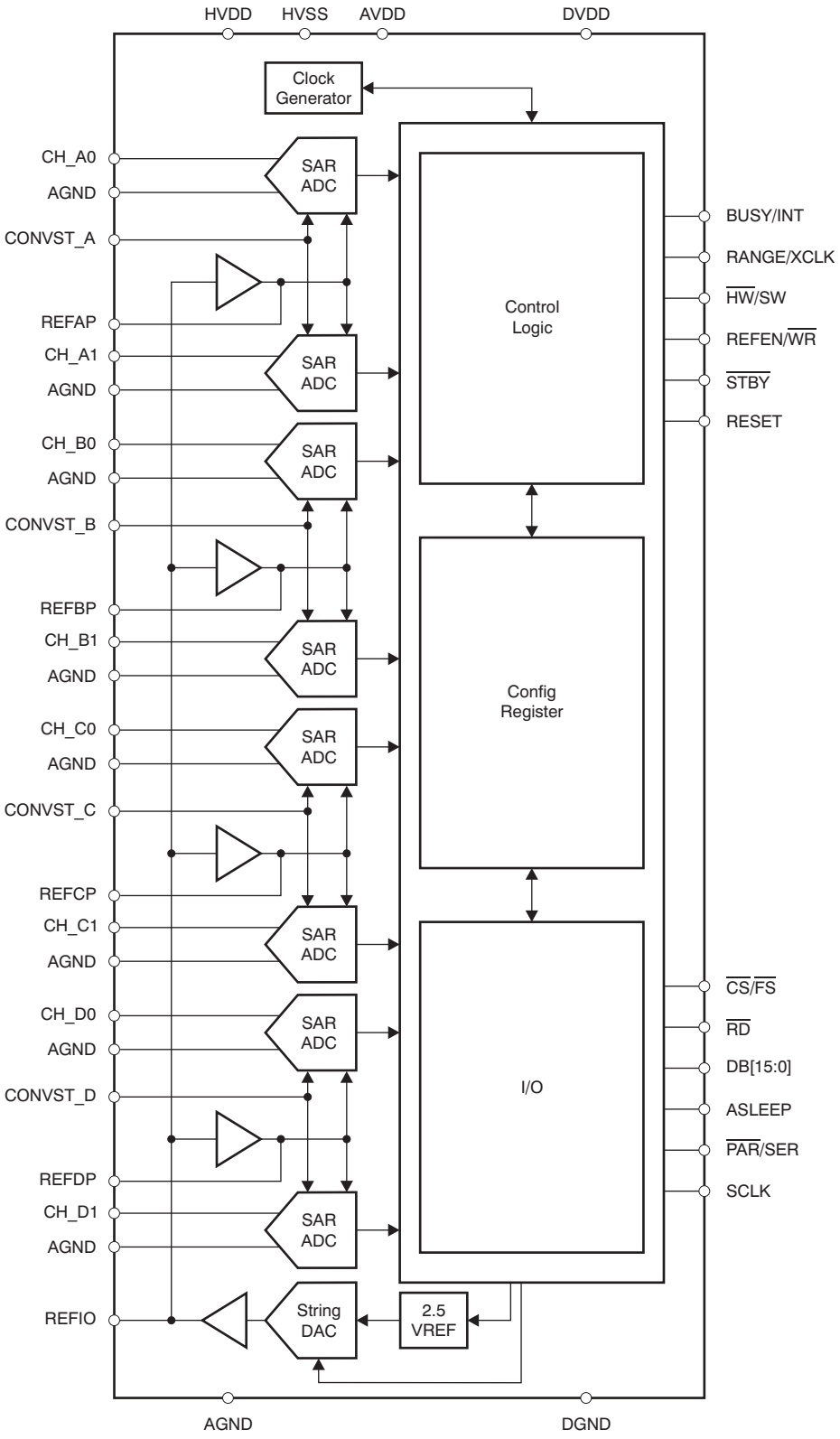
FUNCTIONAL BLOCK DIAGRAM



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TYPICAL CHARACTERISTICS

Graphs are valid for all devices of the family, at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = maximum, unless otherwise noted.

INL vs CODE (ADS8528)

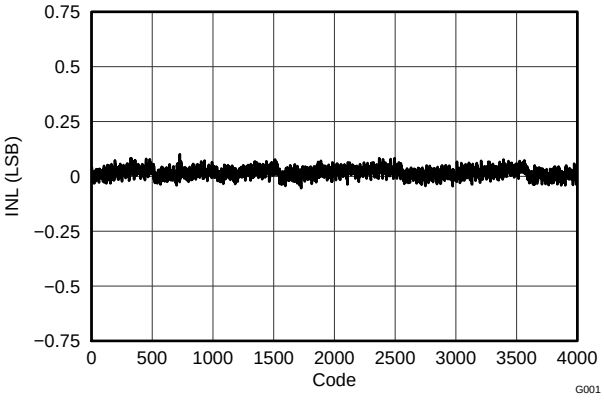

Figure 5.

DNL vs CODE (ADS8528)

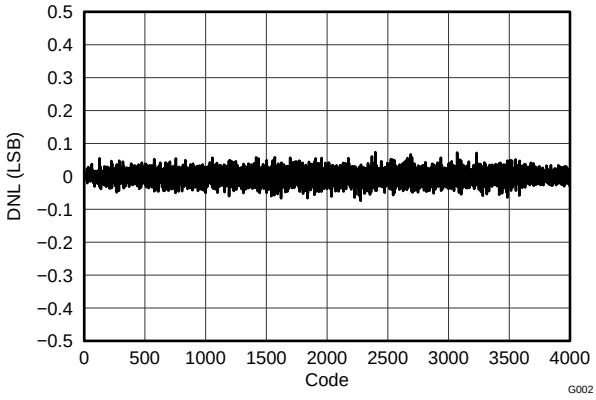

Figure 6.

INL vs CODE (ADS8548 ±10V_{IN} Range)

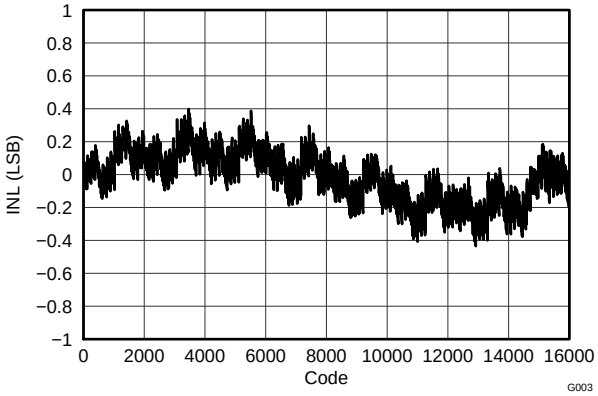

Figure 7.

INL vs CODE (ADS8548 ±5V_{IN} Range)

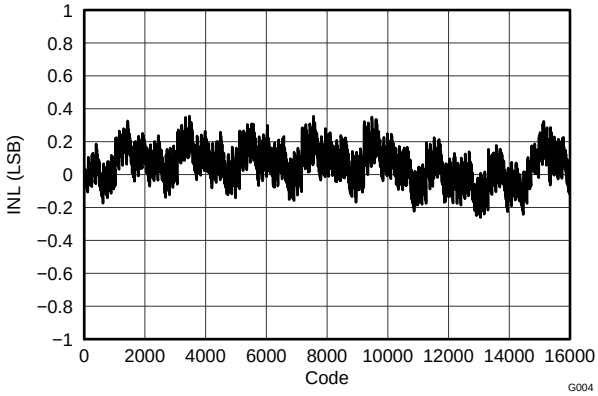

Figure 8.

DNL vs CODE (ADS8548 ±10V_{IN} Range)

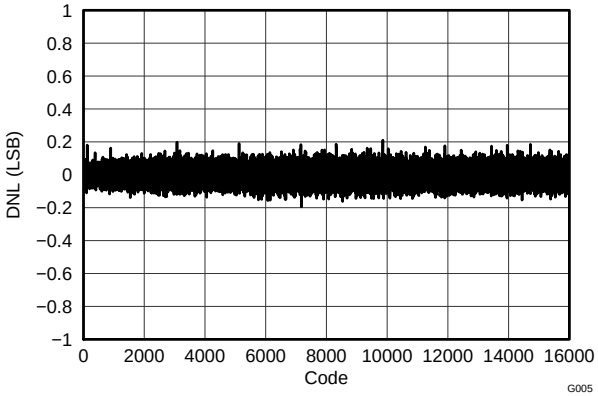

Figure 9.

DNL vs CODE (ADS8548 ±5V_{IN} Range)

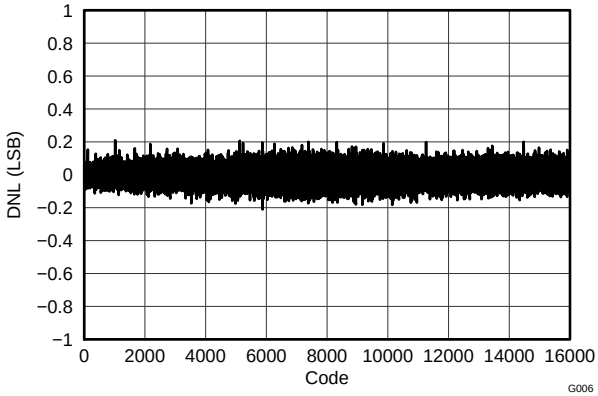

Figure 10.

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TYPICAL CHARACTERISTICS (continued)

Graphs are valid for all devices of the family, at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = maximum, unless otherwise noted.

INL vs CODE
(ADS8568 ±10V_{IN} Range)

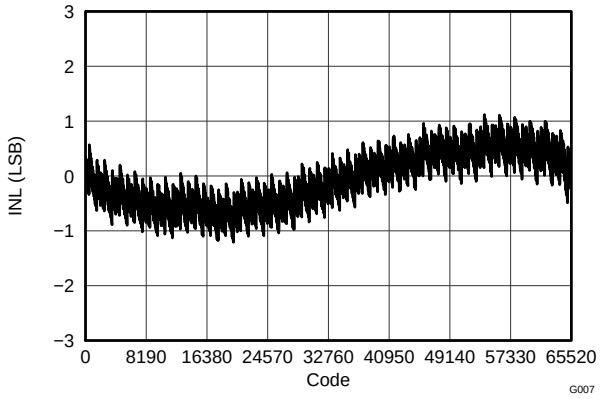

Figure 11.

INL vs CODE
(ADS8568 ±5V_{IN} Range)

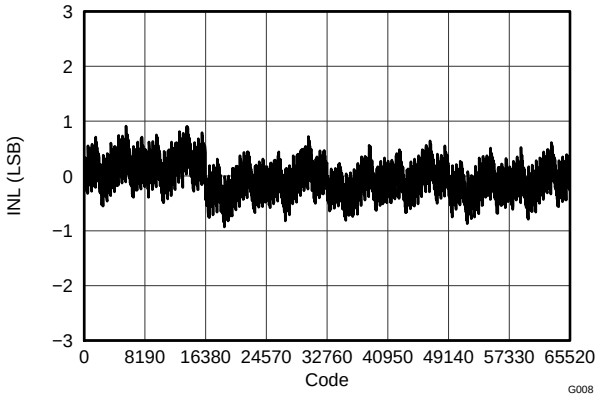

Figure 12.

DNL vs CODE
(ADS8568 ±10V_{IN} Range)

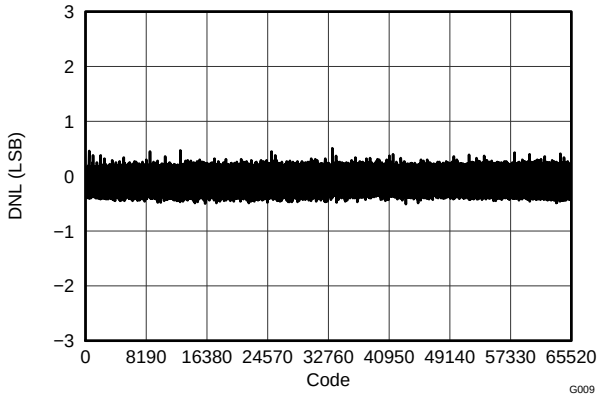

Figure 13.

DNL vs CODE
(ADS8568 ±5V_{IN} Range)

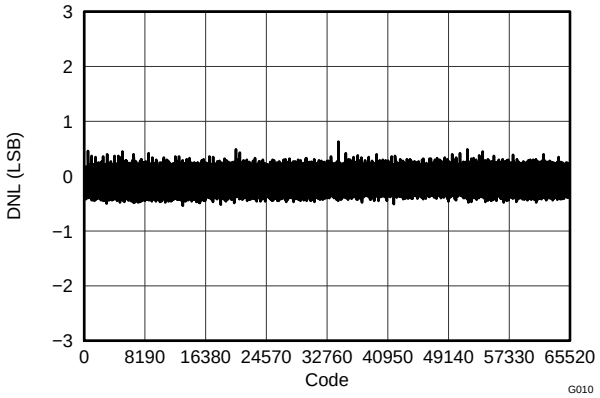

Figure 14.

OFFSET ERROR vs TEMPERATURE

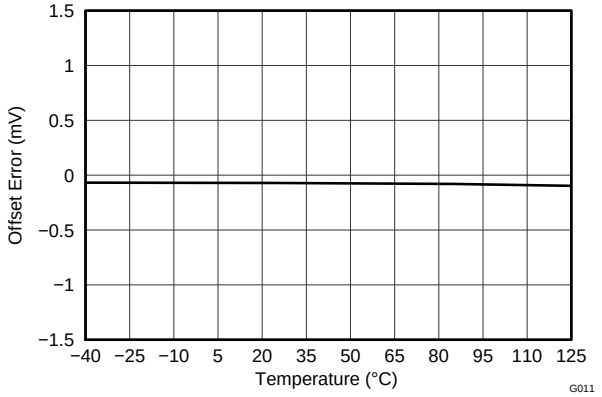

Figure 15.

GAIN ERROR vs TEMPERATURE

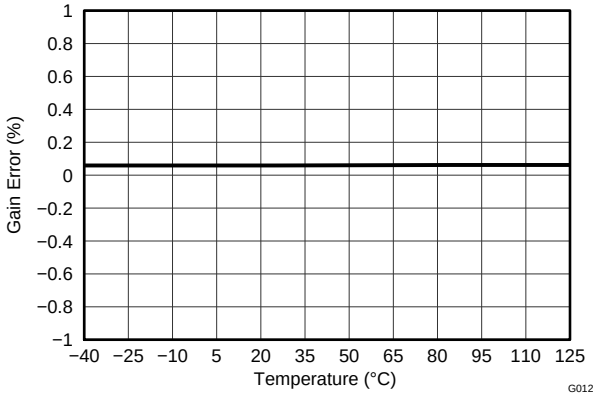

Figure 16.

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TYPICAL CHARACTERISTICS (continued)

Graphs are valid for all devices of the family, at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = maximum, unless otherwise noted.

PSRR vs SUPPLY NOISE FREQUENCY

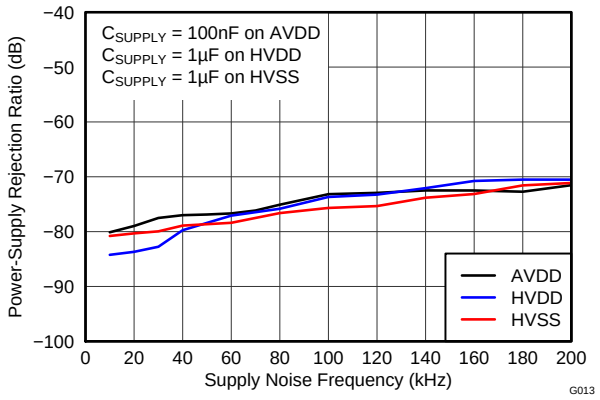

Figure 17.

CONVERSION TIME vs TEMPERATURE

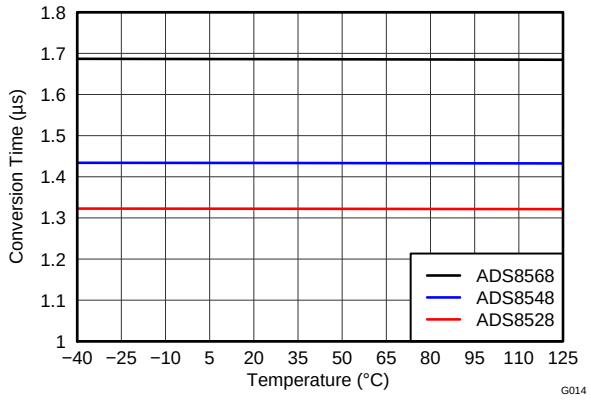

Figure 18.

CODE HISTOGRAM (ADS8568, 16390 Hits)

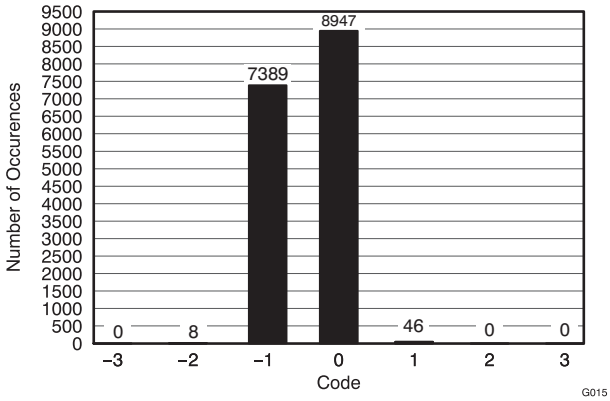

Figure 19.

SNR vs TEMPERATURE

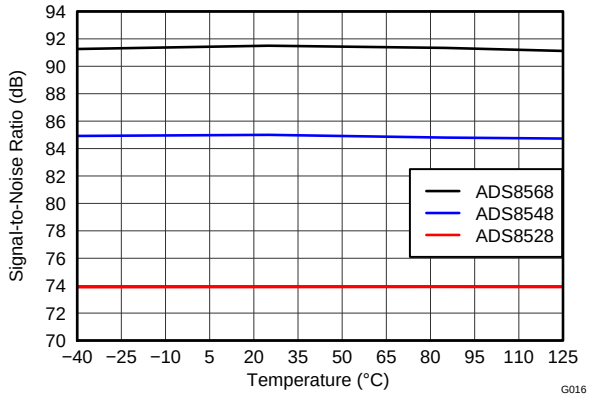

Figure 20.

SINAD vs TEMPERATURE

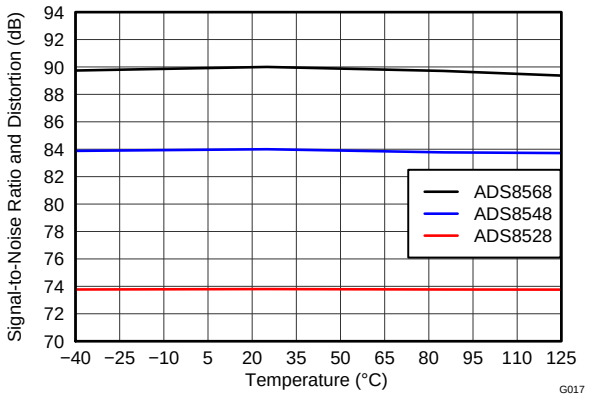

Figure 21.

THD vs TEMPERATURE

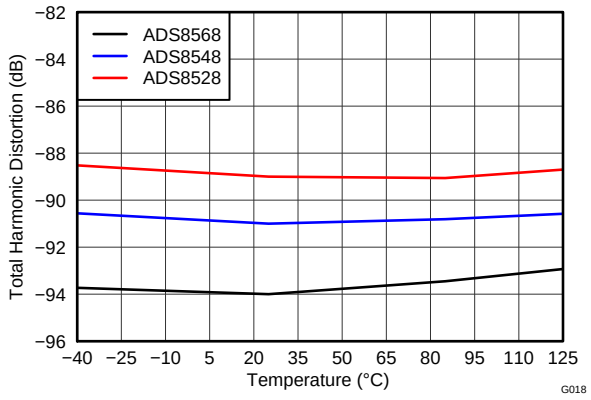

Figure 22.

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TYPICAL CHARACTERISTICS (continued)

Graphs are valid for all devices of the family, at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = maximum, unless otherwise noted.

SFDR vs TEMPERATURE

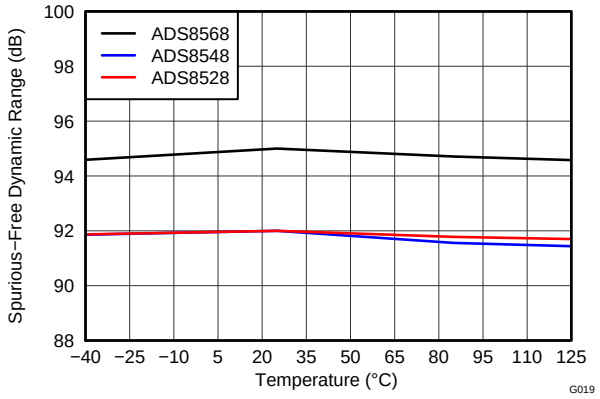

Figure 23.

FREQUENCY SPECTRUM
(ADS8568, 2048-Point FFT, f_{IN} = 10kHz, ±10V_{IN} Range)

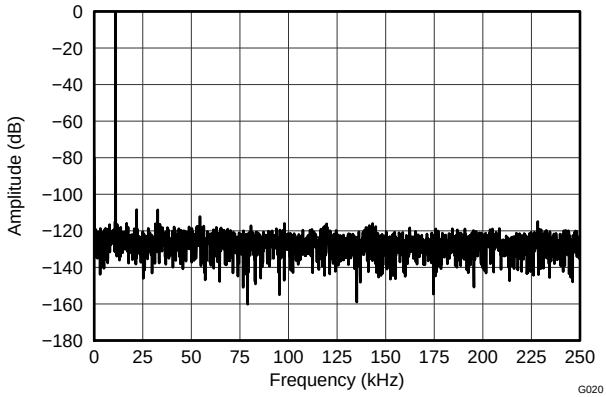

Figure 24.

FREQUENCY SPECTRUM
(ADS8568, 2048-Point FFT, f_{IN} = 10kHz, ±5V_{IN} Range)

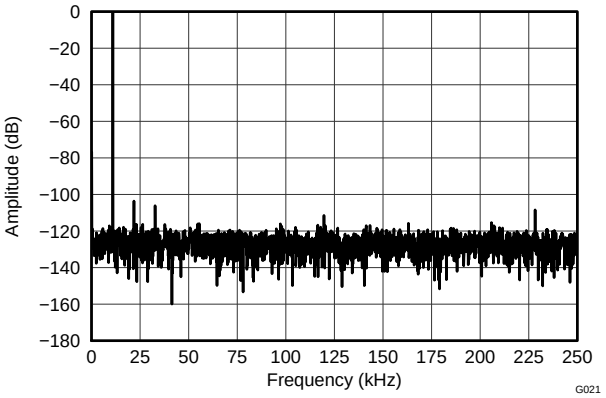

Figure 25.

CHANNEL-TO-CHANNEL ISOLATION vs
INPUT NOISE FREQUENCY

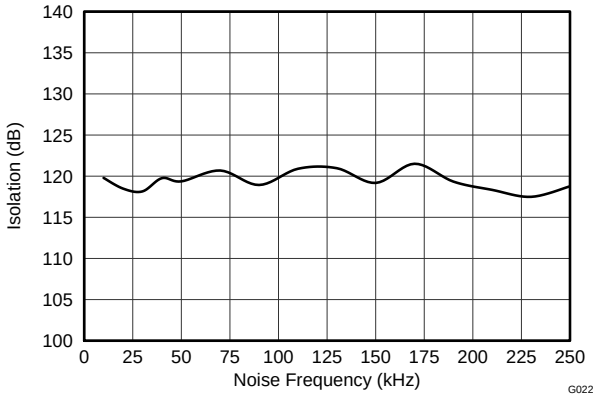

Figure 26.

INTERNAL REFERENCE VOLTAGE vs
ANALOG SUPPLY VOLTAGE (2.5V Mode)

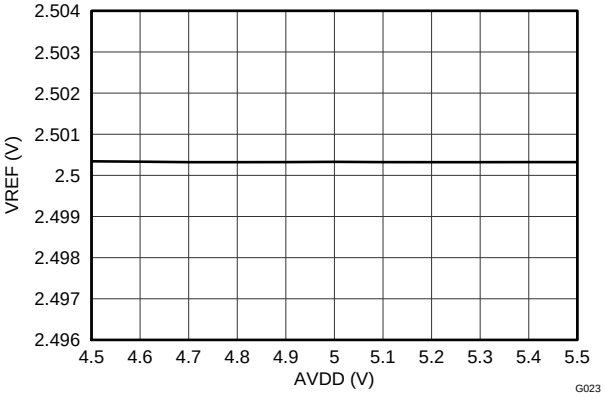

Figure 27.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE
(2.5V Mode)

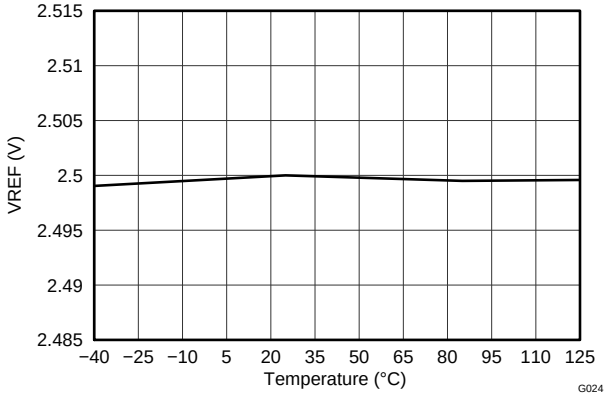

Figure 28.

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TYPICAL CHARACTERISTICS (continued)

Graphs are valid for all devices of the family, at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = maximum, unless otherwise noted.

INTERNAL REFERENCE VOLTAGE vs TEMPERATURE (3.0V Mode)

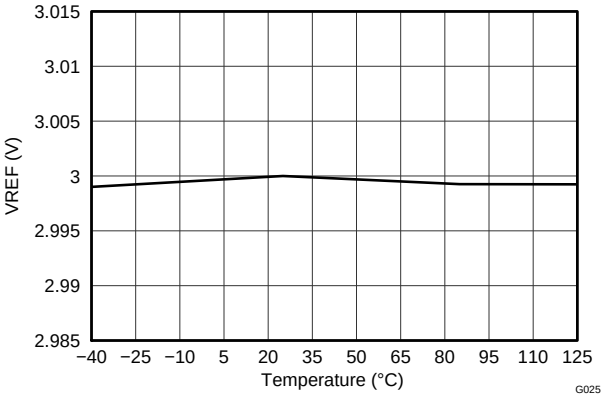

Figure 29.

ADS8568 ANALOG SUPPLY CURRENT vs TEMPERATURE

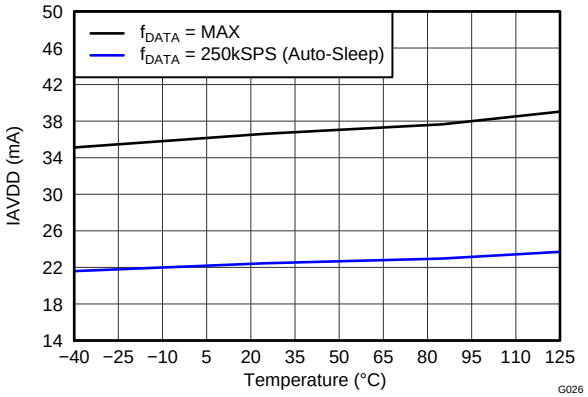

Figure 30.

ADS8568 ANALOG SUPPLY CURRENT vs DATA RATE

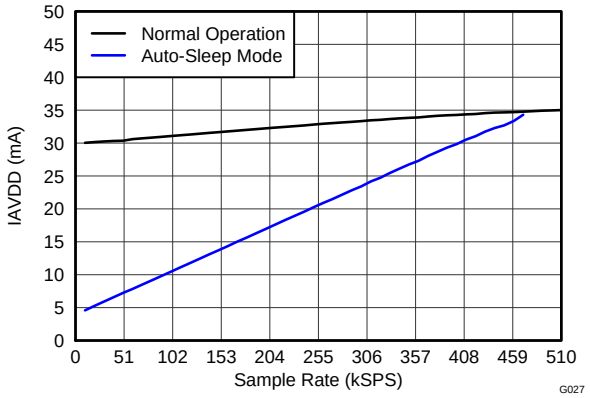

Figure 31.

BUFFER I/O SUPPLY CURRENT vs TEMPERATURE

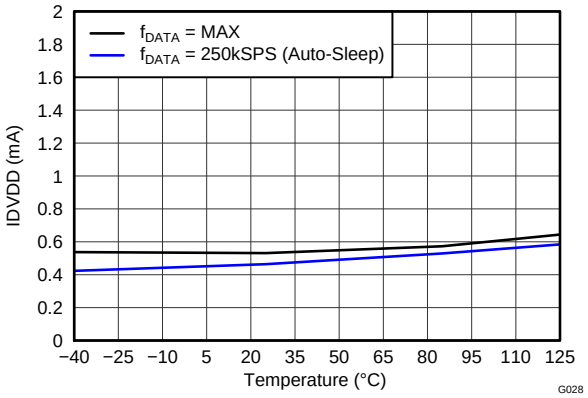

Figure 32.

ADS8568 INPUT SUPPLY CURRENT vs TEMPERATURE

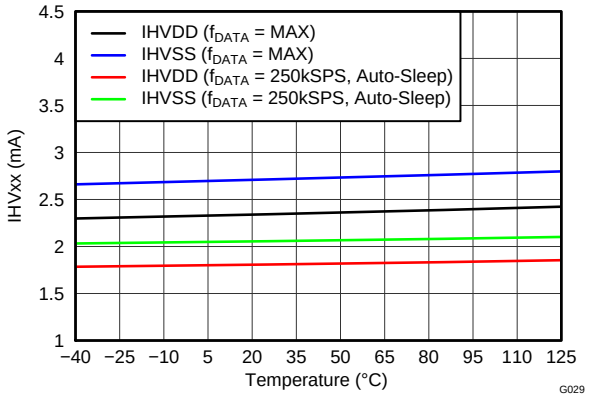

Figure 33.

ADS8568 INPUT SUPPLY CURRENT vs INPUT SUPPLY VOLTAGE

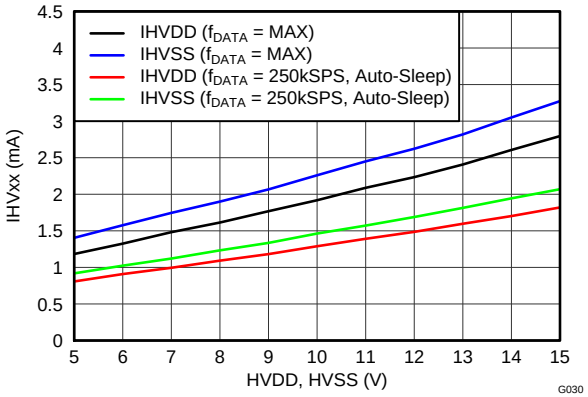

Figure 34.

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TYPICAL CHARACTERISTICS (continued)

Graphs are valid for all devices of the family, at T_A = +25°C, HVDD = 15V, HVSS = –15V, AVDD = 5V, and DVDD = 3.3V, VREF = 2.5V (internal), V_{IN} = ±10V, and f_{DATA} = maximum, unless otherwise noted.

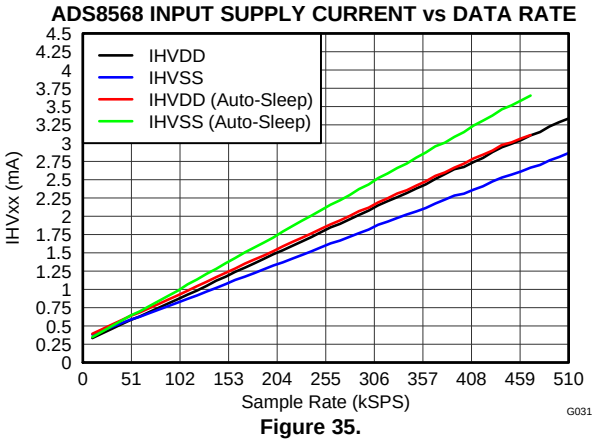

Figure 35.

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GENERAL DESCRIPTION

The ADS8528/48/68 series includes eight 12-, 14-, and 16-bit analog-to-digital converters (ADCs), respectively, that operate based on the successive approximation register (SAR) architecture. This architecture is designed on the charge redistribution principle, which inherently includes a sample-and-hold function. The eight analog inputs are grouped into four channel pairs. These channel pairs can be sampled and converted simultaneously, preserving the relative phase information of the signals of each pair. Separate conversion start signals allow simultaneous sampling on each channel pair of four, six, or eight channels. These devices accept single-ended, bipolar analog input signals in the selectable ranges of ±4VREF or ±2VREF with an absolute value of up to ±12V; see the *Analog Inputs* section.

The devices offer an internal 2.5V or 3V reference source followed by a 10-bit digital-to-analog converter (DAC) that allows the reference voltage VREF to be adjusted in 2.44mV or 2.93mV steps, respectively.

The ADS8528/48/68 also offer a selectable parallel or serial interface that can be used in hardware or software mode; see the *Device Configuration* section for details. The *Analog* and *Digital* sections describe the functionality and control of the device in detail.

ANALOG

This section addresses the analog input circuit, the ADCs and control signals, and the reference design of the device.

Analog Inputs

The inputs and the converters are of single-ended bipolar type. The absolute voltage range can be selected using the RANGE pin (in hardware mode) or RANGE_x bits (in software mode) in the Configuration (CONFIG) Register to either ±4VREF or ±2VREF. With the internal reference set to 2.5V (VREF bit C13 = 0 in the CONFIG Register), the input voltage range can be ±10V or ±5V. With the internal reference source set to 3V (CONFIG bit C13 = 1), an input voltage range of ±12V or ±6V can be configured. The logic state of the RANGE pin is latched with the falling edge of BUSY (if CONFIG bit C26 = 0).

The input current on the analog inputs depends on the actual sample rate, input voltage, and signal source impedance. Essentially, the current into the analog inputs charges the internal capacitor array only during the sampling period (t_{ACQ}). The source of the analog input voltage must be able to charge the input capacitance of 10pF in ±4VREF mode or of 20pF in ±2VREF mode to a 12-, 14-, or 16-bit accuracy level within the acquisition time; see Figure 4. During the conversion period, there is no further input current flow and the input impedance is greater than 1MΩ. To ensure a defined start condition, the sampling capacitors of the ADS8528/48/68 are pre-charged to a fixed internal voltage before switching into sampling mode.

To maintain the linearity of the converter, the inputs should always remain within the specified range shown in the Electrical Characteristics table. The minimum –3dB bandwidth of the driving operational amplifier can be calculated using Equation 1:

$$f_{3dB} = \frac{\ln(2)(n + 1)}{2\pi t_{ACQ}} \quad (1)$$

where:

n = 12, 14, or 16; *n* is the resolution of the ADS8528/48/68

With a minimum acquisition time of t_{ACQ} = 280ns, the required minimum bandwidth of the driving amplifier is 5.2MHz for the ADS8528, 6.0MHz for the ADS8548, or 6.7MHz for the ADS8568. The required bandwidth can be lower if the application allows a longer acquisition time. A gain error occurs if a given application does not fulfill the bandwidth requirement shown in Equation 1.

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A driving operational amplifier may not be required, if the impedance of the signal source (R_{SOURCE}) fulfills the requirement of Equation 2:

$$R_{SOURCE} < \frac{t_{ACQ}}{C_S \ln(2)(n + 1)} - (R_{SER} + R_{SW}) \quad (2)$$

where:

n = 12, 14, or 16; *n* is the resolution of the ADC,
C_S = 10pF is the sample capacitor value in V_{IN} = ±4VREF mode,
R_{SER} = 200Ω is the input resistor value,
and R_{SW} = 130Ω is the switch resistance value.

With a minimum acquisition time of t_{ACQ} = 280ns, the maximum source impedance should be less than 2.7kΩ for the ADS8528, 2.3kΩ for the ADS8548, and 2.0kΩ for the ADS8568 in ±4VREF mode, or less than 1.2kΩ for the ADS8528, 1.0kΩ for the ADS8548, and 0.8kΩ for the ADS8568 in ±2VREF mode. The source impedance can be higher if the application allows longer acquisition time.

Analog-to-Digital Converter (ADC)

The device includes eight ADCs that operate with either an internal or an external conversion clock.

Conversion Clock

The device uses either an internally-generated (CCLK) or an external (XCLK) conversion clock signal (in software mode only). In default mode, the device generates an internal clock. In this case, a complete conversion including the pre-charging of the sample capacitors takes 19 to 20 clock cycles, depending on the setup time of the incoming CONVST_x signal with relation to the rising edge of the CCLK.

When CLKSEL bit is set high (CONFIG bit C29), an external conversion clock can be applied on pin 34. A complete conversion process requires 19 clock cycles in this case if the t_{SCVX} timing requirement is fulfilled. The external clock can remain low between conversions.

If the application requires lowest power dissipation at low data rates, it is recommended to use the auto-sleep mode, activated using pin 36 (ASLEEP). In this case, a conversion cycle takes up to 26 clock cycles (see the *Reset and Power-Down Modes* section for more details).

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CONVST_x

The analog inputs of each channel pair (CH_x0/1) are held with the rising edge of the corresponding CONVST_x signal. The conversion automatically starts with the next rising edge of the conversion clock. CONVST_A is a master conversion start that resets the internal state machine and causes the data output to start with the result of channel A0. In cases where channel pairs of the device are used at different data rates, CONVST_A should always be the one used at the highest frequency.

A conversion start must not be issued during an ongoing conversion on the corresponding channel pair. It is allowed to initiate conversions on the other input pairs, however.

If a parallel interface is used, the content of the output port depends on which CONVST_x signals have been issued. Figure 36 shows examples of different scenarios with all channel pairs active.

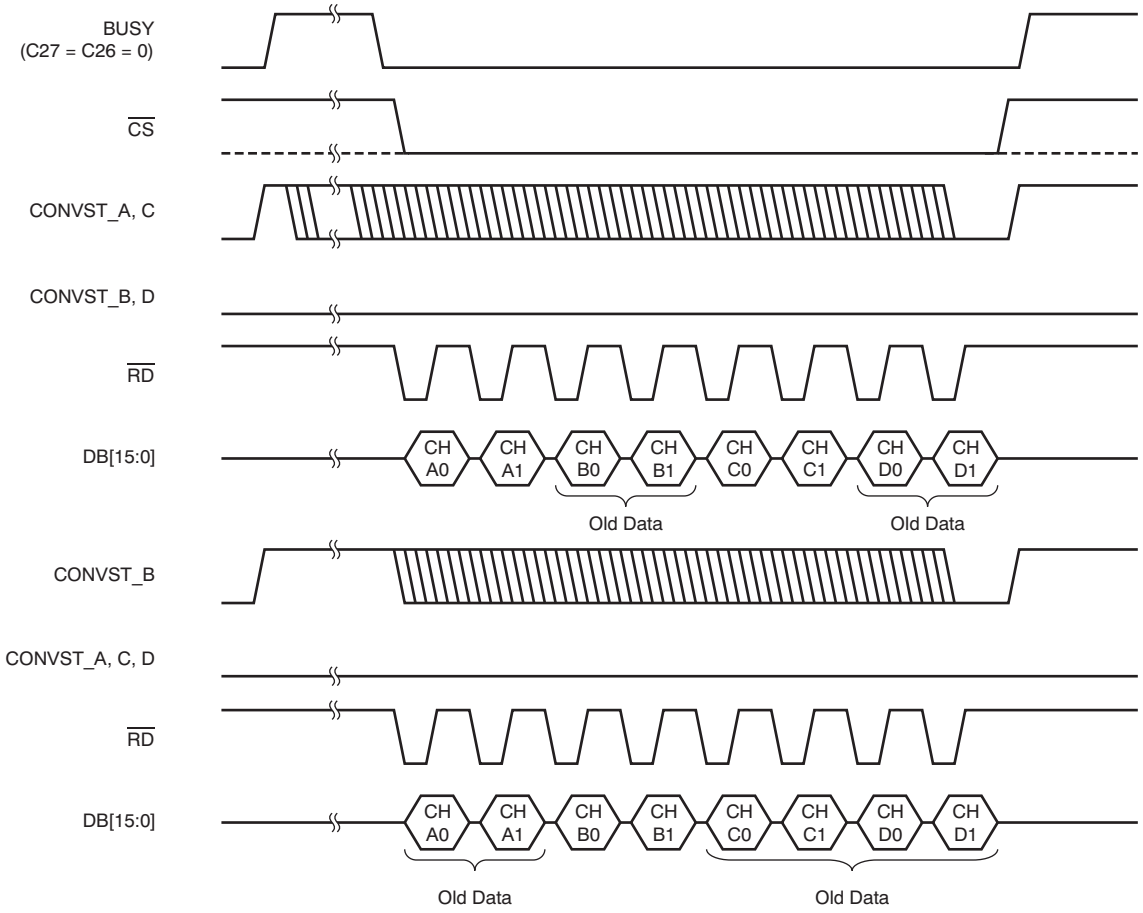

Figure 36. Data Output versus CONVST_x (All Channels Active)

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BUSY/INT

The BUSY signal indicates if a conversion is in progress. It goes high with a rising edge of any CONVST_x signal and goes low when the output data of the last channel pair are available in the respective output register. The readout of the data can be initiated immediately after the falling edge of BUSY.

In contrary, the INT signal goes high when a new conversion result has been loaded in the output register (this is when the conversion has been completed) and remains high until the next read access, as shown in Figure 37.

The polarity of the BUSY/INT signal can be changed using CONFIG bit C26. The mode of pin 35 can be controlled using CONFIG bit C27.

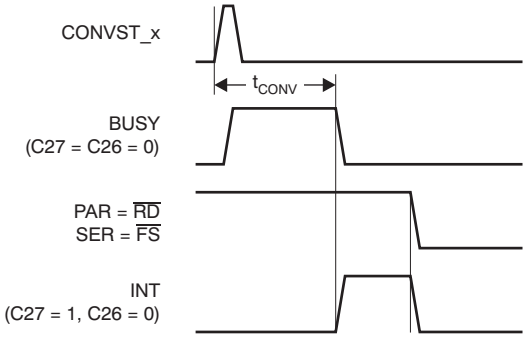

Figure 37. BUSY versus INT Behavior of Pin 35

Reference

The ADS8528/48/68 provides an internal, low-drift, 2.5V reference source. To increase the input voltage range, the reference voltage can be switched to 3V mode using the VREF bit (CONFIG bit C13). The reference feeds a 10-bit string-DAC controlled by bits REFDAC[9:0] in the Configuration (CONFIG) Register. The buffered DAC output is connected to the REFIO pin. In this way, the voltage at this pin is programmable in 2.44mV (2.92mV in 3V mode) steps and adjustable to the applications needs without additional external components. The actual output voltage can be calculated using Equation 3:

$$V_{REF} = \frac{\text{Range} \times (\text{Code} + 1)}{1024} \quad (3)$$

where:

Range = the chosen maximum reference voltage output range (2.5V or 3V),

Code = the decimal value of the DAC register content.

Table 4 lists some examples of internal reference DAC settings with a reference range set to 2.5V. However, to ensure proper performance, the DAC output voltage should not be programmed below 0.5V.

The buffered output of the DAC should be decoupled with a 100nF capacitor (minimum); for best performance, a 470nF capacitor is recommended. If the internal reference is placed into power-down (default), an external reference voltage can drive the REFIO pin.

Table 4. DAC Settings Examples (2.5V Operation)

VREFOUT	DECIMAL CODE	BINARY CODE	HEXADECIMAL CODE
0.5 V	204	00 1100 1100	CCh
1.25 V	511	01 1111 1111	1FFh
2.5 V	1023	11 1111 1111	3FFh

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The voltage at the REFIO pin is buffered with four internal amplifiers, one for each ADC pair. The output of each buffer must be decoupled with a 10µF capacitor between the pin pairs 3 and 6, 43 and 46, 50 and 53, and 60 and 63. The 10µF capacitors are available as ceramic 0805-SMD components and in X5R quality.

The internal reference buffers can be powered down to decrease the power dissipation of the device. In this case, external reference drivers can be connected to the REFAP, REFBP, REFCP, and REFDP pins. With 10µF decoupling capacitors, the minimum required bandwidth can be calculated using Equation 4:

$$f_{3dB} = \frac{\ln(2)}{2\pi t_{CONV}} \quad (4)$$

With the minimum t_{CONV} of 1.33µs, the external reference buffers require a minimum bandwidth of 83kHz.

DIGITAL

This section describes the digital control and the timing of the device in detail.

Device Configuration

Depending on the desired mode of operation, the ADS8528/48/68 can be configured using the external pins and/or the Configuration Register (CONFIG), as shown in Table 5.

Table 5. ADS8528/48/68 Configuration Settings

INTERFACE MODE	HARDWARE MODE ($\overline{HW}$/SW = 0)	SOFTWARE MODE ($\overline{HW}$/SW = 1)
Parallel ($\overline{PAR}$/SER = 0)	Configuration using pins and (optionally) Configuration Register bits C30, C29, C[27:26], C22, C20, C18, C14, C13, and C[9:0]	Configuration using Configuration Register bits C[31:0] only; status of pins 9, 11, 20, and 34 are disregarded (if C29 = C28 = 0)
Serial ($\overline{PAR}$/SER = 1)	Configuration using pins and (optionally) Configuration Register bits C30, C29, C[27:26], C22, C20, C18, C13, and C[9:0]	Configuration using Configuration Register bits C[31:0] only; status of pins 9, 11, 20, and 34 are disregarded (if C29 = C28 = 0)

Hardware Mode

With the $\overline{HW}$/SW input (pin 41) set low, the device functions are controlled via the pins and, optionally, Configuration Register bits C30, C29, C[27:26], C22, C20, C18, C14 (in parallel interface mode only), C13, and C[9:0].

It is possible to generally use the part in hardware mode but to switch it into software mode to initialize or adjust the Configuration Register settings (for example, the internal reference DAC) and back to hardware mode thereafter.

Software Mode

When the $\overline{HW}$/SW input is set high, the device operates in software mode with functionality set only by the Configuration Register bits (corresponding pin settings are ignored).

If parallel interface is used, an update of all Configuration Register settings is performed by issuing two 16-bit write accesses on pins DB[15:0] (to avoid loosing data, the entire sequence must be finished before starting a new conversion). $\overline{CS}$ should be held low during these two accesses. To enable the actual update of the register settings, the first bit (C31) must be set to '1' during the access.

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If the serial interface is used, the update of the register contents can be performed continuously (combined read/write access). Optionally, to reduce the data transfer on the SDI line and the electromagnetic interference (EMI) of the system, the SDI input can be pulled low when a register update is not required. Figure 38 illustrates the different Configuration Register update options.

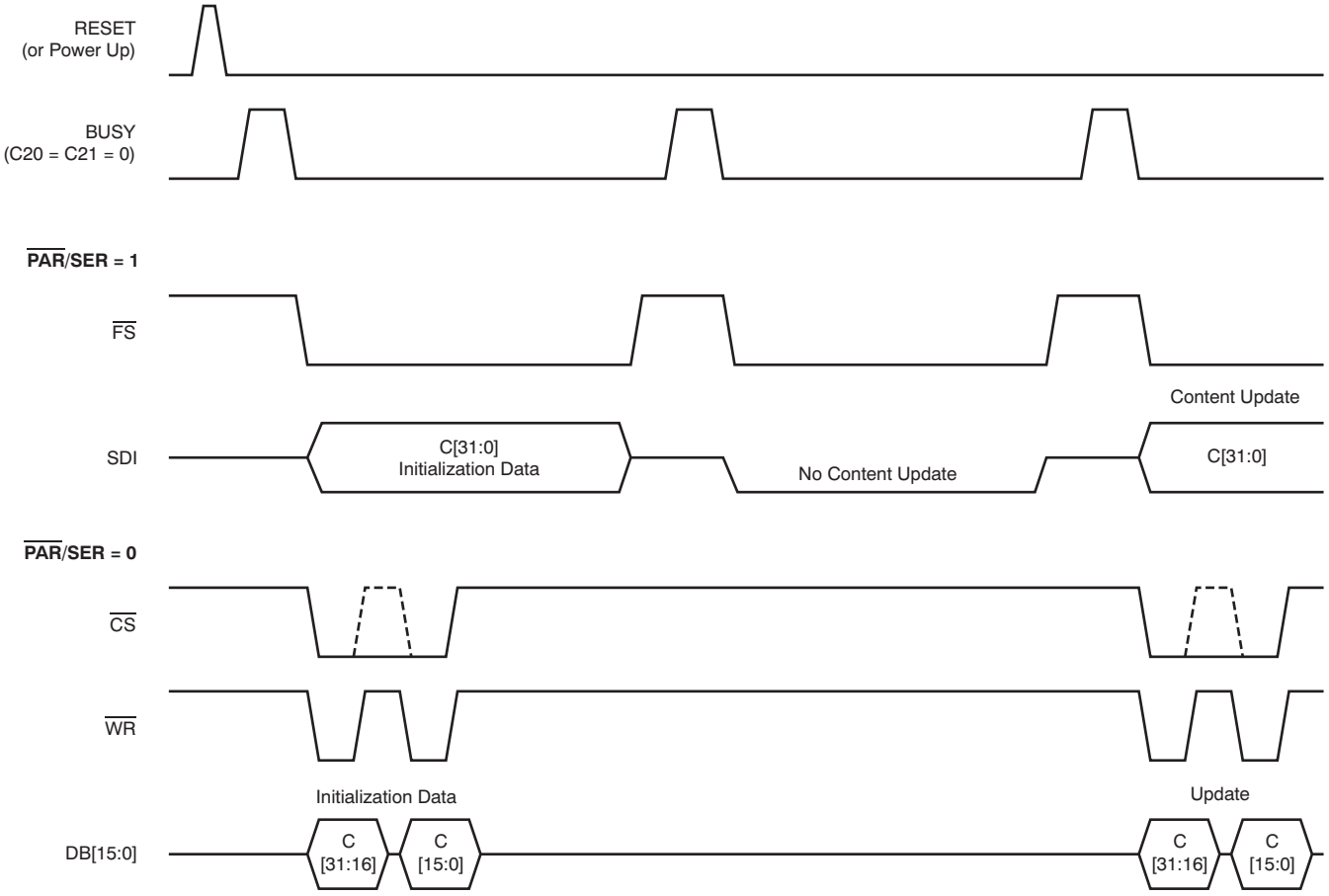

Figure 38. Configuration Register Update Options

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Configuration (CONFIG) Register

The Configuration Register settings can only be changed in software mode and are not affected when switching to hardware mode thereafter. The register values are independent from input pin settings. Changes are active with the second rising edge of $\overline{WR}$ in parallel interface mode or with the 32nd SCLK falling edge of the access in which the register content has been updated in serial mode. The CONFIG content is defined in Table 6.

Table 6. CONFIG: Configuration Register (Default: 000003FFh)

31	30	29	28	27	26	25	24
WRITE_EN	READ_EN	CLKSEL	CLKOUT	BUSY/INT	BUSY POL	STBY	RANGE_A
23	22	21	20	19	18	17	16
RANGE_B	PD_B	RANGE_C	PD_C	RANGE_D	PD_D	Don't care	Don't care
15	14	13	12	11	10	9	8
REFEN	REFBUF	VREF	Don't care	Don't care	Don't care	D9	D8
7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit 31 **WRITE_EN: Register update enable**

This bit is not active in hardware mode.
0 = Register content update disabled (default)
1 = Register content update enabled

Bit 30 **READ_EN: Register read-out access enable**

This bit is not active in hardware mode.
0 = Normal operation (conversion results available on SDO_A)
1 = Configuration Register contents output on SDO_A with next two accesses (READ_EN automatically resets to '0' thereafter)

Bit 29 **CLKSEL: Conversion clock selector**

This bit is active in hardware mode.
0 = Normal operation with internal conversion clock; mandatory in hardware mode (default)
1 = External conversion clock applied through pin 34 (XCLK) is used (conversion takes 19 clock cycles)

Bit 28 **CLKOUT: Internal conversion clock output enable**

This bit is not active in hardware mode.
0 = Normal operation (default)
1 = Internal conversion clock is available at pin 34

Bit 27 **BUSY/INT: Busy/interrupt selector**

This bit is active in hardware mode.
0 = BUSY/INT pin in BUSY mode (default)
1 = BUSY/INT pin in interrupt mode (INT); can only be used if all eight channels are sampled simultaneously (all CONVST_x tied together)

Bit 26 **BUSY POL: BUSY/INT polarity selector**

This bit is active in hardware mode.
0 = BUSY/INT active high (default)
1 = BUSY/INT active low

Bit 25 **$\overline{STBY}$: Power-down enable**

This bit is not active in hardware mode.
0 = Normal operation (default)
1 = Entire device is powered down (including the internal clock and reference)

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Bit 24	**RANGE_A: Input voltage range selector for channel pair A** This bit is not active in hardware mode. 0 = Input voltage range: 4VREF (default) 1 = Input voltage range: 2VREF
Bit 23	**RANGE_B: Input voltage range selector for channel pair B** This bit is not active in hardware mode. 0 = Input voltage range: 4VREF (default) 1 = Input voltage range: 2VREF
Bit 22	**PD_B: Power-down enable for channel pair B** This bit is active in hardware mode. 0 = Normal operation (default) 1 = Channel pair B is powered down
Bit 21	**RANGE_C: Input voltage range selector for channel pair C** This bit is not active in hardware mode. 0 = Input voltage range: 4VREF (default) 1 = Input voltage range: 2VREF
Bit 20	**PD_C: Power-down enable for channel pair C** This bit is active in hardware mode. 0 = Normal operation (default) 1 = Channel pair C is powered down
Bit 19	**RANGE_D: Input voltage range selector for channel pair D** This bit is not active in hardware mode. 0 = Input voltage range: 4VREF (default) 1 = Input voltage range: 2VREF
Bit 18	**PD_D: Power-down enable for channel pair D** This bit is active in hardware mode. 0 = Normal operation (default) 1 = Channel pair D is powered down
Bits[17:16]	**Not used (default = 0)**
Bit 15	**REF_EN: Internal reference enable** This bit is not active in hardware mode. 0 = Internal reference source disabled (default) 1 = Internal reference source enabled
Bit 14	**REFBUF: Internal reference buffers disable** This bit is active in hardware mode if the parallel interface is used. 0 = Internal reference buffers enabled (default) 1 = Internal reference buffers disabled
Bit 13	**VREF: Internal reference voltage selector** This bit is active in hardware mode. 0 = Internal reference voltage set to 2.5V (default) 1 = Internal reference voltage set to 3.0V
Bits[12:10]	**Not used (default = 0)**
Bits[9:0]	**D[9:0]: REFDAC setting bits** These bits are active in hardware mode. These bits correspond to the settings of the internal reference DACs (compare to the *Reference* section). Bit D9 is the MSB of the DAC. Default value is 3FFh (2.5V, nom).

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Parallel Interface

To use the device with the parallel interface, the $\overline{\text{PAR}}$/SER pin should be held low. The maximum achievable data throughput rate is 650kSPS for the ADS8528, 600kSPS for the ADS8548, and 510kSPS for the ADS8568 in this case.

Access to the ADS8528/48/68 is controlled as illustrated in Figure 2 and Figure 3.

Serial Interface

The serial interface mode is selected by setting the $\overline{\text{PAR}}$/SER pin high. In this case, each data transfer starts with the falling edge of the frame synchronization input ($\overline{\text{FS}}$). The conversion results are presented on the serial data output pins SDO_A (always active), SDO_B, SDO_C, and SDO_D, depending on the selections made using the SEL_xx pins. Starting with the most significant bit (MSB), the output data are changed with the falling edge of SCLK. Output data of the ADS8528 and ADS8548 maintain the LSB-aligned 16-bit format with leading bits containing the extended sign (see also Table 7). Serial data input SDI are latched with the falling edge of SCLK.

The serial interface can be used with one, two, or four output ports. Port SDO_B can be enabled using pin 27 (SEL_B) while ports SDO_C and SDO_D are enabled using pin 28 (SEL_CD). If all four serial data output ports are selected, the data can be read with either two 16-bit data transfers or with a single 32-bit data transfer. The data of channels CH_x0 are available first, followed by data from channels CH_x1. The maximum achievable data throughput rate is 480kSPS for the ADS8528, 450kSPS for the ADS8548, and 400kSPS for the ADS8568 in this case.

If the application allows a data transfer using two ports only, the SDO_A and SDO_B outputs are used. The device outputs data from channel CH_A0 followed by CH_A1, CH_C0, and CH_C1 on SDO_A, while data from channel CH_B0 followed by CH_B1, CH_D0, and CH_D1 occur on SDO_B. In this case, a data transfer of four 16-bit words, two 32-bit words, or one continuous 64-bit word is supported. The maximum achievable data throughput rate is 360kSPS for the ADS8528, 345kSPS for the ADS8548, and 315kSPS for the ADS8568 in this case.

The output SDO_A is always active and exclusively used if only one serial data port is used in the application. The data are available in the following order: CH_A0, CH_A1, CH_B0, CH_B1, CH_C0, CH_C1, CH_D0, and CH_D1. Data can be read using eight 16-bit transfers, four 32-bit transfers, two 64-bit transfers, or a single 128-bit transfer. The maximum achievable data throughput rate is 235kSPS for the ADS8528, 230kSPS for the ADS8548 and 215kSPS for the ADS8568 in this case. Figure 1 and Figure 39 show all possible scenarios in more detail.

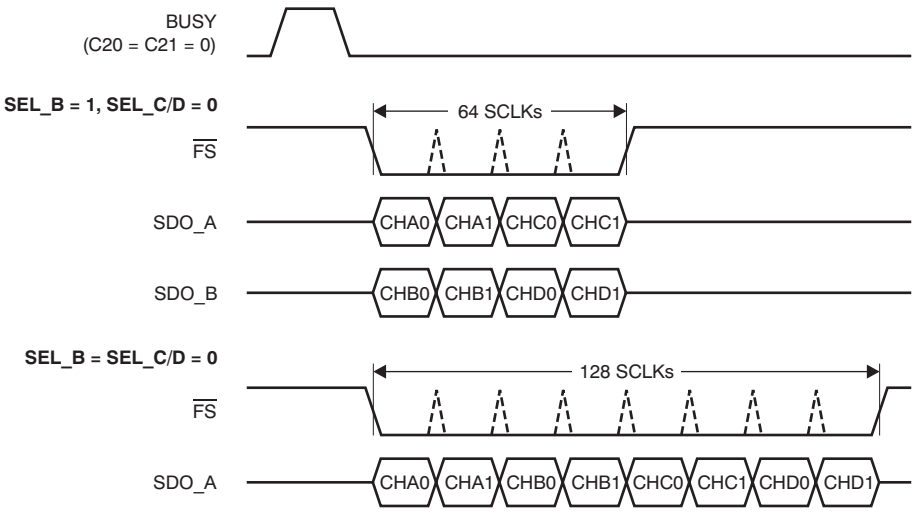

Figure 39. Data Output with One or Two Active SDOs (All Input Channels Active and Converted)

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Daisy-Chain Mode

The serial interface of the ADS8528/48/68 supports a daisy-chain feature that allows cascading of multiple devices to minimize the board space requirements and simplify routing of the data and control lines. In this case, pins DB3/DCIN_A, DB2/DCIN_B, DB1/DCIN_C, and DB0/DCIN_D are used as serial data inputs for channels A, B, C, and D, respectively. Figure 40 shows an example of a daisy-chain connection of three devices sharing a common CONVST line to allow simultaneous sampling of 24 analog channels along with the corresponding timing diagram.

To activate the daisy-chain mode, the DCEN pin must be pulled high. However, the DCEN of the first device in the chain must remain low.

In applications in which not all channel pairs are used, it is recommended to declare the part with disabled channel pair(s) to be the first in the daisy-chain.

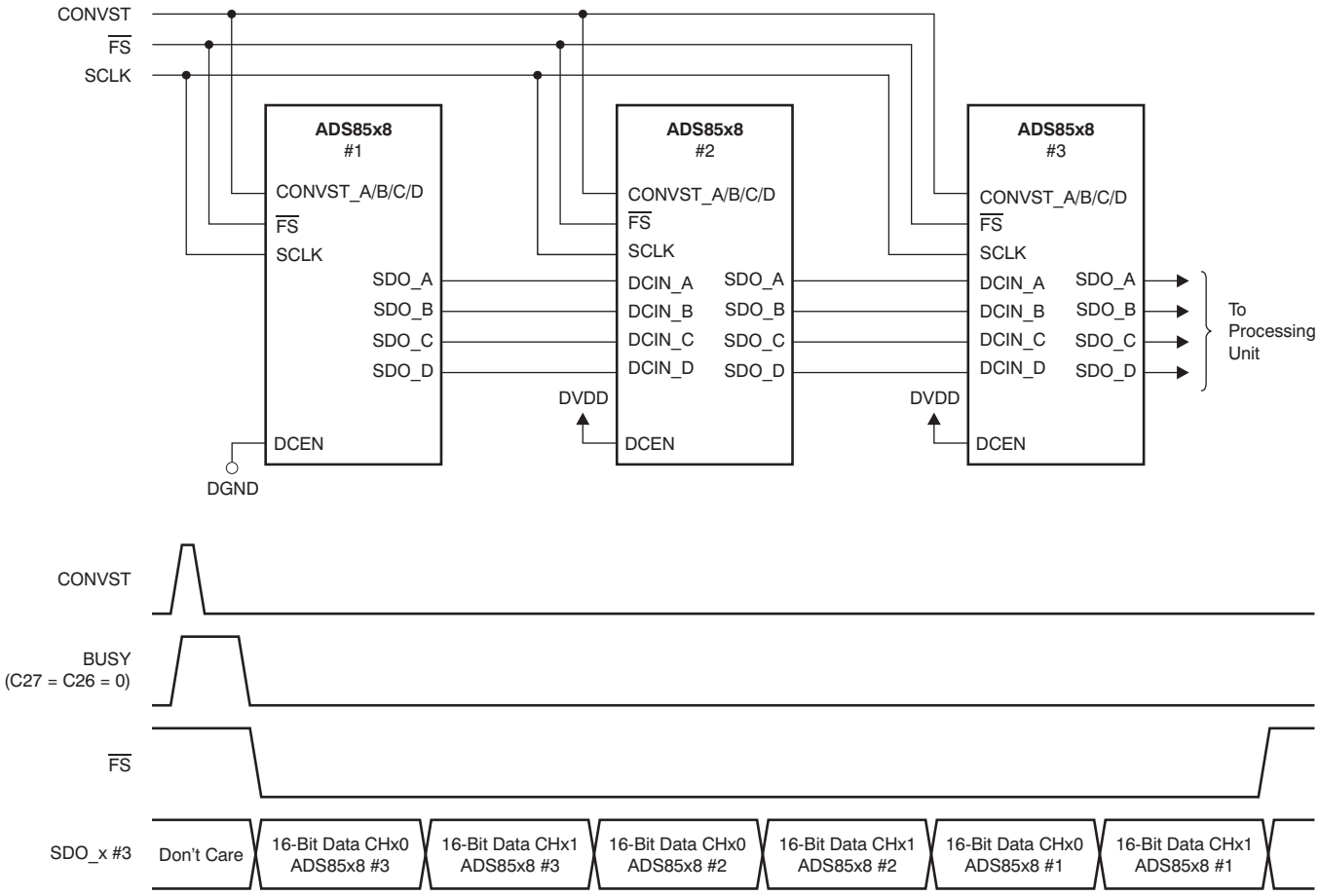

Figure 40. Example of Daisy-Chaining Three Devices

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Output Data Format

The data output format of the ADS8528/48/68 is binary twos complement, as shown in Table 7. For the ADS8528/48 (which deliver 12-bit or 14-bit conversion results, respectively), the leading bits of either the 16-bit frame (serial interface) or the output pins (DB[15:12] for the ADS8528 or DB[15:14] for the ADS8548 in parallel mode) deliver a sign extension.

Table 7. Output Data Format

DESCRIPTION	INPUT VOLTAGE VALUE	BINARY CODE HEXADECIMAL CODE		
		ADS8528	ADSS8548	ADS8568
Positive full-scale	+4VREF or +2VREF	0000 0111 1111 1111 07FFh	0001 1111 1111 1111 1FFFh	0111 1111 1111 1111 7FFFh
Midscale +0.5LSB	VREF/(2 × resolution)	0000 0000 0000 0000 0000h	0000 0000 0000 0000 0000h	0000 0000 0000 0000 0000h
Midscale –0.5LSB	–VREF/(2 × resolution)	1111 1111 1111 1111 FFFFh	1111 1111 1111 1111 FFFFh	1111 1111 1111 1111 FFFFh
Negative full-scale	–4VREF or –2VREF	1111 1000 0000 0000 F800h	1110 0000 0000 0000 E000h	1000 0000 0000 0000 8000h

Reset and Power-Down Modes

The device supports two reset mechanisms: a power-on reset (POR) and a pin-controlled reset (RESET) that can be issued using pin 10. Both, the POR and RESET act as a master reset that causes any ongoing conversion to be interrupted, the Configuration Register content to be set to the default value, and all channels to be switched into the sample mode.

When the device is powered up, the POR sets the device in default mode when AVDD reaches 1.2V. In normal operation, glitches on the AVDD supply below this threshold trigger a device reset.

The entire device, except for the digital interface, can be powered down by pulling the $\overline{\text{STBY}}$ pin low (pin 9). As the digital interface section remains active, data can be retrieved while in stand-by mode. To power the part on again, the $\overline{\text{STBY}}$ pin must be brought high. The device is ready to start a new conversion after the 10ms required to activate and settle the internal circuitry. This user-controlled approach can be used in applications that require lower data throughput rates at lowest power dissipation. The content of CONFIG is not changed during stand-by mode and it is not required to perform a reset after returning to normal operation.

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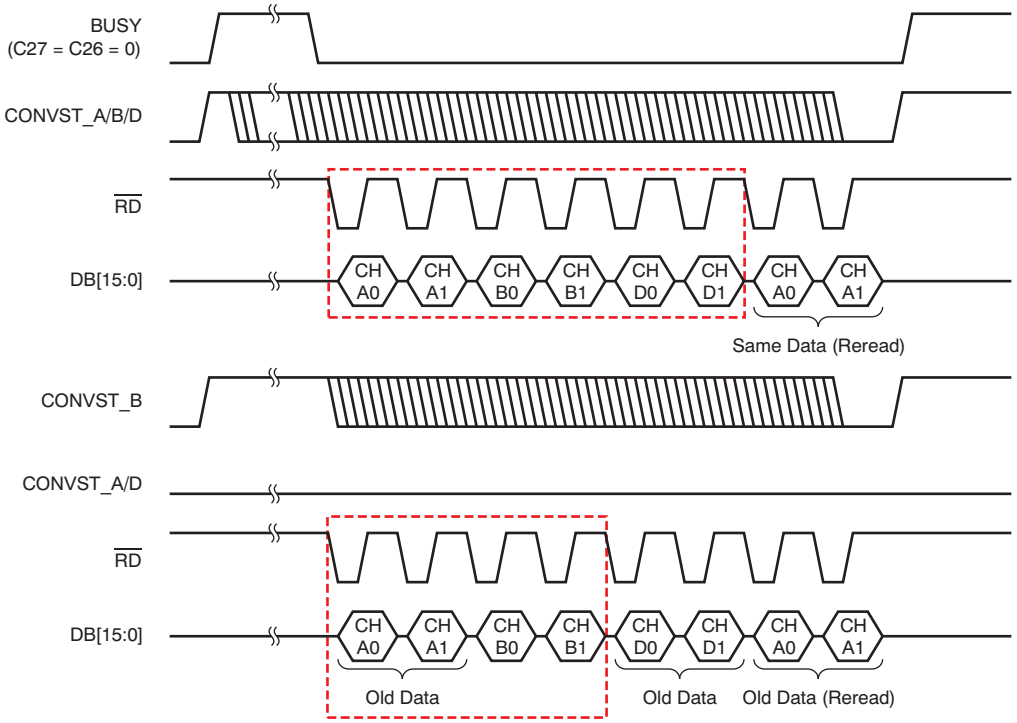
While the standby mode impacts the entire device, each device channel pair (except channel pair A, which as the master channel pair, is always active) can also be individually switched off by setting the Configuration Register bits C22, C20, and C18 (PD_x). If a certain channel pair is powered-down in this manner, the output register is disabled as shown in Figure 41. When reactivated, the relevant channel pair requires 10ms to fully settle before starting a new conversion.



(1) Channel pair C disabled (PD_C = 1), $\overline{CS}$ = 0.

NOTE: Boxed areas indicate the minimum required frame to acquire all new conversion results. The read access might be interrupted, thereafter.

Figure 41. Example of Data Output Order with Channel Pair C Powered Down(1)

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The auto-sleep mode is enabled by pulling pin 36 (ASLEEP) high. If the auto-sleep mode is enabled, the ADS8528/48/68 automatically reduce the current requirement to 7mA (IAVDD) after finishing a conversion; thus, the end of conversion actually activates this power-down mode. Triggering a new conversion by applying a positive CONVST_x edge puts the device back into normal operation, starts the acquisition of the analog input, and automatically starts a new conversion 6 to 7 conversion clock cycles later, as shown in Figure 42. Therefore, a complete conversion process takes 25 to 26 conversion clock cycles; thus, the maximum throughput rate in auto-sleep mode is reduced to a maximum of 400kSPS for the ADS8528, 375kSPS for the ADS8548, and 330kSPS for the ADS8568 in serial interface mode. In parallel mode, the maximum data rates are 510kSPS for the ADS8528, 470kSPS for the ADS8548 and 400kSPS for the ADS8568. If enabled, the internal reference remains active during auto-sleep mode. Table 8 compares the analog current requirements of the device in different modes.

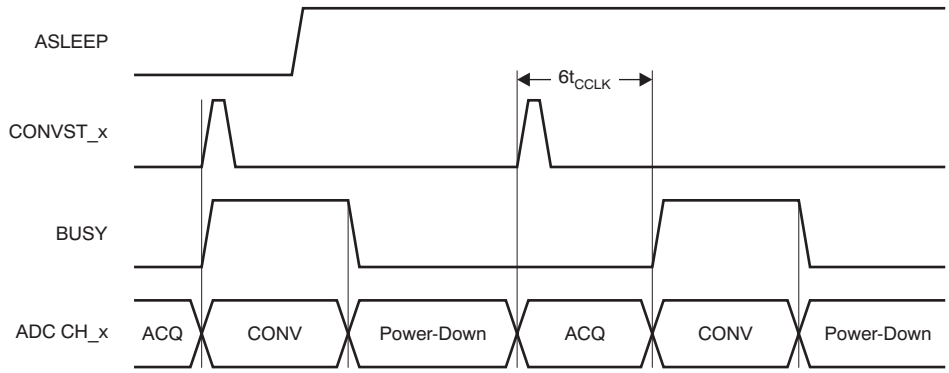

Figure 42. Auto-Sleep Power-Down Mode

Table 8. Maximum Analog Current (IAVDD) Demand of the ADS85x8

OPERATIONAL MODE	ANALOG CURRENT (IAVDD)	ENABLED/DISABLED BY	ACTIVATED BY	NORMAL OPERATION TO POWER-DOWN DELAY	RESUMED BY	POWER-UP TO NORMAL OPERATION DELAY	POWER-UP TO NEXT CONVERSION START TIME
Normal operation	12.5mA/ch pair at maximum data rate	Power on Power off	CONVST_x	—	—	—	—
Auto-sleep	1.75mA/ch pair	ASLEEP = 1 ASLEEP = 0	Each end of conversion	At falling edge of BUSY	CONVST_x	Immediate	7 × t_{CCLK} max
Power-down of channel pair X	16µA (channel pair X)	$\overline{HW}$/SW = 1 $\overline{HW}$/SW = 0	PD_x = 1 (CONFIG bit)	Immediate	PD_x = 0 (CONFIG bit)	Immediate after completing CONFIG update	10ms
Power-down (entire device)	30µA	Power on Power off	$\overline{STBY}$ = 0	Immediate	$\overline{STBY}$ = 1	Immediate	10ms

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APPLICATION INFORMATION

TYPICAL APPLICATION EXAMPLE

An example of a typical application of the ADS8528/48/68 is illustrated in Figure 43. In this case, the device is used to simultaneously sample and convert the voltages and currents on three phases and the neutral line. In this example, the BUSY signal is not used by the controller while the SW generates the required signals in timely manner. TI's OPA2211 is used as an input driver, supporting bandwidth that allows running the device at the maximum data rate. However, because relatively low data rates are generally used in this type of applications, the auto-sleep mode is activated in this example (ASLEEP is high) to minimize the current demand on the AVDD and HVDD/HVSS power supplies. Further, the input drivers may not be necessary if the signal source fulfills the requirements as defined by Equation 2. For example, at 10kSPS, the external drivers are not necessary if the source impedance remains below 830kΩ in ±4VREF mode or 415kΩ in ±2VREF mode.

While the actual values of the resistors and capacitors depend on the bandwidth and performance requirements of the application, for a data rate of 10kSPS, it is recommended to use a filter capacitor C_F value of 1nF and a series resistor R_F of 10kΩ.

In applications supporting only single supply (for example, 5V), it is recommended to use the TPS65130 to generate the bipolar supplies required by the ADC.

GROUNDING

All ground pins should be connected to a clean ground reference. This connection should be kept as short as possible to minimize the inductance of these paths. It is recommended to use vias connecting the pads directly to the corresponding ground plane. In designs without ground planes, the ground trace should be kept as wide and as short as possible to reduce inductance. Avoid connections that are too close to the grounding point of a microcontroller or digital signal processor.

Depending on the circuit density on the board, placement of the analog and digital components, and the related current loops, a single solid ground plane for the entire printed circuit board (PCB) or dedicated analog and digital ground areas may be used. In case of separated ground areas, ensure a low-impedance connection between the analog and digital ground of the ADC by placing a bridge underneath (or next to) the ADC. Otherwise, even short undershoots on the digital interface with a value of lower than –300mV lead to the conduction of ESD diodes, causing current to flow through the substrate and either degrading the analog performance or even damaging the part. It is recommended to use a common ground plane underneath the device as a local ground reference for all xGND pins; see Figure 44. During PCB layout, care should be taken to avoid any return currents crossing sensitive analog areas or signals.

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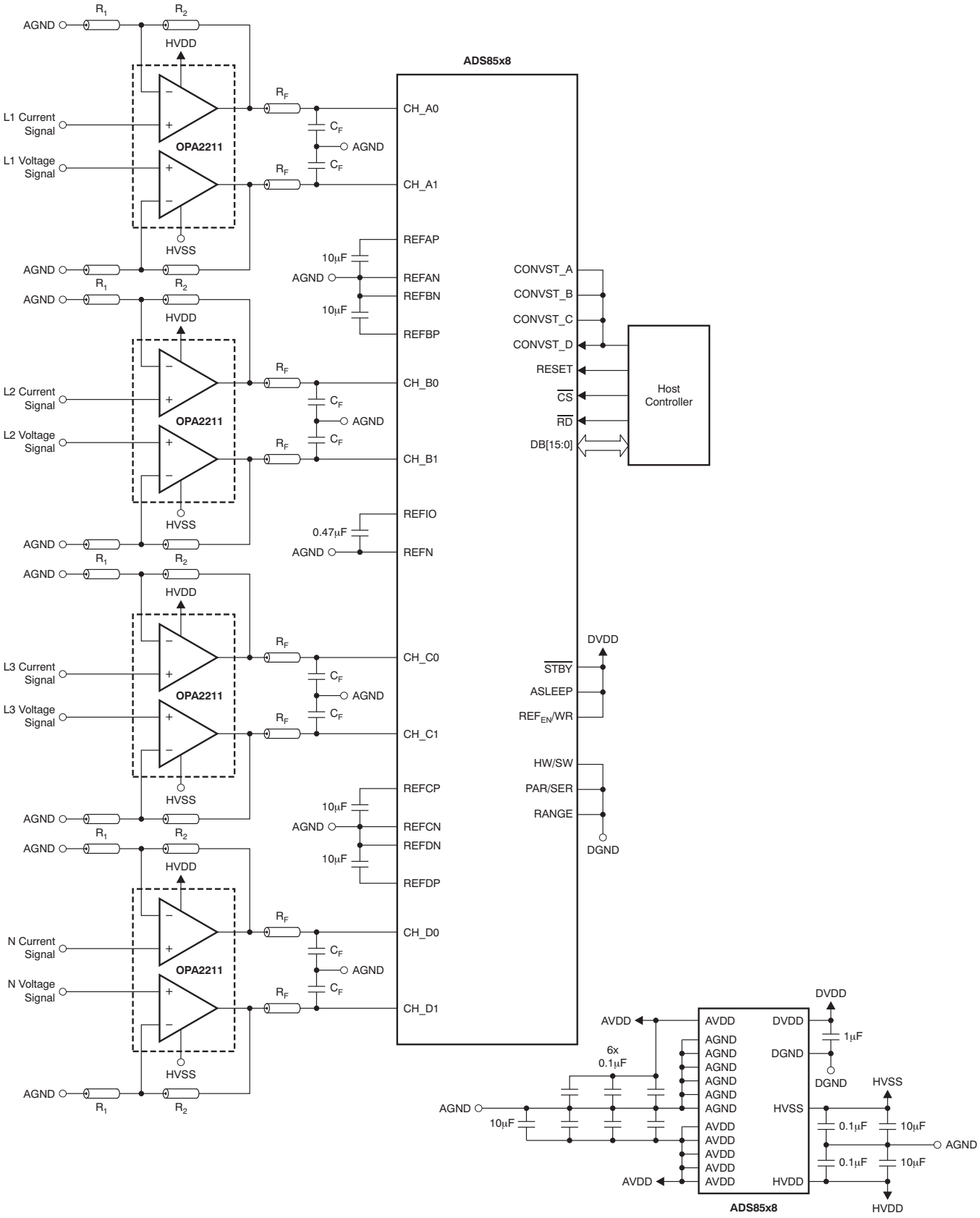

Figure 43. Three-Phase + N Current/Voltage Measurement Application Based on the ADS85x8

POWER SUPPLY

The ADS8528/48/68 require four separate supplies: an analog supply for the ADC (AVDD), the buffer I/O supply for the digital interface (DVDD), and the high-voltage supplies driving the analog input circuitry (HVDD and HVSS). Generally, there are no specific requirements with regard to the power sequencing of the device. However, when HVDD is supplied before AVDD, the internal electrostatic discharge (ESD) structure conducts, increasing the IHVDD beyond the specified value, until the AVDD is applied.

The AVDD supply provides power to the internal circuitry of the ADC. If run at maximum data rate, the IAVDD is too high to allow use of a passive filter between the digital board supply of the application and the AVDD pins. A linear regulator is recommended to generate the analog supply voltage. Each AVDD pin should be decoupled to AGND with a 100nF ceramic capacitor. In addition, a single 10µF capacitor should be placed close to the device but without compromising the placement of the smaller capacitors. Optionally, each supply pin can be decoupled using a 1µF ceramic capacitor without the requirement for the additional 10µF capacitor.

The DVDD supply is only used to drive the digital I/O buffers and allows seamless interface with most state-of-the-art processors and controllers. As a result of the low IDVDD value, a 10Ω series resistor can be used on the DVDD pin to reduce the noise energy from the external digital circuitry influencing the performance of the device. A bypass ceramic capacitor of 1µF (or alternatively, a pair of 100nF and 10µF capacitors) should be placed between pins 24 and 25.

The high-voltage supplies (HVSS and HVDD) are connected to the analog inputs. These supplies are not required to be of symmetrical nature with regard to AGND. Noise and glitches on these supplies directly couple into the input signals. Place a 100nF ceramic decoupling capacitor, located as close to the device as possible, between each of pins 1, 48, and AGND. An additional 10µF capacitor is used that should be placed close to the device but without compromising the placement of the smaller capacitors.

Figure 44 shows a layout recommendation for the ADS8528/48/68 along with the proper decoupling and reference capacitors placement and connections. The layout recommendation takes into account the actual size of the components used.

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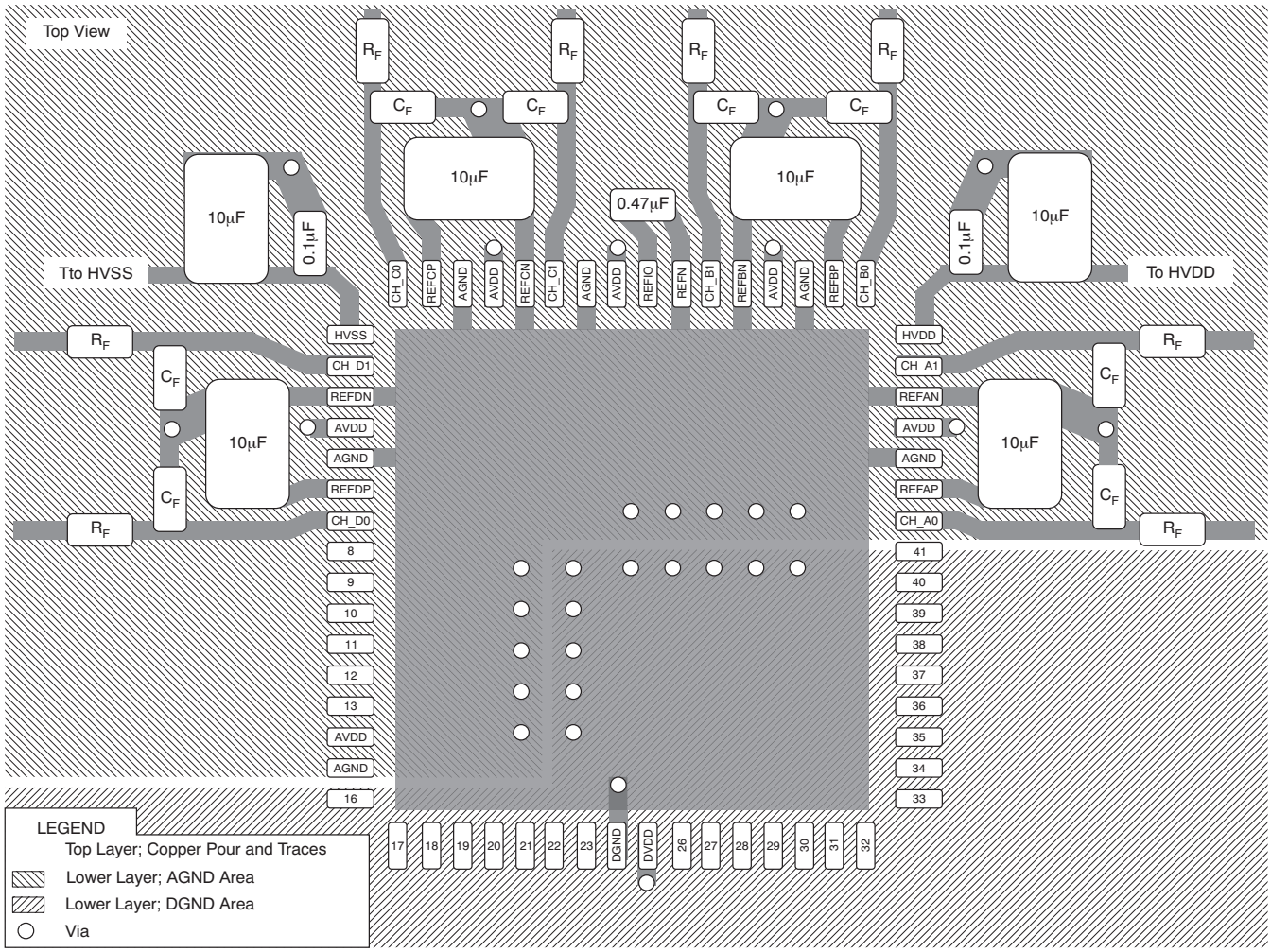

(1) All AVDD/DVDD decoupling capacitors are placed on the bottom layer underneath the device power-supply pins and are connected by vias. All 100nF ceramic capacitors are placed as close as possible to the device while the 10µF capacitors are also close but without compromising the placement of the smaller capacitors.

Figure 44. Layout Recommendation

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2011) to Revision A	Page
• Deleted INL column from Family/Ordering Information table	2
• Changed DC Accuracy, *INL* parameter in ADS8568 Electical Chatacteristics table	5

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
ADS8528SPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8528SPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8528SRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8528SRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8548SPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8548SPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8548SRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8548SRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8568SPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8568SPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8568SRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS8568SRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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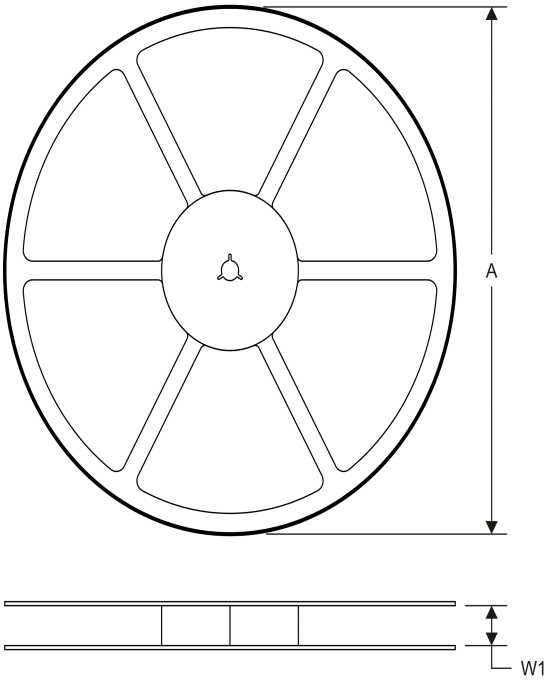
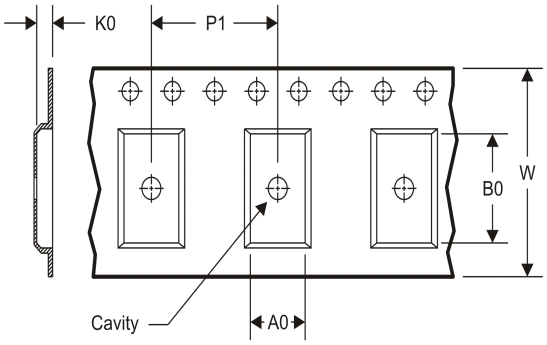
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



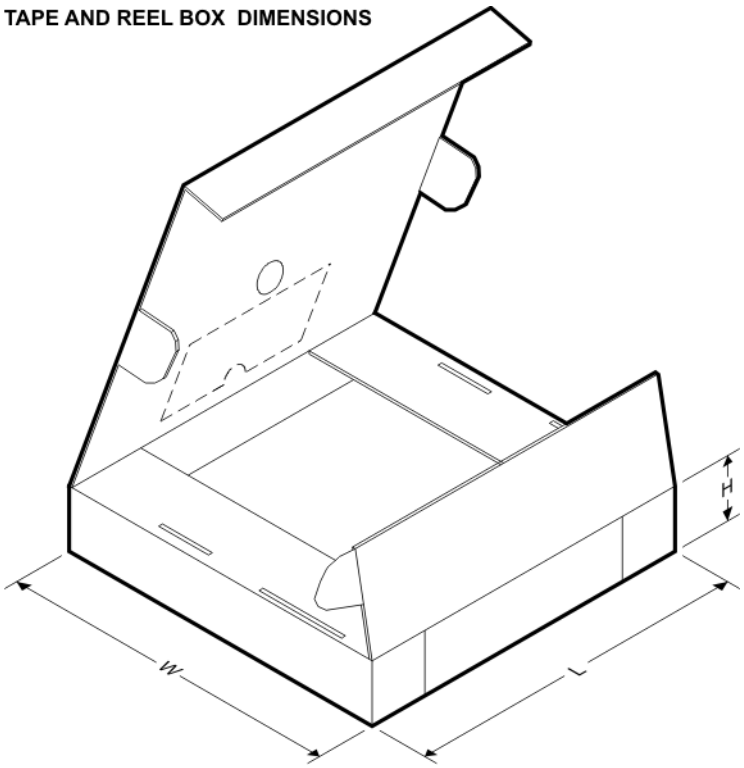
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8528SPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
ADS8528SRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8528SRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8548SPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
ADS8548SRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8548SRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8568SPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
ADS8568SRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS8568SRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

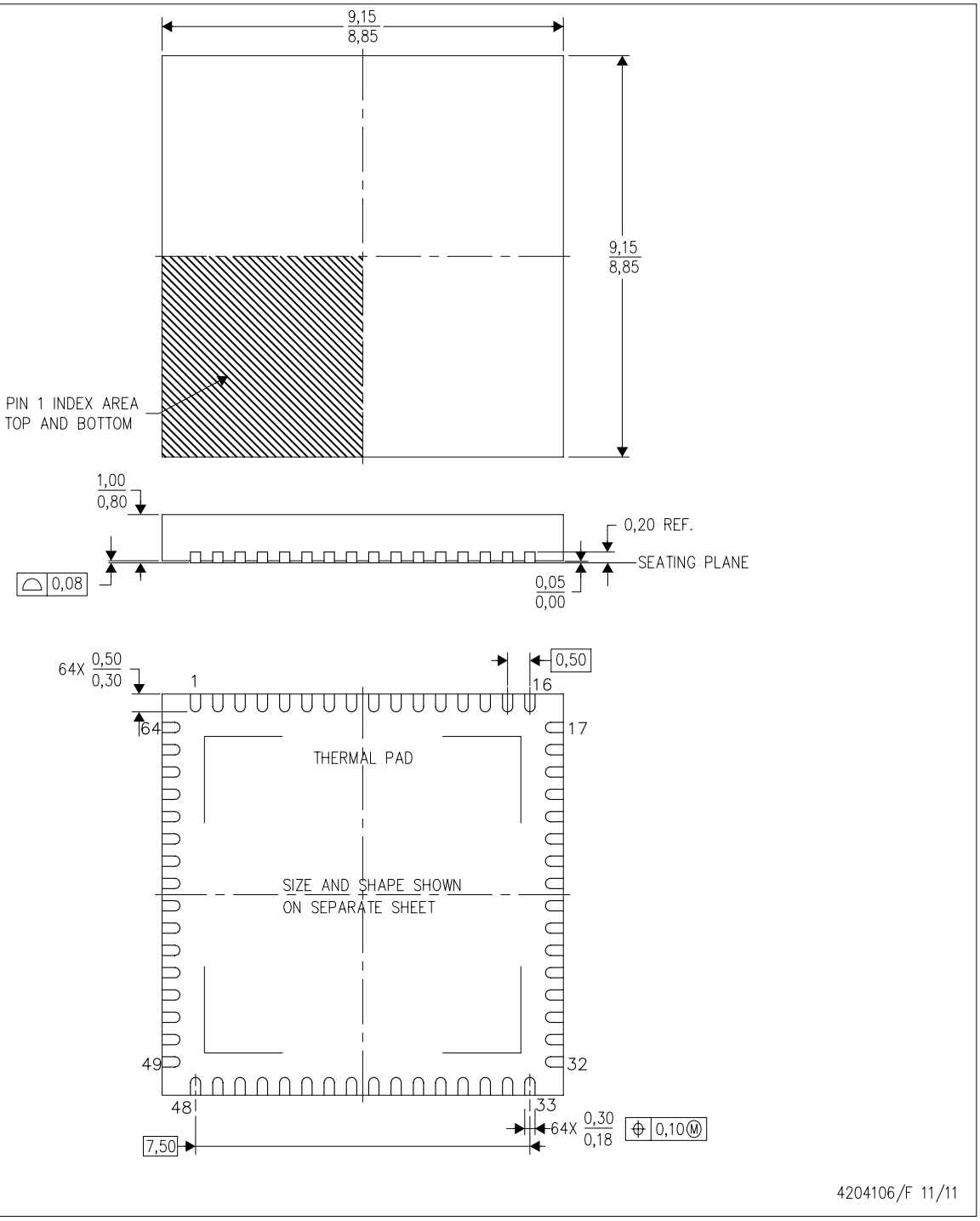
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8528SPMR	LQFP	PM	64	1000	367.0	367.0	45.0
ADS8528SRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
ADS8528SRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
ADS8548SPMR	LQFP	PM	64	1000	367.0	367.0	45.0
ADS8548SRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
ADS8548SRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
ADS8568SPMR	LQFP	PM	64	1000	367.0	367.0	45.0
ADS8568SRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
ADS8568SRGCT	VQFN	RGC	64	250	210.0	185.0	35.0

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

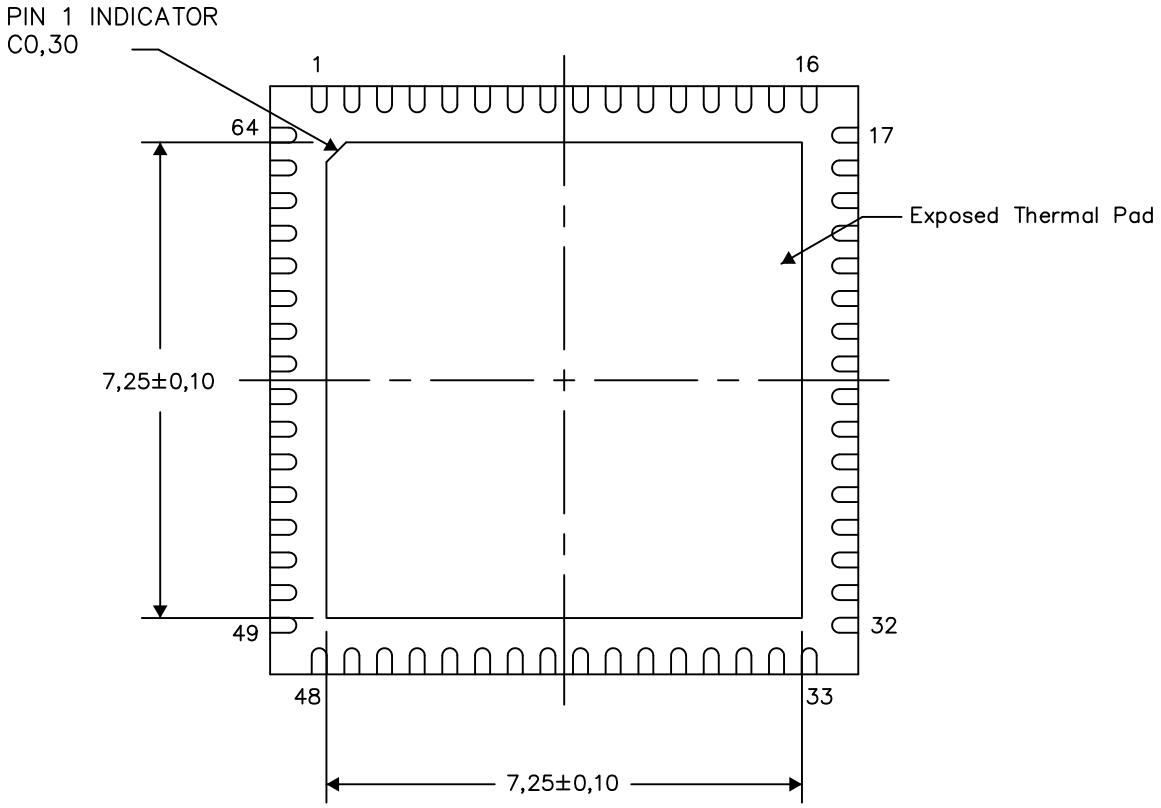
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



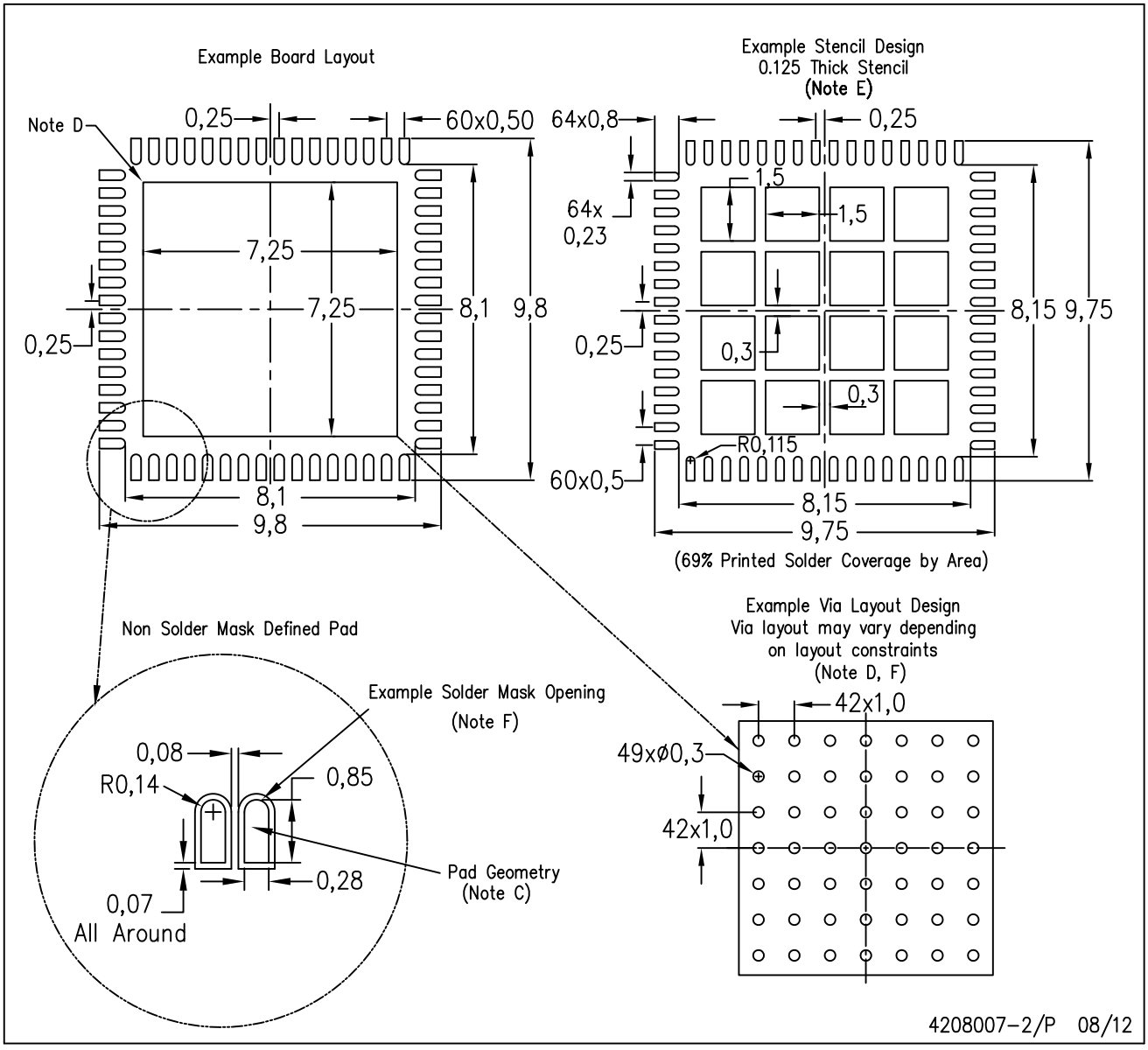
Bottom View

Exposed Thermal Pad Dimensions

4206192–2/T 08/12

NOTE: A. All linear dimensions are in millimeters

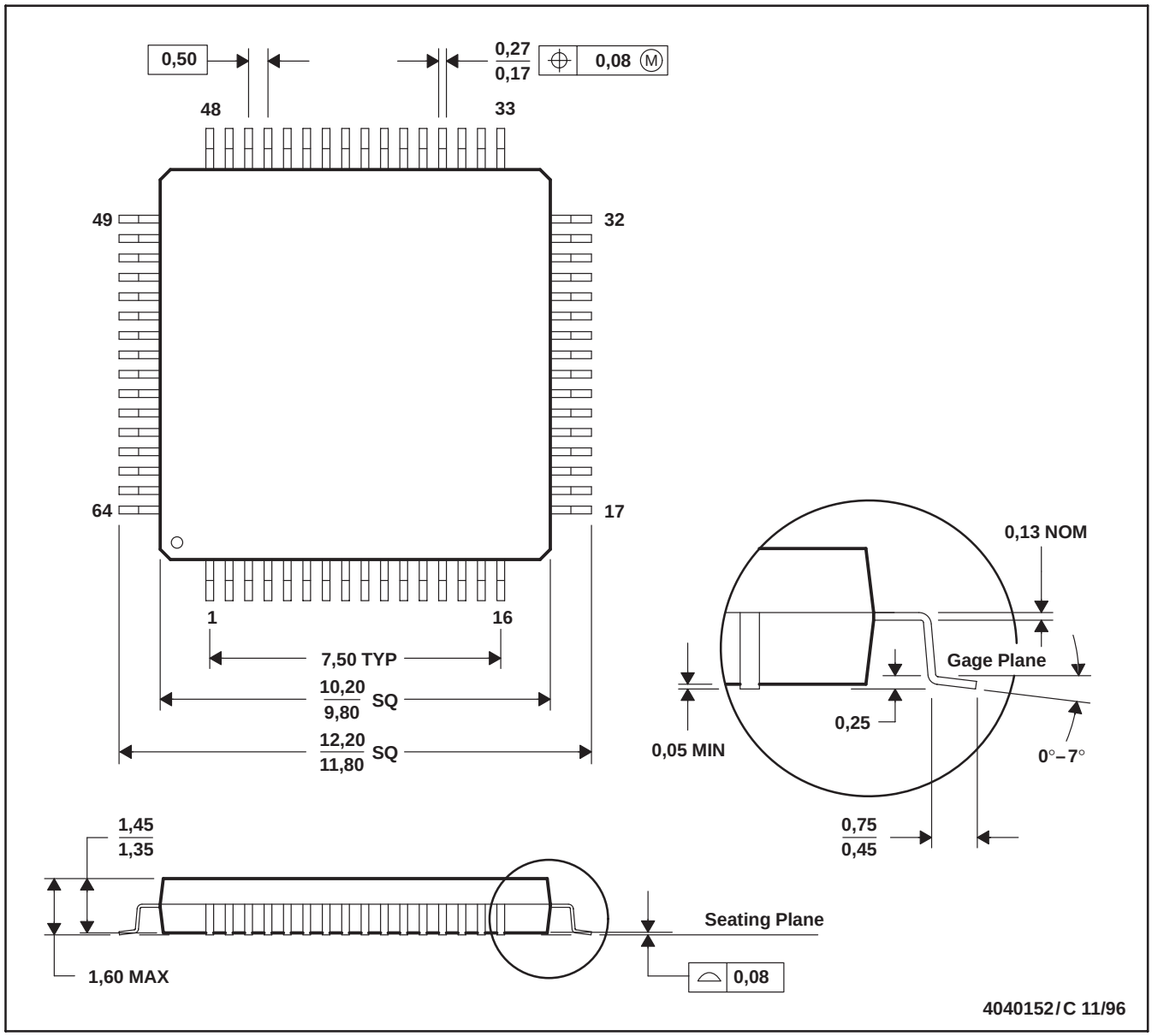
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

MTQF008A – JANUARY 1995 – REVISED DECEMBER 1996

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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