AH5010,AH5011,AH5012

AH5010/AH5011/AH5012 Monolithic Analog Current Switches

![Texas Instruments logo]

N *ational* *Semiconductor*

AH5010/AH5011/AH5012 Monolithic Analog Current Switches

General Description

A versatile family of monolithic JFET analog switches economically fulfills a wide variety of multiplexing and analog switching applications.

Even numbered switches may be driven directly from standard 5V logic, whereas the odd numbered switches are intended for applications utilizing 10V or 15V logic. The monolithic construction guarantees tight resistance match and track.

For voltage switching applications see LF13331, LF13332, and LF13333 Analog Switch Family, or the CMOS Analog Switch Family.

Applications

- A/D and D/A converters
- Micropower converters
- Industrial controllers
- Position controllers
- Data acquisition

- Active filters
- Signal multiplexers/demultiplexers
- Multiple channel AGC
- Quad compressors/expanders
- Choppers/demodulators
- Programmable gain amplifiers
- High impedance voltage buffer
- Sample and hold

Features

Interfaces with standard TTL and CMOS	
"ON" resistance match	2Ω
Low "ON" resistance	100Ω
Very low leakage	50 pA
Large analog signal range	$\pm 10V$ peak
High switching speed	150 ns
Excellent isolation between channels	80 dB at 1 kHz

Connection and Schematic Diagrams (All switches shown are for logical "1" input)
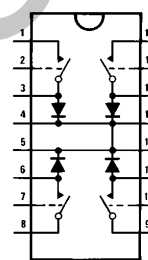
Dual-In-Line Package

TOP VIEW

LOGIC DRIVE	4 CHANNEL MUX	4 SPST SWITCHES
5V LOGIC	AH5010C	AH5012C
15V LOGIC		AH5011C
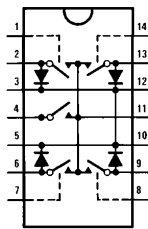
AH5010C MUX Switches
(4-Channel Version Shown)
Order Number AH5010CN
See NS Package Number M14A or N14A

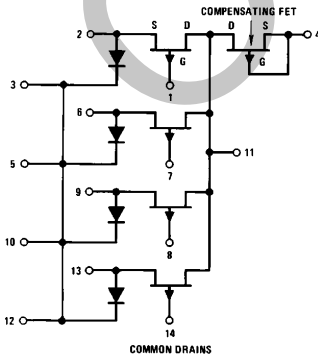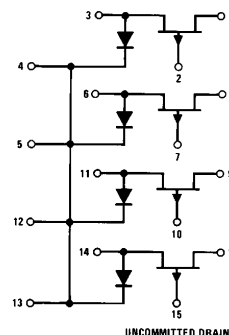**Dual-In-Line Package**

TOP VIEW

AH5011C and AH5012C SPST Switches
(Quad Version Shown)
Order Number AH5011CN,
AH5012CM or AH5012CN
See NS Package Number M16A or N16A

COMPENSATING FET

COMMON DRAINS

UNCOMMITTED DRAINS   TL/H/5659–1

Note: All diode cathodes are internally connected to the substrate.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	
AH5010/AH5011/AH5012	30V
Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10 mA

Drain Current	30 mA
Soldering Information:	
N Package 10 sec	300°C
SO Package Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
Power Dissipation	500 mW
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics AH5010 and AH5012 (Notes 2 and 3)

Symbol	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	$4.5V \leq V_{GD} \leq 11V$, $V_{SD} = 0.7V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V$, $V_{GS} = 3.8V$ $T_A = 85°C$	0.02	0.2 10	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 1$ mA $T_A = 85°C$	0.08	1 200	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 2$ mA $T_A = 85°C$	0.13	5 10	nA μA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = -2$ mA $T_A = 85°C$	0.1	10 20	nA μA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 0.35V$, $I_S = 2$ mA $T_A = +85°C$	90	150 240	Ω Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} = 0V$, $I_D = 1$ mA	4	20	Ω
T_{ON}	Turn "ON" Time	See AC Test Circuit	150	500	ns
T_{OFF}	Turn "OFF" Time	See AC Test Circuit	300	500	ns
CT	Cross Talk	See AC Test Circuit	120		dB

Electrical Characteristics AH5011 (Notes 2 and 3)

Symbol	Parameter	Conditions	Typ	Max	Units
I_{GSX}	Input Current "OFF"	$11V \leq V_{GD} \leq 15V$, $V_{SD} = 0.7V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{D(OFF)}$	Leakage Current "OFF"	$V_{SD} = 0.7V$, $V_{GS} = 10.3V$ $T_A = 85°C$	0.01	0.2 10	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 1$ mA $T_A = 85°C$	0.04	0.5 100	nA nA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = 2$ mA $T_A = 85°C$		2 1	nA μA
$I_{G(ON)}$	Leakage Current "ON"	$V_{GD} = 0V$, $I_S = -2$ mA $T_A = 85°C$		5 2	nA μA
$r_{DS(ON)}$	Drain-Source Resistance	$V_{GS} = 1.5V$, $I_S = 2$ mA $T_A = 85°C$	60	100 160	Ω Ω
V_{DIODE}	Forward Diode Drop	$I_D = 0.5$ mA		0.8	V
$r_{DS(ON)}$	Match	$V_{GS} = 0V$, $I_D = 1$ mA	2	10	Ω
T_{ON}	Turn "ON" Time	See AC Test Circuit	150	50	ns
T_{OFF}	Turn "OFF" Time	See AC Test Circuit	300	500	ns
CT	Cross Talk	See AC Test Circuit. f = 100 Hz.	120		dB

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

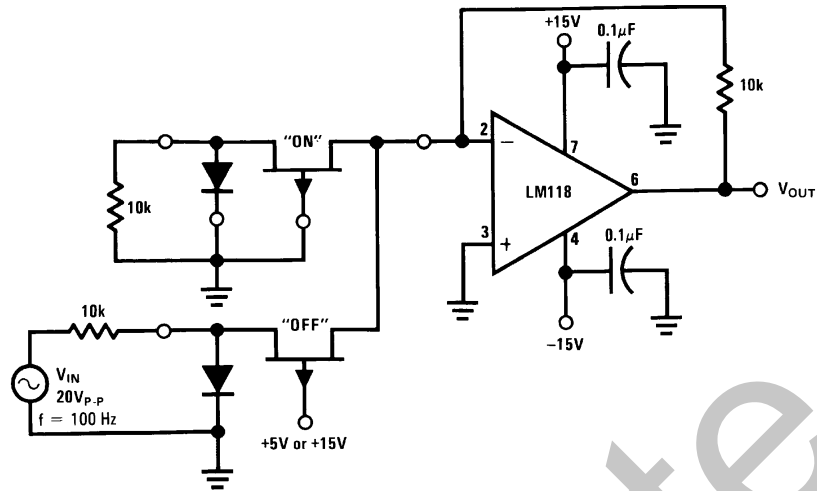**Note 2:** Test conditions 25°C unless otherwise noted.

Note 3: "OFF" and "ON" notation refers to the conduction state of the FET switch.
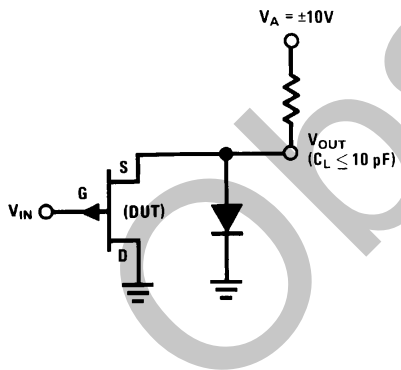
Note 4: Thermal Resistance:

	θ_{JA}
N14A, N16A	92°C/W
M14A, M16A	115°C/W

Test Circuits and Switching Time Waveforms

Cross Talk Test Circuit

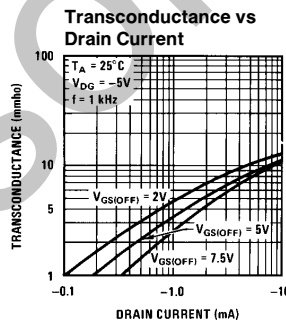**Time Waveforms**

AC Test Circuit

3
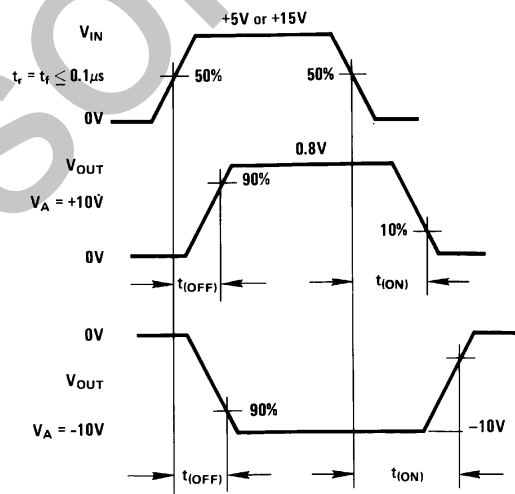
Typical Performance Characteristics

Parameter Interaction

Leakage Current, $I_{D(OFF)}$ vs Temperature

"ON" Resistance, $r_{DS(ON)}$ vs Temperature

Cross Talk, CT vs Frequency

Leakage Current vs Drain-Gate Voltage

Transconductance vs Drain Current

Drain Current vs Bias Voltage

Normalized Drain Resistance vs Bias Voltage

TL/H/5659–3

4
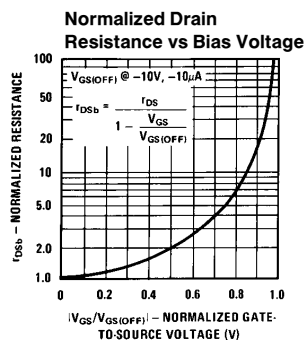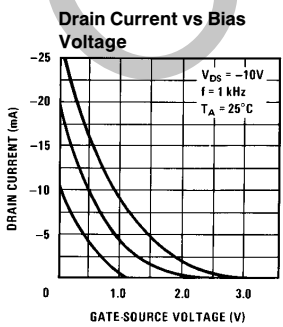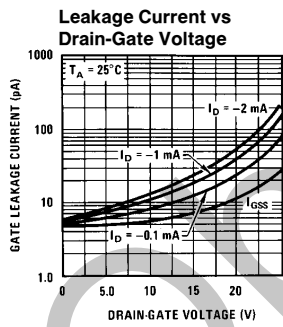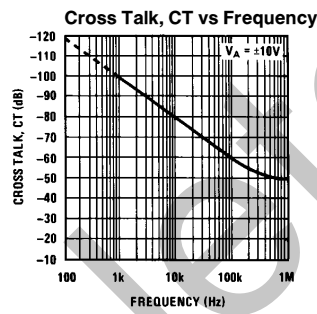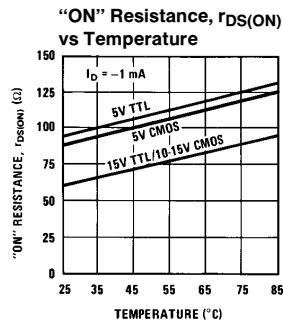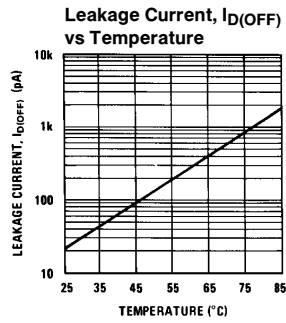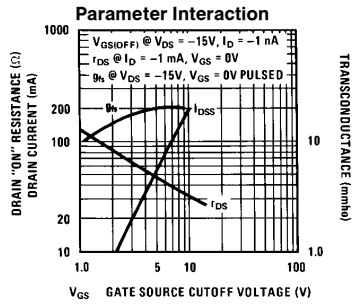
Applications Information

Theory of Operation

The AH series of analog switches are primarily intended for operation in current mode switch applications; i.e., the drains of the FET switch are held at or near ground by operating into the summing junction of an operational amplifier. Limiting the drain voltage to under a few hundred millivolts eliminates the need for a special gate driver, allowing the switches to be driven directly by standard TTL, 5V-10V CMOS, open collector 15V TTL/CMOS.

Two basic switch configurations are available: 4 independent switches (SPST) and 4 pole switches used for multiplexing (4 PST-MUX). The MUX versions such as the AH5010 offer common drains and include a series FET operated at $V_{GS} = 0V$. The additional FET is placed in the feedback path in order to compensate for the "ON" resistance of the switch FET as shown in *Figure 1*.

The closed-loop gain of *Figure 1* is:

$$A_{VCL} = \frac{R2 + r_{DS(ON)Q2}}{R1 + r_{DS(ON)Q1}}$$

For R1 = R2, gain accuracy is determined by the $r_{DS(ON)}$ match between Q1 and Q2. Typical match between Q1 and Q2 is 4 ohms resulting in a gain accuracy of 0.05% (for R1 = R2 = 10 kΩ).

Noise Immunity

The switches with the source diodes grounded exhibit improved noise immunity for positive analog signals in the "OFF" state. With $V_{IN} = 15V$ and the $V_A = 10V$, the source of Q1 is clamped to about 0.7V by the diode ($V_{GS} = 14.3V$) ensuring that ac signals imposed on the 10V input will not gate the FET "ON."

Selection of Gain Setting Resistors

Since the AH series of analog switches are operated in current mode, it is generally advisable to make the signal current as large as possible. However, current through the FET switch tends to forward bias the source to gate junction and the signal shunting diode resulting in leakage through these junctions. As shown in *Figure 2*, $I_{G(ON)}$ represents a finite error in the current reaching the summing junction of the op amp.

Secondly, the $r_{DS(ON)}$ of the FET begins to "round" as I_S approaches I_{DSS}. A practical rule of thumb is to maintain I_S at less than $\frac{1}{10}$ of I_{DSS}.

Combining the criteria from the above discussion yields:

$$R1_{min} \geq \frac{V_{A(MAX)} A_D}{I_{G(ON)}} \tag{2a}$$

or:

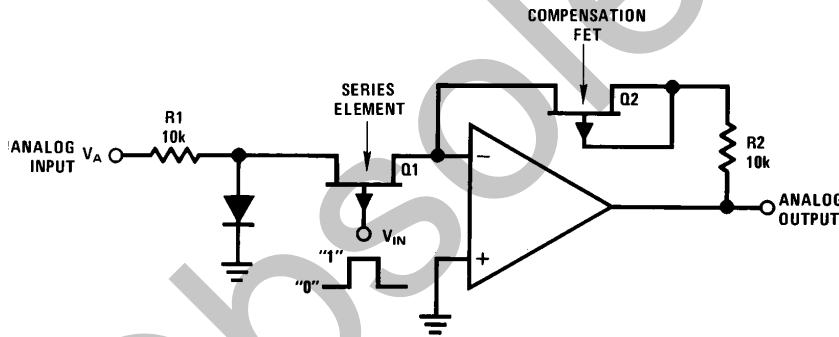$$\geq \frac{V_{A(MAX)}}{I_{DSS}/10} \tag{2b}$$
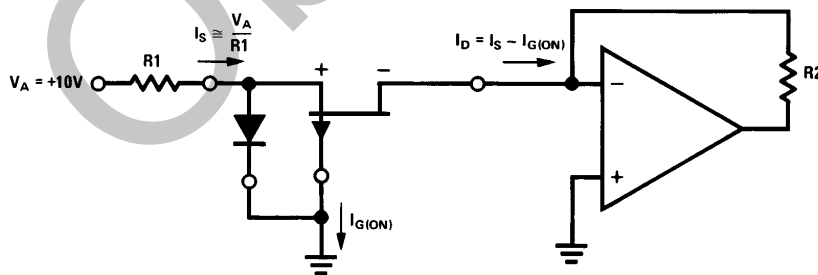
whichever is larger.

FIGURE 1. Use of Compensation FET

TL/H/5659–4

FIGURE 2. On Leakage Current, $I_{G(ON)}$

5

Applications Information (Continued)

Where: $V_{A(MAX)}$ = Peak amplitude of the analog input signal

A_D = Desired accuracy

$I_{G(ON)}$ = Leakage at a given I_S

I_{DSS} = Saturation current of the FET switch

$\cong$ 20 mA

In a typical application, V_A might = ±10V, A_D = 0.1%, 0°C ≤ T_A ≤ 85°C. The criterion of equation (2b) predicts:

$$R1_{(MIN)} \geq \frac{(10V)}{\left(\dfrac{20\ mA}{10}\right)} = 5\ k\Omega$$

For R1 = 5k, $I_S \cong$ 10V/5k or 2 mA. The electrical characteristics guarantee an $I_{G(ON)} \leq 1\mu A$ at 85°C for the AH5010. Per the criterion of equation (2a):

$$R1_{(MIN)} \geq \frac{(10V)(10^{-3})}{1 \times 10^{-6}} \geq 10\ k\Omega$$

Since equation (2a) predicts a higher value, the 10k resistor should be used.

The "OFF" condition of the FET also affects gain accuracy. As shown in *Figure 3*, the leakage across Q2, $I_{D(OFF)}$ represents a finite error in the current arriving at the summing junction of the op amp.

Accordingly:

$$R1_{(MAX)} \leq \frac{V_{A(MIN)}\ A_D}{(N)\ I_{D(OFF)}}$$

Where: $V_{A(MIN)}$ = Minimum value of the analog input signal

A_D = Desired accuracy

N = Number of channels

$I_{D(OFF)}$ = "OFF" leakage of a given FET switch

As an example, if N = 10, A_D = 0.1%, and $I_{D(OFF)} \leq$ 10 nA at 85°C for the AH5010. $R1_{(MAX)}$ is:

$$R1_{(MAX)} \leq \frac{(1V)(10^{-3})}{(10)(10 \times 10^{-9})} = 10k$$

Selection of R2, of course, depends on the gain desired and for unity gain R1 = R2.

Lastly, the foregoing discussion has ignored resistor tolerances, input bias current and offset voltage of the op amp—all of which should be considered in setting the overall gain accuracy of the circuit.

TTL Compatibility

The AH series can be driven with two different logic voltage swings: the even numbered part types are specified to be driven from standard 5V TTL logic and the odd numbered types from 15V open collector TTL.
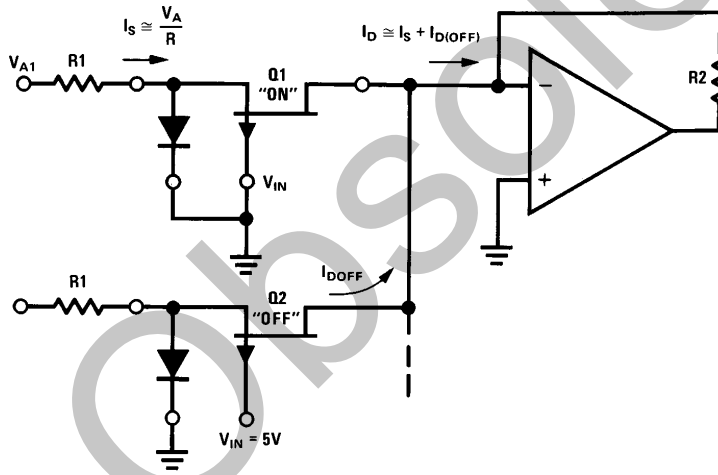

FIGURE 3

TL/H/5659–5

Applications Information (Continued)

Standard TTL gates pull-up to about 3.5V (no load). In order to ensure turn-off of the even numbered switches such as AH5010, a pull-up resistor, R_{EXT}, of at least 10 kΩ should be placed between the 5V V_{CC} and the gate output as shown in *Figure 4*.

Likewise, the open-collector, high voltage TTL outputs should use a pull-up resistor as shown in *Figure 5*. In

both cases, $t_{(OFF)}$ is improved for lower values of R_{EXT} at the expense of power dissipation in the low state.

Definition of Terms

The terms referred to in the electrical characteristics tables are as defined in *Figure 6*.
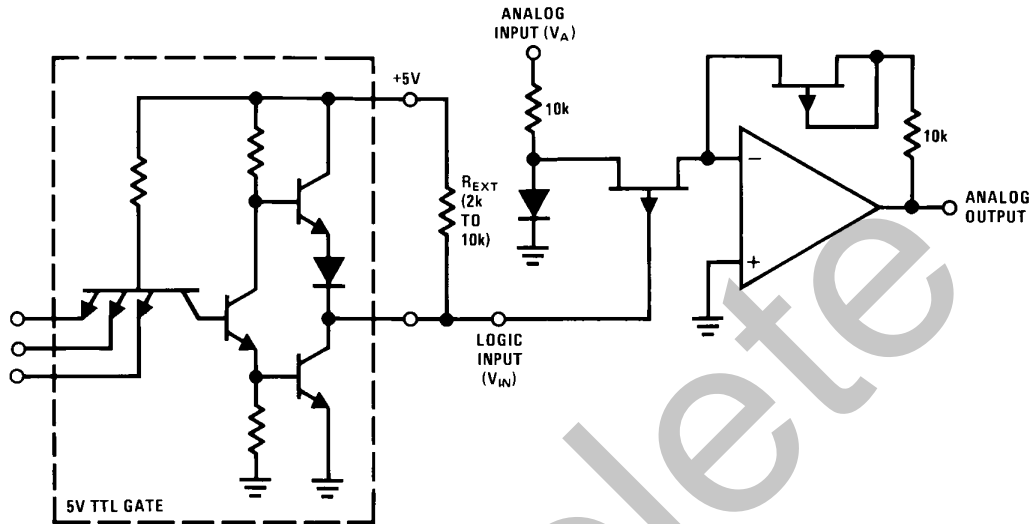

FIGURE 4. Interfacing with +5V TTL
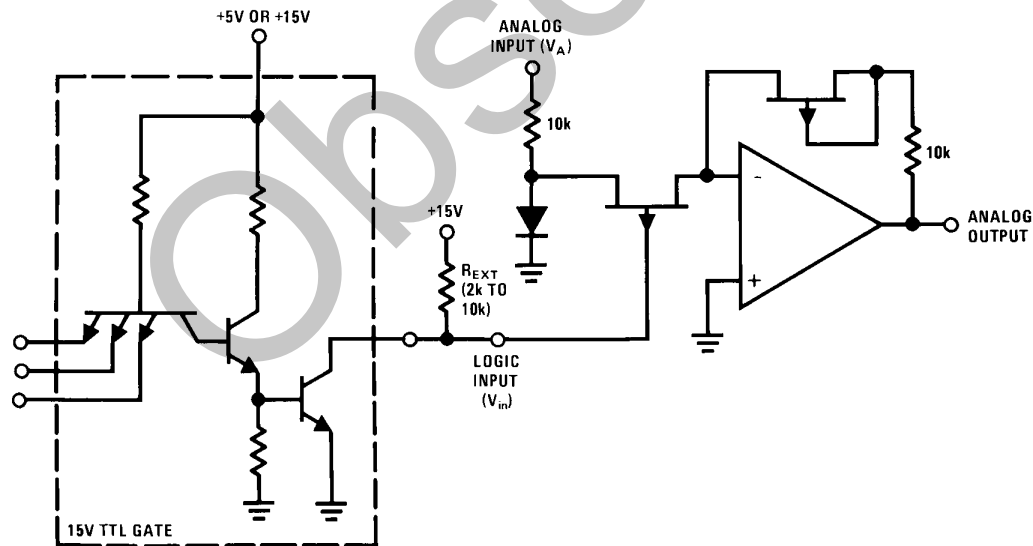

FIGURE 5. Interfacing with +15V Open Collector TTL

TL/H/5659–6

Applications Information (Continued)
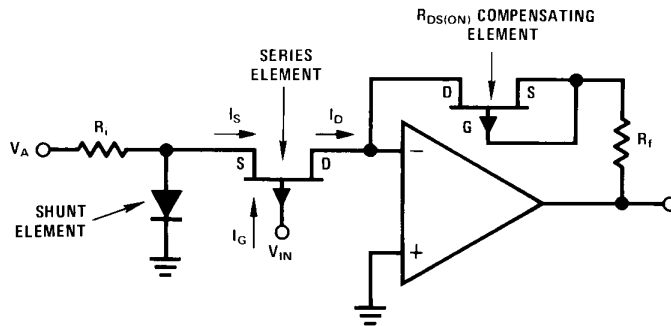
FIGURE 6. Definition of Terms

Typical Applications

De-Glitched Switch for Noiseless Audio Switching

TL/H/5659–7

8
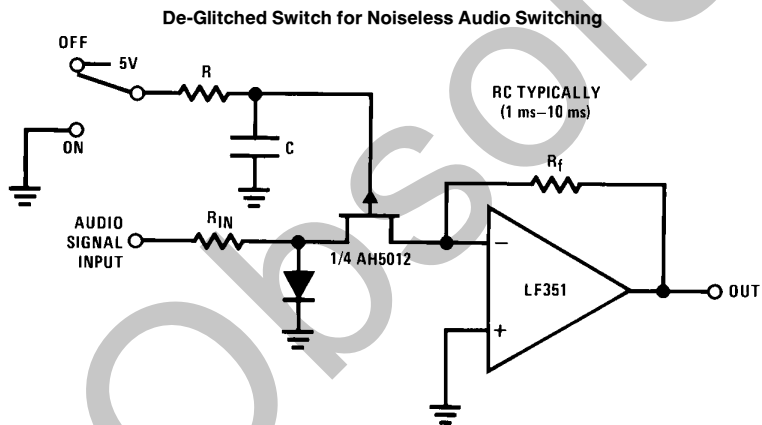
Typical Applications (Continued)

3-Channel Multiplexer with Sample and Hold
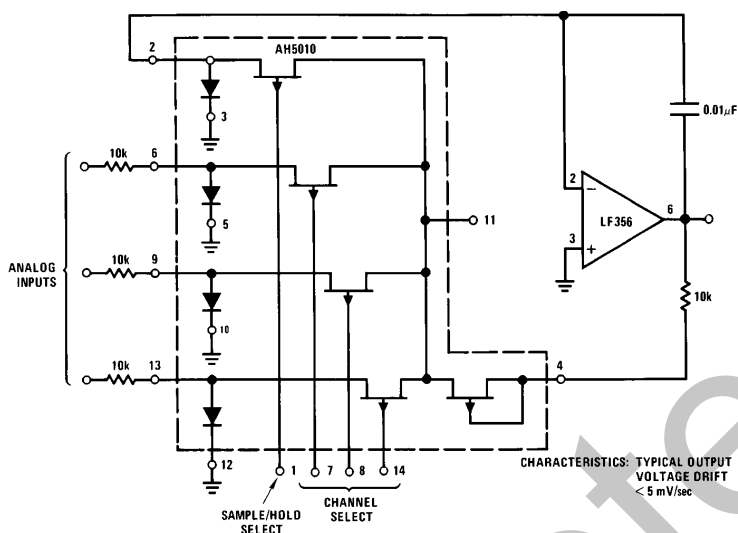
TL/H/5659–8

8-Bit Binary (BCD) Multiplying D/A Converter*

*Recommended resistor array connection for D/A application

TL/H/5659–12

2 Beckman resistor arrays

Part #698-1-R 100k B recommended

$$R_f \left(\overline{G1}\, I_1 + \overline{G2}\, I_2 + \overline{G3}\, I_3 + \overline{G4}\, I_4 + \frac{\overline{G5}\, I_5}{16} + \frac{\overline{G6}\, I_6}{16} + \frac{\overline{G7}\, I_7}{16} + \frac{\overline{G8}\, I_8}{16} \right.$$

Note: The switch is "ON" when G is at 0V (Logic "0")

$$I = \frac{V_R}{R}$$

TL/H/5659–11

9
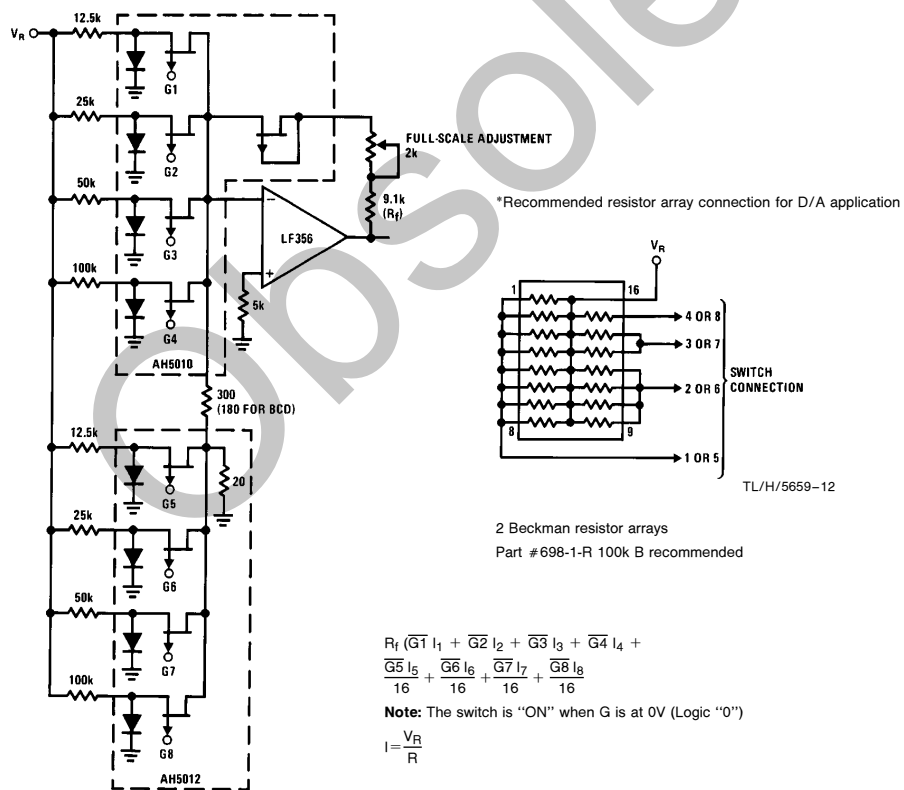
Typical Applications (Continued)

16-Channel Multiplexer
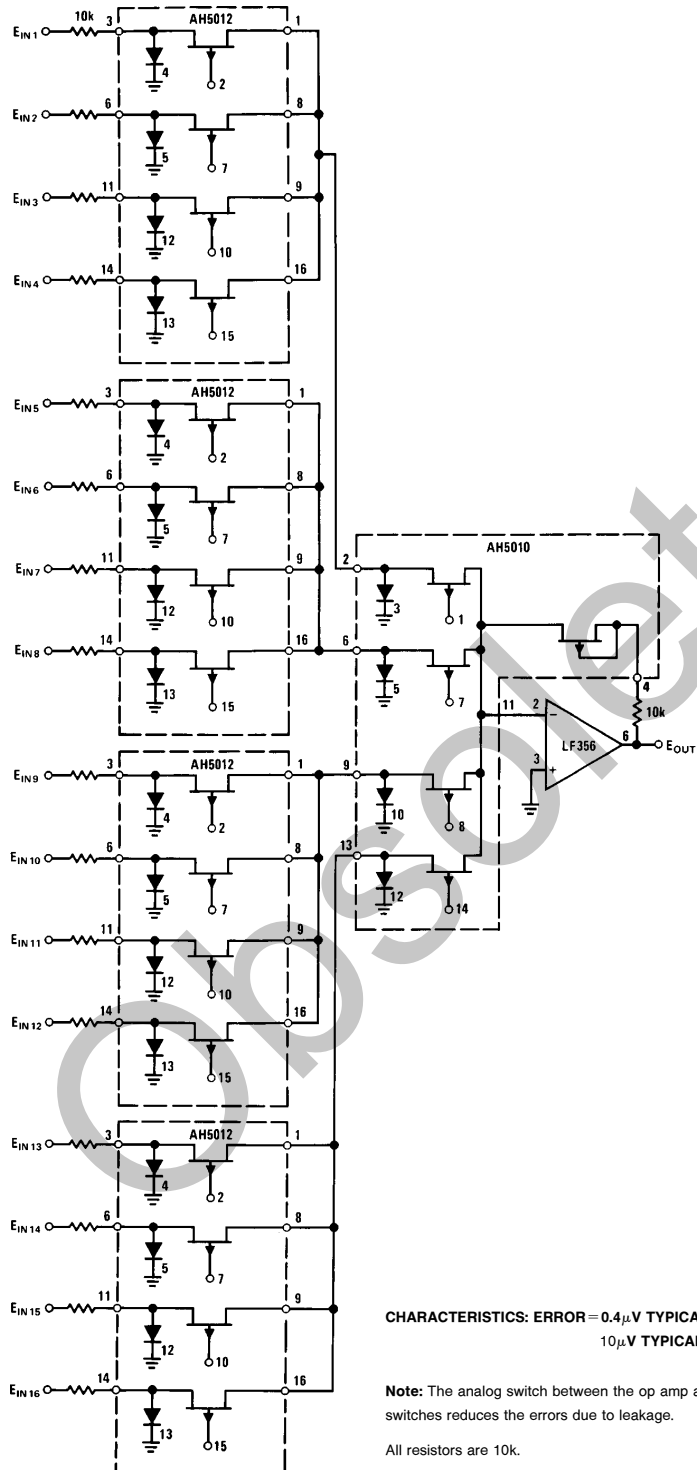
CHARACTERISTICS: ERROR = 0.4 μV TYPICAL @ 25°C
10μV TYPICAL @ 70°C

Note: The analog switch between the op amp and the 16 input switches reduces the errors due to leakage.

All resistors are 10k.

TL/H/5659–9

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Typical Applications (Continued)

Gain Programmable Amplifier

CHARACTERISTICS: $\text{GAIN} = \dfrac{-E_{OUT}}{I_{IN}} = R_{FB}$
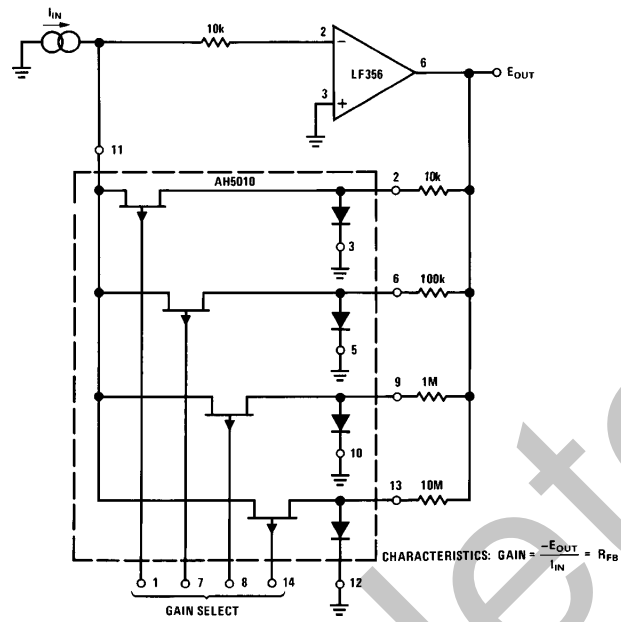
TL/H/5659–10

Physical Dimensions inches (millimeters)

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

30°
TYP

0.010
(0.254) MAX

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.004 − 0.010
(0.102 − 0.254)

0.014 − 0.020
(0.356 − 0.508) TYP

M14A (REV H)
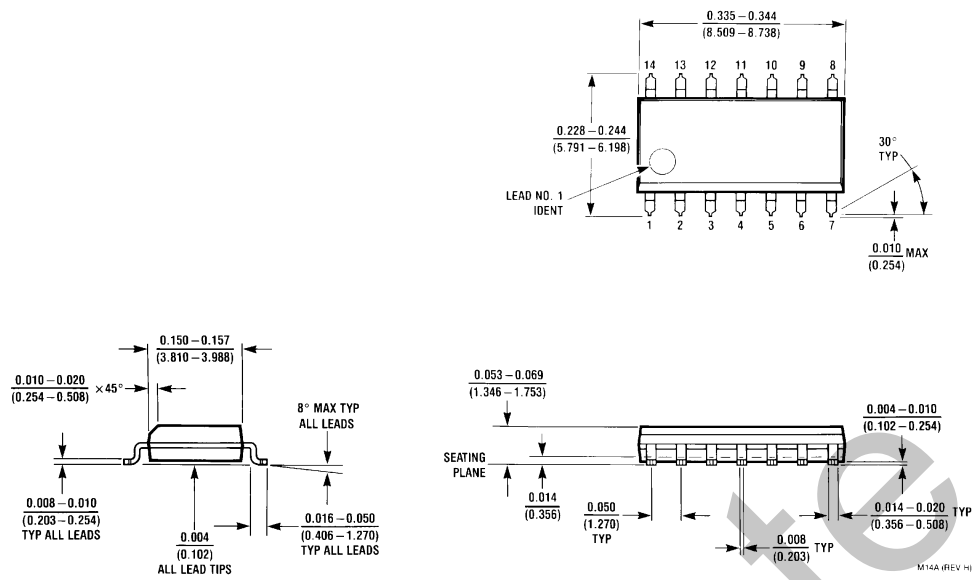
Small Outline Package (M)
Order Number AH5010CM
NS Package Number M14A

12

Physical Dimensions inches (millimeters) (Continued)

0.386 − 0.394
(9.804 − 10.00)

16 15 14 13 12 11 10 9

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO. 1
IDENT

1 2 3 4 5 6 7 8

0.010
(0.254) MAX

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) ×45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

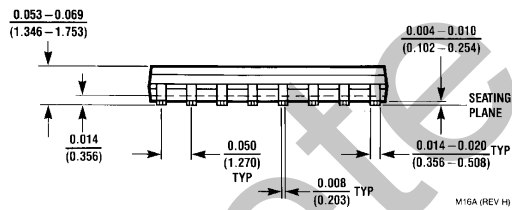0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020 TYP
(0.356 − 0.508)

M16A (REV H)
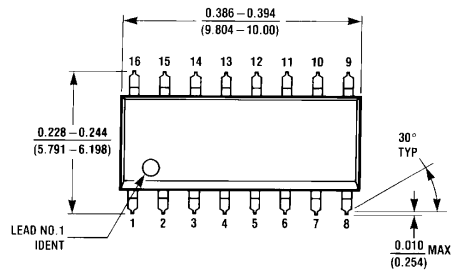
Small Outline Package (M)
Order Number AH5012CM
NS Package Number M16A

0.740 − 0.770
(18.80 − 19.56)

0.090
(2.286)

14 13 12 11 10 9 8

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7

0.092
(2.337) DIA

0.030 MAX
(0.762) DEPTH

OPTION 1

INDEX
AREA

14 13 12

PIN NO. 1
IDENT

1 2 3

OPTION 02

0.135 ± 0.005
(3.429 ± 0.127)

0.145 − 0.200
(3.683 − 5.080)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.020
(0.508)
MIN

0.125 − 0.150
(3.175 − 3.810)

90° ± 4° TYP

0.075 ± 0.015
(1.905 ± 0.381)

0.014 − 0.023 TYP
(0.356 − 0.584)

0.100 ± 0.010 TYP
(2.540 ± 0.254)

0.050 ± 0.010 TYP
(1.270 − 0.254)

0.300 − 0.320
(7.620 − 8.128)

0.065
(1.651)

95° ± 5°

0.008 − 0.016 TYP
(0.203 − 0.406)

0.280
(7.112)
MIN

0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

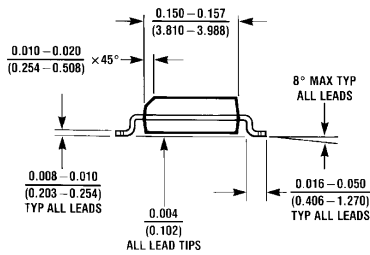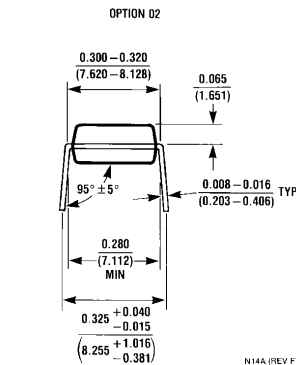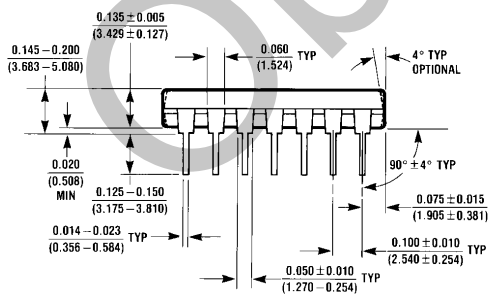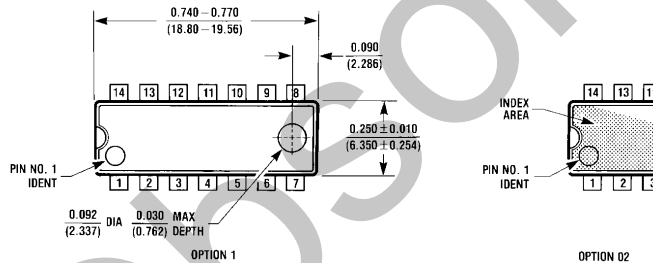N14A (REV F)

Dual-In-Line Package (N)
Order Number AH5010CN
NS Package Number N14A

13

Physical Dimensions inches (millimeters) (Continued)

0.092
(2.337)
DIA NOM
(2X)

0.090
(2.286)
NOM

0.843–0.870
(21.41–22.10)

PIN NO. 1 IDENT

0.250 ±0.005
(6.350 ±0.127)

0.280
(7.112)
MIN

0.030
(0.762)
MAX

0.300–0.320
(7.620–8.128)

0.065
(1.651)

0.060
(1.524)

0.040
(1.016)
TYP

0.130 ±0.005
(3.302 ±0.127)

0.145–0.200
(3.683–5.080)

95° ±5°

0.009–0.015
(0.229–0.381)

90° ±4°
TYP

0.020
(0.508)
MIN

0.325 $\begin{pmatrix} +0.040 \\ -0.015 \end{pmatrix}$

$\begin{pmatrix} 8.255 & +1.016 \\ & -0.381 \end{pmatrix}$

0.075 ±0.015
(1.905 ±0.381)

0.018 ±0.003
(0.457 ±0.076)

0.125–0.140
(3.175–3.556)

0.100 ±0.010
(2.540 ±0.254)
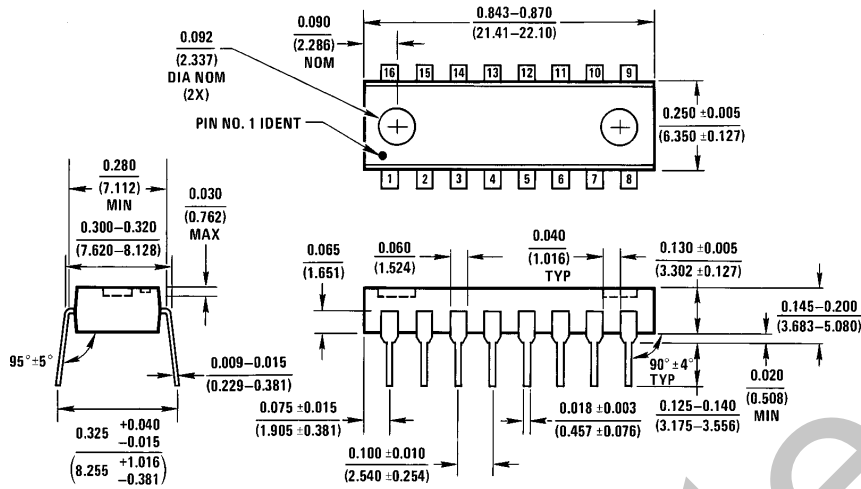
Dual-In-Line Package (N)
Order Number AH5011CN or AH5012CN
NS Package Number N16A

N16A (REV E)

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