0.35 Micron CMOS Pad Library Datasheets
AMI350XXPE 3.3/5.0 Volt
Section 4

AMI350XXPE 0.35 micron CMOS Pad Library

Input Drive Pieces

Pull Pieces

AMI350XXPE 0.35 micron CMOS Pad Library

Output Drive Pieces

AMI350XXPE 0.35 micron CMOS Pad Library

Power Pad Cells

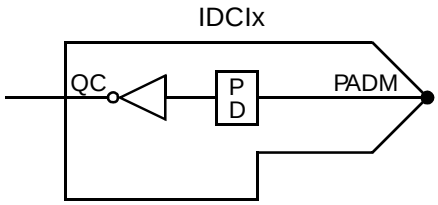
Special Pad Cells

DATASHEETS

Description

IDCIx is a family of inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

HDL Syntax

Verilog ..... IDCIx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCIx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCI3	IDCI6
PADM (pF)	4.76	4.76

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCI3	1.0	4.803	11.1
IDCI6	1.0	8.260	17.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} =3.3V, Typical Process

IDCI3	Number of Equivalent Loads		1	10	21	32	42 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.418 0.494	0.506 0.567	0.590 0.645	0.674 0.719	0.753 0.784
IDCI6	Number of Equivalent Loads		1	20	40	60	80 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.478 0.490	0.526 0.606	0.601 0.674	0.688 0.722	0.786 0.759

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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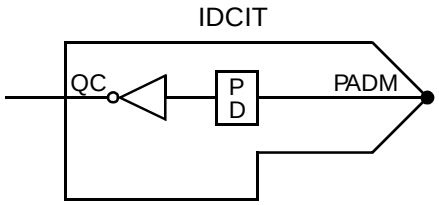
Description

IDCIT is an inverting 5 volt tolerant, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDCIT *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCIT port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.206	nA
EQL_{pd}	27.6	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

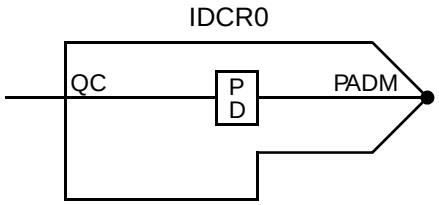
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	0.582 0.571	0.668 0.667	0.741 0.734	0.817 0.795	0.896 0.853

Note: This special purpose, “resistive input” pad is not intended for use as a general input pad.

Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDCR0 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCR0 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.084	nA
EQL_{pd}	2.6	Eq-load

See page 2-13 for power equation.

Note: This special purpose, “resistive input” pad is not intended for use as a general input pad.

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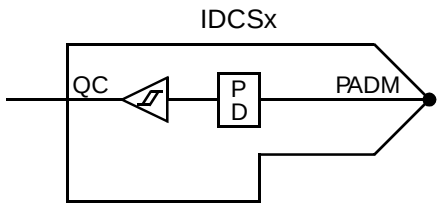
Description

IDCSx is a family of non-inverting, CMOS-level Schmitt trigger input buffer pieces with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

HDL Syntax

Verilog ..... IDCSx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCSx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCS3	IDCS6
PADM (pF)	4.76	4.76

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCS3	1.0	4.564	14.7
IDCS6	1.0	7.156	19.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

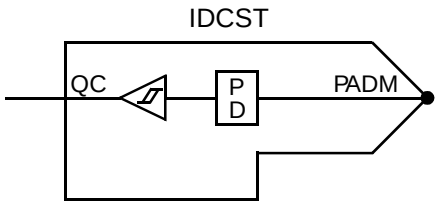
	Number of Equivalent Loads		1	10	21	32	42 (max)
IDCS3	From: PADM To: QC	t_{PLH} t_{PHL}	0.928 0.867	1.030 0.923	1.126 1.013	1.211 1.114	1.282 1.213
	Number of Equivalent Loads		**1**	**20**	**40**	**60**	**80 (max)**
IDCS6	From: PADM To: QC	t_{PLH} t_{PHL}	1.235 1.047	1.286 1.181	1.379 1.302	1.500 1.399	1.643 1.475

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDCST is a 5 volt tolerant non-inverting, CMOS Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDCST *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCST port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.476	nA
EQL_{pd}	23.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH}	1.546	1.719	1.813	1.845	1.853
		t_{PHL}	1.777	1.892	1.946	1.981	2.007

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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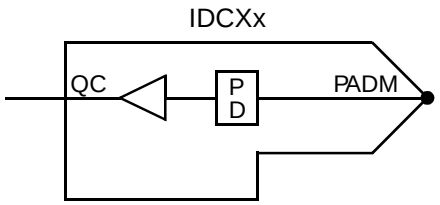
Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDCXx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	4.76	4.76

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCX3	1.0	3.939	9.2
IDCX6	1.0	7.635	15.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

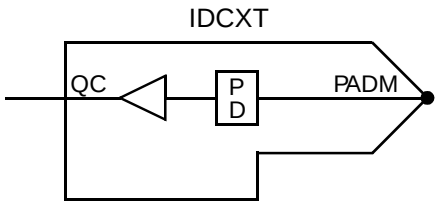
IDCX3	Number of Equivalent Loads		1	10	21	32	42 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.361 0.357	0.506 0.472	0.621 0.566	0.708 0.648	0.774 0.717
IDCX6	Number of Equivalent Loads		1	20	40	60	80 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.370 0.306	0.496 0.459	0.589 0.539	0.662 0.604	0.726 0.664

Delay will vary with input conditions. See page 2-15 for interconnect estimates

Description

IDCXT is a 5 volt tolerant non-inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDCXT *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCXT port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.477	nA
EQL_{pd}	24.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	0.578 0.514	0.675 0.643	0.758 0.740	0.838 0.815	0.918 0.878

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

IDDB6

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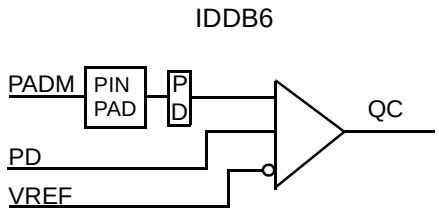
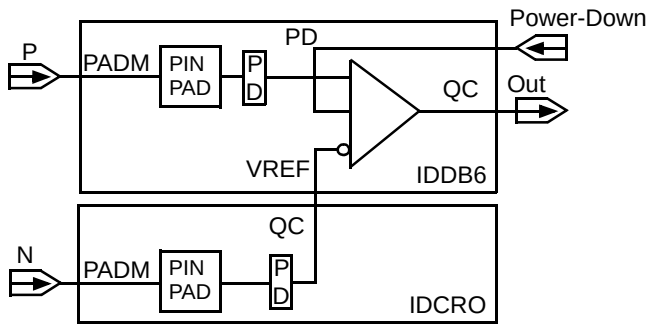
Description

IDDB6 is a 3.3 volt differential input receiver intended for single-ended operation with a user-supplied reference voltage and power-down. The reference voltage is typically supplied by a IDCR0 analog input pad and may be shared with multiple IDDB6 channels. The IDCR0 requires a separate bond pad site. Operates up to 140 MHz.

Logic Symbol



Logic Schematic



Pad Logic

Truth Table

PD	PADM	VREF	QC
L	L	L	IL
L	L	H	L
L	H	L	H
L	H	H	IL
H	X	X	L

IL= Illegal Condition

Pin Loading

	Load
PADM(pF)	4.76
PD(eql)	2.7
VREF(eql)	3.9

HDL Syntax

Verilog ..... IDDB6 *inst_name (*QC, PADM, PD, VREF);

VHDL..... *inst_name*: IDDB6 port map (QC, PADM, PD, VREF);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.657	nA
EQL_{pd}	26.2	Eq-load

Specification Summary

- General purpose differential input
- Pad Vcc= 3.3V +/- 5%
- Differential Voltage = 0.1V

DC CHARACTERISTICS Vdd=3.0V to 3.6V; Temperature=0°C to 100°C;

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current (Inputs set to HIGH)	I_{DDH}			1.44	mA
Power Supply Current (Inputs set to VDD/2)	I_{DDM}			1.26	mA
Power Supply Current (Inputs set to LOW)	I_{DDL}			1.18	mA
Input HIGH Current	I_{IH}			1	uA
Input LOW Current	I_{IH}			1	uA

AC CHARACTERISTICS 0.1 Volt Differential , Vdd=3.0V to 3.6V; Temperature=0°C to 100°C;

Characteristic	Symbol	Min	Typ	Max	Unit
Maximum Frequency	f_{max}			140	MHz
Propagation Delay to Output Differential	t_{PLH} t_{PHL}				ns
Input-to-Output Skew	t_{SK}			400	ps
Input Voltage Swing (Differential)	v_{PP}	100			mV
Input LOW Voltage Common Mode Range	v_{INLCMR}	0			V
Input HIGH Voltage Common Mode Range	v_{INHCMR}			VDD	V

AC CHARACTERISTICS 1.0 Volt Differential , Vdd=3.0V to 3.6V; Temperature=0°C to 100°C;

Characteristic	Symbol	Min	Typ	Max	Unit
Maximum Frequency	f_{max}			215	MHz
Propagation Delay to Output Differential	t_{PLH} t_{PHL}				ns
Input-to-Output Skew	t_{SK}			235	ps
Input Voltage Swing (Differential)	v_{PP}	1000			mV
Input LOW Voltage Common Mode Range	v_{INLCMR}	0			V
Input HIGH Voltage Common Mode Range	v_{INHCMR}			VDD	V

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Propagation Delays (ns)

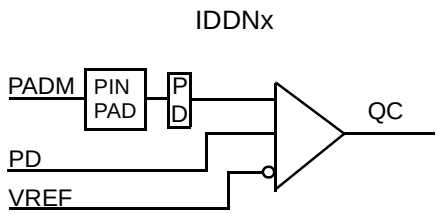
Conditions: T_J = 25°C, Vcc = 3.3V, Typical Process, Differential Voltage=0.35.

Number of Equivalent Loads		1	20	40	60	80 (max)
From: PADM	t_{PLH}	1.433	1.515	1.595	1.672	1.747
To: QC	t_{PHL}	1.457	1.556	1.640	1.726	1.816
From: VREF	t_{PLH}	1.433	1.515	1.595	1.672	1.747
To: QC	t_{PHL}	1.457	1.556	1.640	1.726	1.816
From: PD	t_{PLH}	2.248	2.316	2.338	2.352	2.362
To: QC	t_{PHL}	0.936	0.997	1.075	1.156	1.235

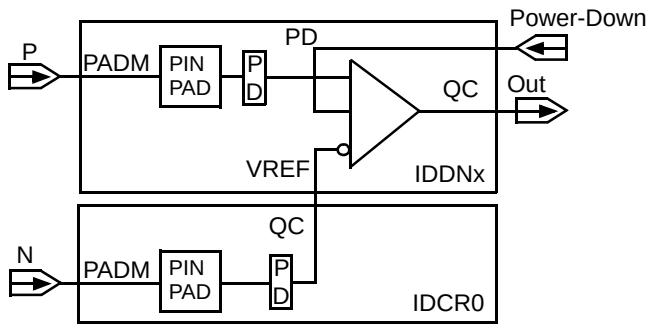
Description

IDDNx is a 3.3 volt differential input receiver intended for single-ended operation with a user-supplied reference voltage and power-down. The reference voltage is typically supplied by a IDCR0 analog input pad and may be shared with multiple IDDNx channels. The IDCR0 requires a separate bond pad site. Operates up to 62 MHz.

Logic Symbol



Logic Schematic



Truth Table

PD	PADM	VREF	QC
L	L	L	IL
L	L	H	L
L	H	L	H
L	H	H	IL
H	X	X	L

IL= Illegal Condition

Pin Loading

Pin Name	Load	
	IDDN3	IDDN6
PADM (pF)	4.76	4.76
VREF (eql)	3.6	3.6
PD (eql)	3.2	3.2

HDL Syntax

Verilog ..... IDDNx *inst_name (*QC, PADM, PD, VREF);

VHDL..... *inst_name*: IDDNx port map (QC, PADM, PD, VREF);

Specification Summary

- General purpose differential input
- Pad Vcc= 3.3V +/- 5%
- Differential Voltage = 0.1V

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDDN3	1.0	9.065	30.8
IDDN6	1.0	11.577	35.4

a. See page 2-13 for power equation.

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DC CHARACTERISTICS Vdd=3.0V to 3.6V; Temperature=0°C to 100°C;

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current (Inputs set to HIGH)	I_{DDH}			1.86	mA
Power Supply Current (Inputs set to VDD/2)	I_{DDM}			1.30	mA
Power Supply Current (Inputs set to LOW)	I_{DDL}			0.50	mA
Input HIGH Current	I_{IH}			1	uA
Input LOW Current	I_{IH}			1	uA

AC CHARACTERISTICS 0.1 Volt Differential , Vdd=3.0V to 3.6V; Temperature=0°C to 100°C;

Characteristic	Symbol	Min	Typ	Max	Unit
Maximum Frequency	f_{max}			62	MHz
Propagation Delay to Output Differential	t_{PLH} t_{PHL}				ns
Input-to-Output Skew	t_{SK}			807	ps
Input Voltage Swing (Differential)	v_{PP}	100			mV
Input LOW Voltage Common Mode Range	v_{INLCMR}	0			V
Input HIGH Voltage Common Mode Range	v_{INHCMR}			VDD	V

AC CHARACTERISTICS 1.0 Volt Differential , Vdd=3.0V to 3.6V; Temperature=0°C to 100°C;

Characteristic	Symbol	Min	Typ	Max	Unit
Maximum Frequency	f_{max}			65	MHz
Propagation Delay to Output Differential	t_{PLH} t_{PHL}				ns
Input-to-Output Skew	t_{SK}			769	ps
Input Voltage Swing (Differential)	v_{PP}	1000			mV
Input LOW Voltage Common Mode Range	v_{INLCMR}	0			V
Input HIGH Voltage Common Mode Range	v_{INHCMR}			VDD	V

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	10	21	32	42 (max)
IDDN3	From: PADM To: QC	t_{PLH} t_{PHL}	0.857 1.072	0.936 1.125	1.010 1.203	1.082 1.288	1.147 1.370
	From: VREF To: QC	t_{PLH} t_{PHL}	0.857 1.072	0.936 1.125	1.010 1.203	1.082 1.288	1.147 1.370
	From: PD To: QC	t_{PLH} t_{PHL}	1.607 0.471	1.666 0.552	1.720 0.633	1.767 0.707	1.807 0.770
	Number of Equivalent Loads		**1**	**20**	**40**	**60**	**80 (max)**
IDDN6	From: PADM To: QC	t_{PLH} t_{PHL}	0.874 1.120	0.985 1.232	1.060 1.305	1.114 1.359	1.157 1.402
	From: VREF To: QC	t_{PLH} t_{PHL}	0.874 1.120	0.985 1.232	1.060 1.305	1.114 1.359	1.157 1.402
	From: PD To: QC	t_{PLH} t_{PHL}	1.731 0.539	1.814 0.654	1.850 0.734	1.879 0.800	1.905 0.863

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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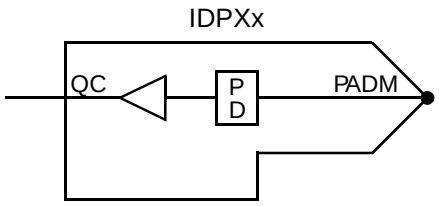
Description

IDPXx is a family of non-inverting, PCI-level input buffer pieces. IDPXx is intended to be used in conjunction with the 33MHz PCI ODPSXE33 piece whereas IDPX6 is intended to be used with the 66MHz PCI ODPHXE66 piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDPXx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDPX3	IDPX6
PADM (pF)	4.76	4.76

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDPX3	1.0	3.618	9.7
IDPX6	1.0	7.107	15.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

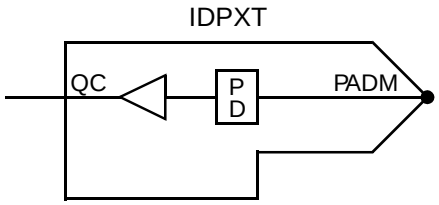
IDPX3	Number of Equivalent Loads		1	10	21	32	42 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.423 0.354	0.544 0.436	0.640 0.524	0.721 0.608	0.789 0.681
IDPX6	Number of Equivalent Loads		1	20	40	60	80 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.373 0.372	0.459 0.457	0.545 0.523	0.630 0.590	0.714 0.659

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDPXT is a 5 volt tolerant non-inverting, 33MHz PCI-level input buffer piece to be used in conjunction with 33MHz PCI ODPHTE66 piece

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDPXT *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPXT port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.477	nA
EQL_{pd}	25.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	0.522 0.519	0.642 0.631	0.722 0.703	0.780 0.753	0.825 0.790

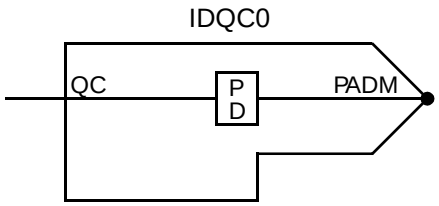
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

IDQC0 is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol



Truth Table

PADM	QO
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDQC0 *inst_name* (QO, PADM);

VHDL..... *inst_name*: IDQC0 port map (QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.084	nA
EQL_{pd}	2.5	Eq-load

See page 2-13 for power equation.

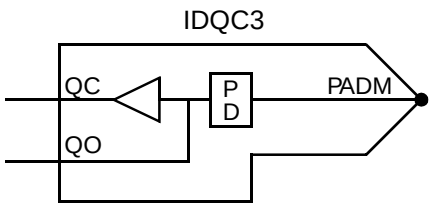
Design Notes:

The IDQC0 cell is for backward compatibility with existing oscillator methodologies.

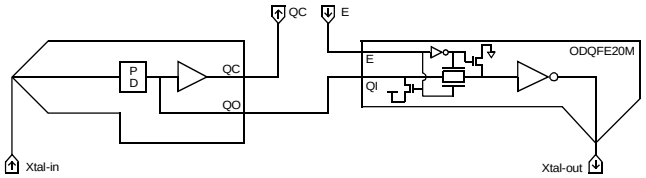
Description

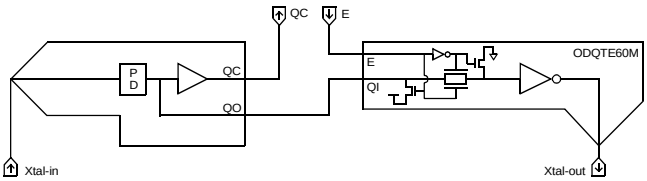
IDQC3 is a crystal oscillator input receiver pad piece with a non-inverting, CMOS clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

Logic Symbol



The Possible Logic Schematic Combinations





Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.76 pF

Pad Logic

HDL Syntax

Verilog ..... IDQC3 *inst_name (*QC, QO, PADM);

VHDL..... *inst_name*: IDQC3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.939	nA
EQL_{pd}	10.5	Eq-load

See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.407 0.349	0.524 0.499	0.632 0.597	0.727 0.669	0.808 0.721
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

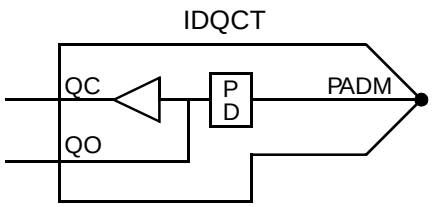
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes: The IDQC3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

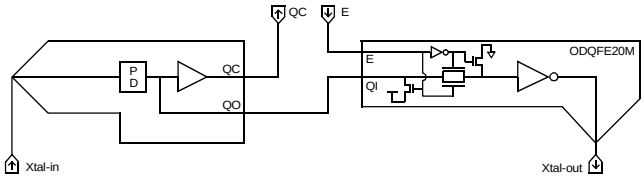
Description

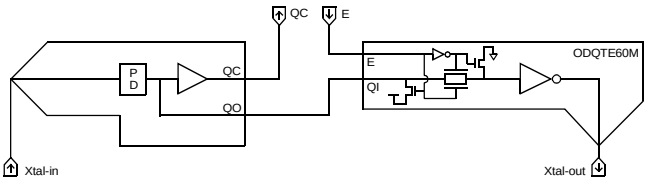
IDQCT is a 5-volt tolerant crystal oscillator input receiver pad piece with a non-inverting, CMOS clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

Logic Symbol



The Possible Logic Schematic Combinations





Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.76 pF

Pad Logic

HDL Syntax

Verilog ..... IDQCT *inst_name (*QC, QO, PADM);

VHDL..... *inst_name*: IDQCT port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.558	nA
EQL_{pd}	25.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.593 0.623	0.645 0.690	0.703 0.733	0.761 0.764	0.814 0.788
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

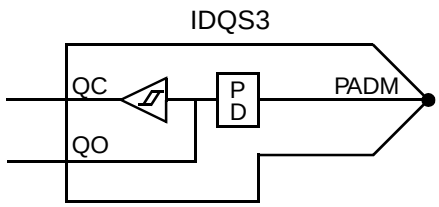
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes: The IDQCT is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator

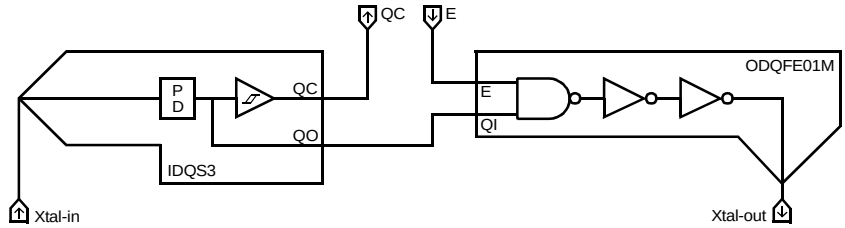
Description

IDQS3 is a crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS Schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol



Logic Schematic



Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDQS3 *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQS3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.564	nA
EQL_{pd}	15.8	Eq-load

See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.956 0.865	1.049 0.966	1.141 1.053	1.222 1.126	1.288 1.185
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

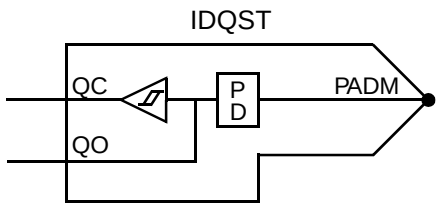
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Design Notes: The IDQS3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

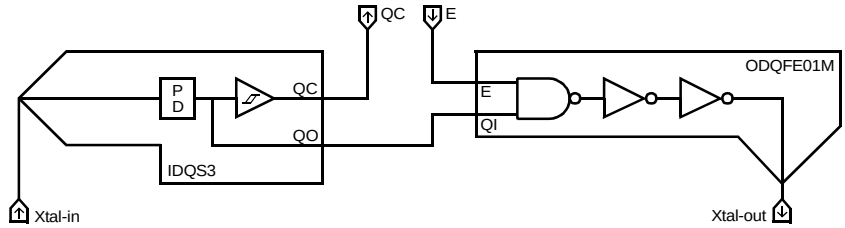
Description

IDQST is a 5-volt tolerant crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS Schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol



Logic Schematic



Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.76 pF

Pad Logic

HDL Syntax

Verilog ..... IDQST *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQST port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.557	nA
EQL_{pd}	24.8	Eq-load

See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	1.792 1.818	1.837 1.822	1.850 1.837	1.857 1.868	1.862 1.909
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

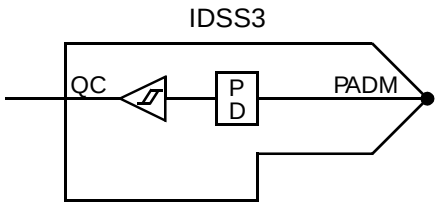
Design Notes:

The IDQST is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator

Description

IDSS3 is a non-inverting, SCSI-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDSS3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDSS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.740	nA
EQL_{pd}	17.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	1.114 1.377	1.224 1.517	1.320 1.657	1.401 1.773	1.467 1.859

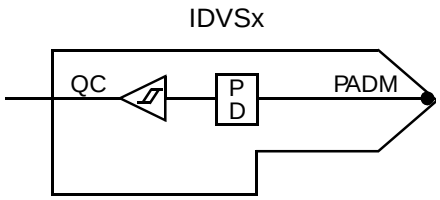
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

IDVSx is a family of non-inverting, LVTTL-level Schmitt input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDVXx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDVXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDVS3	IDVS6
PADM (pF)	4.76	4.76

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDVS3	1.0	4.564	14.5
IDVS6	1.0	7.156	19.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

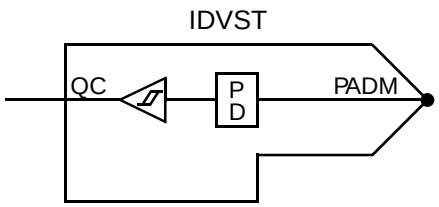
IDVS3	Number of Equivalent Loads		1	10	21	32	42 (max)
	From: PADM	t_{PLH}	0.667	0.777	0.876	0.962	1.035
	To: QC	t_{PHL}	0.738	0.848	0.939	1.016	1.080
IDVS6	Number of Equivalent Loads		1	20	40	60	80 (max)
	From: PADM	t_{PLH}	0.778	0.942	1.050	1.126	1.184
	To: QC	t_{PHL}	0.920	1.060	1.152	1.234	1.311

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

3.3 Description

IDVST is 5 volt tolerant non-inverting, LVTTL-level Schmitt input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDVST inst_IDVST (QC, PADM);

VHDL..... inst_IDVST : IDVST port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.781	nA
EQL_{pd}	26.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	20	40	60	80 (max)
PADM	QC	t_{PLH} t_{PHL}	1.099 1.002	1.197 1.081	1.265 1.144	1.324 1.201	1.376 1.253

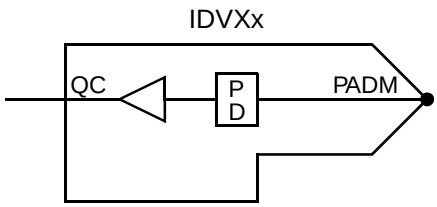
Delay will vary with input conditions. See page 2-15 for interconnect estimates

AMI350XXPE 0.35 micron CMOS Pad Library

Description

IDVXx is family of non-inverting, LVTTL-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

Pin Name	Load	
	IDVX3	IDVX6
PADM (pF)	4.76	4.76

HDL Syntax

Verilog ..... IDVXx inst_IDVXx (QC, PADM);

VHDL..... inst_IDVXx : IDVXx port map (QC, PADM);

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDVX3	1.0	3.699	9.2
IDVX6	1.0	7.155	14.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

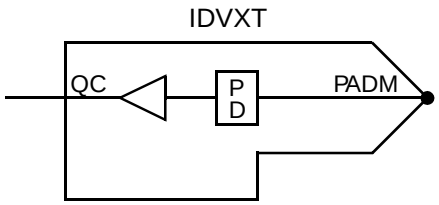
	Number of Equivalent Loads		1	10	21	32	42 (max)
IDVX3	From: PADM To: QC	t_{PLH} t_{PHL}	0.362 0.388	0.470 0.484	0.572 0.561	0.662 0.623	0.738 0.673
	Number of Equivalent Loads		**1**	**10**	**21**	**32**	**42 (max)**
IDVX6	From: PADM To: QC	t_{PLH} t_{PHL}	0.340 0.353	0.391 0.401	0.447 0.449	0.505 0.495	0.561 0.536

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDVXT is a 5-volt tolerant non-inverting, LVTTL-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDVXT inst_IDVXT (QC, PADM);

VHDL..... inst_IDVXT : IDVXT port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.558	nA
EQL_{pd}	24.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.543 0.470	0.610 0.525	0.677 0.570	0.727 0.607	0.769 0.638

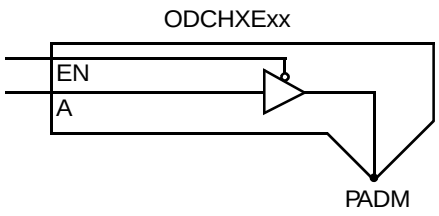
Delay will vary with input conditions. See page 2-15 for interconnect estimates

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCHXExx is a family of 8 to 24 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enable outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCHXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCHXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load			
	ODCHXE08	ODCHXE12	ODCHXE16	ODCHXE24
A (eq-load)	5.7	5.7	5.7	5.7
EN (eq-load)	8.2	8.2	8.2	8.2
PADM (pF)	4.79	4.80	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCHXE08	8	129.791	292.5
ODCHXE12	12	129.791	313.9
ODCHXE16	16	129.791	338.2
ODCHXE24	24	129.791	354.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCHXE08	From: A To: PADM	t_{PLH} t_{PHL}	0.897 0.667	1.884 1.272	3.272 2.120	6.048 3.819	8.856 5.534
	From: EN To: PADM	t_{ZH} t_{ZL}	0.841 0.683	1.829 1.270	3.230 2.133	6.016 3.856	8.789 5.542
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCHXE12	From: A To: PADM	t_{PLH} t_{PHL}	0.751 0.578	1.386 0.983	2.307 1.557	4.126 2.686	5.942 3.814
	From: EN To: PADM	t_{ZH} t_{ZL}	0.689 0.615	1.346 1.022	2.260 1.587	4.048 2.713	5.901 3.847
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCHXE16	From: A To: PADM	t_{PLH} t_{PHL}	0.707 0.583	1.218 0.910	1.932 1.331	3.362 2.173	4.815 3.055
	From: EN To: PADM	t_{ZH} t_{ZL}	0.656 0.584	1.160 0.906	1.872 1.350	3.307 2.195	4.754 3.056
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCHXE24	From: A To: PADM	t_{PLH} t_{PHL}	0.718 0.570	1.213 0.804	1.940 1.096	3.392 1.667	4.808 2.244
	From: EN To: PADM	t_{ZH} t_{ZL}	0.662 0.565	1.161 0.808	1.870 1.118	3.306 1.694	4.742 2.256

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

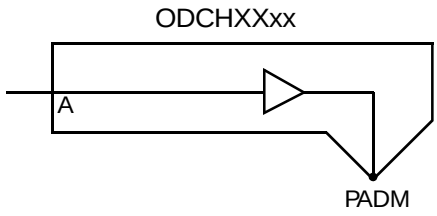
Delay (ns) From	To	Parameter	Cell ODCHXE08	ODCHXE12	ODCHXE16	ODCHXE24
EN	PADM	t_{HZ} t_{LZ}	0.317 0.460	0.361 0.493	0.406 0.536	0.406 0.590

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCHXXxx is a family of 8 to 24 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCHXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCHXXxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODCHXX08	ODCHXX12	ODCHXX16	ODCHXX24
A (eq-load)	19.4	19.4	19.4	19.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCHXX08	8	109.528	242.7
ODCHXX12	12	109.528	264.1
ODCHXX16	16	109.528	288.4
ODCHXX24	24	109.528	304.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCHXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.639 0.472	1.614 1.071	3.005 1.920	5.790 3.620	8.582 5.325
ODCHXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.476 0.405	1.127 0.799	2.049 1.361	3.856 2.487	5.682 3.618
ODCHXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.446 0.401	0.956 0.712	1.669 1.134	3.095 1.979	4.542 2.831
ODCHXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.502 0.325	0.994 0.561	1.698 0.844	3.127 1.417	4.575 1.977

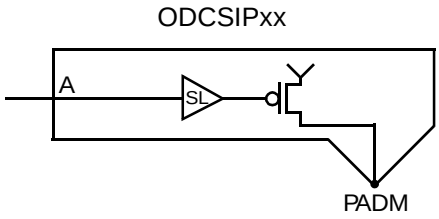
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCSIPxx is a family of 4 to 16 mA, inverting, CMOS-level output buffer pieces with P-channel open-drains (pull-up) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCSIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSIPxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODCSIP04	ODCSIP08	ODCSIP12	ODCSIP16
A (eq-load)	3.6	5.1	5.1	5.1
PADM (pF)	4.77	4.79	4.80	4.81

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSIP04	4	98.487	308.8
ODCSIP08	8	99.591	321.6
ODCSIP12	12	99.592	336.3
ODCSIP16	16	99.592	348.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCSIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.288	4.325	7.098	12.650	18.146
ODCSIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.871	2.841	4.284	7.136	9.924
ODCSIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.599	2.467	3.491	5.381	7.199
ODCSIP16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.600	2.358	3.184	4.699	6.186

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

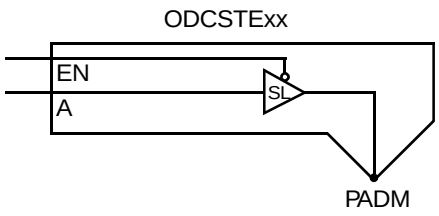
Delay (ns)		Parameter	Cell			
From	**To**		**ODCSIP04**	**ODCSIP08**	**ODCSIP12**	**ODCSIP16**
A	PADM	t_{HZ}	0.924	0.723	0.561	0.657

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCSTExx is a family of 4 to 12 mA, 5-volt tolerant, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSTExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSTExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODCSTE04	ODCSTE08	ODCSTE12
A (eq-load)	2.8	2.8	2.8
EN (eq-load)	8.6	8.6	8.6
PADM (pF)	4.82	4.67	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSTE04	4	113.253	462.3
ODCSTE08	8	113.253	477.1
ODCSTE12	12	113.253	499.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSTE04	From: A To: PADM	t_{PLH} t_{PHL}	3.241 2.158	5.247 3.524	8.057 5.040	13.591 7.808	19.058 10.566
	From: EN To: PADM	t_{ZH} t_{ZL}	2.933 1.969	5.079 3.381	7.837 4.918	13.344 7.705	18.984 10.448
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSTE08	From: A To: PADM	t_{PLH} t_{PHL}	2.421 1.656	3.546 2.605	5.104 3.676	8.044 5.210	10.748 6.654
	From: EN To: PADM	t_{ZH} t_{ZL}	2.248 1.496	3.369 2.471	4.923 3.570	7.859 5.131	10.567 6.575
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSTE12	From: A To: PADM	t_{PLH} t_{PHL}	1.619 1.651	3.205 2.403	4.234 3.232	6.238 4.520	8.103 5.534
	From: EN To: PADM	t_{ZH} t_{ZL}	2.099 1.444	3.060 2.243	4.121 3.127	6.028 4.436	8.014 5.464

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

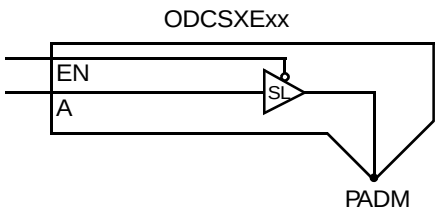
Delay (ns) From	To	Parameter	Cell ODCSTE04	ODCSTE08	ODCSTE12
EN	PADM	t_{HZ} t_{LZ}	8.099 0.691	8.842 0.797	9.622 0.897

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCSXExx is a family of 4 to 24 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16	ODCSXE24
A (eq-load)	2.9	2.9	2.9	2.9	2.9
EN (eq-load)	6.8	6.8	6.8	6.8	6.8
PADM (pF)	4.77	4.79	4.80	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXE04	4	113.228	350.0
ODCSXE08	8	113.228	372.4
ODCSXE12	12	113.228	393.8
ODCSXE16	16	113.228	418.1
ODCSXE24	24	113.228	434.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXE04	From: A To: PADM	t_{PLH} t_{PHL}	2.667 2.414	4.704 4.128	7.515 6.026	13.085 9.573	18.595 13.103
	From: EN To: PADM	t_{ZH} t_{ZL}	2.522 2.512	4.493 4.132	7.293 5.977	12.873 9.438	18.375 13.068
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.918 1.515	3.230 2.845	4.684 4.100	7.463 5.932	10.315 7.741
	From: EN To: PADM	t_{ZH} t_{ZL}	1.998 1.986	3.093 3.031	4.574 4.189	7.432 5.986	10.215 7.787
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE12	From: A To: PADM	t_{PLH} t_{PHL}	1.705 1.391	2.663 2.390	3.727 3.372	5.627 4.846	7.485 6.041
	From: EN To: PADM	t_{ZH} t_{ZL}	1.720 1.834	2.629 2.646	3.678 3.516	5.576 4.895	7.439 6.046
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.428 1.450	2.257 2.246	3.104 3.117	4.400 4.444	5.648 5.384
	From: EN To: PADM	t_{ZH} t_{ZL}	1.611 1.932	2.301 2.637	3.087 3.386	4.400 4.528	5.545 5.497
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE24	From: A To: PADM	t_{PLH} t_{PHL}	1.464 1.254	2.221 2.053	3.054 2.821	4.426 3.852	5.615 4.704
	From: EN To: PADM	t_{ZH} t_{ZL}	1.599 1.848	2.350 2.498	3.106 3.126	4.337 4.047	5.613 4.770

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

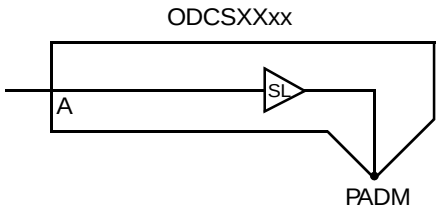
Delay (ns) From	To	Parameter	Cell				
			ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16	ODCSXE24
ENPADM		t_{HZ} t_{LZ}	0.509 0.457	0.591 0.504	0.677 0.541	0.760 0.592	0.760 0.655

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCSXXxx is a family of 4 to 24 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCSXX04	ODCSXX08	ODCSXX12	ODCSXX16	ODCSXX24
A (eq-load)	4.4	4.4	4.4	4.4	4.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXX04	4	110.634	341.4
ODCSXX08	8	110.634	363.7
ODCSXX12	12	110.634	385.1
ODCSXX16	16	110.634	409.4
ODCSXX24	24	110.634	425.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.166 2.441	4.411 3.902	7.260 5.770	12.776 9.353	18.337 12.863
ODCSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.711 1.350	2.904 2.676	4.363 3.922	7.206 5.759	10.056 7.584
ODCSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.339 1.183	2.378 2.185	3.422 3.219	5.345 4.688	7.180 5.895
ODCSXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.350 1.127	2.196 2.027	3.098 2.969	4.675 4.211	6.147 5.259
ODCSXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.290 1.158	2.139 1.868	3.073 2.587	4.665 3.716	6.098 4.527

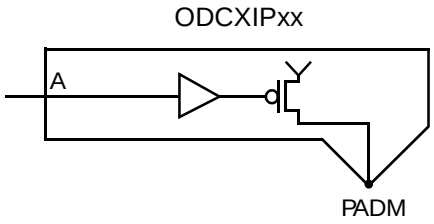
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCXIPxx is a family of 1 to 16 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCXIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXIPxx port map (PADM, A);

Pin Loading

Pin Name	Load					
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12	ODCXIP16
A (eq-load)	3.1	3.2	3.2	4.5	6.2	6.2
PADM (pF)	4.76	4.77	4.77	4.79	4.80	4.81

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXIP01	1	98.487	196.5
ODCXIP02	2	99.591	201.1
ODCXIP04	4	100.696	208.9
ODCXIP08	8	102.904	223.3
ODCXIP12	12	106.217	240.1
ODCXIP16	16	106.217	252.0

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXIP01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{ZH}	4.283	6.476	8.668	11.969	17.517
ODCXIP02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZH}	2.188	6.147	8.875	11.597	17.117
ODCXIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.276	3.231	5.985	11.447	16.998
ODCXIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	0.741	1.744	3.154	5.928	8.729
ODCXIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	0.581	1.223	2.121	3.930	5.769
ODCXIP16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	0.513	1.037	1.765	3.196	4.646

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

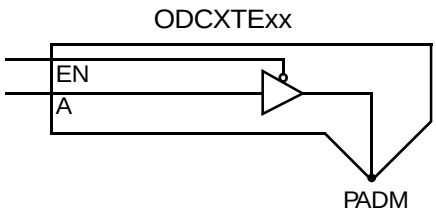
Delay (ns) From	To	Parameter	Cell					
			ODCXIP01	**ODCXIP02**	**ODCXIP04**	**ODCXIP08**	**ODCXIP12**	**ODCXIP16**
A	PADM	t_{HZ}	0.455	0.378	0.405	0.425	0.417	0.496

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCXTExx is a family of 1 to 12 mA 5-volt tolerant, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXTExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXTExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODCXTE01	ODCXTE02	ODCXTE04	ODCXTE08	ODCXTE12
A (eq-load)	2.8	2.8	2.8	2.8	2.8
EN (eq-load)	8.6	8.6	8.6	8.6	8.6
PADM (pF)	4.82	4.82	4.82	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXTE01	1	116.564	350.0
ODCXTE02	2	116.564	355.4
ODCXTE04	4	116.564	364.5
ODCXTE08	8	116.564	384.0
ODCXTE12	12	116.564	401.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODCXTE01	From: A To: PADM	t_{PLH} t_{PHL}	5.214 2.669	7.389 3.757	9.569 4.849	12.860 6.505	18.399 9.310
	From: EN To: PADM	t_{ZH} t_{ZL}	4.980 2.587	7.211 3.691	9.434 4.787	12.748 6.437	18.223 9.230
	Capacitive Load (pF)		**15**	**50**	**75**	**100**	**150 (max)**
ODCXTE02	From: A To: PADM	t_{PLH} t_{PHL}	2.845 1.512	6.689 3.427	9.431 4.793	12.175 6.159	17.671 8.890
	From: EN To: PADM	t_{ZH} t_{ZL}	2.733 1.560	6.563 3.384	9.297 4.767	12.040 6.146	17.552 8.851
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXTE04	From: A To: PADM	t_{PLH} t_{PHL}	1.743 1.007	3.652 1.969	6.352 3.310	11.935 6.006	17.362 8.751
	From: EN To: PADM	t_{ZH} t_{ZL}	1.557 0.969	3.492 1.928	6.276 3.270	11.797 5.967	17.263 8.710
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXTE08	From: A To: PADM	t_{PLH} t_{PHL}	1.191 0.789	2.206 1.271	3.606 1.942	6.345 3.284	9.195 4.642
	From: EN To: PADM	t_{ZH} t_{ZL}	1.055 0.746	2.043 1.223	3.453 1.913	6.232 3.274	9.030 4.602
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXTE12	From: A To: PADM	t_{PLH} t_{PHL}	1.040 0.784	1.732 1.118	2.716 1.597	4.553 2.534	6.491 3.453
	From: EN To: PADM	t_{ZH} t_{ZL}	0.941 0.715	1.612 1.071	2.573 1.556	4.458 2.491	6.346 3.401

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

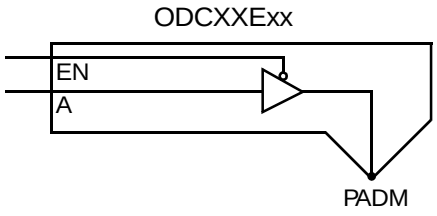
Delay (ns) From	To	Parameter	Cell ODCXTE01	ODCXTE02	ODCXTE04	ODCXTE08	ODCXTE12
EN	PADM	t_{HZ} t_{LZ}	0.646 0.409	0.762 0.437	0.983 0.494	1.606 0.597	2.339 0.692

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCXXExx is a family of 1 to 24 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load						
	ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16	ODCXXE24
A (eq-load)	7.1	9.9	9.9	2.8	5.7	5.7	5.7
EN (eq-load)	5.1	6.6	6.6	6.3	8.2	8.2	8.2
PADM (pF)	4.76	4.77	4.77	4.79	4.80	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXE01	1	100.887	203.6
ODCXXE02	2	104.393	214.4
ODCXXE04	4	104.393	225.6
ODCXXE08	8	118.748	280.1
ODCXXE12	12	129.791	313.9
ODCXXE16	16	129.791	338.1
ODCXXE24	24	129.791	354.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXXE01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.226 2.899	6.443 4.289	8.678 5.677	12.019 7.763	17.477 11.257
	From: EN To: PADM	t_{ZH} t_{ZL}	4.379 2.949	6.592 4.323	8.799 5.690	12.104 7.762	17.624 11.297
ODCXXE02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.096 1.551	6.022 3.994	8.757 5.736	11.478 7.477	16.995 10.959
	From: EN To: PADM	t_{ZH} t_{ZL}	2.300 1.561	6.128 3.991	8.869 5.746	11.614 7.497	17.115 10.957
ODCXXE04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.238 0.998	3.174 2.233	5.924 3.981	11.430 7.469	16.936 10.962
	From: EN To: PADM	t_{ZH} t_{ZL}	1.333 1.084	3.245 2.285	6.005 4.006	11.531 7.485	17.015 10.994
ODCXXE08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.099 0.814	2.072 1.415	3.459 2.272	6.256 3.978	9.036 5.680
	From: EN To: PADM	t_{ZH} t_{ZL}	0.954 0.730	1.924 1.330	3.330 2.186	6.143 3.894	8.911 5.600
ODCXXE12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.762 0.595	1.399 1.001	2.318 1.573	4.145 2.706	5.946 3.829
	From: EN To: PADM	t_{ZH} t_{ZL}	0.682 0.613	1.334 1.020	2.259 1.593	4.081 2.726	5.881 3.850
ODCXXE16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.720 0.599	1.231 0.908	1.942 1.338	3.372 2.195	4.828 3.045
	From: EN To: PADM	t_{ZH} t_{ZL}	0.676 0.627	1.172 0.957	1.873 1.370	3.324 2.220	4.752 3.082
ODCXXE24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.744 0.545	1.239 0.790	1.948 1.098	3.380 1.678	4.826 2.239
	From: EN To: PADM	t_{ZH} t_{ZL}	0.650 0.594	1.157 0.856	1.879 1.144	3.319 1.706	4.755 2.303

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Tristate Timing

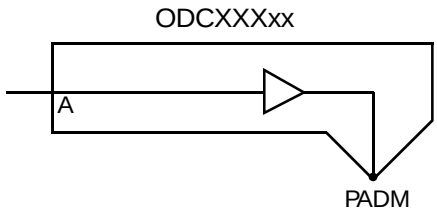
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell						
			ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16	ODCXXE24
EN	PADM	t_{HZ} t_{LZ}	0.617 0.231	0.498 0.192	0.625 0.257	0.399 0.472	0.380 0.506	0.429 0.555	0.429 0.618

Description

ODCXXXxx is a family of 1 to 24 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12	ODCXXX16	ODCXXX24
A (eq-load)	5.2	5.2	8.0	10.7	10.7	10.7	10.7

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXX01	1	98.486	197.1
ODCXXX02	2	98.486	202.8
ODCXXX04	4	100.694	214.2
ODCXXX08	8	102.903	238.2
ODCXXX12	12	102.903	259.6
ODCXXX16	16	102.903	283.9
ODCXXX24	24	102.903	300.2

a. See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

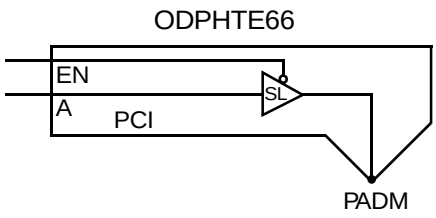
ODCXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.212 2.789	6.413 4.181	8.619 5.572	11.932 7.660	17.444 11.145
ODCXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.188 1.566	6.042 3.996	8.801 5.730	11.549 7.469	17.010 10.964
ODCXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.218 0.851	3.099 2.078	5.834 3.837	11.375 7.302	16.832 10.800
ODCXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.706 0.572	1.679 1.180	3.076 2.032	5.856 3.733	8.651 5.440
ODCXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.599 0.558	1.221 0.978	2.124 1.540	3.940 2.661	5.756 3.797
ODCXXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.599 0.576	1.057 0.906	1.766 1.337	3.202 2.194	4.637 3.044
ODCXXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.601 0.532	1.092 0.787	1.802 1.101	3.231 1.682	4.664 2.236

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODPHTE66 is a 3.3v drive ONLY, (33/66) MHz PSEUDO PCI compliant, 5V-Tolerant, non-inverting, tri-state buffer pad piece with controlled slew rate output. There is no high clamp diode (Ich) in this cell.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	6.5 eql
EN	9.1 eql
PADM	4.82 pF

HDL Syntax

Verilog ..... ODPHTE66 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODPHTE66 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	107.345	nA
EQL_{pd}	347.3	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	1.334 1.390	2.258 2.331	3.426 3.581	5.695 5.926	8.064 8.301
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	2.434 0.435 1.503 1.395	 2.261 2.326	 3.415 3.569	 5.742 5.916	 8.051 8.294

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

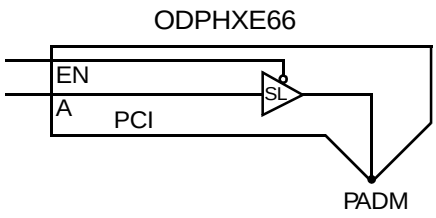
ODPHXE66

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODPHXE66 is a 3.3v drive ONLY, NON-5V tolerant, (33/66) MHz, PCI compliant, non-inverting, tri-state buffer piece with controlled slew rate output.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	9.6 eql
EN	9.8 eql
PADM	4.79 pF

HDL Syntax

Verilog ..... ODPHXE66 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODPHXE66 port map (PADM, A, EN);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	106.218	nA
EQL_{pd}	361.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

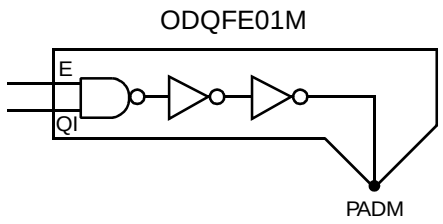
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	0.933 1.116	1.868 1.849	3.081 2.777	5.322 4.457	7.540 6.001
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.701 0.904 1.083 1.307	 1.977 2.040	 3.151 2.925	 5.386 4.577	 7.564 6.043

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

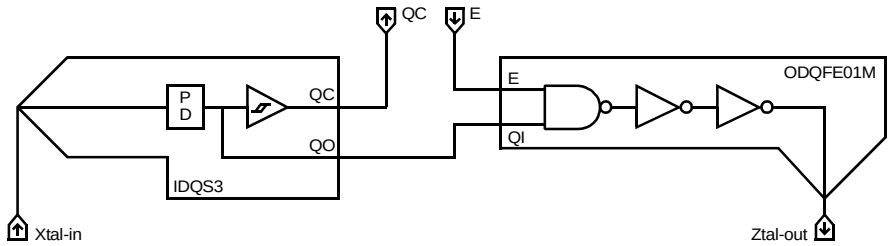
Description

ODQFE01M is a fundamental mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 32 kHz - 1 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
L	H	H
H	H	L
H	L	X

Pin Loading

	Load
E	5.0 eql
QI	3.7 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE01M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE01M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	98.486	nA
EQL_{pd}	201.1	Eq-load

See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	25	35	50	75 (max)
E	PADM	t_{PLH} t_{PHL}	4.399 3.268	6.542 4.660	8.777 6.053	12.129 8.143	17.582 11.625
QI	PADM	t_{PLH} t_{PHL}	4.539 3.244	6.708 4.602	8.881 5.984	12.176 8.089	17.764 11.655

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

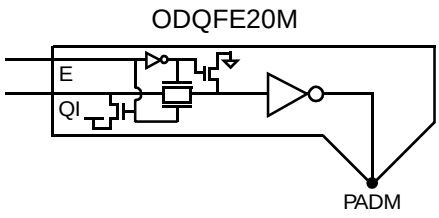
Design Notes:

The ODQFE01M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQS3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

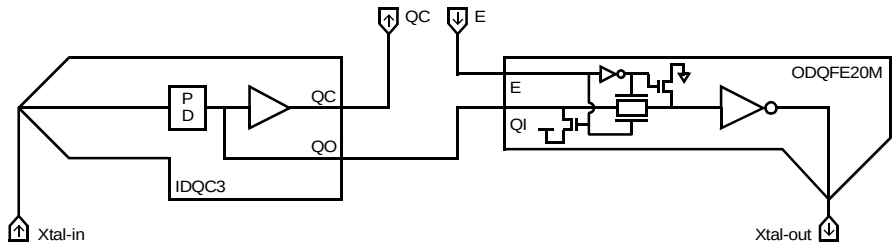
Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	8.1 eql
QI	6.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE20M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE20M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	98.672	nA
EQL_{pd}	216.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
E	PADM	t_{PLH} t_{PHL}	2.661 1.459	6.481 3.894	9.206 5.634	11.945 7.375	17.471 10.862
QI	PADM	t_{PLH} t_{PHL}	2.141 1.460	5.982 3.942	8.718 5.670	11.455 7.398	16.942 10.876

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

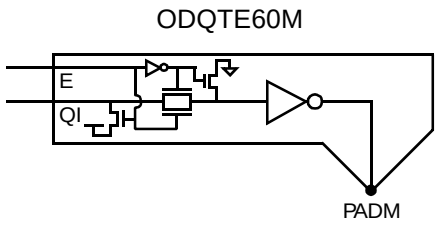
Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

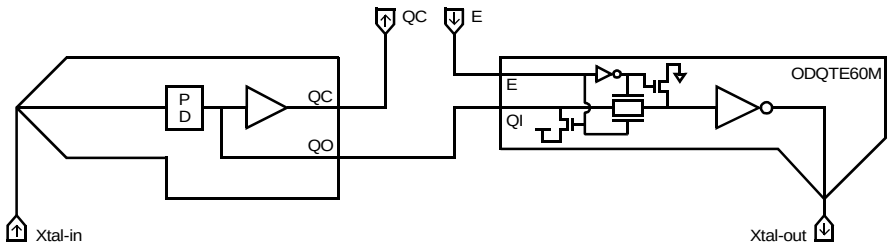
Description

ODQTE60M is an third-overtone mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	8.1 eql
QI	6.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQTE60M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQTE60M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	98.672	nA
EQL_{pd}	227.6	Eq-load

See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
E	PADM	t_{PLH} t_{PHL}	1.753 0.850	3.662 2.067	6.403 3.817	11.915 7.291	17.413 10.784
QI	PADM	t_{PLH} t_{PHL}	1.150 0.929	3.082 2.156	5.835 3.871	11.365 7.361	16.869 10.845

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

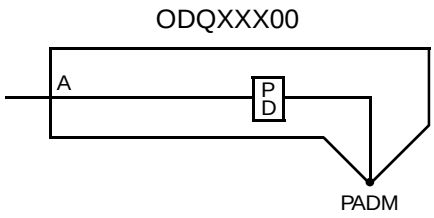
Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

Description

ODQXXX00 is a non-buffered, resistive analog crystal oscillator output pad piece with ESD protection.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	2.9 eql

HDL Syntax

Verilog ..... ODQXXX00 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODQXXX00 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	96.267	nA
EQL_{pd}	186.0	Eq-load

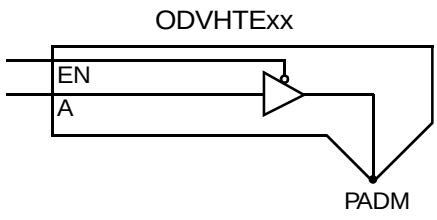
See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODVHTExx is a family of 8 to 12 mA, 5 volt tolerant , high performance, non-inverting, LVTTL-level, tristate output buffer pieces with active low enable outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVHTExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVHTExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load	
	ODVHTE08	ODVHTE12
A (eq-load)	2.8	2.8
EN (eq-load)	8.6	8.6
PADM (pF)	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVHTE08	8	116.564	384.0
ODVHTE12	12	116.564	401.9

a. See page 2-13 for power equation.

3.33.3 Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVHTE08	From: A To: PADM	t_{PLH} t_{PHL}	1.097 0.864	1.932 1.432	3.085 2.236	5.367 3.849	7.718 5.473
	From: EN To: PADM	t_{ZH} t_{ZL}	0.966 0.825	1.792 1.396	2.955 2.197	5.248 3.792	7.581 5.395
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVHTE12	From: A To: PADM	t_{PLH} t_{PHL}	1.150 0.817	1.552 1.221	2.304 1.790	3.910 2.898	5.428 4.017
	From: EN To: PADM	t_{ZH} t_{ZL}	0.852 0.749	1.423 1.150	2.218 1.727	3.768 2.853	5.340 3.957

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

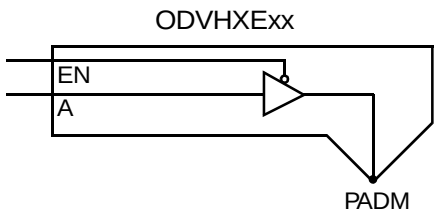
Delay (ns) From	To	Parameter	Cell ODVHTE08	Cell ODVHTE12
EN	PADM	t_{HZ} t_{LZ}	1.548 0.579	2.246 0.665

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODVHXExx is a family of 8 to 24 mA, non-inverting. TTL-level, tristate output buffer pieces with active low enable outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVHXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVHXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load			
	ODVHXEODVHTE12	ODVHXE12	ODVHXE16	ODVHXE24
A (eq-load)	5.7	5.7	5.7	5.7
EN (eq-load)	8.2	8.2	8.2	8.2
PADM (pF)	4.79	4.80	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVHXE08	8	129.791	292.5
ODVHXE12	12	129.791	313.9
ODVHXE16	16	129.791	338.2
ODVHXE24	24	129.791	354.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVHXE08	From: A To: PADM	t_{PLH} t_{PHL}	0.821 0.721	1.622 1.429	2.789 2.459	5.114 4.519	7.401 6.547
	From: EN To: PADM	t_{ZH} t_{ZL}	0.793 0.746	1.591 1.476	2.726 2.498	5.028 4.529	7.362 6.592
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVHXE12	From: A To: PADM	t_{PLH} t_{PHL}	0.724 0.656	1.252 1.137	1.998 1.804	3.515 3.146	5.024 4.514
	From: EN To: PADM	t_{ZH} t_{ZL}	0.643 0.648	1.173 1.131	1.928 1.818	3.443 3.177	4.952 4.520
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVHXE16	From: A To: PADM	t_{PLH} t_{PHL}	0.662 0.601	1.089 0.979	1.679 1.505	2.853 2.527	4.055 3.550
	From: EN To: PADM	t_{ZH} t_{ZL}	0.594 0.678	1.012 1.007	1.608 1.515	2.798 2.557	3.982 3.556
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVHXE24	From: A To: PADM	t_{PLH} t_{PHL}	0.650 0.592	1.068 0.858	1.663 1.209	2.848 1.907	4.037 2.574
	From: EN To: PADM	t_{ZH} t_{ZL}	0.597 0.664	1.014 0.883	1.611 1.226	2.802 1.930	3.985 2.594

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

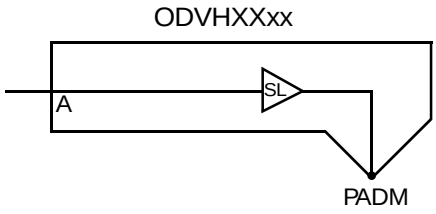
Delay (ns) From	To	Parameter	Cell			
			ODVHXE08	**ODVHXE12**	**ODVHXE16**	**ODVHXE24**
EN	PADM	t_{HZ} t_{LZ}	0.317 0.460	0.361 0.493	0.406 0.536	0.406 0.590

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODVHXXxx is a family of 4 to 24 mA, non-inverting, LVTTL-level, output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODVHXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVHXXxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODVHXX08	ODVHXX12	ODVHXX16	ODVHXX24
A (eq-load)	19.4	19.4	19.4	19.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVHXX08	8	109.528	242.7
ODVHXX12	12	109.528	264.1
ODVHXX16	16	109.528	288.4
ODVHXX24	24	109.528	304.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVHXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	0.542 0.521	1.359 1.237	2.520 2.261	4.823 4.306	7.142 6.356
ODVHXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	0.420 0.446	0.955 0.926	1.720 1.596	3.225 2.940	4.741 4.301
ODVHXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	0.397 0.454	0.817 0.816	1.412 1.317	2.595 2.340	3.777 3.352
ODVHXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	0.420 0.377	0.836 0.635	1.429 0.976	2.610 1.650	3.789 2.331

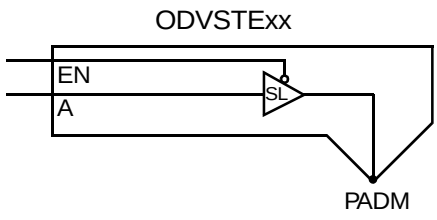
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODVSTExx is a family of 4 to 12 mA, 5 volt tolerant, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVSTExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVSTExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODVSTE04	ODVSTE08	ODVSTE12
A (eq-load)	2.8	2.8	2.8
EN (eq-load)	8.6	8.6	8.6
PADM (pF)	4.67	4.67	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSTE04	4	113.253	457.6
ODVSTE08	8	113.253	477.1
ODVSTE12	12	113.253	499.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVSTE04	From: A To: PADM	t_{PLH} t_{PHL}	2.475 2.129	4.177 3.584	6.566 5.367	11.198 8.747	15.634 12.085
	From: EN To: PADM	t_{ZH} t_{ZL}	2.314 1.830	4.014 3.418	6.400 5.265	11.029 8.669	15.464 11.956
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSTE08	From: A To: PADM	t_{PLH} t_{PHL}	1.863 1.599	2.988 2.651	4.269 3.723	6.480 5.525	8.845 7.190
	From: EN To: PADM	t_{ZH} t_{ZL}	1.741 1.442	2.802 2.519	4.125 3.612	6.395 5.442	8.709 7.148
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSTE12	From: A To: PADM	t_{PLH} t_{PHL}	2.081 1.770	2.948 2.616	3.915 3.516	5.505 4.935	7.152 6.115
	From: EN To: PADM	t_{ZH} t_{ZL}	2.047 1.588	2.782 2.475	3.701 3.462	5.368 4.904	6.916 6.095

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

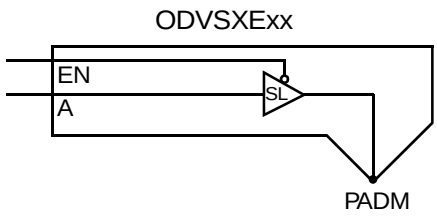
Delay (ns) From	To	Parameter	Cell ODVSTE04	ODVSTE08	ODVSTE12
EN	PADM	t_{HZ} t_{LZ}	0.616 0.603	0.715 0.703	9.622 0.897

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODVSXExx is a family of 4 to 24 mA, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODVSXE04	ODVSXE08	ODVSXE12	ODVSXE16	ODVSXE24
A (eq-load)	2.9	2.9	2.9	2.9	2.9
EN (eq-load)	6.8	6.8	6.8	6.8	6.8
PADM (pF)	4.77	4.79	4.80	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSXE04	4	113.228	350.0
ODVSXE08	8	113.228	372.4
ODVSXE12	12	113.228	393.8
ODVSXE16	16	113.228	418.1
ODVSXE24	24	113.228	434.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVSXE04	From: A To: PADM	t_{PLH} t_{PHL}	2.310 2.581	4.106 4.484	6.510 6.746	11.181 11.007	15.667 15.189
	From: EN To: PADM	t_{ZH} t_{ZL}	2.168 2.732	3.948 4.485	6.293 6.702	10.909 10.948	15.505 15.169
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.741 1.831	2.833 3.159	4.119 4.451	6.503 6.649	8.811 8.762
	From: EN To: PADM	t_{ZH} t_{ZL}	1.814 2.230	2.814 3.297	4.031 4.527	6.397 6.733	8.728 8.776
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSXE12	From: A To: PADM	t_{PLH} t_{PHL}	1.767 1.592	2.415 2.671	3.357 3.721	4.969 5.375	6.520 6.746
	From: EN To: PADM	t_{ZH} t_{ZL}	1.614 2.102	2.398 2.958	3.320 3.846	4.930 5.388	6.388 6.834
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.474 1.558	2.245 2.530	3.068 3.458	4.421 4.845	5.600 5.967
	From: EN To: PADM	t_{ZH} t_{ZL}	1.632 2.276	2.301 2.861	3.057 3.604	4.370 4.918	5.536 6.033
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVSXE24	From: A To: PADM	t_{PLH} t_{PHL}	1.508 1.326	2.251 2.263	3.065 3.122	4.404 4.261	5.613 5.079
	From: EN To: PADM	t_{ZH} t_{ZL}	1.678 1.942	2.350 2.620	3.083 3.309	4.375 4.330	5.585 5.116

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

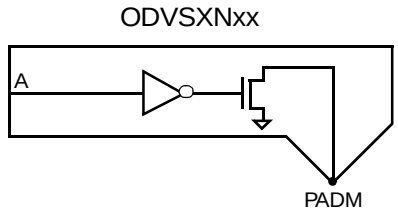
Delay (ns) From	To	Parameter	Cell ODVSXE04	ODVSXE08	ODVSXE12	ODVSXE16	ODVSXE24
EN	PADM	t_{HZ} t_{LZ}	0.509 0.459	0.592 0.501	0.679 0.539	0.760 0.592	0.760 0.655

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODVSXNxx is a family of 4 to 24 mA, non-inverting, LVTTL-level, output buffer pieces with N-channel open-drains (pull-down) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODVSXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVSXNxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODVSXN04	ODVSXN08	ODVSXN12	ODVSXN16	ODVSXN24
A (eq-load)	6.6	6.6	6.6	6.6	6.6
PADM (pF)	4.76	4.76	4.76	4.76	4.76

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSXN04	4	102.903	302.9
ODVSXN08	8	102.903	313.2
ODVSXN12	12	102.903	322.4
ODVSXN16	16	102.903	334.8
ODVSXN24	24	102.903	351.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVSXN04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	2.691	4.322	6.485	10.726	14.930
ODVSXN08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	2.143	3.130	4.341	6.551	8.559
ODVSXN12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	2.064	2.860	3.708	5.227	6.669
ODVSXN16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.941	2.676	3.464	4.734	5.823
ODVSXN24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.840	2.563	3.220	4.200	5.056

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

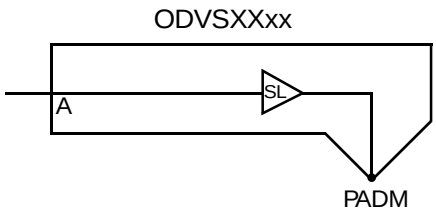
Delay (ns)		Parameter	Cell				
From	**To**		**ODVSXN04**	**ODVSXN08**	**ODVSXN12**	**ODVSXN16**	**ODVSXN24**
A	PADM	t_{HZ}	0.176	0.221	0.268	0.325	0.395

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODVSXXxx is a family of 4 to 24 mA, non-inverting, LVTTL-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog..... ODVSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODVSXX04	ODVSXX08	ODVSXX12	ODVSXX16	ODVSXX24
A (eq-load)	4.4	4.4	4.4	4.4	4.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSXX04	4	110.634	341.4
ODVSXX08	8	110.634	363.7
ODVSXX12	12	110.634	385.1
ODVSXX16	16	110.634	409.4
ODVSXX24	24	110.634	425.8

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.991 2.596	3.840 4.305	6.233 6.546	10.856 10.836	15.416 14.989
ODVSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.415 1.621	2.545 2.996	3.833 4.293	6.199 6.488	8.544 8.605
ODVSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.237 1.540	2.107 2.673	3.069 3.730	4.707 5.363	6.220 6.777
ODVSXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.160 1.287	1.928 2.311	2.773 3.323	4.149 4.668	5.325 5.836
ODVSXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PLH}	1.193 1.268	1.968 2.084	2.784 2.910	4.136 4.093	5.336 4.921

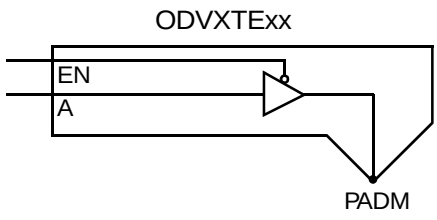
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODVXTExx is a family of 1 to 12 mA, 5-volt tolerant, non-inverting, LVTTL-level, tristate output buffer pieces with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVXTExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVXTExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODVXTE01	ODVXTE02	ODVXTE04	ODVXTE08	ODVXTE12
A (eq-load)	2.8	2.8	2.8	2.8	2.8
EN (eq-load)	8.6	8.6	8.6	8.6	8.6
PADM (pF)	4.82	4.82	4.82	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXTE01	1	116.564	350.0
ODVXTE02	2	116.564	355.4
ODVXTE04	4	116.564	364.5
ODVXTE08	8	116.564	384.0
ODVXTE12	12	116.564	401.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVXTE01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.368 3.070	6.216 4.410	8.079 5.747	10.860 7.740	15.402 11.032
	From: EN To: PADM	t_{ZH} t_{ZL}	4.265 3.100	6.083 4.394	7.896 5.669	10.640 7.618	15.305 11.040
ODVXTE02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.530 1.683	5.636 4.058	7.936 5.680	10.228 7.299	14.772 10.600
	From: EN To: PADM	t_{ZH} t_{ZL}	2.365 1.686	5.565 3.975	7.848 5.613	10.130 7.251	14.695 10.529
ODVXTE04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.503 1.090	3.127 2.220	5.425 3.842	9.963 7.097	14.572 10.348
	From: EN To: PADM	t_{ZH} t_{ZL}	1.327 1.008	2.954 2.189	5.285 3.853	9.884 7.064	14.415 10.358
ODVXTE08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.172 0.860	1.949 1.435	3.066 2.248	5.419 3.864	7.690 5.471
	From: EN To: PADM	t_{ZH} t_{ZL}	0.985 0.808	1.797 1.405	2.946 2.202	5.270 3.792	7.570 5.455
ODVXTE12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.002 0.841	1.559 1.271	2.340 1.801	3.899 2.882	5.463 4.056
	From: EN To: PADM	t_{ZH} t_{ZL}	0.851 0.760	1.412 1.179	2.206 1.754	3.773 2.860	5.321 3.989

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

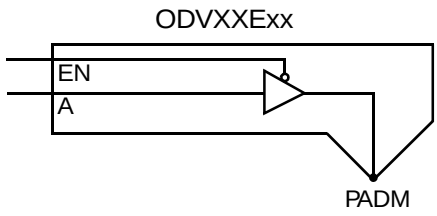
Delay (ns) From	To	Parameter	Cell ODVXTE01	ODVXTE02	ODVXTE04	ODVXTE08	ODVXTE12
EN	PADM	t_{HZ} t_{LZ}	0.646 0.409	0.762 0.437	0.983 0.494	1.606 0.597	2.342 0.690

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODVXXExx is a family of 1 to 24 mA, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODVXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load						
	XXE01	ODVXXE02	ODVXXE04	ODVXXE08	ODVXXE12	ODVXXE16	ODVXXE24
A (eq-load)	7.1	9.9	9.9	2.8	5.7	5.7	5.7
EN (eq-load)	5.1	6.6	6.6	6.3	8.2	8.2	8.2
PADM (pF)	4.76	4.77	4.77	4.79	4.80	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXXE01	1	100.887	203.6
ODVXXE02	2	104.393	214.4
ODVXXE04	4	104.393	225.6
ODVXXE08	8	118.748	280.1
ODVXXE12	12	129.791	313.9
ODVXXE16	16	129.791	338.1
ODVXXE24	24	129.791	354.5

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVXXE01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.582 3.423	5.451 5.085	7.297 6.745	10.035 9.245	14.545 13.442
	From: EN To: PADM	t_{ZH} t_{ZL}	3.675 3.468	5.506 5.117	7.325 6.737	10.062 9.193	14.689 13.469
ODVXXE02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.856 1.808	5.009 4.707	7.280 6.779	9.563 8.864	14.154 13.071
	From: EN To: PADM	t_{ZH} t_{ZL}	1.984 1.801	5.151 4.731	7.415 6.825	9.695 8.915	14.298 13.076
ODVXXE04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.070 1.116	2.664 2.601	4.943 4.708	9.523 8.875	14.091 13.054
	From: EN To: PADM	t_{ZH} t_{ZL}	1.206 1.124	2.776 2.618	5.035 4.712	9.627 8.880	14.187 13.059
ODVXXE08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.018 0.877	1.837 1.586	2.997 2.612	5.304 4.675	7.620 6.698
	From: EN To: PADM	t_{ZH} t_{ZL}	0.886 0.784	1.713 1.535	2.849 2.562	5.140 4.563	7.491 6.660
ODVXXE12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.706 0.647	1.230 1.130	1.995 1.806	3.515 3.156	5.018 4.514
	From: EN To: PADM	t_{ZH} t_{ZL}	0.627 0.706	1.161 1.170	1.918 1.828	3.429 3.171	4.942 4.557
ODVXXE16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.665 0.624	1.089 0.991	1.687 1.527	2.873 2.535	4.048 3.574
	From: EN To: PADM	t_{ZH} t_{ZL}	0.623 0.651	1.039 1.025	1.634 1.547	2.820 2.575	4.005 3.590
ODVXXE24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.676 0.584	1.093 0.868	1.688 1.234	2.875 1.923	4.062 2.602
	From: EN To: PADM	t_{ZH} t_{ZL}	0.609 0.585	1.030 0.876	1.627 1.243	2.816 1.927	4.001 2.612

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Tristate Timing

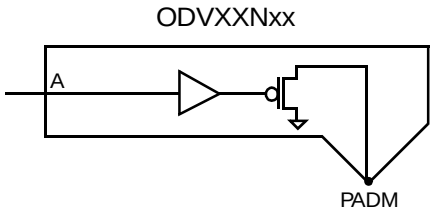
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell						
			ODVXXE01	ODVXXE02	ODVXXE04	ODVXXE08	ODVXXE12	ODVXXE16	ODVXXE24
EN	PADM	t_{HZ} t_{LZ}	0.617 0.231	0.498 0.192	0.625 0.257	0.399 0.472	0.380 0.506	0.429 0.555	0.426 0.616

Description

ODVXXNxx is a family of 1 to 24 mA, non-inverting, LVTTL-level, output buffer pieces with N-channel, open-drains (pull-down).

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODVXXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVXXNxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODVXXN01	ODVXXN02	ODVXXN04	ODVXXN08	ODVXXN12	ODVXXN16	ODVXXN24
A (eq-load)	5.4	5.4	5.4	7.9	7.9	10.7	10.7
PADM (pF)	4.76	4.76	4.76	4.76	4.76	4.76	4.76

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXXN01	1	98.486	191.2
ODVXXN02	2	98.486	193.8
ODVXXN04	4	98.486	199.3
ODVXXN08	8	100.694	210.6
ODVXXN12	12	100.694	219.7
ODVXXN16	16	102.902	233.1
ODVXXN24	24	102.902	249.5

a. See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVXXN01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{ZL}	3.131	4.801	6.473	8.980	13.152
ODVXXN02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZL}	1.558	4.482	6.569	8.656	12.827
ODVXXN04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.955	2.432	4.511	8.692	12.859
ODVXXN08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.553	1.276	2.293	4.336	6.390
ODVXXN12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.459	0.957	1.642	2.994	4.341
ODVXXN16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.413	0.781	1.286	2.305	3.324
ODVXXN24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.373	0.622	0.979	1.665	2.350

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

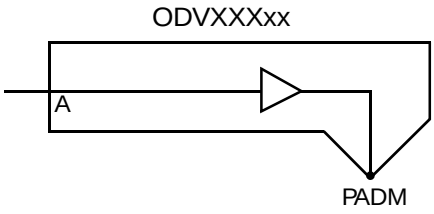
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell						
			ODVXXN01	**ODVXXN02**	**ODVXXN04**	**ODVXXN08**	**ODVXXN12**	**ODVXXN16**	**ODVXXN24**
A	PADM	t_{HZ}	0.138	0.166	0.229	0.214	0.263	0.255	0.317

Description

ODVXXXxx is a family of 1 to 24 mA, non-inverting, LVTTL-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODVXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODVXXX01	ODVXXX02	ODVXXX04	ODVXXX08	ODVXXX12	ODVXXX16	ODVXXX24
A (eq-load)	5.2	5.2	8.0	10.7	10.7	10.7	10.7

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXXX01	1	98.486	197.1
ODVXXX02	2	98.486	202.8
ODVXXX04	4	100.694	214.2
ODVXXX08	8	102.903	238.2
ODVXXX12	12	102.903	259.6
ODVXXX16	16	102.903	283.9
ODVXXX24	24	102.903	300.2

a. See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Propagation Delays (ns)

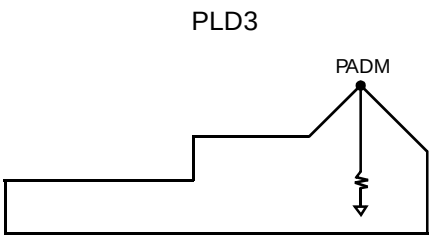
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.519 3.258	5.350 4.899	7.180 6.557	9.929 9.066	14.534 13.289
ODVXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.912 1.812	5.061 4.750	7.333 6.846	9.617 8.933	14.213 13.085
ODVXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.994 0.987	2.588 2.461	4.874 4.562	9.453 8.715	14.024 12.908
ODVXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.614 0.632	1.422 1.356	2.582 2.374	4.888 4.414	7.201 6.465
ODVXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.514 0.600	1.051 1.088	1.809 1.754	3.300 3.115	4.829 4.459
ODVXXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.519 0.641	0.938 1.010	1.530 1.521	2.706 2.552	3.896 3.566
ODVXXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.581 0.543	0.986 0.850	1.565 1.221	2.747 1.904	3.925 2.594

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
	N/A	N/A

HDL Syntax

Verilog ..... PLD3 *inst_name* (PADM);

VHDL..... *inst_name*: PLD3 port map (PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.677	nA
EQL_{pd}	184.7	Eq-load

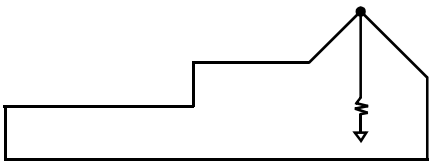
See page 2-13 for power equation.

PLDT

AMI350XXPE 0.35 micron CMOS Pad Library

Description

PLDT is a 5-volt tolerant active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLDT PADM 	N/A	N/A

HDL Syntax

Verilog ..... PLDT *inst_name* (PADM);

VHDL..... *inst_name*: PLDT port map (PADM);

Power Characteristics

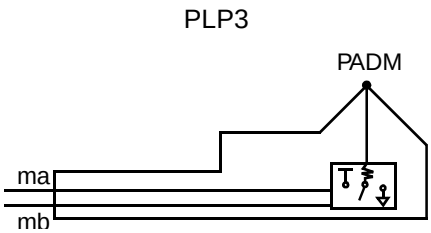
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.451	nA
EQL_{pd}	169.1	Eq-load

See page 2-13 for power equation.

Description

PLP3 is a programmable pull-up/pull-down buffer piece.

Logic Symbol



Truth Table

MA	MB	PADM Function
L	L	Pull-down
H	H	Pull-up
H	L	Tristate
L	H	Tristate

Pin Loading

	Load
MA	2.0 eql
MB	2.5 eql

HDL Syntax

Verilog ..... PLP3 *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLP3 port map (PADM, MA, MB);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.677	nA
EQL_{pd}	186.0	Eq-load

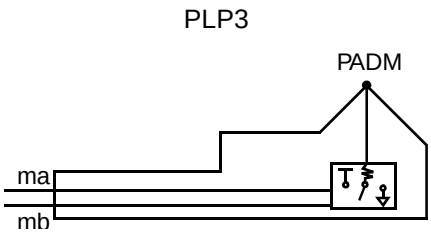
See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

PLPT is a programmable pull-up/pull-down buffer piece for use in 5 volt tolerant applications.

Logic Symbol



Truth Table

MA	MB	PADM Function
L	L	Pull-down
H	H	Pull-up
H	L	Tristate
L	H	Tristate

Pin Loading

	Load
MA	1.5 eql
MB	1.4 eql

HDL Syntax

Verilog ..... PLPT *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLPT port map (PADM, MA, MB);

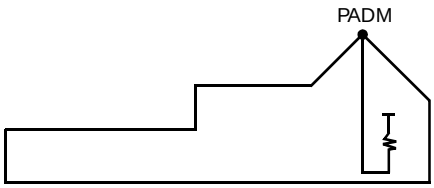
Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.052	nA
EQL_{pd}	175.6	Eq-load

See page 2-13 for power equation.

Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLU3 PADM 	N/A	N/A

HDL Syntax

Verilog ..... PLU3 *inst_name* (PADM);

VHDL..... *inst_name*: PLU3 port map (PADM);

Power Characteristics

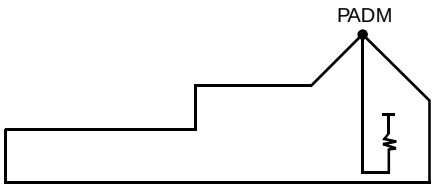
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.677	nA
EQL_{pd}	189.4	Eq-load

See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

PLUT is a 5-volt tolerant active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLUT  	N/A	N/A

HDL Syntax

Verilog ..... PLUT *inst_name* (PADM);

VHDL..... *inst_name*: PLUT port map (PADM);

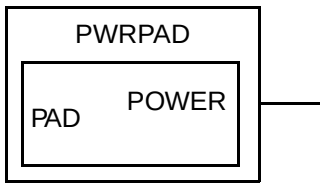
Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.707	nA
EQL_{pd}	165.1	Eq-load

See page 2-13 for power equation.

Description

PWRPAD is a generic power pad used to define the connection of a chip power pin to logical buses in the device. For more information on power and ground buses, as well as PWRPAD usage see “Interconnect Load Estimation” on page 2-15.



PWRPAD has the following parameters:

- LVDD: this parameter receives a string value that defines the name of the power supply that PWRPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that PWRPAD connects to.

Verilog Syntax

```
defparam SUPPLY_3.3V.LVDD = "PAD_3.3",
         SUPPLY_3.3.CONTACT = "IPWR,OPWR1";
PWRPAD SUPPLY_3.3 (.PADM(VDD_3.3));
```

VHDL syntax

```
SUPPLY_3.3 : PWRPAD generic map (LVDD => "PAD_3.3", CONTACT => "IPWR,OPWR1")
         port map (PADM => VDD_3.3);
```

Bolt syntax

```
PWRPAD/SUPPLY_3.3 VDD_3.3 (LVDD='PAD_3.3' CONTACT="IPWR,OPWR1");
```

where:

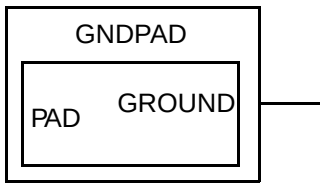
- SUPPLY_3.3 is the instance name for PWRPAD
- PAD_3.3 is the name of the supply
- IPWR, OPWR1 are logical buses
- VDD_3.3 is the chip port name

GNDPAD

AMI350XXPE 0.35 micron CMOS Pad Library

Description

GNDPAD is a generic ground pad used to define the connection of a chip ground pin to logical buses in the device. For more information on power and ground buses, as well as GNDPAD usage see “Interconnect Load Estimation” on page 2-15.



GNDPAD has the following parameters:

- LVSS: this parameter receives a string value that defines the name of the ground that GNDPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that GNDPAD connects to.

Verilog syntax

```
defparam GROUND1.LVSS = "VSS",
         GROUND1.CONTACT = "CGND,OGND";
GNDPAD GROUND1 (.PADM(VSS1));
```

VHDL syntax

```
GROUND1 : GNDPAD generic map (LVSS => "VSS", CONTACT => "CGND,OGND")
         port map (PADM => VSS1);
```

Bolt syntax

```
.GNDPAD/GROUND1 VSS1 (LVSS='VSS' CONTACT="CGND,OGND");
```

where:

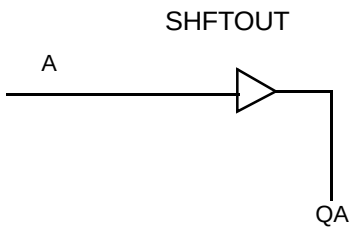
- GROUND1 is the instance name for GNDPAD
- VSS is the name of the supply
- CGND,OGND are logical buses

VSS1 is the chip port name

Description

SHFTOUT is a mixed voltage single output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol



Truth Table

A	QA
L	L
H	H

Pin Loading

	Load
A	5.3

HDL Syntax

Verilog ..... SHFTOUT *inst_name* (QA, A);

VHDL..... *inst_name*: SHFTOUT port map (QA, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.990	nA
EQL_{pd}	9.9	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 2.5V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	6	12	17	23 (max)
A	QA	t_{PLH} t_{PHL}	0.117 0.097	0.160 0.131	0.209 0.166	0.249 0.193	0.296 0.225

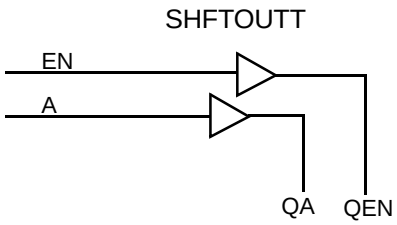
SHFTOUTT

AMI350XXPE 0.35 micron CMOS Pad Library

Description

SHFTOUTT is a mixed voltage dual output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol



Truth Table

A	EN	QA	QEN
L	X	L	X
H	X	H	X
X	L	X	L
X	H	X	H

Pin Loading

	Load
A(eql)	3.8
EN(eql)	4.1

HDL Syntax

Verilog ..... SHFTOUTT *inst_name* (QA, QEN, A, EN);

VHDL..... *inst_name*: SHFTOUTT port map (QA, QEN, A, EN);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.990	nA
EQL_{pd}	11.1	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 2.5V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	10	13 (max)
A	QA	t_{PLH} t_{PHL}	0.126 0.183	0.159 0.254	0.205 0.358	0.264 0.495	0.307 0.595
EN	QEN	t_{PLH} t_{PHL}	0.139 0.189	0.172 0.260	0.217 0.362	0.277 0.493	0.323 0.590