0.35 Micron CMOS Pad Library Datasheets
AMI350XXPE 3.3/5.0 Volt
Section 4

AMI350XXPE 0.35 micron CMOS Pad Library

Input Drive Pieces

Pull Pieces

Pad Selection Guide

AMI350XXPE 0.35 micron CMOS Pad Library

Output Drive Pieces

DATASHEETS

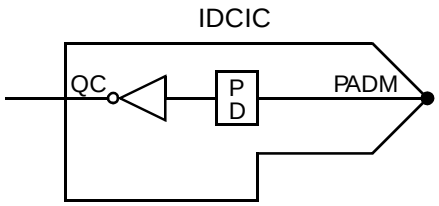
IDCIC

AMI350XXPE 0.35 micron CMOS Pad Library

Description

IDCIC is an inverting 5 volt capable (cascode-gate), CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDCIC *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCIC port map (QC, PADM);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	10.201	nA
EQL_{pd}	28.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

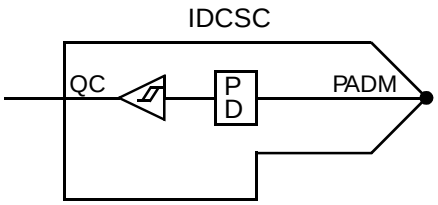
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	18	36	54	72 (max)
PADM	QC	t_{PLH} t_{PHL}	0.672 2.136	0.747 2.180	0.807 2.208	0.857 2.234	0.904 2.258

Description

IDCSC is a 5 volt cascoded-gate non-inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDCSC *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCSC port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.930	nA
EQL_{pd}	36.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	18	36	54	72 (max)
PADM	QC	t_{PLH} t_{PHL}	4.651 0.891	4.678 0.963	4.698 1.015	4.717 1.057	4.736 1.092

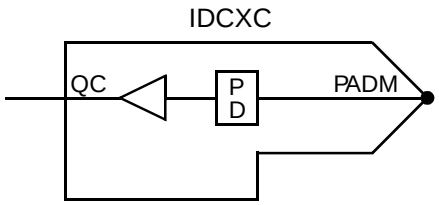
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

IDCXC is a 5 volt cascoded-gate non-inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDCXC *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCXC port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.929	nA
EQL_{pd}	31.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} =5.0V, Typical Process

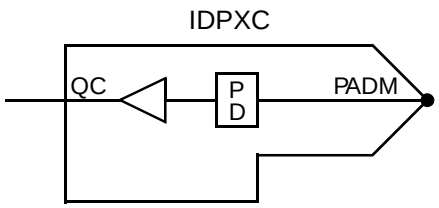
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	18	36	54	72 (max)
PADM	QC	t_{PLH} t_{PHL}	2.133 0.665	2.173 0.750	2.206 0.801	2.235 0.838	2.262 0.870

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDPXC is a 5 volt capable (cascode-gate) non-inverting, 33MHz PCI-level input buffer piece to be used in conjunction with 33MHz PCI ODPSCE33 piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDPXC *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPXC port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.558	nA
EQL_{pd}	26.9	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	18	36	54	72 (max)
PADM	QC	t_{PLH} t_{PHL}	0.521 0.509	0.605 0.619	0.686 0.685	0.751 0.733	0.801 0.771

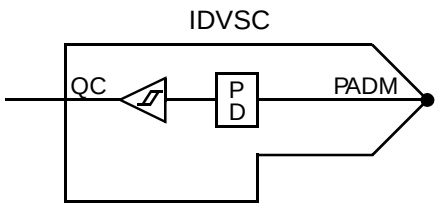
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

IDVSC is a 5-volt capable (cascode-gate) non-inverting, LVTTL-level Schmitt input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDVSC inst_IDVSC (QC, PADM);

VHDL..... inst_IDVSC : IDVSC port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.781	nA
EQL_{pd}	27.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = V, Typical Process

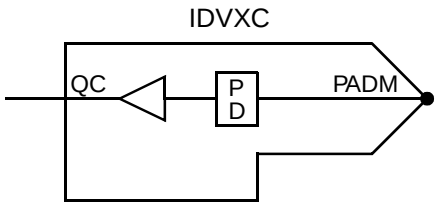
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	18	36	54	72 (max)
PADM	QC	t_{PLH} t_{PHL}	1.118 1.055	1.200 1.083	1.240 1.137	1.273 1.208	1.305 1.292

Delay will vary with input conditions. See page 2-15 for interconnect estimates

Description

IDVXC is a 5-volt capable (cascode-gate) non-inverting, TTL-level input buffer piece

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.76 pF

HDL Syntax

Verilog ..... IDVXC inst_IDVXC (QC, PADM);

VHDL..... inst_IDVXC : IDVXC port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.558	nA
EQL_{pd}	25.9	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	19	28	38 (max)
PADM	QC	t_{PLH} t_{PHL}	0.637 0.479	0.685 0.534	0.710 0.566	0.730 0.592	0.749 0.617

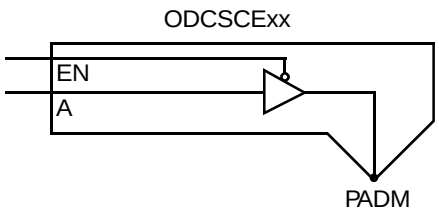
Delay will vary with input conditions. See page 2-15 for interconnect estimates

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCSCExx is a family of 4 to 12 mA, 5-volt capable (cascode-gate), non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSCExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSCExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODCSCE04	ODCSCE08	ODCSCE12
A (eq-load)	3.5	3.5	3.5
EN (eq-load)	3.4	3.4	3.4
PADM (pF)	4.82	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSCE04	4	108.464	477.3
ODCSCE08	8	108.464	522.7
ODCSCE12	12	108.464	543.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSCE04	From: A To: PADM	t_{PLH} t_{PHL}	5.159 3.951	7.638 5.755	11.140 7.671	18.080 11.371	25.037 15.278
	From: EN To: PADM	t_{ZH} t_{ZL}	5.264 2.652	7.686 4.295	11.182 6.289	18.064 10.062	25.026 13.833
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSCE08	From: A To: PADM	t_{PLH} t_{PHL}	4.560 3.313	5.941 4.436	7.667 5.719	11.059 7.793	14.600 9.525
	From: EN To: PADM	t_{ZH} t_{ZL}	4.310 2.023	5.785 3.175	7.701 4.359	11.190 6.377	14.432 8.280
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSCE12	From: A To: PADM	t_{PLH} t_{PHL}	4.244 3.114	5.885 4.057	7.668 5.133	10.943 6.749	14.711 7.922
	From: EN To: PADM	t_{ZH} t_{ZL}	4.327 1.799	5.737 2.777	7.637 3.784	11.187 5.333	14.513 6.597

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ODCSCE04	ODCSCE08	ODCSCE12
EN	PADM	t_{HZ} t_{LZ}	1.400 1.122	1.513 1.315	1.512 1.516

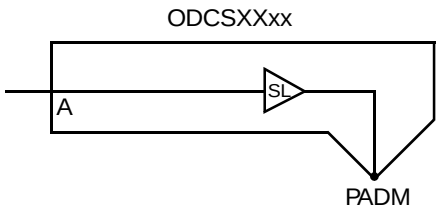
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCSCXxx is a family of 4 to 12 mA, non-inverting, 5-volt capable (cascode-gate), CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSCXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSCXxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCSCX04	ODCSCX08	ODCSCX12
A (eq-load)	4.5	4.5	4.5

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSCX04	4	106.975	468.8
ODCSCX08	8	106.975	514.2
ODCSCX12	12	106.975	535.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

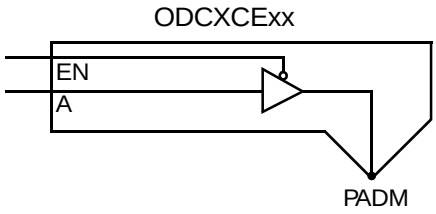
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSCX04	From: A To: PADM	t_{PLH} t_{PHL}	5.016 3.905	7.525 5.516	11.078 7.457	18.054 11.302	24.903 14.989
ODCSCX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.131 3.484	5.671 4.431	7.529 5.582	10.829 7.631	14.484 9.501
ODCSCX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.207 3.135	5.638 4.081	7.449 5.129	10.910 6.586	14.417 7.951

AMI350XXPE 0.35 micron CMOS Pad Library

Description

ODCXCExx is a family of 1 to 12 mA, 5-volt capable (cascode-gate), non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXCExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXCExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODCXCE01	ODCXCE02	ODCXCE04	ODCXCE08	ODCXCE12
A (eq-load)	3.5	3.5	3.5	3.5	3.5
EN (eq-load)	3.4	3.4	3.4	3.4	3.4
PADM (pF)	4.82	4.82	4.82	4.82	4.82

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXCE01	1	110.671	332.8
ODCXCE02	2	110.671	345.0
ODCXCE04	4	110.671	369.1
ODCXCE08	8	110.671	414.5
ODCXCE12	12	110.671	435.4

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXCE01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	8.943 4.959	11.705 6.491	14.456 8.100	18.621 10.506	25.716 14.192
	From: EN To: PADM	t_{ZH} t_{ZL}	8.692 3.783	11.583 5.316	14.457 6.849	18.710 9.150	25.657 12.993
ODCXCE02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	5.761 3.480	10.404 6.168	13.822 8.076	17.305 9.988	24.407 13.839
	From: EN To: PADM	t_{ZH} t_{ZL}	5.577 2.049	10.591 4.826	14.081 6.730	17.528 8.626	24.332 12.491
ODCXCE04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	4.091 2.742	6.507 4.026	9.978 5.887	16.938 9.626	23.905 13.349
	From: EN To: PADM	t_{ZH} t_{ZL}	4.166 1.350	6.611 2.660	10.104 4.521	17.066 8.268	23.988 12.005
ODCXCE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	3.569 2.495	4.771 3.113	6.395 4.006	9.755 5.853	13.383 7.783
	From: EN To: PADM	t_{ZH} t_{ZL}	3.531 1.056	4.772 1.706	6.457 2.655	9.879 4.551	13.430 6.376
ODCXCE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	3.411 2.370	4.673 2.911	6.413 3.503	9.818 4.710	13.355 6.038
	From: EN To: PADM	t_{ZH} t_{ZL}	3.403 1.035	4.697 1.512	6.472 2.165	9.901 3.423	13.407 4.650

AMI350XXPE 0.35 micron CMOS Pad Library

Tristate Timing

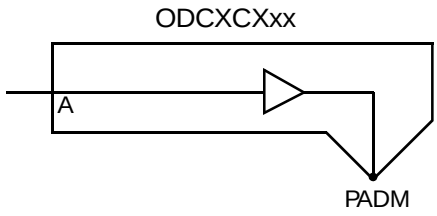
Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell				
			ODCXCE01	ODCXCE02	ODCXCE04	ODCXCE08	ODCXCE12
EN	PADM	t_{HZ} t_{LZ}	1.213 0.419	1.240 0.479	1.287 0.594	1.380 0.781	1.380 0.977

Description

ODCXCXxx is a family of 1 to 12 mA, 5-volt capable (cascode-gate), non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXCXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXCXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCXCX01	ODCXCX02	ODCXCX04	ODCXCX08	ODCXCX12
A (eq-load)	4.4	4.4	4.4	4.4	4.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXCX01	1	109.182	326.8
ODCXCX02	2	109.182	339.0
ODCXCX04	4	109.182	363.1
ODCXCX08	8	109.182	408.5
ODCXCX12	12	109.182	429.4

a. See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXCX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	8.536 5.283	11.378 6.775	14.253 8.280	18.543 10.568	25.500 14.449
ODCXCX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	5.389 3.320	10.309 6.165	13.776 8.139	17.220 10.053	24.061 13.743
ODCXCX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.999 2.578	6.422 3.920	9.820 5.809	16.721 9.542	23.762 13.242
ODCXCX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.254 2.315	4.557 3.001	6.244 3.953	9.616 5.813	13.239 7.641
ODCXCX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.372 2.192	4.509 2.693	6.172 3.326	9.719 4.567	13.111 5.813

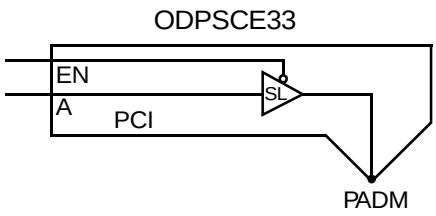
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODPSCE33 is a 33 MHz, 3.3v/ 5.0v, PCI Rev 2.1 compliant, 3V/5V -capable drive.

NOTE: ODPSCE33 is not 5V tolerant.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	3.5 eql
EN	3.4 eql
PADM	4.82 pF

HDL Syntax

Verilog ..... ODPSCE33 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODPSCE33 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	108.464	nA
EQL_{pd}	423.8	Eq-load

See page 2-13 for power equation.

AMI350XXPE 0.35 micron CMOS Pad Library

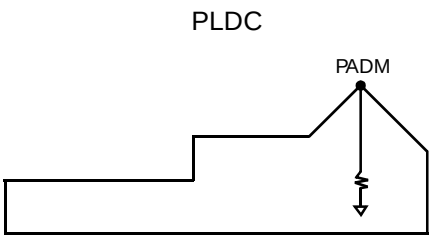
Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	3.556 2.668	4.352 3.600	5.378 4.859	7.268 7.275	9.043 9.718
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.755 1.383 3.674 2.154	4.372 3.208	5.395 4.559	7.336 7.042	9.156 9.371

Description

PLDC is a 5-volt capable (cascode-gate) active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
	N/A	N/A

HDL Syntax

Verilog ..... PLDC *inst_name* (PADM);

VHDL..... *inst_name*: PLDC port map (PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.446	nA
EQL_{pd}	179.2	Eq-load

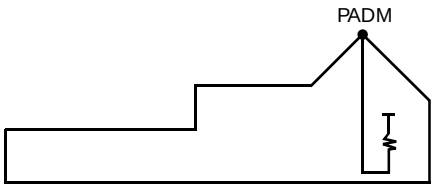
See page 2-13 for power equation.

PLUC

AMI350XXPE 0.35 micron CMOS Pad Library

Description

PLUC is a 5-volt capable (cascode-gate) active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLUC PADM 	N/A	N/A

HDL Syntax

Verilog ..... PLUC *inst_name* (PADM);

VHDL..... *inst_name*: PLUC port map (PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.713	nA
EQL_{pd}	175.1	Eq-load

See page 2-13 for power equation.