0.35 Micron CMOS Pad Library Datasheets
AMI350XXPR 3.3/5.0 Volt
Section 4

DATASHEETS

Input Drive Pieces

Pull Pieces

Output Drive Pieces

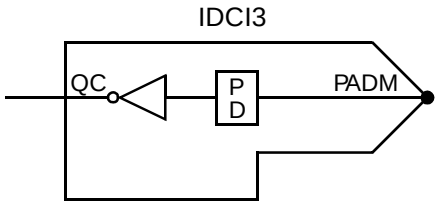
Power Pad Cells

Special Pad Cells

Description

IDCI3 is an inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	4.70 pF

HDL Syntax

Verilog ..... IDCI3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCI3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.810	nA
EQL_{pd}	10.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.410 0.471	0.494 0.546	0.589 0.624	0.678 0.696	0.754 0.757

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

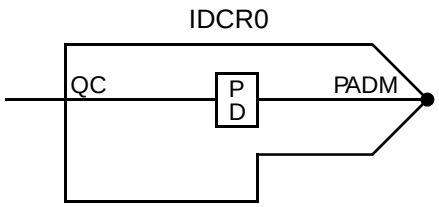
IDCR0

AMI350XXPR 0.35 micron CMOS Pad Library

Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.70 pF

HDL Syntax

Verilog ..... IDCR0 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCR0 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.090	nA
EQL_{pd}	1.9	Eq-load

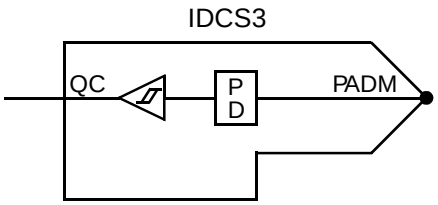
See page 2-13 for power equation.

Note: This special purpose, “resistive input” pad is not intended for use as a general input pad.

Description

IDCS3 is a non-inverting, CMOS-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.70 pF

HDL Syntax

Verilog ..... IDCS3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.571	nA
EQL_{pd}	14.1	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.936 0.860	1.041 0.956	1.125 1.041	1.190 1.106	1.239 1.154

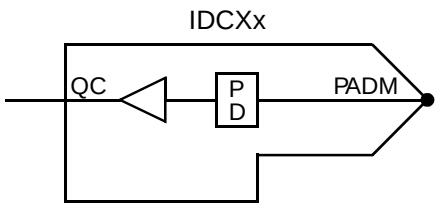
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPR 0.35 micron CMOS Pad Library

Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDCXx *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDCXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	4.70	4.70

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCX3	1.0	3.946	8.5
IDCX6	1.0	7.643	14.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

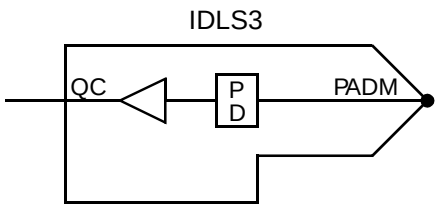
IDCX3	Number of Equivalent Loads		1	10	21	32	42 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.410 0.357	0.519 0.470	0.604 0.554	0.683 0.631	0.757 0.701
IDCX6	Number of Equivalent Loads		1	20	40	60	80 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.362 0.300	0.504 0.455	0.599 0.544	0.669 0.612	0.723 0.673

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDLS3 is a non-inverting, low power, SCSI-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.70 pF

HDL Syntax

Verilog ..... IDLS3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDLS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	18.759	nA
EQL_{pd}	18.4	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	19	28	38 (max)
PADM	QC	t_{PLH} t_{PHL}	3.84 5.38	3.90 5.39	4.00 5.42	4.11 5.49	4.27 5.62

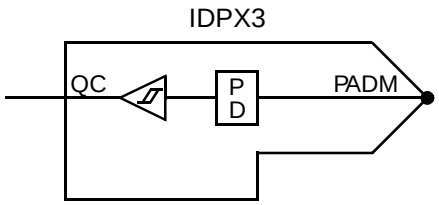
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPR 0.35 micron CMOS Pad Library

Description

IDPXx is a family of non-inverting, PCI-level input buffer pieces. IDPX3 is for the 33MHz PCI ODPSXE16 piece whereas IDPX6 is for the 66MHz PCI ODPHXE16 piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDPX3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDPX3 port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDPX3	IDPX6
PADM (pF)	4.70	4.70

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDPX3	1.0	3.738	9.2
IDPX6	1.0	7.771	15.7

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

IDPX3	**Number of Equivalent Loads**		**1**	**10**	**21**	**32**	**42 (max)**
	From: PADM To: QC	t_{PLH} t_{PHL}	0.385 0.379	0.479 0.473	0.576 0.556	0.666 0.625	0.743 0.680
IDPX6	**Number of Equivalent Loads**		**1**	**20**	**40**	**60**	**80 (max)**
	From: PADM To: QC	t_{PLH} t_{PHL}	0.370 0.356	0.488 0.454	0.571 0.512	0.641 0.575	0.704 0.633

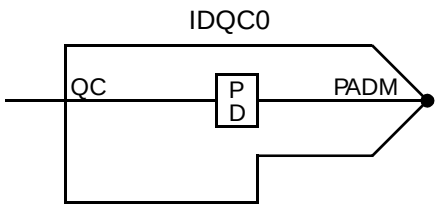
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPR 0.35 micron CMOS Pad Library

Description

IDQC0 is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol



Truth Table

PADM	QO
L	L
H	H

Pin Loading

	Load
PADM	4.70 pF

HDL Syntax

Verilog ..... IDQC0 *inst_name* (QO, PADM);

VHDL..... *inst_name*: IDQC0 port map (QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	0.090	nA
EQL_{pd}	1.8	Eq-load

See page 2-13 for power equation.

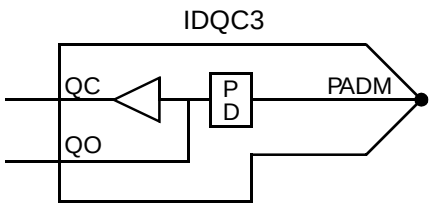
Design Notes:

The IDQC0 cell is for backward compatibility with existing oscillator methodologies.

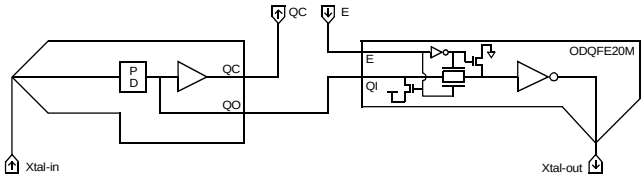
Description

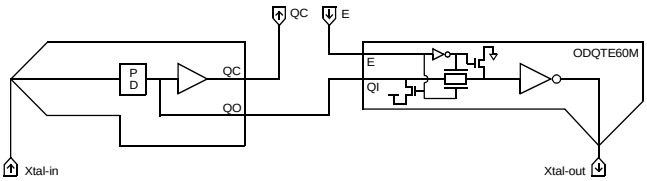
IDQC3 is a crystal oscillator input receiver pad piece with a non-inverting, CMOS-level clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

Logic Symbol



The Possible Logic Schematic Combinations





Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.70 pF

Pad Logic

HDL Syntax

Verilog ..... IDQC3 *inst_name (*QC, QO, PADM);

VHDL..... *inst_name*: IDQC3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	5.674	nA
EQL_{pd}	9.6	Eq-load

See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.417 0.468	0.499 0.560	0.561 0.638	0.621 0.704	0.676 0.758
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

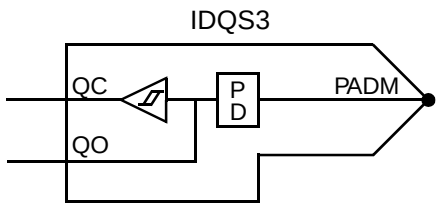
Design Notes:

The IDQC3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

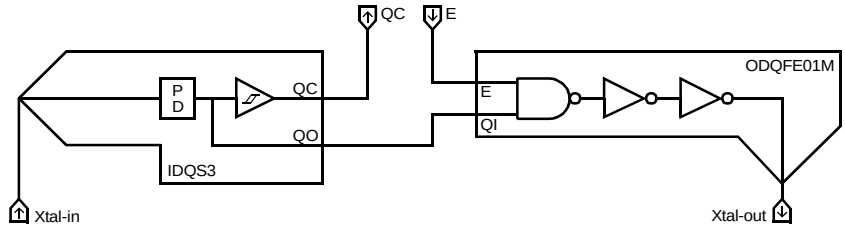
Description

IDQS3 is a crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS-level schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol



Logic Schematic



Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.70 pF

Pad Logic

HDL Syntax

Verilog ..... IDQS3 *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQS3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	9.755	nA
EQL_{pd}	15.1	Eq-load

See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.991 1.203	1.037 1.264	1.075 1.350	1.107 1.440	1.133 1.526
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

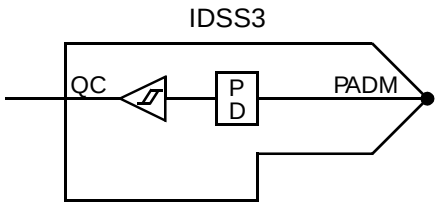
Design Notes:

The IDQS3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

Description

IDSS3 is a non-inverting, SCSI-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.70 pF

HDL Syntax

Verilog ..... IDSS3 *inst_name* (QC, PADM);

VHDL..... *inst_name*: IDSS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.747	nA
EQL_{pd}	16.8	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	1.103 1.365	1.200 1.487	1.296 1.635	1.382 1.766	1.457 1.866

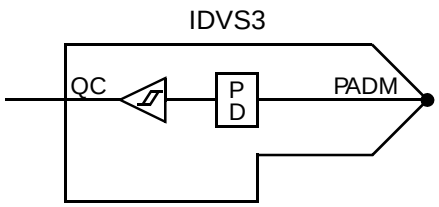
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPR 0.35 micron CMOS Pad Library

Description

IDVS3 is a non-inverting, LVTTL-level Schmitt input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.70 pF

HDL Syntax

Verilog ..... IDVS3 inst_IDVS3 (QC, PADM);

VHDL..... inst_IDVS3 : IDVS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	4.571	nA
EQL_{pd}	13.9	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

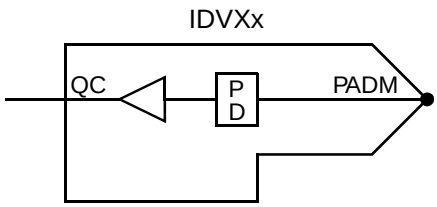
Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	10	21	32	42 (max)
PADM	QC	t_{PLH} t_{PHL}	0.653 0.729	0.761 0.826	0.857 0.921	0.940 1.007	1.009 1.081

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDVXx is a family of non-inverting, LVTTL-level, input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDVXx *inst_name (*QC, PADM);

VHDL..... *inst_name*: IDVXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	idvx3	idvx6
PADM (pF)	4.70	4.70

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
idvx3	1.0	3.706	8.5
idvx6	1.0	7.131	14.7

a. See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

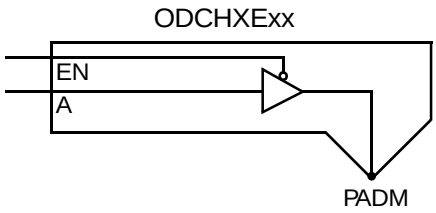
idvx3	**Number of Equivalent Loads**		**1**	**10**	**21**	**32**	**42 (max)**
	From: PADM To: QC	t_{PLH} t_{PHL}	0.358 0.386	0.471 0.467	0.568 0.544	0.653 0.617	0.726 0.684
idvx6	**Number of Equivalent Loads**		**1**	**20**	**40**	**60**	**80 (max)**
	From: PADM To: QC	t_{PLH} t_{PHL}	0.347 0.410	0.462 0.484	0.554 0.548	0.635 0.620	0.712 0.699

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCHXExx is a family of high performance, 8 to16 mA, non-inverting, CMOS-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCHXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCHXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODCHXE08	ODCHXE12	ODCHXE16
A (eq-load)	16.9	16.9	16.9
EN (eql)	12.3	12.3	12.3
PADM (pF)	4.70	4.71	4.71

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCHXE08	4	95.208	249.1
ODCHXE12	12	95.208	269.9
ODCHXE16	16	95.208	290.9

a. See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCHXE08	From: A To: PADM	t_{PLH} t_{PHL}	0.733 0.587	1.662 1.184	3.009 2.046	5.725 3.760	8.430 5.446
	From: EN To: PADM	t_{ZH} t_{ZL}	0.803 0.610	1.768 1.226	3.126 2.071	5.814 3.764	8.551 5.481
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCHXE12	From: A To: PADM	t_{PLH} t_{PHL}	0.571 0.659	1.201 0.955	2.102 1.502	3.905 2.646	5.707 3.755
	From: EN To: PADM	t_{ZH} t_{ZL}	0.667 0.514	1.296 0.952	2.205 1.539	4.019 2.647	5.816 3.782
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCHXE16	From: A To: PADM	t_{PLH} t_{PHL}	0.561 0.534	1.038 0.852	1.717 1.287	3.072 2.137	4.424 2.971
	From: EN To: PADM	t_{ZH} t_{ZL}	0.605 0.534	1.088 0.867	1.776 1.304	3.135 2.152	4.466 2.993

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

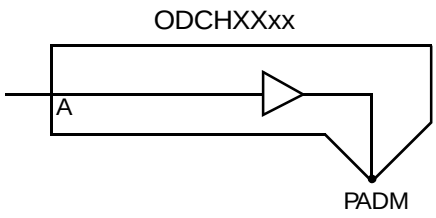
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell ODCHXE08	ODCHXE12	ODCHXE16
EN	PADM	t_{HZ} t_{LZ}	0.666 0.244	0.809 0.294	0.956 0.342

Description

ODCHXXxx is a family of high performance, 8 to 16 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCHXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCHXXxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODCHXX08	ODCHXX12	ODCHXX16
A (eq-load)	18.2	18.4	18.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCHXX08	4	92.611	230.4
ODCHXX12	12	92.611	251.0
ODCHXX16	16	92.611	272.0

a. See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Output Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

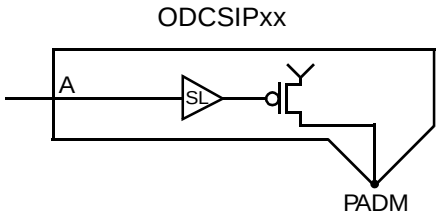
ODCHXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.665	1.613	2.968	5.679	8.390
	To: PADM	t_{PHL}	0.496	1.112	1.964	3.644	5.366
ODCHXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.665	1.613	2.968	5.679	8.390
	To: PADM	t_{PHL}	0.496	1.112	1.964	3.644	5.366
ODCHXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.453	0.922	1.597	2.943	4.282
	To: PADM	t_{PHL}	0.414	0.733	1.150	1.993	2.858

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCSIPxx is a family of 4 to 16 mA, inverting, CMOS-level output buffer pieces with P-channel open-drains (pull-up) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCSIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSIPxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODCSIP04	ODCSIP08	ODCSIP12	ODCSIP16
A (eq-load)	4.6	4.6	4.6	4.6
PADM (pF)	4.70	4.70	4.70	4.70

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSIP04	4	105.573	232.0
ODCSIP08	8	105.573	242.7
ODCSIP12	12	105.573	253.4
ODCSIP16	16	105.573	264.9

a. See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCSIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.491	6.332	11.769	22.688	33.598
ODCSIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.375	3.295	6.009	11.421	16.880
ODCSIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.018	2.299	4.105	7.706	11.341
ODCSIP16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	0.938	1.850	3.184	5.937	8.603

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

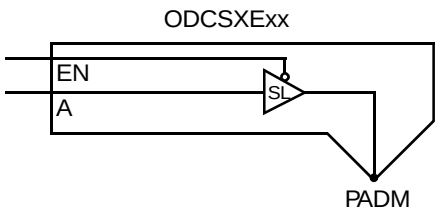
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns)		Parameter	Cell			
From	**To**		**ODCSIP04**	**ODCSIP08**	**ODCSIP12**	**ODCSIP16**
A	PADM	t_{HZ}	0.434	0.402	0.455	0.513

Description

ODCSXExx is a family of 4 to 16 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load			
	ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16
A (eq-load)	2.7	2.7	2.7	2.7
EN (eq-load)	8.7	8.7	8.7	8.7
PADM (pF)	4.70	4.70	4.70	4.70

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXE04	4	108.888	266.9
ODCSXE08	8	108.888	286.7
ODCSXE12	12	108.888	307.1
ODCSXE16	16	108.888	327.6

a. See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXE04	From: A To: PADM	t_{PLH} t_{PHL}	3.006 1.902	6.407 4.314	11.080 7.758	20.578 14.616	29.831 21.494
	From: EN To: PADM	t_{ZH} t_{ZL}	2.648 1.802	6.171 4.213	10.983 7.683	20.396 14.527	29.689 21.416
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.647 1.317	3.614 2.489	6.179 4.185	10.915 7.610	15.611 11.061
	From: EN To: PADM	t_{ZH} t_{ZL}	1.588 1.149	3.483 2.351	5.984 4.056	10.768 7.475	15.432 10.892
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE12	From: A To: PADM	t_{PLH} t_{PHL}	1.345 1.079	2.655 1.884	4.444 3.048	7.761 5.325	10.860 7.546
	From: EN To: PADM	t_{ZH} t_{ZL}	1.199 0.986	2.504 1.792	4.275 2.933	7.583 5.196	10.701 7.447
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.155 1.033	1.916 1.639	3.049 2.502	5.343 4.216	7.569 5.910
	From: EN To: PADM	t_{ZH} t_{ZL}	0.973 0.904	1.768 1.509	2.897 2.396	5.149 4.131	7.412 5.777

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

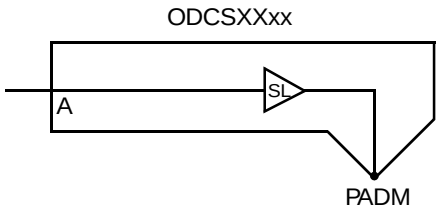
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16
EN	PADM	t_{HZ} t_{LZ}	0.363 0.484	0.417 0.538	0.468 0.592	0.525 0.642

Description

ODCSXXxx is a family of 4 to 16 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODCSXX04	ODCSXX08	ODCSXX12	ODCSXX16
A (eq-load)	11.3	11.3	11.3	11.3

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXX04	4	100.389	241.2
ODCSXX08	8	100.389	261.0
ODCSXX12	12	100.389	281.4
ODCSXX16	16	100.389	301.9

a. See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

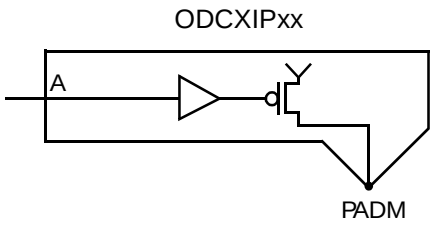
ODCSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.342 1.502	6.094 3.932	11.273 7.388	21.457 14.233	31.590 21.118
ODCSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.167 0.909	3.132 2.097	5.863 3.800	11.090 7.215	16.122 10.631
ODCSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.965 0.729	2.200 1.512	4.000 2.636	7.560 4.894	11.028 7.154
ODCSXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.764 0.663	1.679 1.261	3.011 2.117	5.711 3.811	8.388 5.517

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCXIPxx is a family of 1 to 16 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCXIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXIPxx port map (PADM, A);

Pin Loading

Pin Name	Load					
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12	ODCXIP16
A (eq-load)	3.1	3.1	3.1	4.5	5.9	5.9
PADM (pF)	4.70	4.70	4.70	4.70	4.71	4.71

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXIP01	1	79.650	187.7
ODCXIP02	2	80.946	192.2
ODCXIP04	4	82.243	199.8
ODCXIP08	8	84.835	213.8
ODCXIP12	12	88.724	229.3
ODCXIP16	16	88.724	240.8

a. See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXIP01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{ZH}	4.610	6.811	9.003	12.295	17.826
ODCXIP02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZH}	2.230	6.107	8.851	11.579	17.002
ODCXIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.352	3.256	6.004	11.426	16.876
ODCXIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	0.800	1.748	3.093	5.817	8.517
ODCXIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	0.600	1.233	2.146	3.957	5.751
ODCXIP16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	0.547	1.020	1.699	3.060	4.406

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

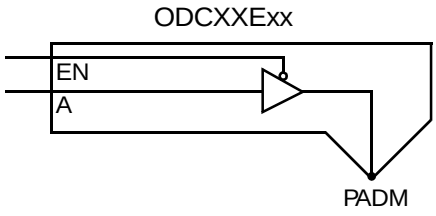
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell					
			ODCXIP01	**ODCXIP02**	**ODCXIP04**	**ODCXIP08**	**ODCXIP12**	**ODCXIP16**
A	PADM	t_{HZ}	0.425	0.370	0.406	0.437	0.427	0.504

Description

ODCXXExx is a family of 1 to 16 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load					
	ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16
A (eq-load)	6.6	9.5	9.5	2.6	2.6	2.6
EN (eq-load)	4.7	6.3	6.3	6.5	6.5	6.5
PADM (pF)	4.70	4.70	4.70	4.70	4.71	4.71

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXE01	1	82.962	194.9
ODCXXE02	2	86.468	204.8
ODCXXE04	4	86.468	215.2
ODCXXE08	8	102.215	267.5
ODCXXE12	12	102.215	288.2
ODCXXE16	16	102.215	309.3

a. See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXXE01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.602 3.144	6.760 4.509	8.935 5.857	12.234 7.891	17.813 11.375
	From: EN To: PADM	t_{ZH} t_{ZL}	4.685 3.094	6.888 4.495	9.087 5.864	12.387 7.906	17.905 11.360
ODCXXE02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.401 1.613	6.162 4.038	8.867 5.770	11.597 7.490	17.121 10.892
	From: EN To: PADM	t_{ZH} t_{ZL}	2.458 1.661	6.281 4.102	9.012 5.823	11.743 7.535	17.205 10.937
ODCXXE04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.278 1.080	3.187 2.289	5.910 4.002	11.343 7.443	16.784 10.871
	From: EN To: PADM	t_{ZH} t_{ZL}	1.403 1.064	3.306 2.311	6.035 4.049	11.474 7.442	16.903 10.918
ODCXXE08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.147 0.868	2.086 1.464	3.407 2.309	6.105 4.010	8.862 5.724
	From: EN To: PADM	t_{ZH} t_{ZL}	0.952 0.764	1.905 1.395	3.275 2.240	5.994 3.904	8.687 5.662
ODCXXE12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.963 0.832	1.593 1.209	2.498 1.755	4.311 2.882	6.111 4.036
	From: EN To: PADM	t_{ZH} t_{ZL}	0.823 0.692	1.444 1.106	2.354 1.674	4.179 2.801	5.957 3.936
ODCXXE16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.879 0.750	1.366 1.089	2.050 1.535	3.399 2.375	4.757 3.234
	From: EN To: PADM	t_{ZH} t_{ZL}	0.744 0.696	1.221 1.028	1.903 1.466	3.260 2.319	4.609 3.172

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

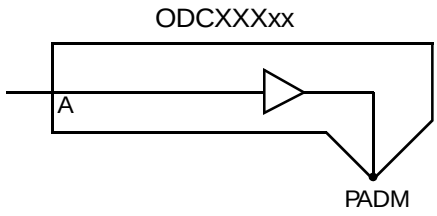
Delay (ns) From	To	Parameter	Cell					
			ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16
EN	PADM	t_{HZ}	0.647	0.528	0.652	0.395	0.452	0.512
		t_{LZ}	0.215	0.194	0.255	0.474	0.529	0.581

AMI350XXPR 0.35 micron CMOS Pad Library

Description

ODCXXXxx is a family of 1 to 16 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load					
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12	ODCXXX16
A (eq-load)	4.9	4.9	7.4	10.1	10.1	10.1

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXX01	1	79.649	188.6
ODCXXX02	2	79.649	193.8
ODCXXX04	4	82.241	204.4
ODCXXX08	8	84.834	226.6
ODCXXX12	12	84.834	247.3
ODCXXX16	16	84.834	268.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.516 2.974	6.755 4.356	8.969 5.735	12.255 7.800	17.672 11.236
ODCXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.336 1.658	6.158 4.062	8.897 5.780	11.632 7.496	17.079 10.928
ODCXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.199 0.913	3.130 2.119	5.847 3.855	11.283 7.275	16.716 10.718
ODCXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.728 0.605	1.688 1.213	3.042 2.068	5.730 3.768	8.468 5.474
ODCXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.599 0.570	1.224 0.973	2.122 1.548	3.927 2.690	5.729 3.791
ODCXXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.581 0.576	1.059 0.911	1.722 1.354	3.056 2.211	4.429 3.049

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

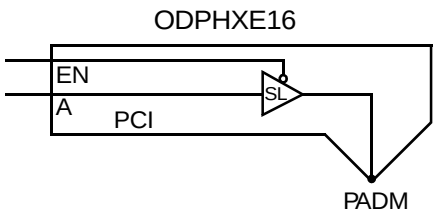
ODPHXE16

AMI350XXPR 0.35 micron CMOS Pad Library

Description

ODPHXE16 is a high performance, 33 and 66MHz PCI Rev 2.1 compliant, non-inverting, tristate buffer piece.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	4.1 eql
EN	3.0 eql
PADM	4.71 pF

HDL Syntax

Verilog ..... ODPHXE16 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODPHXE16 port map (PADM, A, EN);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	96.119	nA
EQL_{pd}	268.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

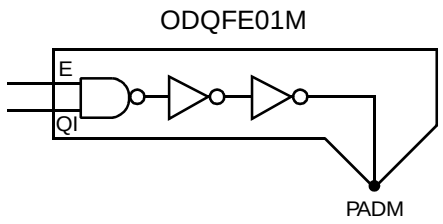
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	1.008 0.848	1.692 1.481	2.768 2.345	4.987 4.102	7.232 5.939
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.691 1.259 1.001 0.721	1.769 1.353	2.878 2.269	5.134 4.099	7.441 5.905

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

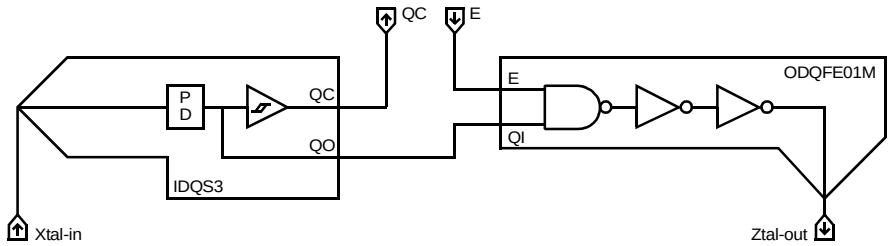
Description

ODQFE01M is a fundamental mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 32 kHz - 1 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
L	H	H
H	H	L
H	L	X

Pin Loading

	Load
E	4.5 eql
QI	3.4 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE01M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE01M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	81.729	nA
EQL_{pd}	191.4	Eq-load

See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	25	35	50	75 (max)
E	PADM	t_{PLH} t_{PHL}	4.753 3.469	6.928 4.845	9.096 6.221	12.377 8.283	17.960 11.710
QI	PADM	t_{PLH} t_{PHL}	4.719 3.430	6.900 4.755	9.097 6.106	12.413 8.168	17.976 11.679

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

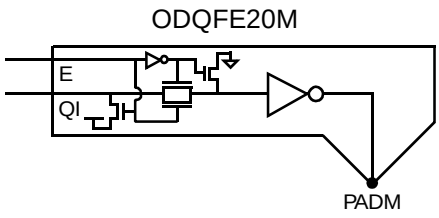
Design Notes:

The ODQFE01M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQS3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

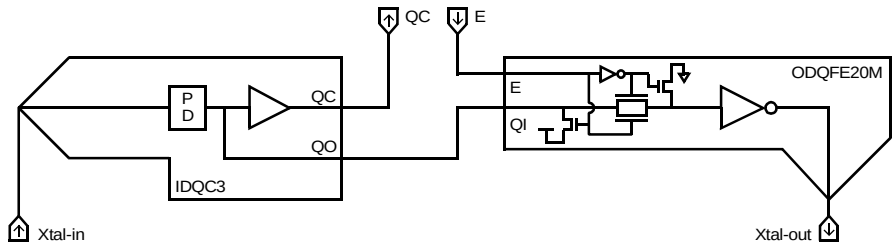
Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	7.8 eql
QI	6.1 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE20M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE20M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	79.653	nA
EQL_{pd}	206.8	Eq-load

See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
E	PADM	t_{PLH} t_{PHL}	2.818 1.569	6.603 3.959	9.331 5.677	12.071 7.397	17.576 10.826
QI	PADM	t_{PLH} t_{PHL}	2.272 1.616	6.090 4.021	8.834 5.741	11.570 7.462	16.995 10.905

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

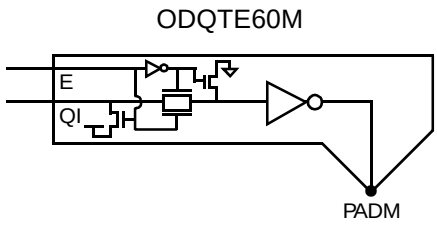
Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

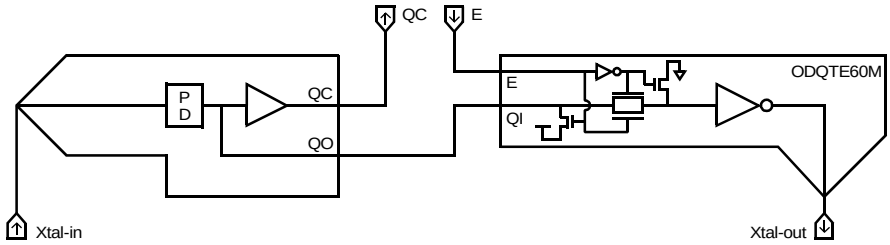
Description

ODQTE60M is an enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	7.8 eql
QI	6.1 eql

Pad Logic

HDL Syntax

Verilog ..... ODQTE60M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQTE60M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	79.653	nA
EQL_{pd}	217.2	Eq-load

See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
E	PADM	t_{PLH} t_{PHL}	1.857 0.974	3.756 2.132	6.472 3.834	11.907 7.281	17.342 10.705
QI	PADM	t_{PLH} t_{PHL}	1.266 0.994	3.177 2.213	5.879 3.926	11.296 7.343	16.727 10.763

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

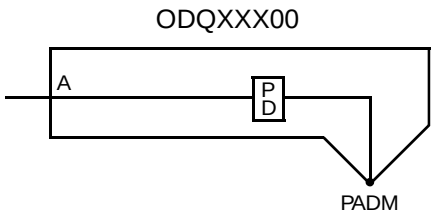
Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

Description

ODQXXX00 is a non-buffered, resistive analog crystal oscillator output pad piece with ESD protection.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	2.2 eql

HDL Syntax

Verilog ..... ODQXXX00 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODQXXX00 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	77.055	nA
EQL_{pd}	178.2	Eq-load

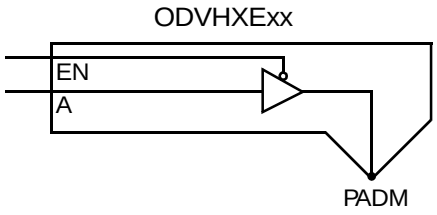
See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Description

ODVHXExx is a family of high performance, 8 to 16 mA, non-inverting, LVTTL-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVHXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVHXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load		
	ODVHXE08	ODVHXE12	ODVHXE16
A (eq-load)	16.9	16.9	16.9
EN (eql)	12.3	12.3	12.3
PADM (pF)	4.70	4.71	4.71

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVHXE08	4	95.208	249.1
ODVHXE12	12	95.208	269.9
ODVHXE16	16	95.208	290.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVHXE04	From: A To: PADM	t_{PLH} t_{PHL}	0.601 0.664	1.396 1.381	2.536 2.405	4.800 4.446	7.044 6.496
	From: EN To: PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.666 0.244 0.698 0.680	 1.482 1.404	 2.617 2.427	 4.879 4.470	 7.130 6.521
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVHXE12	From: A To: PADM	t_{PLH} t_{PHL}	0.519 0.602	1.047 1.076	1.797 1.748	3.298 3.096	4.801 4.449
	From: EN To: PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.809 0.294 0.599 0.559	 1.134 1.070	 1.882 1.762	 3.378 3.111	 4.891 4.465
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODVHXE16	From: A To: PADM	t_{PLH} t_{PHL}	0.502 0.578	0.880 0.963	1.428 1.482	2.559 2.478	3.677 3.515
	From: EN To: PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	0.956 0.342 0.565 0.585	 0.970 0.949	 1.538 1.468	 2.667 2.500	 3.789 3.511

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

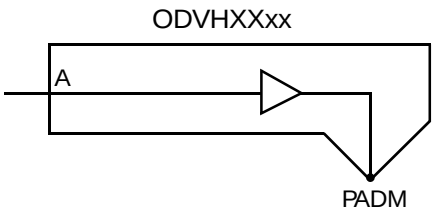
Delay (ns) From	To	Parameter	Cell ODVHXE08	ODVHXE12	ODVHXE16
EN	PADM	t_{HZ} t_{LZ}	0.666 0.244	0.809 0.294	0.956 0.342

AMI350XXPR 0.35 micron CMOS Pad Library

Description

ODVHXXxx is a family of high performance, 8 to16 mA, non-inverting, LVTTL-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODVHXXxx *inst_name* (PADM, A);
VHDL..... *inst_name*: ODVHXXxx port map (PADM, A);

Pin Loading

Pin Name	Load		
	ODVHXX08	ODVHXX12	ODVHXX16
A (eq-load)	18.4	18.4	18.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVHXX08	4	92.611	230.2
ODVHXX12	12	92.611	251.0
ODVHXX16	16	92.611	272.0

a. See page 2-13 for power equation.

Output Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVHXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.603 0.576	1.384 1.300	2.510 2.311	4.780 4.343	7.024 6.410
ODVHXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.603 0.576	1.384 1.300	2.510 2.311	4.780 4.343	7.024 6.410
ODVHXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.400 0.445	0.801 0.821	1.367 1.328	2.492 2.352	3.615 3.369

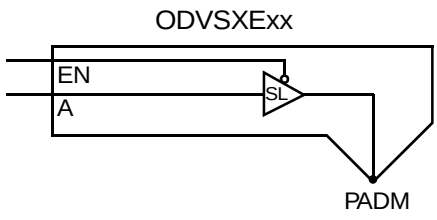
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPR 0.35 micron CMOS Pad Library

Description

ODVSXExx is a family of 4 to 16 mA, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODVSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load			
	ODVSXE04	ODVSXE08	ODVSXE12	ODVSXE16
A (eq-load)	2.7	2.7	2.7	2.7
EN (eq-load)	8.7	8.7	8.7	8.7
PADM (pF)	4.70	4.70	4.70	4.70

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSXE04	4	108.888	266.9
ODVSXE08	8	108.888	286.7
ODVSXE12	12	108.888	307.1
ODVSXE16	16	108.888	327.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVSXE04	From: A To: PADM	t_{PLH} t_{PHL}	2.390 2.217	5.604 5.092	10.064 9.208	18.688 17.454	27.070 25.679
	From: EN To: PADM	t_{ZH} t_{ZL}	2.252 2.067	5.453 4.949	9.895 9.071	18.513 17.307	26.908 25.540
ODVSXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.098 2.175	3.092 3.605	5.365 5.660	9.876 9.753	14.235 13.855
	From: EN To: PADM	t_{ZH} t_{ZL}	1.305 1.224	2.919 2.728	5.228 4.767	9.713 8.877	14.063 12.963
ODVSXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.212 1.197	2.318 2.133	3.788 3.485	6.849 6.207	9.805 8.911
	From: EN To: PADM	t_{ZH} t_{ZL}	1.091 1.046	2.154 2.023	3.669 3.367	6.669 6.092	9.692 8.794
ODVSXE16	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.131 1.131	1.923 1.835	3.053 2.860	5.310 4.938	7.568 6.940
	From: EN To: PADM	t_{ZH} t_{ZL}	0.968 0.976	1.768 1.701	2.901 2.721	5.144 4.769	7.417 6.812

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

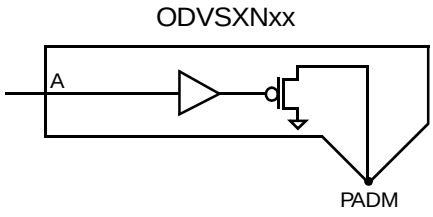
Delay (ns) From	To	Parameter	Cell ODVSXE04	ODVSXE08	ODVSXE12	ODVSXE16
EN	PADM	t_{HZ} t_{LZ}	0.363 0.484	0.417 0.538	0.468 0.592	0.525 0.642

AMI350XXPR 0.35 micron CMOS Pad Library

Description

ODVSXNxx is a family of 4 to 16 mA, non-inverting, LVTTL-level, output buffer pieces with N-channel open-drains (pull-down) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODVSXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVSXNxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODVSXN04	ODVSXN08	ODVSXN12	ODVSXN16
A (eq-load)	10.5	10.5	10.5	10.5
PADM (pF)	4.70	4.70	4.70	4.70

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSXN04	4	92.610	211.1
ODVSXN08	8	92.610	220.2
ODVSXN12	12	92.610	229.9
ODVSXN16	16	92.610	238.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVSXN04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.762	4.649	8.767	17.002	25.238
ODVSXN08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.899	2.383	4.445	8.531	12.640
ODVSXN12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.720	1.661	3.012	5.719	8.429
ODVSXN16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.583	1.308	2.336	4.381	6.418

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

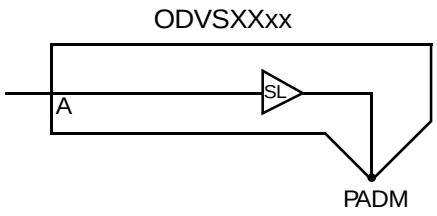
Delay (ns)		Parameter	Cell			
From	**To**		**ODVSXN04**	**ODVSXN08**	**ODVSXN12**	**ODVSXN16**
A	PADM	t_{LZ}	0.435	0.469	0.501	0.538

AMI350XXPR 0.35 micron CMOS Pad Library

Description

ODVSXXxx is a family of 4 to 16 mA, non-inverting, LVTTL-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODVSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODVSXX04	ODVSXX08	ODVSXX12	ODVSXX16
A (eq-load)	11.3	11.3	11.3	11.3

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVSXX04	4	100.389	241.2
ODVSXX08	8	100.389	261.0
ODVSXX12	12	100.389	281.4
ODVSXX16	16	100.389	301.9

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.954	5.098	9.629	18.731	27.815
	To: PADM	t_{PLH}	1.799	4.682	8.834	17.101	25.281
ODVSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.096	2.654	4.902	9.423	13.946
	To: PADM	t_{PLH}	1.054	2.489	4.534	8.617	12.728
ODVSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.838	1.854	3.347	6.363	9.360
	To: PADM	t_{PLH}	0.851	1.793	3.144	5.853	8.564
ODVSXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.702	1.468	2.595	4.854	7.104
	To: PADM	t_{PLH}	0.756	1.454	2.470	4.517	6.568

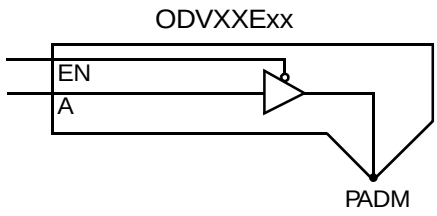
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPR 0.35 micron CMOS Pad Library

Description

ODVXXExx is a family of 1 to 16 mA, non-inverting, LVTTL-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODVXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODVXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load					
	ODVXXE01	ODVXXE02	ODVXXE04	ODVXXE08	ODVXXE12	ODVXXE16
A (eq-load)	6.6	9.5	9.5	2.6	2.6	2.6
EN (eq-load)	4.7	6.3	6.3	6.5	6.5	6.5
PADM (pF)	4.70	4.70	4.70	4.70	4.71	4.71

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXXE01	1	82.962	194.9
ODVXXE02	2	86.468	204.8
ODVXXE04	4	86.468	215.2
ODVXXE08	8	102.215	267.5
ODVXXE12	12	102.215	288.2
ODVXXE16	16	102.215	309.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODVXXE01	From: A To: PADM	t_{PLH} t_{PHL}	3.894 3.694	5.672 5.362	7.474 7.029	10.221 9.509	14.891 13.583
	From: EN To: PADM	t_{ZH} t_{ZL}	3.902 3.762	5.743 5.360	7.581 6.956	10.334 9.399	14.913 13.623
	Capacitive Load (pF)		15	50	75	100	150 (max)
ODVXXE02	From: A To: PADM	t_{PLH} t_{PHL}	2.018 1.922	5.151 4.828	7.433 6.905	9.717 8.967	14.246 13.048
	From: EN To: PADM	t_{ZH} t_{ZL}	2.100 1.948	5.283 4.839	7.577 6.903	9.862 8.963	14.373 13.068
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVXXE04	From: A To: PADM	t_{PLH} t_{PHL}	1.107 1.193	2.727 2.634	4.996 4.708	9.476 8.846	14.048 12.939
	From: EN To: PADM	t_{ZH} t_{ZL}	1.250 1.192	2.820 2.665	5.066 4.766	9.609 8.842	14.117 12.997
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVXXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.234 0.920	1.806 1.619	2.911 2.667	5.190 4.728	7.449 6.732
	From: EN To: PADM	t_{ZH} t_{ZL}	0.880 0.843	1.657 1.562	2.789 2.587	5.068 4.634	7.298 6.676
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVXXE12	From: A To: PADM	t_{PLH} t_{PHL}	0.878 0.764	1.407 1.241	2.167 1.929	3.674 3.297	5.166 4.638
	From: EN To: PADM	t_{ZH} t_{ZL}	0.733 0.777	1.253 1.251	2.012 1.931	3.527 3.295	5.016 4.662
	Capacitive Load (pF)		15	50	100	200	300 (max)
ODVXXE16	From: A To: PADM	t_{PLH} t_{PHL}	0.842 0.865	1.243 1.183	1.809 1.691	2.935 2.729	4.064 3.738
	From: EN To: PADM	t_{ZH} t_{ZL}	0.709 0.703	1.111 1.094	1.678 1.630	2.804 2.656	3.932 3.696

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPR 0.35 micron CMOS Pad Library

Tristate Timing

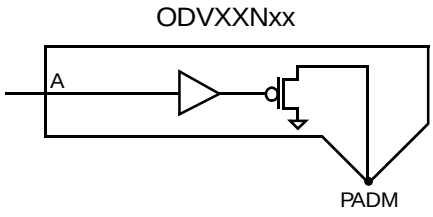
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell					
			ODVXXE01	ODVXXE02	ODVXXE04	ODVXXE08	ODVXXE12	ODVXXE16
EN	PADM	t_{HZ} t_{LZ}	0.647 0.215	0.528 0.194	0.652 0.255	0.395 0.474	0.452 0.529	0.512 0.581

Description

ODVXXNxx is a family of 1 to 16 mA, non-inverting, LVTTL-level, output buffer pieces with N-channel, open-drains (pull-down).

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODVXXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVXXNxx port map (PADM, A);

Pin Loading

Pin Name	Load					
	ODVXXN01	ODVXXN02	ODVXXN04	ODVXXN08	ODVXXN12	ODVXXN16
A (eq-load)	4.9	4.9	4.9	10.1	10.1	10.1
PADM (pF)	4.70	4.70	4.70	4.70	4.70	4.70

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXXN01	1	79.648	182.9
ODVXXN02	2	79.648	185.3
ODVXXN04	4	79.648	190.4
ODVXXN08	8	84.833	201.1
ODVXXN12	12	84.833	210.6
ODVXXN16	16	84.833	220.1

a. See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODVXXN01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{ZL}	3.444	5.065	6.724	9.213	13.312
ODVXXN02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZL}	1.797	4.682	6.750	8.813	12.916
ODVXXN04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.028	2.470	4.538	8.651	12.774
ODVXXN08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.555	1.264	2.290	4.333	6.381
ODVXXN12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.452	0.938	1.618	2.963	4.322
ODVXXN16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	0.416	0.781	1.297	2.323	3.334

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

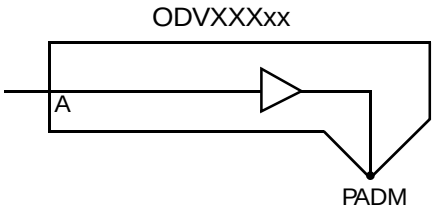
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell					
			ODVXXN01	**ODVXXN02**	**ODVXXN04**	**ODVXXN08**	**ODVXXN12**	**ODVXXN16**
A	PADM	t_{LZ}	0.133	0.160	0.221	0.169	0.211	0.247

Description

ODVXXXxx is a family of 1 to 16 mA, non-inverting, LVTTL-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODVXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODVXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load					
	ODVXXX01	ODVXXX02	ODVXXX04	ODVXXX08	ODVXXX12	ODVXXX16
A (eq-load)	4.9	4.9	7.4	10.1	10.1	10.1

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODVXXX01	1	79.649	188.6
ODVXXX02	2	79.649	193.8
ODVXXX04	4	82.241	204.4
ODVXXX08	8	84.834	226.6
ODVXXX12	12	84.834	247.3
ODVXXX16	16	84.834	268.3

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

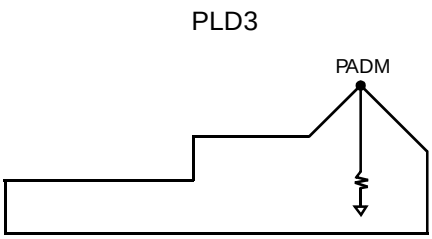
ODVXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.707 3.532	5.578 5.178	7.433 6.825	10.191 9.296	14.736 13.413
ODVXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.016 1.990	5.175 4.869	7.442 6.945	9.716 9.014	14.278 13.098
ODVXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.026 1.055	2.623 2.515	4.897 4.580	9.412 8.687	13.941 12.813
ODVXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.625 0.663	1.405 1.383	2.535 2.419	4.799 4.462	7.047 6.502
ODVXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.545 0.583	1.062 1.079	1.812 1.764	3.329 3.115	4.822 4.470
ODVXXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	0.543 0.609	0.921 1.005	1.476 1.539	2.601 2.558	3.723 3.582

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI350XXPR 0.35 micron CMOS Pad Library

Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
	N/A	N/A

HDL Syntax

Verilog ..... PLD3 *inst_name* (PADM);

VHDL..... *inst_name*: PLD3 port map (PADM);

Power Characteristics

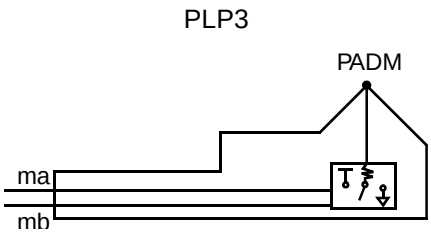
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.603	nA
EQL_{pd}	186.7	Eq-load

See page 2-13 for power equation.

Description

PLP3 is a programmable pull-up/pull-down buffer piece.

Logic Symbol



Truth Table

MA	MB	PADM Function
L	L	Pull-down
H	H	Pull-up
H	L	Tristate
L	H	Tristate

Pin Loading

	Load
MA	2.3 eql
MB	1.9 eql

HDL Syntax

Verilog ..... PLP3 *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLP3 port map (PADM, MA, MB);

Power Characteristics

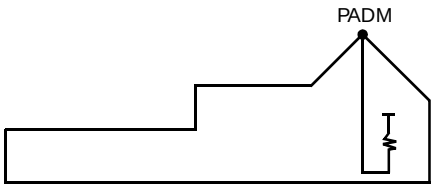
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.603	nA
EQL_{pd}	183.4	Eq-load

See page 2-13 for power equation.

AMI350XXPR 0.35 micron CMOS Pad Library

Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLU3  	N/A	N/A

HDL Syntax

Verilog ..... PLU3 *inst_name* (PADM);

VHDL..... *inst_name*: PLU3 port map (PADM);

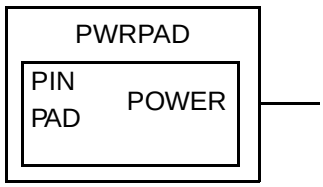
Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	2.603	nA
EQL_{pd}	186.6	Eq-load

See page 2-13 for power equation.

Description

PWRPAD is a generic power pad used to define the connection of a chip power pin to logical buses in the device. For more information on power and ground buses, as well as PWRPAD usage see “Interconnect Load Estimation” on page 2-15.



PWRPAD has the following parameters:

- LVDD: this parameter receives a string value that defines the name of the power supply that PWRPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that PWRPAD connects to.

Verilog Syntax

```
defparam SUPPLY_5V.LVDD = "PAD_5V",
         SUPPLY_5V.CONTACT = "IPWR,OPWR1";
PWRPAD SUPPLY_5V (.PADM(VDD_5V));
```

VHDL syntax

```
SUPPLY_5V : PWRPAD generic map (LVDD => "PAD_5V", CONTACT => "IPWR,OPWR1")
         port map (PADM => VDD_5V);
```

Bolt syntax

```
PWRPAD/SUPPLY_5V VDD_5V (LVDD='PAD_5V' CONTACT="IPWR,OPWR1");
```

where:

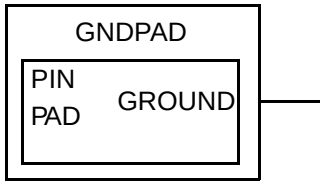
- SUPPLY_5V is the instance name for PWRPAD
- PAD_5V is the name of the supply
- IPWR, OPWR1 are logical buses (see section ...)
- VDD_5V is the chip port name

GNDPAD

AMI350XXPR 0.35 micron CMOS Pad Library

Description

GNDPAD is a generic ground pad used to define the connection of a chip ground pin to logical buses in the device. For more information on power and ground buses, as well as GNDPAD usage see “Interconnect Load Estimation” on page 2-15.



GNDPAD has the following parameters:

- LVSS: this parameter receives a string value that defines the name of the ground that GNDPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that GNDPAD connects to.

Verilog syntax

```
defparam GROUND1.LVSS = "VSS",
         GROUND1.CONTACT = "CGND,OGND";
GNDPAD GROUND1 (.PADM(VSS1));
```

VHDL syntax

```
GROUND1 : GNDPAD generic map (LVSS => "VSS", CONTACT => "CGND,OGND")
          port map (PADM => VSS1);
```

Bolt syntax

```
.GNDPAD/GROUND1 VSS1 (LVSS='VSS' CONTACT="CGND,OGND");
```

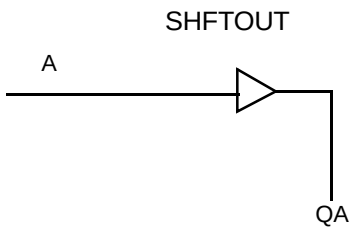
where:

- GROUND1 is the instance name for GNDPAD
- VSS is the name of the supply
- CGND,OGND are logical buses (see section ...)
- VSS1 is the chip port name

Description

SHFTOUT is a mixed voltage single output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol



Truth Table

A	QA
L	L
H	H

Pin Loading

	Load
A	4.4

HDL Syntax

Verilog ..... SHFTOUT *inst_name* (QA, A);

VHDL..... *inst_name*: SHFTOUT port map (QA, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	8.842	nA
EQL_{pd}	5.8	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 2.5V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	6	12	17	23 (max)
A	QA	t_{PLH} t_{PHL}	0.132 0.109	0.177 0.144	0.224 0.181	0.261 0.209	0.304 0.242

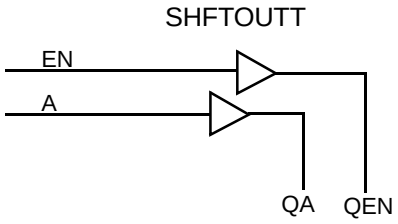
SHFTOUTT

AMI350XXPR 0.35 micron CMOS Pad Library

Description

SHFTOUTT is a mixed voltage dual output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol



Truth Table

A	EN	QA	QEN
L	X	L	X
H	X	H	X
X	L	X	L
X	H	X	H

Pin Loading

	Load
A(eql)	3.1
EN(eql)	3.1

HDL Syntax

Verilog ..... SHFTOUTT *inst_name* (QA, QEN, A, EN);

VHDL..... *inst_name*: SHFTOUTT port map (QA, QEN, A, EN);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	11.049	nA
EQL_{pd}	6.6	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 2.5V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	10	13 (max)
A	QA	t_{PLH} t_{PHL}	0.154 0.130	0.187 0.156	0.231 0.192	0.287 0.236	0.328 0.267
EN	QEN	t_{PLH} t_{PHL}	0.148 0.121	0.178 0.146	0.219 0.183	0.275 0.232	0.320 0.268