0.5 Micron CMOS Pad Library Datasheets
AMI500HXPR 3.3 Volt
Section 4
Revision 1.1

Input Drive Pieces

Pull Pieces

Output Drive Pieces

Selection Guide

AMI500HXPR 0.5 micron CMOS Pad Library

Power Pad Cells

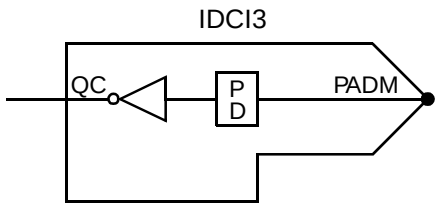
Special Pad Cells

DATASHEETS

Description

IDCI3 is an inverting, CMOS-level input buffer piece.

Logic Symbol



Truth Table

PADM	QC
L	H
H	L

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCI3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCI3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.405	nA
EQL_{pd}	12.7	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.732 0.913	0.897 1.058	1.049 1.180	1.170 1.294	1.287 1.425

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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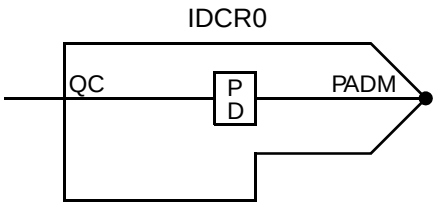
Description

IDCR0 is a non-buffered, resistive analog interface input piece with ESD protection.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	5.01 pF

HDL Syntax

Verilog ..... IDCR0 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCR0 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	3.615	nA
EQL_{pd}	2.5	Eq-load

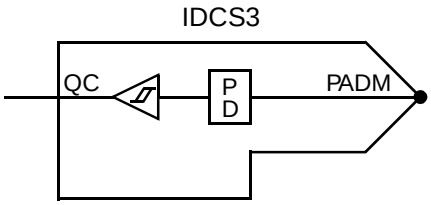
See page 2-13 for power equation.

Note: This special purpose, “resistive input” pad is not intended for use as a general input pad.

Description

IDCS3 is a non-inverting, CMOS-level Schmitt trigger input buffer piece with voltage hysteresis.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDCS3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCS3 port map (QC, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.416	nA
EQL_{pd}	17.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.307 1.076	1.486 1.244	1.653 1.405	1.797 1.544	1.950 1.690

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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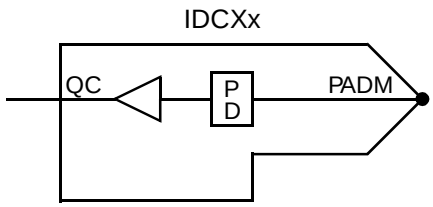
Description

IDCXx is a family of non-inverting, CMOS-level input buffer pieces.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDCXx *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDCXx port map (QC, PADM);

Pin Loading

Pin Name	Load	
	IDCX3	IDCX6
PADM (pF)	4.90	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDCX3	0.0	1.399	10.4
IDCX6	0.0	1.411	18.1

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

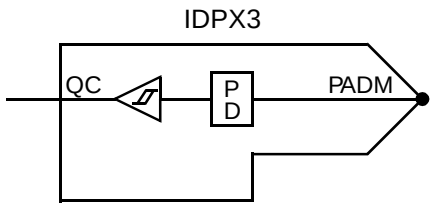
IDCX3	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.779 0.597	0.953 0.848	1.100 1.010	1.227 1.132	1.368 1.256
IDCX6	Number of Equivalent Loads		1	11	22	32	43 (max)
	From: PADM To: QC	t_{PLH} t_{PHL}	0.584 0.632	0.787 0.709	0.901 0.813	0.972 0.898	1.033 0.968

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

IDPX3 is a non-inverting, PCI-level input buffer piece. IDPX3 is for the 33MHz PCI ODPSXE16 piece.

Logic Symbol



Truth Table

PADM	QC
L	L
H	H

HDL Syntax

Verilog ..... IDPX3 *inst_name* (QC, PADM);
VHDL..... *inst_name*: IDPX3 port map (QC, PADM);

Pin Loading

Pin Name	Load
	IDPX3
PADM (pF)	4.90

Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
IDPX3	0.0	1.405	12.6

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Number of Equivalent Loads		1	11	22	32	43 (max)
IDPX3	From: PADM	t_{PLH}	0.737	0.876	1.008	1.132	1.271
	To: QC	t_{PHL}	0.919	1.055	1.173	1.313	1.508

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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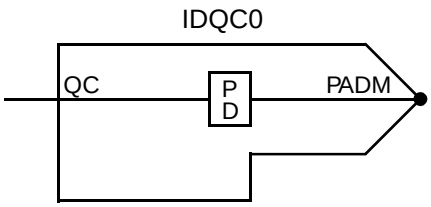
Description

IDQC0 is a non-buffered, resistive crystal oscillator input receiver piece with ESD protection.

Logic Symbol



Truth Table

PADM	QO
L	L
H	H

Pin Loading

	Load
PADM	4.90 pF

HDL Syntax

Verilog ..... IDQC0 *inst_name* (QO, PADM);
VHDL..... *inst_name*: IDQC0 port map (QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.382	nA
EQL_{pd}	2.1	Eq-load

See page 2-13 for power equation.

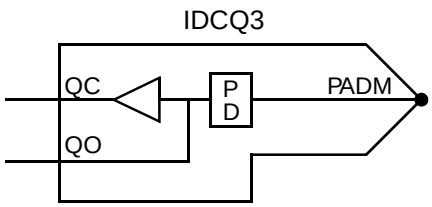
Design Notes:

The IDQC0 cell is for backward compatibility with existing oscillator methodologies.

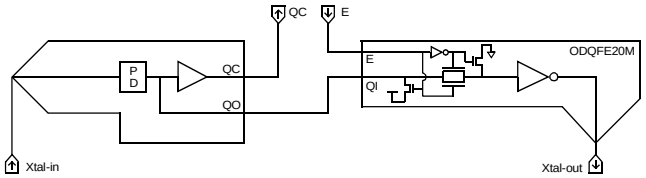
Description

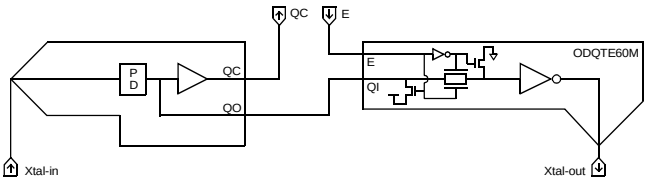
IDQC3 is a crystal oscillator input receiver pad piece with a non-inverting, CMOS-level clock input. QO is the output to either the ODQFE20M or the ODQTE60M. PADM is the bond pad from the Xtal-in.

Logic Symbol



The Possible Logic Schematic Combinations





Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load
PADM	4.90 pF

Pad Logic

HDL Syntax

Verilog ..... IDQC3 *inst_name (*QC, QO, PADM);

VHDL..... *inst_name*: IDQC3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.399	nA
EQL_{pd}	11.4	Eq-load

See page 2-13 for power equation.

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Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	0.786 0.698	0.955 0.864	1.117 1.016	1.255 1.144	1.401 1.277
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

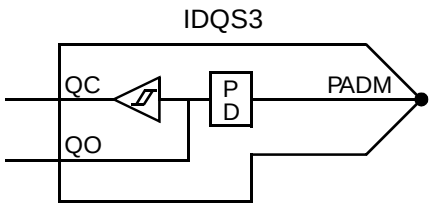
Design Notes:

The IDQC3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of either the ODQFE20M or the ODQTE60M oscillator output driver pad pieces. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

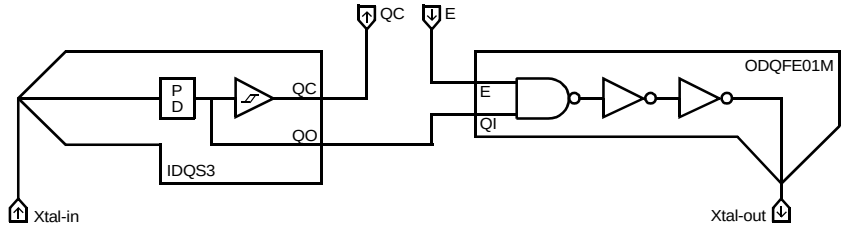
Description

IDQS3 is a crystal oscillator input receiver pad piece. QC is a non-inverting, CMOS-level schmitt trigger clock input buffer. QO is the output to the ODQFE01M. PADM is the bond pad from the Xtal-in.

Logic Symbol



Logic Schematic



Truth Table

PADM	QC	QO
L	L	L
H	H	H

Pin Loading

	Load	
PADM	4.90	pF

HDL Syntax

Verilog ..... IDQS3 *inst_name* (QC, QO, PADM);

VHDL..... *inst_name*: IDQS3 port map (QC, QO, PADM);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.416	nA
EQL_{pd}	18.0	Eq-load

See page 2-13 for power equation.

AMI500HXPR 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	11	22	32	43 (max)
PADM	QC	t_{PLH} t_{PHL}	1.288 1.131	1.462 1.276	1.638 1.417	1.785 1.560	1.938 1.731
PADM	QO	t_{PLH} t_{PHL}	0.000 0.000				

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

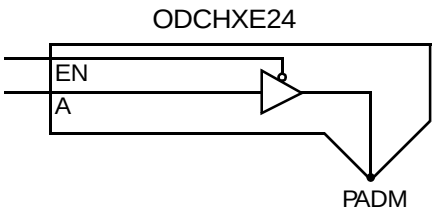
Design Notes:

The IDQS3 is the input cell of a two cell oscillator circuit. Its function is to connect the QO pin with the QI pin of the ODQFE01M oscillator output driver pad piece. The buffered QC pin is for driving the oscillator into the core. Two package pins are required to create a complete oscillator.

Description

ODCHXE24 is a high performance, 24 mA, non-inverting, CMOS-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	3.5 eql
EN	6.5 eql
PADM	4.93 pF

HDL Syntax

Verilog ..... ODCHXE24 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCHXE24 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.551	nA
EQL_{pd}	297.0	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	1.405 1.454	2.040 1.789	2.969 2.295	4.793 3.310	6.574 4.312
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.265 1.325 1.300 1.353	 1.900 1.784	 2.779 2.341	 4.586 3.366	 6.430 4.329

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

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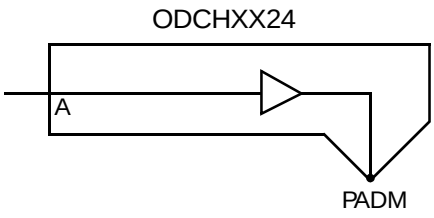
Description

ODCHXX24 is a high performance, 24 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	14.5 eql

HDL Syntax

Verilog ..... ODCHXX24 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCHXX24 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.435	nA
EQL_{pd}	249.7	Eq-load

See page 2-13 for power equation.

Output Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

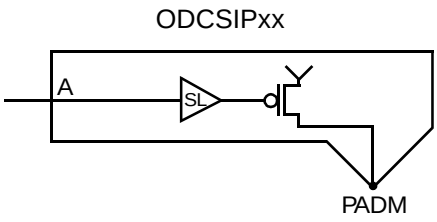
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH}	0.903	1.530	2.429	4.236	6.053
		t_{PHL}	0.892	1.316	1.850	2.863	3.864

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCSIPxx is a family of 4 to 16 mA, inverting, CMOS-level output buffer pieces with P-channel open-drains (pull-up) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCSIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSIPxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODCSIP04	ODCSIP08	ODCSIP12	ODCSIP16
A (eq-load)	4.1	4.1	4.1	5.0
PADM (pF)	4.94	4.94	4.94	4.94

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSIP04	4	1.445	190.5
ODCSIP08	8	1.445	203.6
ODCSIP12	12	1.445	216.8
ODCSIP16	16	79.615	235.3

a. See page 2-13 for power equation.

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Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCSIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	3.717	8.762	15.949	30.329	44.734
ODCSIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.500	4.998	8.605	15.941	23.210
ODCSIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.99	3.72	6.20	11.13	15.99
ODCSIP16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.868	3.073	4.835	8.460	12.165

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

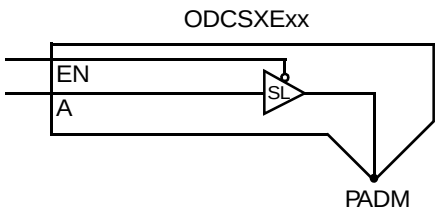
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns)		Parameter	Cell			
From	**To**		**ODCSIP04**	**ODCSIP08**	**ODCSIP12**	**ODCSIP16**
A	PADM	t_{HZ}	0.887	1.098	1.30	1.262

Description

ODCSXExx is a family of 4 to 24 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16	ODCSXE24
A (eq-load)	2.3	2.3	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9	6.9	6.9
PADM (pF)	4.94	4.94	4.94	4.94	4.94

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXE04	4	1.513	218.9
ODCSXE08	8	1.513	240.3
ODCSXE12	12	1.513	261.1
ODCSXE16	16	1.513	283.9
ODCSXE24	24	1.535	302.7

a. See page 2-13 for power equation.

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Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXE04	From: A To: PADM	t_{PLH} t_{PHL}	4.254 3.787	9.499 8.115	16.681 14.386	30.368 26.852	43.491 39.171
	From: EN To: PADM	t_{ZH} t_{ZL}	4.012 3.331	9.148 7.898	16.289 14.151	30.013 26.510	43.108 38.972
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE08	From: A To: PADM	t_{PLH} t_{PHL}	3.282 2.943	5.862 5.165	9.538 8.325	16.811 14.644	24.007 20.974
	From: EN To: PADM	t_{ZH} t_{ZL}	2.655 2.492	5.328 4.647	9.054 7.840	16.331 14.241	23.478 20.482
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE12	From: A To: PADM	t_{PLH} t_{PHL}	2.801 2.490	4.497 3.915	6.981 6.010	11.942 10.195	16.791 14.272
	From: EN To: PADM	t_{ZH} t_{ZL}	2.590 2.233	4.354 3.740	6.836 5.774	11.737 9.856	16.592 14.061
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE16	From: A To: PADM	t_{PLH} t_{PHL}	2.702 2.599	3.722 3.651	5.243 5.139	8.296 8.166	11.324 11.237
	From: EN To: PADM	t_{ZH} t_{ZL}	1.971 2.116	3.284 3.240	4.833 4.798	7.835 7.848	10.910 10.852
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCSXE24	From: A To: PADM	t_{PLH} t_{PHL}	2.645 2.072	3.802 2.869	5.386 3.971	8.442 6.024	11.415 7.953
	From: EN To: PADM	t_{ZH} t_{ZL}	2.357 1.895	3.421 2.666	4.949 3.686	8.019 5.707	11.099 7.746

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

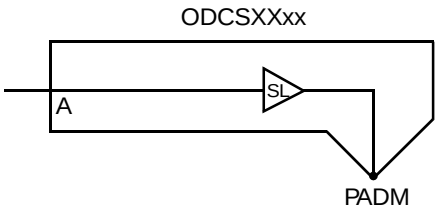
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16	ODCSXE24
EN	PADM	t_{HZ} t_{LZ}	0.930 1.103	1.142 1.273	1.353 1.422	1.592 1.579	1.469 1.666

Description

ODCSXXxx is a family of 4 to 24 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCSXX04	ODCSXX08	ODCSXX12	ODCSXX16	ODCSXX24
A (eq-load)	9.3	9.3	9.3	9.3	11.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXX04	4	1.477	198.6
ODCSXX08	8	1.477	220.0
ODCSXX12	12	1.477	240.8
ODCSXX16	16	1.477	263.6
ODCSXX24	24	1.499	282.3

a. See page 2-13 for power equation.

AMI500HXPR 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

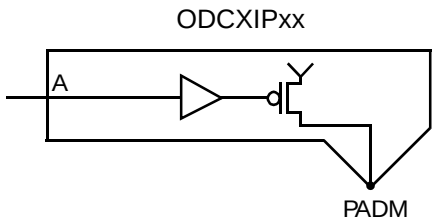
ODCSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.751 3.225	8.336 7.305	15.541 13.459	28.810 25.924	42.060 38.289
ODCSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.057 1.926	4.547 4.121	8.200 7.270	15.446 13.581	22.331 19.901
ODCSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.761 1.729	3.435 3.150	5.855 5.198	10.742 9.315	15.665 13.446
ODCSXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.663 1.718	2.924 2.798	4.741 4.293	8.370 7.285	11.986 10.340
ODCSXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.670 1.333	2.897 2.074	4.663 3.115	8.255 5.166	11.907 7.176

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

ODCXIPxx is a family of 1 to 16 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCXIPxx *inst_name* (PADM, A);
VHDL..... *inst_name*: ODCXIPxx port map (PADM, A);

Pin Loading

Pin Name	Load					
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08	ODCXIP12	ODCXIP16
A (eq-load)	2.8	2.8	2.8	3.9	3.9	3.9
PADM (pF)	4.92	4.92	4.92	4.93	4.93	4.93

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
ODCXIP01	1	1.393	148.8
ODCXIP02	2	1.394	153.6
ODCXIP04	4	1.399	162.0
ODCXIP08	8	1.405	178.9
ODCXIP12	12	70.557	195.7
ODCXIP16	16	70.557	210.4

a. See page 2-13 for power equation.

AMI500HXPR 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXIP01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{ZH}	6.523	9.453	12.385	16.772	24.043
ODCXIP02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZH}	3.579	8.640	12.254	15.854	23.016
ODCXIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	2.362	4.946	8.604	15.892	23.201
ODCXIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.744	3.024	4.791	8.462	12.073
ODCXIP12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.623	2.557	3.810	6.260	12.073
ODCXIP16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.554	2.336	3.354	5.224	6.974

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

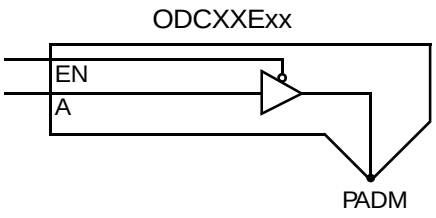
Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Cell					
			ODCXIP01	**ODCXIP02**	**ODCXIP04**	**ODCXIP08**	**ODCXIP12**	**ODCXIP16**
APADM		t_{HZ}	1.231	1.021	1.148	1.399	1.589	1.973

Description

ODCXXExx is a family of 1 to 24 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load						
	ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16	ODCXXE24
A (eq-load)	5.6	7.9	7.9	2.3	2.3	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5	5.5	5.5
PADM (pF)	4.92	4.92	4.93	4.93	4.93	4.93	4.93

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXE01	1	57.878	49.4
ODCXXE02	2	1.446	164.2
ODCXXE04	4	1.446	174.8
ODCXXE08	8	1.488	223.0
ODCXXE12	12	1.488	243.9
ODCXXE16	16	1.488	268.0
ODCXXE24	24	1.488	279.9

a. See page 2-13 for power equation.

AMI500HXPR 0.5 micron CMOS Pad Library

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODCXXE01	From: A To: PADM	t_{PLH} t_{PHL}	6.541 5.939	9.316 8.525	12.331 11.098	16.802 14.929	23.926 21.261
	From: EN To: PADM	t_{ZH} t_{ZL}	6.848 5.989	9.767 8.397	12.686 11.025	17.065 14.949	24.362 21.178
	Capacitive Load (pF)		**15**	**50**	**75**	**100**	**150 (max)**
ODCXXE02	From: A To: PADM	t_{PLH} t_{PHL}	3.464 3.179	8.487 7.506	12.113 10.609	15.729 13.717	22.880 19.947
	From: EN To: PADM	t_{ZH} t_{ZL}	3.767 3.199	8.807 7.548	12.375 10.657	15.955 13.762	23.201 19.959
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXXE04	From: A To: PADM	t_{PLH} t_{PHL}	2.279 2.100	4.824 4.353	8.470 7.459	15.781 13.611	23.106 19.803
	From: EN To: PADM	t_{ZH} t_{ZL}	2.556 2.175	5.103 4.413	8.776 7.566	16.104 13.753	23.364 19.845
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXXE08	From: A To: PADM	t_{PLH} t_{PHL}	2.356 1.952	3.658 3.013	5.528 4.544	9.191 7.596	12.768 10.605
	From: EN To: PADM	t_{ZH} t_{ZL}	2.138 1.765	3.420 2.866	5.219 4.364	8.847 7.374	12.511 10.450
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXXE12	From: A To: PADM	t_{PLH} t_{PHL}	2.269 1.989	3.231 2.730	4.523 3.762	6.986 5.790	9.361 7.798
	From: EN To: PADM	t_{ZH} t_{ZL}	2.059 1.598	3.011 2.415	4.250 3.499	6.685 5.545	9.157 7.502
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.429 1.980	3.119 2.634	4.145 3.478	5.879 5.022	7.796 6.467
	From: EN To: PADM	t_{ZH} t_{ZL}	2.041 1.768	2.831 2.410	3.777 3.182	5.590 4.706	7.447 6.272
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODCXXE24	From: A To: PADM	t_{PLH} t_{PHL}	2.281 2.016	3.092 2.494	4.110 3.122	5.946 4.240	7.644 5.221
	From: EN To: PADM	t_{ZH} t_{ZL}	1.972 1.733	2.751 2.271	3.762 2.872	5.625 3.958	7.375 5.006

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

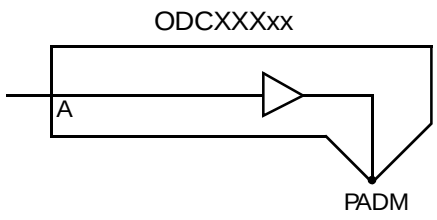
Delay (ns) From	To	Parameter	Cell						
			ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16	ODCXXE24
EN	PADM	t_{HZ}	1.748	1.409	1.822	1.242	1.560	1.894	1.892
		t_{LZ}	0.460	0.424	0.574	1.228	1.406	1.665	1.967

AMI500HXPR 0.5 micron CMOS Pad Library

Description

ODCXXXxx is a family of 1 to 24 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXXXxx *inst_name* (PADM, A);
VHDL..... *inst_name*: ODCXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12	ODCXXX16	ODCXXX24
A (eq-load)	4.3	4.3	6.2	8.3	8.2	8.2	10.3

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXX01	1	1.403	149.5
ODCXXX02	2	1.403	155.0
ODCXXX04	4	1.403	165.6
ODCXXX08	8	1.413	189.8
ODCXXX12	12	1.413	210.7
ODCXXX16	16	1.413	234.8
ODCXXX24	24	1.424	248.2

a. See page 2-13 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

ODCXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	6.345 5.687	9.140 8.266	12.106 10.840	16.568 14.676	23.749 21.008
ODCXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	3.525 3.232	8.546 7.564	12.092 10.729	15.666 13.868	22.950 19.976
ODCXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.021 1.954	4.558 4.131	8.201 7.229	15.505 13.403	22.797 19.561
ODCXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.468 1.705	2.773 2.610	4.623 4.099	8.274 7.168	11.878 10.165
ODCXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To PADM	t_{PLH} t_{PHL}	1.454 1.461	2.392 2.249	3.646 3.320	6.102 5.369	8.544 7.348
ODCXXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.500 1.681	2.247 2.381	3.253 3.200	5.139 4.720	6.908 6.276
ODCXXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.496 1.277	2.232 1.794	3.188 2.425	5.027 3.531	6.837 4.531

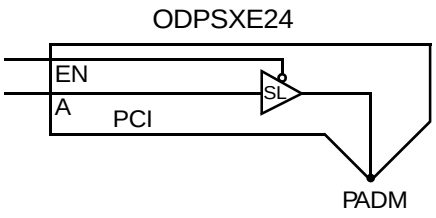
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

AMI500HXPR 0.5 micron CMOS Pad Library

Description

ODPSXE24 is a 33 MHz PCI, non-inverting, tristate buffer piece with active low enable and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	8.2 pF
EN	5.5 pF
PADM	4.93 pF

HDL Syntax

Verilog ..... ODPSXE24 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODPSXE24 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.441	nA
EQL_{pd}	229.2	Eq-load

See page 2-13 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

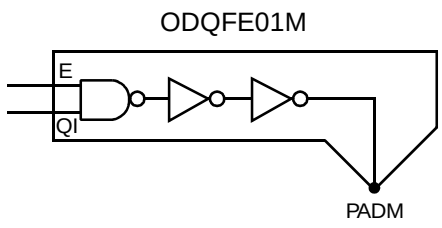
Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	2.056 2.229	2.830 2.974	3.841 3.919	5.843 5.694	7.873 7.420
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	3.832 2.447 2.081 1.865	 2.916 2.754	 4.020 3.779	 6.121 5.640	 8.145 7.410

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

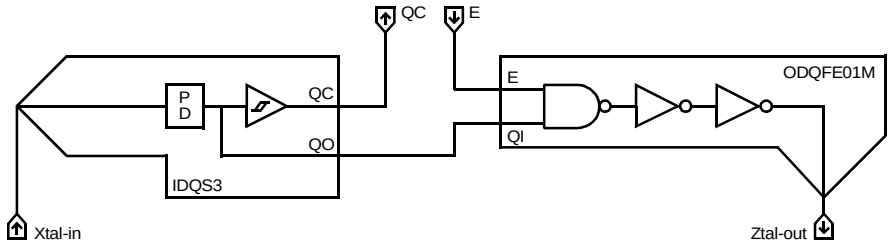
Description

ODQFE01M is a fundamental mode, enabled crystal oscillator, output driver pad piece that runs over a frequency range of 32 kHz - 1 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
L	H	H
H	H	L
H	L	X

Pin Loading

	Load
E	4.0 eql
QI	3.2 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE01M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE01M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.405	nA
EQL_{pd}	151.7	Eq-load

See page 2-13 for power equation.

AMI500HXPR 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	25	35	50	75 (max)
E	PADM	t_{PLH} t_{PHL}	6.678 6.854	9.645 9.402	12.577 11.948	16.931 15.770	24.108 22.163
QI	PADM	t_{PLH} t_{PHL}	7.057 6.866	9.823 9.406	12.658 11.948	17.027 15.773	24.539 22.173

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

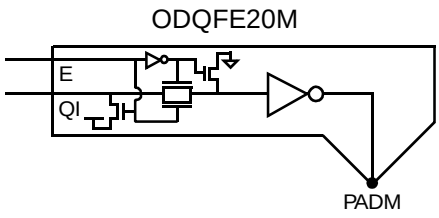
Design Notes:

The ODQFE01M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQS3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

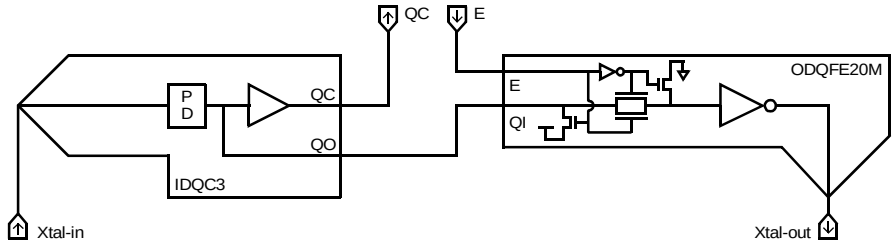
Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	6.5 eql
QI	5.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQFE20M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQFE20M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.442	nA
EQL_{pd}	165.4	Eq-load

See page 2-13 for power equation.

AMI500HXPR 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	75	100	150 (max)
E	PADM	t_{PLH} t_{PHL}	4.674 2.784	9.672 7.381	13.256 10.439	16.855 13.501	24.084 19.782
QI	PADM	t_{PLH} t_{PHL}	3.262 3.025	8.288 7.326	11.879 10.407	15.472 13.507	22.665 19.758

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

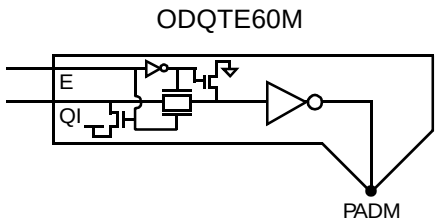
Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

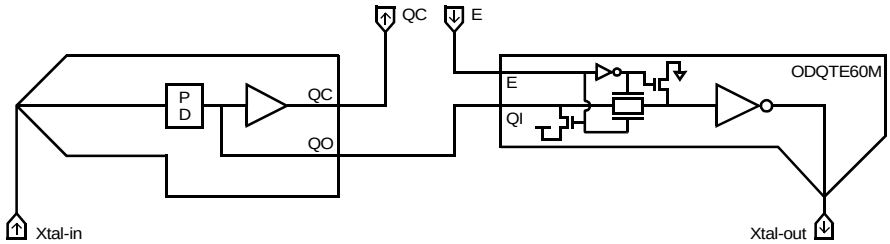
Description

ODQTE60M is an enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	6.5 eql
QI	5.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQTE60M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQTE60M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.442	nA
EQL_{pd}	176.1	Eq-load

See page 2-13 for power equation.

AMI500HXPR 0.5 micron CMOS Pad Library

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 3.3V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
E	PADM	t_{PLH} t_{PHL}	3.499 1.920	6.088 4.076	9.782 7.153	17.097 13.331	24.342 19.500
QI	PADM	t_{PLH} t_{PHL}	2.007 1.931	4.576 4.159	8.232 7.236	15.517 13.356	22.784 19.548

Delay will vary with input conditions. See page 2-15 for interconnect estimates.

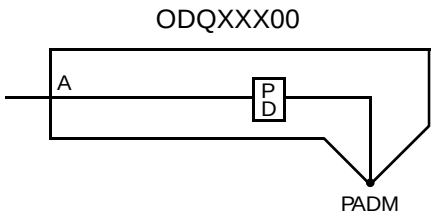
Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.

Description

ODQXXX00 is a non-buffered, resistive analog crystal oscillator output pad piece with ESD protection.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	2.4 eql

HDL Syntax

Verilog ..... ODQXXX00 *inst_name* (PADM, A);

VHDL..... *inst_name*: ODQXXX00 port map (PADM, A);

Power Characteristics

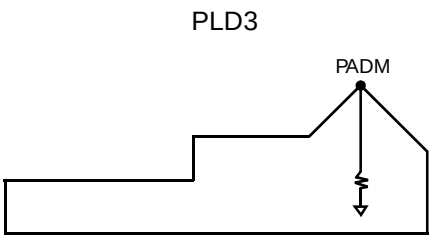
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.382	nA
EQL_{pd}	137.5	Eq-load

See page 2-13 for power equation.

AMI500HXPR 0.5 micron CMOS Pad Library

Description

PLD3 is an active pull-down buffer piece.

Logic Symbol	Truth Table	Pin Loading
	N/A	N/A

HDL Syntax

Verilog ..... PLD3 *inst_name* (PADM);

VHDL..... *inst_name*: PLD3 port map (PADM);

Power Characteristics

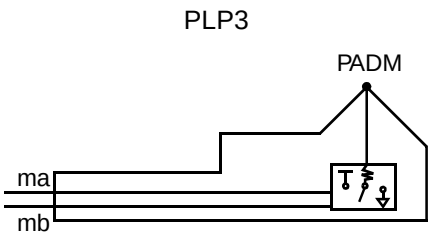
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.394	nA
EQL_{pd}	149.8	Eq-load

See page 2-13 for power equation.

Description

PLP3 is a programmable pull-up/pull-down buffer piece.

Logic Symbol



Truth Table

MA	MB	PADM Function
L	L	Pull-down
H	H	Pull-up
H	L	Tristate
L	H	Tristate

Pin Loading

	Load
MA	2.1 eql
MB	1.8 eql

HDL Syntax

Verilog ..... PLP3 *inst_name* (PADM, MA, MB);

VHDL..... *inst_name*: PLP3 port map (PADM, MA, MB);

Power Characteristics

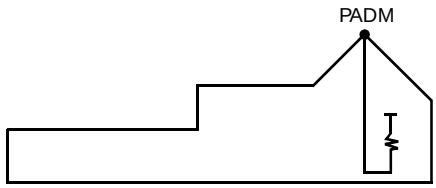
Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.393	nA
EQL_{pd}	146.8	Eq-load

See page 2-13 for power equation.

AMI500HXPR 0.5 micron CMOS Pad Library

Description

PLU3 is an active pull-up buffer piece.

Logic Symbol	Truth Table	Pin Loading
PLU3  	N/A	N/A

HDL Syntax

Verilog ..... PLU3 *inst_name* (PADM);
VHDL..... *inst_name*: PLU3 port map (PADM);

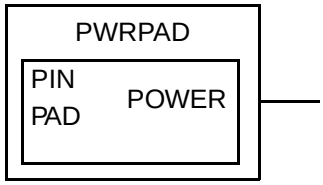
Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.393	nA
EQL_{pd}	149.7	Eq-load

See page 2-13 for power equation.
Delay will vary with input conditions. See page 2-15 for interconnect estimates.

Description

PWRPAD is a generic power pad used to define the connection of a chip power pin to logical buses in the device. For more information on power and ground buses, as well as PWRPAD usage see “Interconnect Load Estimation” on page 2-15.



PWRPAD has the following parameters:

- LVDD: this parameter receives a string value that defines the name of the power supply that PWRPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that PWRPAD connects to.

Verilog Syntax

```
defparam SUPPLY_5V.LVDD = "PAD_5V",
         SUPPLY_5V.CONTACT = "IPWR,OPWR1";
PWRPAD SUPPLY_5V (.PADM(VDD_5V));
```

VHDL syntax

```
SUPPLY_5V : PWRPAD generic map (LVDD => "PAD_5V", CONTACT => "IPWR,OPWR1")
         port map (PADM => VDD_5V);
```

Bolt syntax

```
PWRPAD/SUPPLY_5V VDD_5V (LVDD='PAD_5V' CONTACT="IPWR,OPWR1");
```

where:

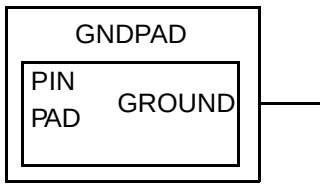
- SUPPLY_5V is the instance name for PWRPAD
- PAD_5V is the name of the supply
- IPWR, OPWR1 are logical buses (see section ...)
- VDD_5V is the chip port name

GNDPAD

AMI500HXPR 0.5 micron CMOS Pad Library

Description

GNDPAD is a generic ground pad used to define the connection of a chip ground pin to logical buses in the device. For more information on power and ground buses, as well as GNDPAD usage see “Interconnect Load Estimation” on page 2-15.



GNDPAD has the following parameters:

- LVSS: this parameter receives a string value that defines the name of the ground that GNDPAD drives.
- CONTACT: this parameter receives a string value that defines the logical buses that GNDPAD connects to.

Verilog syntax

```
defparam GROUND1.LVSS = "VSS",
         GROUND1.CONTACT = "CGND,OGND";
GNDPAD GROUND1 (.PADM(VSS1));
```

VHDL syntax

```
GROUND1 : GNDPAD generic map (LVSS => "VSS", CONTACT => "CGND,OGND")
          port map (PADM => VSS1);
```

Bolt syntax

```
.GNDPAD/GROUND1 VSS1 (LVSS='VSS' CONTACT="CGND,OGND");
```

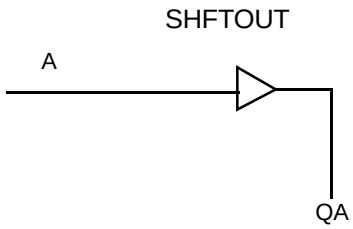
where:

- GROUND1 is the instance name for GNDPAD
- VSS is the name of the supply
- CGND,OGND are logical buses (see section ...)
- VSS1 is the chip port name

Description

SHFTOUT is a mixed voltage single output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol



Truth Table

A	QA
L	L
H	H

Pin Loading

	Load
A	4.1

HDL Syntax

Verilog ..... SHFTOUT *inst_name* (QA, A);

VHDL..... *inst_name*: SHFTOUT port map (QA, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.432	nA
EQL_{pd}	8.3	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 2.5V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	3	6	10	13 (max)
A	QA	t_{PLH} t_{PHL}	0.25 0.20	0.30 0.23	0.37 0.27	0.47 0.31	0.54 0.34

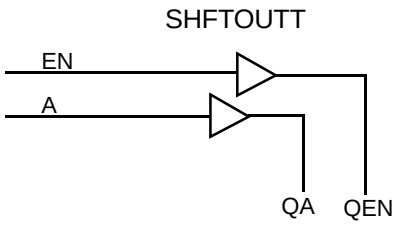
SHFTOUTT

AMI500HXPR 0.5 micron CMOS Pad Library

Description

SHFTOUTT is a mixed voltage dual output pad piece used for level-shifting from a 2.5V core to a 3.3V pad.

Logic Symbol



Truth Table

A	EN	QA	QEN
L	X	L	X
H	X	H	X
X	L	X	L
X	H	X	H

Pin Loading

	Load
A(eql)	1.9
EN(eql)	2.5

HDL Syntax

Verilog ..... SHFTOUTT *inst_name* (QA, QEN, A, EN);

VHDL..... *inst_name*: SHFTOUTT port map (QA, QEN, A, EN);

Pad Logic

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	1.413	nA
EQL_{pd}	9.6	eql

Propagation Delays *See note at beginning of section to compute total delay.

Conditions: T_J = 25°C, V_{DD} = 2.5V, Typical Process

Delay (ns) From	To	Parameter	Number of Equivalent Loads				
			1	2	4	6	8 (max)
A	QA	t_{PLH} t_{PHL}	0.32 0.23	0.37 0.26	0.46 0.31	0.56 0.36	0.66 0.40
EN	QEN	t_{PLH} t_{PHL}	0.33 0.23	0.37 0.26	0.45 0.31	0.55 0.36	0.65 0.40