AN5165K

A Single Chip IC for NTSC Color-TV

■ Overview

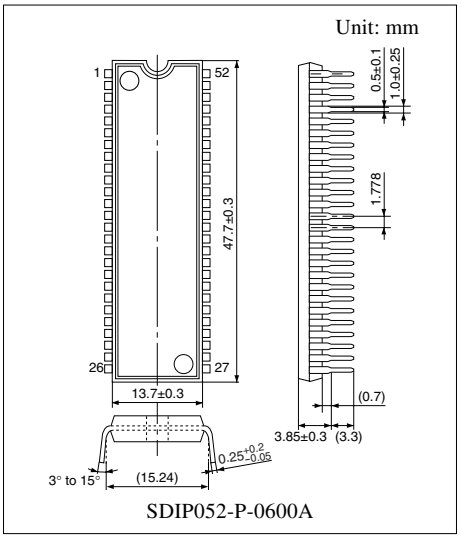
The AN5165K is an IC in which all of the NTSC system color television signal processing circuits are integrated on a single chip. The rationalization of set production line can be realized by this IC incorporating I^2C bus interface.

■ Features

- Built-in video IF circuit, sound IF circuit, video signal processing circuit, color signal processing circuit, deflection correction circuit and sync. signal processing circuit
- Built-in I^2C bus interface

■ Applications

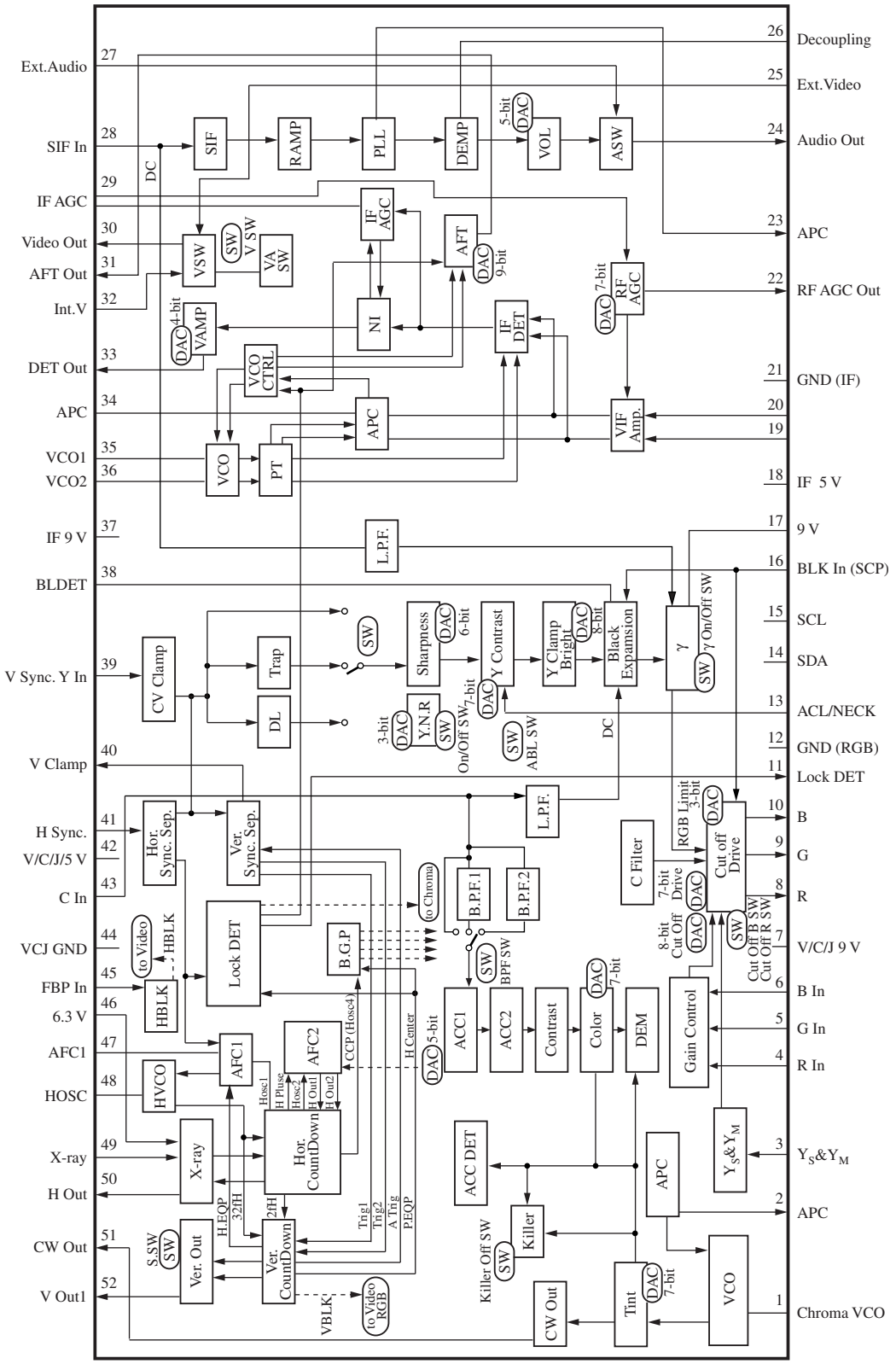
- TVs



SDIP052-P-0600A

Note) The package of this product will be changed to lead-free type (SDIP052-P-0600F). See the new package dimensions section later of this datasheet.

■ Block Diagram



■ Pin Description

Pin No.	Description	Pin No.	Description
1	Chroma VCO (3.58 MHz)	28	SIF Input/White Expand-Level
2	Chroma APC Filter	29	IF AGC Filter
3	Y_S & Y_M Input	30	Video Output
4	External R Input	31	AFT Output
5	External G Input	32	Internal Video Input
6	External B Input	33	VIF Detect Output
7	V_{CC1-1} 9 V (VCJ)	34	VIF APC Filter
8	R Output	35	VIF VCO (1)
9	G Output	36	VIF VCO (2)
10	B Output	37	V_{CC1-2} 9 V
11	Hor. Lock Detect	38	Black Detect
12	GND (RGB/I^{2}C/ DAC)	39	Y/Ver. Sync. Input
13	ACL/NECK Protect	40	Ver. Sync. Clamp
14	SDA	41	Hor. Sync. Input
15	SCL	42	V_{CC2-2} 5 V (Chroma/jungle/DAC)
16	BLK Pulse Input/H_{SYNC2} Output	43	Chroma Input/Black Expansion Start
17	White Detect	44	GND (Video/Chroma/Jungle)
18	V_{CC2-1} 5 V (VIF/SIF)	45	FBP Input
19	VIF Input (1)	46	V_{CC3} 6.2 V
20	VIF Input (2)	47	AFC1 Filter
21	GND (VIF/SIF)	48	Hor. VCO (32 f_H)
22	RF AGC Output	49	X-ray Protection Input
23	SIF APC Filter	50	Hor. Pulse Output
24	Audio Output	51	CW Output/Spot KILLER Off Input/ X-ray Protection Output
25	External Video Input		
26	DC Decoupling Filter	52	Ver. Pulse Output
27	External Audio Input		

■ Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
Supply voltage	V_{CC}	V_{CC1} (7·37)	10.5	V
		V_{CC2} (18·42)	6.0	
		V_{CC3} (46)	6.5	
Supply current	I_{CC}	I_{7+37}	117	mA
		I_{18+42}	68	
		I_{46}	6.3	

■ Absolute Maximum Ratings (continued)

Parameter	Symbol	Rating	Unit
Power dissipation *2	P_D	1 481	mW
Operating ambient temperature *1	T_{opr}	−20 to +70	°C
Storage temperature *1	T_{stg}	−55 to +150	°C

Note) ∗1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
∗2: The power dissipation shown is the value for T_a = 70°C

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1}	8.1 to 9.9	V
	V_{CC2}	4.5 to 5.5	
	V_{CC3}	6.05 to 6.35	

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power supply						
Supply current 1	$I_{7+}I_{37}$	Current at V_7 = 9 V, current at V_{37} = 9 V	68	85	100.5	mA
Supply current 2	$I_{18+}I_{42}$	Current at V_{18} = 5 V, current at V_{42} = 5 V	38	48	57	mA
Supply current 3	I_{46}	Current, when V_{46} = 6.2 V	2	5	6	mA
Supply current 4	I_{46}	Current at V_{46} = 6.2 V. However all other power supplies are off state	5	7	9	mA
VIF circuit (Typical input f_P = 45.75 MHz, V_{IN} = 90 dBμ)						
Video detection output (typ.)	V_{PO}	Modulation factor m = 87.5% Data 0D = 88	1.75	2.1	2.5	V[p-p]
Video detection output (max.)	V_{POmax}	Data 0D = F8	2.15	2.6	3.3	V[p-p]
Video detection output (min.)	V_{POmin}	Data 0D = 08	1.1	1.6	2.0	V[p-p]
Video detection output f characteristics	f_{PC}	Frequency of output −3 dB for 1 MHz	5.5	8	12	MHz
Synchronous peak value voltage	V_{SP}	Voltage in V_{PO} measurement	1.6	2.0	2.4	V
APC pull-in range (Hu)	f_{PPHU}	High band side pull-in range (Difference from f_P = 45.75 MHz)	1.0	1.5	—	MHz
APC pull-in range (Lu)	f_{PPLU}	Low band side pull-in range (Difference from f_P = 45.75 MHz)	—	−1.5	−1.0	MHz
RF AGC delay point adjustment range	DV_{RFDP}	Input to become delay point (V_{22} = approx. 6.5 V), when Data 0C = 00 to 7F	75	—	95	dBm
RF AGC maximum sink current	I_{RFmax}	Maximum current IC can sink when pin 22 is low	1.5	3.0	—	mA

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF Circuit (continued) (Typical input f_P = 45.75 MHz, V_{IN} = 90 dBμ)						
RF AGC minimum sink current	I_{RFmin}	Leak current of IC, when pin 22 is high	−50	0	50	mA
AFT discrimination sensitivity	μ_{AFT}	Df = ±25 kHz	40	57	75	mV/kHz
AFT center voltage	V_{AFT}	V_{31} without V_{IN}	4.0	4.5	5.0	V
AFT maximum output voltage	V_{AFTmax}	V_{31} at f = f_P−500 kHz	7.8	8.1	8.7	V
AFT minimum output voltage	V_{AFTmin}	V_{31} at f = f_P+500 kHz	0.3	0.8	1.0	V
SIF circuit (Typical input f_S = 4.5 MHz, f_M = 400 Hz, V_{IN} = 90 dBμ)						
Audio detection output	V_{SO}	Df = ±25 kHz, 0A = 10	250	350	450	mV[rms]
Audio detection output (max.)	V_{SOmax}	Data 0A = 1F	300	390	480	mV[rms]
Audio detection output (min.)	V_{SOmin}	Data 0A = 00	150	256	350	mV[rms]
SIF pull-in range	f_{SP}		3.3	—	5.7	MHz
AV SW circuit						
Video SW voltage gain	G_{VSW}	f = 1 MHz, V_{IN} = 1 V[p-p]	6.2	7.2	8.2	dB
Video SW frequency characteristics	f_{VSW}	Frequency of output −3 dB from 1 MHz	10	—	—	MHz
Audio SW voltage gain	G_{ASW}	Data 0 F–D5 = 1 (external) f = 400 Hz, V_{IN} = 1 V[p-p]	−3	−1	1	dB
Video signal processing circuit (In the following test conditions, the measurements are made withinput: 2.0 V[p-p] (V_{WB} = 1.43 V[0-p]stair-step) at G_{OUT}.)						
Video output (typ.)	V_{YO}	Data 03 = 40 (typ.) (Contrast)	1.9	2.4	2.9	V[0-p]
Video output (max.)	V_{YOmax}	Data 03 = 7 F (max.)	3.8	4.8	5.8	V[0-p]
Video output (min.)	V_{YOmin}	Data 03 = 00 (min.)	0.07	0.3	0.6	V[0-p]
Contrast variable range	$Y_{Cmax/min}$	$\frac{03 = 7F}{03 = 00}$	19	22	26	dB
Video frequency characteristics	f_{YC}	Data 0F–D7 = 0 (Trap Off) Data 04 = 00 (Sharpness) Frequency to become −3 dB from f = 0.5 MHz	6.0	8.0	10.0	MHz
Sharpness variable range	$Y_{Smax/min}$	$\frac{04 = 3F}{04 = 00}$ f = 3.8 MHz Data 0F − D7 = 0	7	10.5	14	dB
Pedestal level (typical)	V_{PED}	Data 02 = 80 (typ.) (Brightness)	2.4	3.0	3.6	V
Pedestal variable width	ΔV_{PED}	Difference between Data 02 = 00 and FF	2.2	2.6	3.0	V
Brightness control sensitivity	ΔV_{BRT}	Average amount of change per 1 step, when Data 02 = 60 and A0	9.5	12.5	15.5	mV/Step
ACL sensitivity	ACL	Change of Y_{OUT} from V_{13} = 3.0 V to 3.5 V	2.3	2.9	3.6	V/V
Blanking level	V_{YBL}	DC voltage of blanking pulse	0.9	1.4	1.9	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video signal processing circuit (continued)		(In the following test conditions, the measurements are made with input: 2.0 V[p-p] (V_{WB} = 1.43 V[0-p] stair-step) at G_{OUT}.)				
Video input clamp current	I_{YCLP}	DC measurement: Sink current inside IC	5	10	15	µA
ACL start point	V_{ACL}	V_{13} voltage at which output amplitude becomes 90% when ACL pin (V_{13}) is being decreased from 5 V.	3.5	4.0	4.5	V
Color signal processing circuit		(In the following test conditions, burst = 300 mV[p-p], reference is B_{OUT})				
Color difference output (typ.)	V_{CO}	Input: Color bar Data 00 = 40 (typ.), 03 = 40 (typ.)	2.8	3.5	4.2	V[p-p]
Color difference output (max.)	V_{COmax}	Data 00 = 7 F one side amplitude Data 03 = 40	2.3	3.4	—	V[0-p]
Color difference output (min.)	V_{COmin}	Data 00 = 00, Data 03 = 40	0	—	100	mV[p-p]
Contrast variable range	$C_{Cmax/min}$	$\frac{03 = FF}{03 = 00}$ Data 00 = 40	15	20	25	dB
ACC characteristics 1	ACC1	Burst 300 mV[p-p]→600 mV[p-p] Input: Color bar	0.8	1.0	1.2	Time
ACC characteristics 2	ACC2	Burst 300 mV[p-p]→60 mV[p-p] Input: Color bar	0.7	1.0	1.2	Time
Tint center	$\Delta\theta_C$	Difference (Tint) between Data 01 = 40 and that of tint adjusted at center	−13	0	13	STEP
Tint variable range 1	$\Delta\theta_1$	Data 01 = 7F	30	45	60	deg
Tint variable range 2	$\Delta\theta_2$	Data 01 = 00	−60	−45	−30	deg
Demodulation output ratio (R)	R/B	Input: Rainbow	0.81	0.95	1.09	Time
Demodulation output ratio (G)	G/B	Input: Rainbow	0.3	0.36	0.42	Time
Demodulation output angle (R)	∠R	Input: Rainbow	92	104	116	deg
Demodulation output angle (G)	∠G	Input: Rainbow	223	235	237	deg
APC pull-in range (H)	f_{CPH}		450	900	—	Hz
APC pull-in range (L)	f_{CPL}		—	−900	−450	Hz
RGB processing circuit						
Pedestal difference voltage	ΔV_{IPL}	Difference voltage of RGB out pedestal	− 0.3	—	0.3	V
Brightness voltage tracking	ΔT_{BL}	Ratio of R, G, B out fluctuation level for Data 02 (Bright) 02 = 40 to C0	0.9	1.0	1.1	Time
Video voltage gain relative ratio	ΔG_{YC}	Output ratio of R, B out to G_{OUT}	0.8	1.0	1.2	Time
Video voltage gain tracking	ΔT_{CONT}	Gain ratio of R, G, B out for Data 03 (Contrast) 03 = 20 to 60	0.9	1.0	1.1	Time/ Time
Drive adjustment range	G_{DV}	AC change amount of R, B out between drive adjustment max. and min.	5.9	7.1	8.3	dB

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
RGB processing circuit (continued)						
Cutoff adjustment range	V_{CUTOFF}	DC change amount of R, G, B out between drive adjustment max. and min.	1.8	2.4	3.0	V
Y_S threshold voltage	V_{YS}	Minimum DC voltage at which Y_S turns on	2.7	3.1	3.6	V
Y_M threshold voltage	V_{YM}	Minimum DC voltage at which Y_M turns on	0.7	1.0	1.3	V
Y_M operating voltage gain	ΔG_{YM}	Y_M on/off gain difference	−12	−9	−6	dB
External RGB pedestal voltage	V_{EPL}	Y_S is on	2.1	2.7	3.3	V
External RGB pedestal difference voltage	ΔV_{EPL}	Y_S is on, R−G, G−B	−250	—	250	mV
Internal/external pedestal difference voltage	$\Delta V_{PL/IE}$	Internal−external	−100	200	500	mV
External RGB output voltage	V_{ERGB}	Input 3 V[p-p], contrast 03 =7 F	1.2	1.7	2.2	V[0-p]
External RGB output difference voltage	ΔV_{ERGB}	Input 3 V[p-p], contrast 03 = 7F	− 0.6	0	0.6	V
External RGB contrast variable range	$E_{Cmax/min}$	$\frac{03 = 7F}{03 = 00}$	5	8	11	dB
External RGB frequency characteristics	f_{RGBC}	Input 0.2 V[p-p], DC = 1 V	8	12	—	MHz
Synchronizing signal processing circuit						
Horizontal free-running oscillation frequency	f_{HO}	Without sync. signal input	15.4	15.75	16	kHz
Horizontal pull-in range	f_{HP}	Difference from f_H = 15.75 kHz	±500	±650	—	Hz
Vertical free-running oscillation frequency	f_{VO-N}	Without sync. signal input	58	60	62	Hz
Vertical output pulse width	τ_{VO}		5.5	6.5	7.5	$1/f_H$
Picture center variable range	ΔT_{HC}	Change amount of phase difference between H_{SYNC} and H_{OUT} Data from 0E: 00 to 1F	5.9	7.3	9.1	µs
I^2C interface						
SCL, SDA signal input high level	V_{IHI}		3.1	—	5.0	V
SCL, SDA signal input low level	V_{ILO}		0	—	0.9	V
Allowable maximum input frequency	f_{Imax}		100	—	—	kbit/s

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF Circuit (Typical input f_P = 45.75 MHz, V_{IN} = 90 dBµ)						
Input sensitivity	V_{PS}	Input level to become V_{PO} = −3 dB	—	52	60	dBµ

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF circuit (continued) (Typical input f_P = 45.75 MHz, V_{IN} = 90 dBμ)						
Maximum allowable input	V_{Pmax}	Input level to become V_{PO} = +1 dB	104	110	—	dBμ
SN ratio	SN_P		50	53	—	dB
Differential gain	DG_P		0	3	5	%
Differential phase	DP_P		0	3	5	deg
Black noise detection level	ΔV_{BN}	Difference from sync. peak value	−55	−45	−35	IRE
Black noise clamp level	ΔV_{BNC}	Difference from sync. peak value	35	45	55	IRE
RF AGC operation sensitivity	G_{RF}	Input level difference to become V_{22} = 1 V→7 V	0.5	1.5	3.0	dB
VCO switch on drift	Δf_{PD}	Frequency drift from 5 seconds after SW On to 5 mins. after	—	70	—	kHz
Intermodulation	IM	V_{FC}–V_{FP} = −2 dB, V_{FS}–V_{FP} = −12 dB	46	52	—	dB
RF AGC adjustment sensitivity	S_{RF}	Average amount of change of output voltage V_{22} for Data 1Step	1.0	1.7	2.5	V/Step
AFT offset adjustment sensitivity	S_{AFT}	Average amount of change of output voltage V_{31} for Data 1Step	0.15	0.2	0.25	V/Step
Video detection output fluctuation with V_{CC}	$\Delta V_{P/V}$	V_{CC} = ±10%	—	±10	±15	%
Video detection output-temperature characteristics	$\Delta V_{P/T}$	T_a = −20°C to +70°C	—	±5	±10	%
Input resistance (pin 19, 20)	$R_{I19,20}$	f = 45.75 MHz	—	1.2	—	kΩ
Input capacitance (pin 19, 20)	$C_{I19,20}$	f = 45.75 MHz	—	4.0	—	pF
Sound IF output level	V_{SIF}	f_S = 45.75 MHz–4.50 MHz, P/S = 20 dB	94	100	106	dBm
VCO control sensitivity 1	β_{PU}	DV_{34} = 2.0 V–3.8 V, f = 45.75 MHz	1.3	2.2	3.1	kHz/mV
VCO control sensitivity 2	β_{PJ}	DV_{34} = 2.0 V–3.8 V, f = 58.75 MHz	1.3	2.2	3.1	kHz/mV
RF AGC delay point -temperature characteristics	$\Delta V_{DP/T}$	T_a = −20°C to +70°C	0	3	5	dB
VCO free-running frequency -temperature characteristics	$\Delta f_{P/T}$	T_a = −20°C to +70°C	—	300	—	kHz
AFT center frequency -temperature characteristics	$\Delta f_{AFT/T}$	T_a = −20°C to +70°C Input frequency at which AFT output voltage becomes 4.5 V	—	300	—	kHz
VCO free-run adjustment	V_{AFTADJ}	AFT center voltage adjustment	—	4.5	—	V
VCO free-running frequency 1	Δf_{P1}	Dispersion without V_{IN}. V_{29} (IF AGC) = 0 V (Difference from 45.75 MHz is measured)	−300	0	300	kHz

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIF circuit (continued) (Typical input f_P = 45.75 MHz, V_{IN} = 90 dBμ)						
VCO free-running frequency 2	Δf_{P2}	Dispersion without V_{IN}. V_{29} (IF AGC) = 0 V (Difference from 58.75 MHz is measured)	−300	0	300	kHz
APC pull-in range (Hj)	f_{PPHJ}	High band side pull-in range (Difference from f_P = 58.75 MHz)	1.0	1.5	—	MHz
APC pull-in range (Lj)	f_{PPLJ}	Low band side pull-in range (Difference from f_P = 58.75 MHz)	—	−1.5	−1.0	MHz
Detection output resistance	R_{O33}	DC measurement	70	120	170	Ω
SIF circuit (Typical input f_S = 4.5 MHz, f_M = 400 Hz, V_{IN} = 90 dBμ)						
Input limiting level	V_{LIM}	Input level to become V_{SOP} = −3 dB	—	44	50	dBμ
AM rejection ratio	AMR	AM = 30%	60	70	—	dB
Total harmonic distortion	THD	Df = ±50 kHz	0	0.3	0.5	%
SN ratio	SN_A		50	55	—	dB
Audio detection output linearity	ΔV_{SOP}	Ratio of Δf = ±50 kHz to Δf = ±25 kHz	5	6	7	dB
Audio output fluctuation with V_{CC}	$\Delta V_{S/V}$	V_{CC} = ±10%	—	±3	±6	%
Audio output-temperature characteristics	$\Delta V_{S/T}$	T_a = −20°C to +70°C	—	±5	±10	%
Audio output-frequency characteristics 1	f_{SOP1}	APC pin C = 100 pF	100	—	—	kHz
Audio output-frequency characteristics 2	f_{SOP2}	APC pin C = 5600 pF	—	2.2	—	kHz
AV SW circuit						
Video SW crosstalk	CT_{VSW}	f = 1 MHz, V_{IN} = 1 V[p-p], Inside→Outside, Outside→Inside	—	−60	−50	dB
Video SW external input terminal voltage	V_{25}	DC measurement	1.3	1.6	1.9	V
Video SW internal input terminal voltage	V_{32}	DC measurement	1.3	1.6	1.9	V
Video SW internal output DC voltage	V_{30I}	DC measurement Data 04–D6 = 0	3.4	4.2	5.0	V
Video SW external output DC voltage	V_{30E}	DC measurement Data 0F–D5 = 1	3.4	4.2	5.0	V
Video SW input resistance	$R_{I25, 32}$	DC measurement	—	524	—	Ω
Video SW output resistance	R_{O30}	DC measurement	20	50	100	Ω

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AV SW circuit (continued)						
Audio SW crosstalk (Internal→External)	CT_{AIE}	f_S = 4.5 MHz, f_M = 400 Hz, No external input	—	−73	−67	dB
Audio SW crosstalk (External→Internal)	CT_{AEI}	f_S = 4.5 MHz, f_M = 0 Hz, External f = 400 Hz, V_{IN} = 600 mV[rms]	—	−73	−67	dB
Audio SW input terminal voltage	V_{27}	DC measurement	3.7	4.2	4.7	V
Audio SW internal output DC voltage	V_{24I}	DC measurement	3.7	4.2	4.7	V
Audio SW external output DC voltage	V_{24E}	DC measurement	3.7	4.2	4.7	V
Audio SW internal/external DC difference voltage	ΔV_{24}	DC measurement	−300	0	300	mV
Audio SW input resistance	R_{I27}	DC measurement	61	72	83	kΩ
Audio SW output resistance	R_{O24}	DC measurement	200	400	600	Ω
Video signal processing circuit (In the following test conditions, the measurements are made with input 2.0 V[p-p] (V_{WB} = 1.43 V[0-p]) G_{OUT})						
Y signal delay time 1	T_{DL1}	Phase difference from Y-input (For both trap on/off)	620	690	760	ns
Y signal delay time 2	T_{DL2}	Phase difference from Y-input (Trap through)	—	200	—	ns
Black level extension 1	V_{BL1}	Input: Total black, difference between pin 38 of 9 V and open (With RC filter)	−100	0	100	mV
Black level extension 2	V_{BL2}	Input: Total black, pin 38 GND and black slice potential V_{43} = 2.5 V	700	900	1 300	mV
Black level extension 3	V_{BL3}	Voltage difference between pin 38 open and 9V. Black slice potential V_{43} = 2.5 V	400	600	800	mV
Contrast variation with sharpness	DV_{CS}	Y_{OUT} output level difference between sharpness max. and min.	−300	0	300	mV
Contrast variation with sharpness	DV_{BS}	Pedestal level DC difference between sharpness max. and min.	−250	0	250	mV
Input dynamic range	V_{Imax}	Contrast 03 = 40	2.8	—	—	V[p-p]
Y signal SN ratio	SN_Y	Contrast 03 = 7F	51	56	—	dB
Black level extension start point	V_{BLS}	Start point when V_{43} = 4.5 V	50	57	64	IRE
Trap on/off through-gain difference	DG_{TRAP}	Trap on/off/through	−1	0	1	dB
Trap frequency error	Df_{TRAP}	Trap center frequency at chroma input 3.58 MHz	−70	0	70	kHz
Trap attenuation amount	Att_{TRAP}	3.58 MHz component attenuation amount at chroma input 3.58 MHz	26	30	—	dB

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Video Signal Processing Circuit (continued) (In the following test conditions, the measurements are made with input 2.0 V[p-p] (V_{WB} = 1.43 V[0-p]) G_{OUT})						
Trap automatic adjustment range	f_{TRAP}	VCO frequency of $\Delta f_{TRAP} \leq$ 70 kHz	3	—	4	MHz
Video output fluctuation with V_{CC}	$\Delta V_{Y/V}$	V_{CC1} = 9 V (allowance: ±10%)	0	100	250	mV/V
Video output-temperature characteristics	$\Delta V_{Y/T}$	T_a = −20°C to +70°C	0	5	10	%
YNR operation I	SN_{YNR}	S/N, when YNR: min.→max. and sharpness max.	—	−4	—	dB
YNR operation II	SN_{YNR} (IFAGC)	Sharpness max., YNR: max. S/N at IF AGC 2 V→4 V	—	−1.5	—	dB
ABL sensitivity	ABL	01–D7 = 1, when V_{13} = 1.5 V→3.5 V Pedestal level fluctuation	0.3	0.5	0.7	V/V
White gradation correction 1	γ_1	White detection pin V_{17} = 4.5 V Difference of amplitude between G_{OUT} gamma on/off	120	125	130	%
White gradation correction 2	γ_2	White detection pin V_{17} = 2.0 V Difference of amplitude between G_{OUT} gamma on/off	70	75	80	%
Neck protector threshold voltage	V_{NP}		0.3	0.5	1.0	V
DC restoration ratio	T_{DC}	APL 10% to 90% $T_{DC} = \frac{\Delta_{AC} - \Delta_{DC}}{\Delta_{AC}} \times 100$	90	100	110	%
Color signal processing circuit (Burst 300 mV[p-p], reference is B_{OUT})						
Demodulation output residual carrier	V_{CAR}	f_{SC} level of pin 8, 9, 10	0	—	50	mV[p-p]
VCO free running frequency	f_{CN}	Difference from f = 3.579545 MHz	−300	0	300	Hz
f_{CO} fluctuation with V_{CC}	$\Delta V_{C/V}$	V_{CC1} = 9 V (allowance: ±10%)	−300	0	300	Hz
Static phase error	$\Delta\theta_N$	Tint shift at Δf_C = −300 to +300 Hz change	—	1	3	deg/100 Hz
Demodulation output bandwidth	f_{CC}	Band to become −3 dB	400	600	800	kHz
Demodulation output fluctuation with V_{CC}	$\Delta V_{C/V}$	V_{CC1} = 9 V (allowance: ±10%)	—	±4	—	%
Demodulation output -temperature characteristics	$\Delta V_{C/T}$	T_a = −20°C to +70°C	—	±10	±20	%
Brightness variation with color	V_{BC}	Pedestal level DC difference between color max. and min.	−250	0	250	mV
Brightness variation difference voltage with color	ΔV_{BC}	R, G, B Out variation voltage difference	0	—	20	mV

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing circuit (continued) (Burst 300 mV[p-p], reference is B_{OUT})						
Color killer allowance 1	V_{KILL1}	0 dB = 300 mV[p-p], 00–D7 = 0	–53	–46	–39	dB
Color killer allowance 2	V_{KILL2}	0 dB = 300 mV[p-p], 00–D7 = 1	–50	–43	–36	dB
CW output level (3.58 MHz)	V_{CW}	AC component of (3.58 MHz)	0.6	1.1	1.4	V[p-p]
B.P.F. (Symmetrical) frequency characteristics	$f_{B.P.F.}$	Band to become –3 dB from 3.58 MHz	400	600	800	kHz
B.P.F. (Asymmetrical) slant	$V_{B.P.F./f}$	Slant of 3.58 MHz ±500 kHz	—	9.0	—	dB/MHz
RGB processing circuit						
(C–Y)/Y	$R_{C/Y}$	Color bar input, B_{OUT} Contrast typ. color Data 00 = 60	0.9	1.2	1.5	V[0-p]/ V[p-p]
(C–Y), Y delay difference	$\Delta T_{C/Y}$	Color bar input, B_{OUT} Phase of green→magenta	–100	0	100	ns
Y_S changeover speed	f_{YS}	f_{YS}, when external input is 3 V, output level –3 dB	7	11	—	MHz
External RGB input dynamic range	V_{DEXT}	Contrast max. Data 03 = 7F	6.5	7.0	—	V[0-p]
Internal/external crosstalk	CT_{RGB}	Leakage when f = 1 MHz, 1 V[p-p], Y_S = 5 V	—	–60	–50	dB
Spot killer operation	V_{SPK}	V_9 at which spot killer turns on by decreasing V_9 from 9 V	7.3	7.7	8.0	V
Brightness variation with contrast	V_{BAC}	Pedestal level DC difference between contrast max. and min.	–250	0	250	mV
Brightness variation difference voltage with contrast	DV_{BAC}	R, G, B Out variation voltage difference	0	—	20	mV
Color /B&W DC difference voltage	DV_{CBW}	Pedestal level voltage difference between with and without burst signal	–60	0	60	mV
Pedestal level fluctuation with V_{CC}	$DV_{PL/V}$	V_{CC1} = 9 V (allowance: ±10%)	0	200	400	mV/V
Pedestal level-temperature characteristics	$DV_{PL/T}$	T_a = –20°C to +70°C	—	– 0.6	—	mV/°C
Pedestal level difference voltage fluctuation with V_{CC}	$DV_{PD/V}$	V_{CC1} = 9 V (allowance: ±10%) R–G, B–G	—	0	—	mV/V
External RGB output blanking voltage	V_{BLK}	Burst input only	0.8	1.3	1.8	V
RGB limiter control range 1	V_{BEAM1}	Input 2 V[p-p], contrast max. RGB limiter 0E = 70	6.4	6.7	7.0	V
RGB limiter control range 2	V_{BEAM2}	Input 2 V[p-p], contrast max. RGB limiter 0E = F0	5.6	6.0	6.4	V

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Synchronizing signal processing circuit						
Horizontal output start voltage	V_{fHS}	Minimum V_{46}, when H osc. output is 1 V[p-p] or more and f_0 becomes >10 kHz	3.9	4.4	4.9	V
Lock detection output voltage 1	V_{LD1}	V_{11}, when horizontal AFC is locked	3.8	4.3	4.8	V
Lock detection output voltage 2	V_{LD2}	V_{11}, when horizontal AFC is unlocked.	0	0.1	0.5	V
Lock detection charge and discharge current	I_{LD}	DC measurement	±0.5	±0.7	±1.1	mA
EBP (BLK) slice level	V_{FBP}	Minimum voltage of pin 45, when blanking is applied to RGB output	0.3	0.66	1.0	V
EBP (AFC2) slice level	V_{FBPH}	Minimum voltage of pin 45, when AFC2 operates	1.45	1.85	2.25	V
Horizontal AFC μ	μ_H	DC measurement	26	33	40	μA/μs
Horizontal VCO β	β_H	β curve gradient near f = 15.75 kHz	1.4	1.8	2.2	Hz/mV
Burst gate pulse position	P_{BGP}	Delay from H_{SYNC} rise	0.2	0.4	0.6	μs
Burst gate pulse width	W_{BGPN}		2.5	3.0	3.5	μs
V blanking pulse width	W_{VN}	Pulse width, when f_H = 15.75 kHz	1.04	1.14	1.24	ms
EBP allowable range	T_{FBP}	Time from H_{OUT} rise to FBP center	12	—	19	μs
Overvoltage protective operation voltage	V_{XRAY}	Dispersion from the minimum voltage at which H osc. comes to be out of synchronization	–60	—	60	mV
Black-out operation voltage	V_{BLOUT}	Difference voltage from hold-down to black out	10	110	160	mV
H_{SYNC2} output level	V_{SCP}	H_{SYNC2} output DC level	8.0	8.2	8.4	V
H_{SYNC2} output width	W_{SCP}	H_{SYNC2} output pulse width	—	2	—	μs
H_{SYNC2} output position	P_{SCP}	The period of time from H_{SYNC} center to H_{SYNC2} rise	—	3	—	μs
Horizontal output pulse duty cycle	t_{HO}	Upward going pulse duty cycle	32	38	44	%
Horizontal output voltage (high)	V_{50H}	High level DC voltage	2.8	3.1	3.4	V
Horizontal output voltage (low)	V_{50L}	Low level DC voltage	0	—	0.3	V
Vertical output voltage (high)	V_{52H}	High level DC voltage	3.9	4.2	4.5	V
Vertical output voltage (low)	V_{52L}	Low level DC voltage	0	—	0.3	V
Synchronizing signal clamp voltage (Ver.)	V_{39}	V_{39} clamp voltage	3.2	3.6	4.0	V
Synchronizing signal clamp voltage (Hor.)	V_{41}	V_{41} clamp voltage	3.2	3.6	4.0	V
External blanking input threshold level	V_{16I}		0.4	0.75	1.1	V
Vertical pull-in range	f_{VP-N}	f_H = 15.75 kHz	56	—	64	Hz

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C interface						
Sink current when ACK	I_{ACK}	Maximum value of sink current for pin 14 at ACK	1.8	2.5	5.0	mA
Bus free before start	t_{BUF}		4.0	—	—	µs
Start condition set-up time	$t_{SU, STA}$		4.0	—	—	µs
Start condition hold time	$t_{HD, STA}$		4.0	—	—	µs
Low period SCL,SDA	t_{LOW}		4.0	—	—	µs
High period SCL	t_{HIGH}		4.0	—	—	µs
Rise time SCL,SDA	t_R		—	—	1.0	µs
Fall time SCL,SDA	t_F		—	—	0.35	µs
Data set-up time(write)	$t_{SU, DAT}$		0.25	—	—	µs
Data hold time(write)	$t_{HD, DAT}$		0	—	—	µs
Acknowledge set-up time	$t_{SU, ACK}$		—	—	3.5	µs
Acknowledge hold time	$t_{HD, ACK}$		0	—	—	µs
Stop condition set-up time	$t_{SU, STO}$		4.0	—	—	µs
DAC						
3, 4, 5, 6, 7-bit DAC DNLE	$L_{3, 4, 5, 6, 7}$	1LSB = {Data (max.)–Data (00)} /7, 15, 31, 63, 127	0.1	1.0	1.9	LSB/Step
8-bit DAC DNLE	L_8	1LSB = {Data (FF)–Data (00)}/255	0.1	1.0	1.9	LSB/Step
Cut-Off DAC overlap	D_{STEP}	Overlap of 8-bit 2-stage changeover of R, B cut-off (Same for AFT)	27	32	37	Step

• Standard conditions when testing

1. Input signal
   1) VIF : f_P = 45.75 MHz, V_{IN} = 90 dBµ, at video modulation: Modulation signal is 10-staircase Modulation m = 87.5%, pin 19 input level 84 dBµ when V_{IN} = 90 dBµ
   2) SIF : f_S = 4.5 MHz, V_{IN} = 90 dBµ, modulation signal f_M = 400 Hz, deviation: NTSC ±25 kHz
   3) Video : 10-staircase 2 V[p-p] (V_{BW} = 1.43 V[0-p])
   4) Chroma : Color bar signal: Burst level 300 mV[p-p]
      Rainbow signal : Burst level 300 mV[p-p]
   5) Sync. signal: Video signal 1.5 V[p-p] to 2.5 V[p-p] for both horizontal and vertical sync. signal input

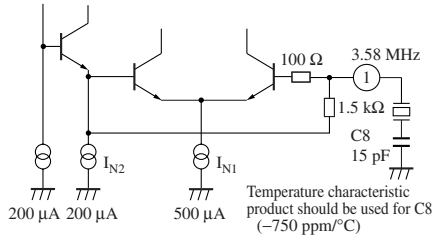
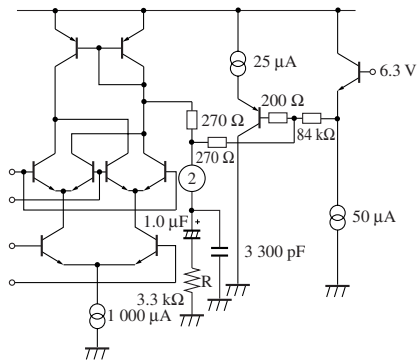
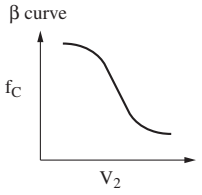
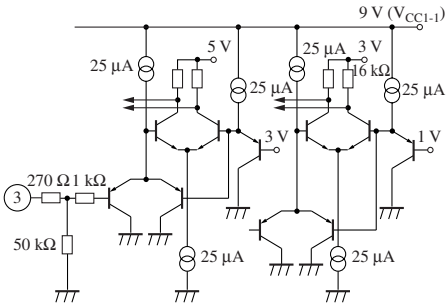
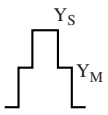
■ Electrical Characteristics at T_a = 25°C (continued)

• Standard conditions when testing (continued)

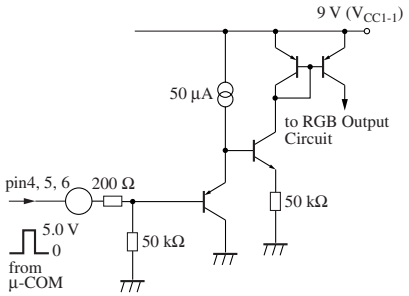
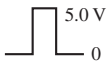
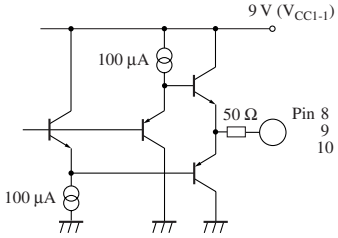
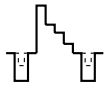
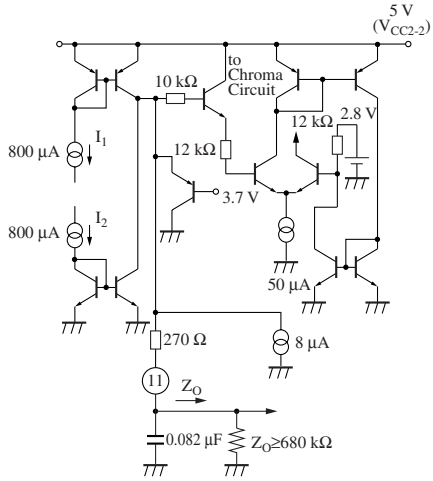
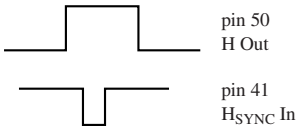
2. I^2C BUS condition

Sub Address		Data (H)	Sub Address		Data (H)
00	Color	40	08	Drive R	40
01	Tint	40	09	Drive B	40
02	Bright	80	0A	Audio Adj, YNR	10
03	Contrast	40	0B	AFT	10
04	Sharpness	00	0C	RFAGC	40
05	Cut-off R	80	0D	Video Adj	08
06	Cut-off G	40	0E	H center, RGB limiter	10
07	Cut-off B	80			

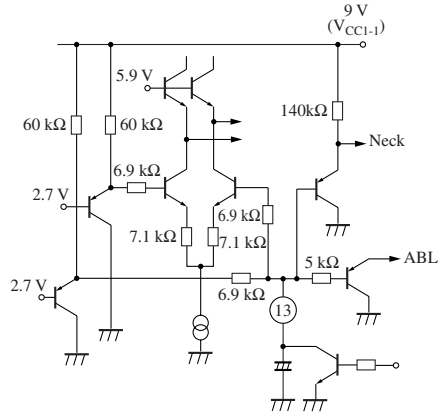
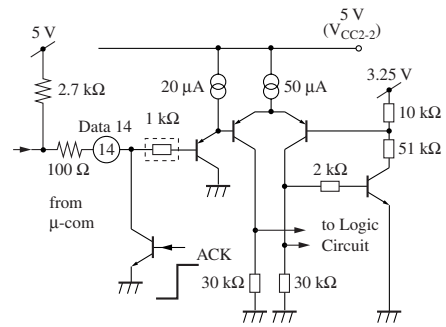
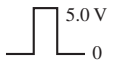
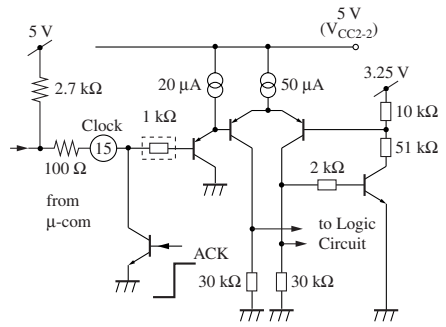
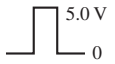
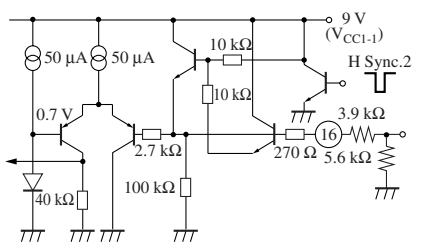
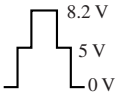
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1		Chroma oscillation pin (3.58 MHz) • Pin for chroma oscillation of 3.58 MHz. • The pattern between pin and oscillator should be made as short as possible.	AC $f = f_C$ approx. 0.3 V[p-p]
2		APC filter pin • Filter pin for APC detection circuit (Operates for BGP period) • Detection sensitivity becomes high when external R→Large (Tends to be easily pulled in and afffected by noise.) 	DC approx. 5.6 V
3		Y_S/Y_M input pin • Fast blanking pulse input pin for OSD • Y_M On (Half-tone) at 1.0 V[0-p] or higher • Y_S ON(OSD input) at 3.0 V[0-p] or higher • Recommended use range: 0 V to 6 V	AC (Pulse) 

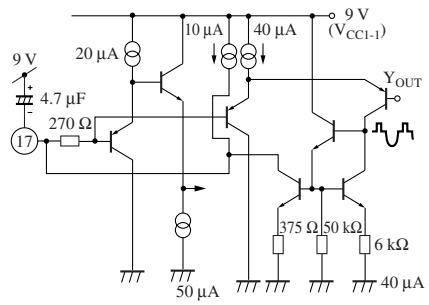
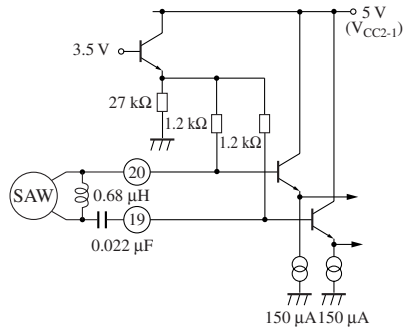
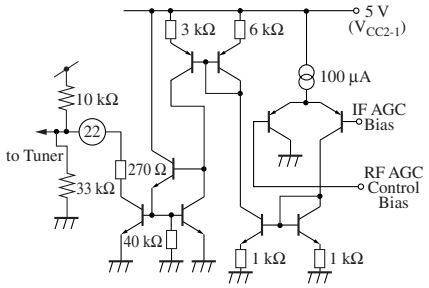
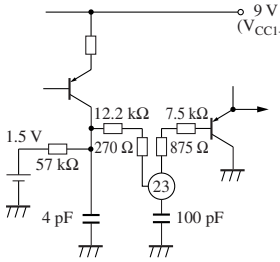
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
4 5 6		External R input pin External G input pin External B input pin • External input pin for OSD • Output linearly changes according to input level • Recommended use range: 0 V to 6 V	AC (Pulse) 
7	—	V_{CC1-1} (typ.9 V) • Video circuit • Chroma circuit • RGB circuit • Sync. circuit • DAC circuit	DC 9 V
8 9 10		R Out pin G Out pin B Out pin • BLK level approx. 1.5 V • Black (Pedestal) level approx. 3.0 V • Recommended use range: −2.4 mA to +4.8 mA	AC 
11		Horizontal sync. detection pin • Phase of horizontal synchronizing signal and horizontal output pulse are detected and outputted • Pin 11 becomes low at out of synchronization • Color control becomes min. and chroma output disappears and V_{OUT} goes into free-running state in a asynchronous condition • Pay attention to impedance when pin 11 voltage is used for microcomputer ($Z_O \geq 680$ kΩ required)  • H_{SYNC} period, when pin 50 at high: I_1 ON at low: I_2 ON	DC when synchronized 4.5 V when asynchronous 0.1 V
12	—	GND • RGB circuit • DAC. I^2C circuit • VIF (VCO) circuit	DC

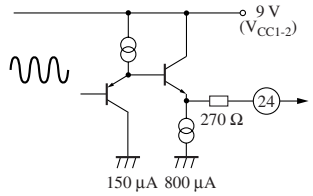
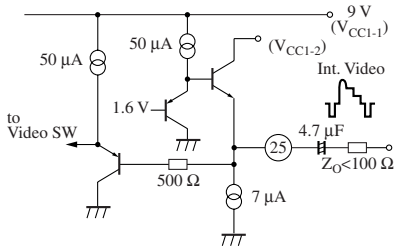
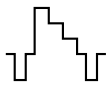
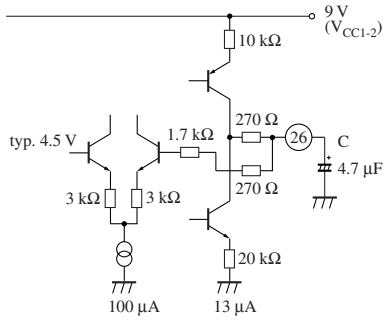
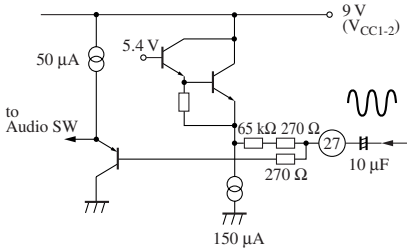
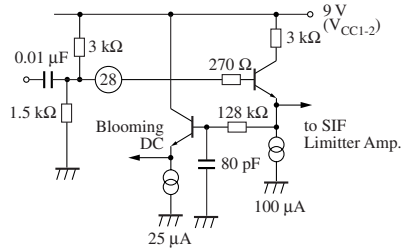
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
13		ACL/ABL pin • RGB output is blacked out when DC voltage of pin 13 is decreased from the outside. However, it is not blacked out when service switch has been turned on. (Service switch priority) • When 01–D7 = 1, ABL functions, and brightness decreases by lowering DC voltage of pin 13 • When pin 13 is grounded, ACC gain becomes min. and it is possible to measure chroma free-running frequency. Measuring point is pin 51. • Recommended use range: 0 V to V_{CC1}	DC approx. 3.5 V
14		I^2C BUS Data input pin • Input low level: 0.9 V or less • Input high level: 3.1 V or more • ACK sink capability: 1.8 mA • Recommended use range: 0 V to V_{CC2}	AC (Pulse) 
15		I^2C clock input pin • Input low level: 0.9 V or less • Input high level: 3.1 V or more • Recommended use range: 0 V to V_{CC2}	AC (Pulse) 
16		External blanking input pin • RGB out blanking is applied when a voltage of 0.8 V or more is applied • H_{SCP} pulse output pin Horizontally synchronized 2 μs pulse is outputted. • Recommended use range: – 0.8 mA to 0.2 mA, 0 V to 5.0 V	AC (Pulse) 

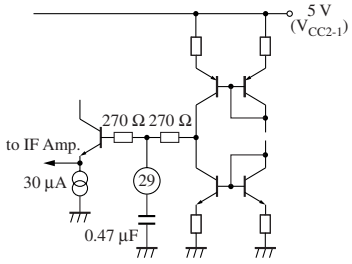
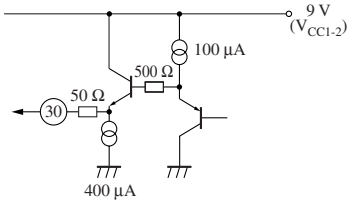
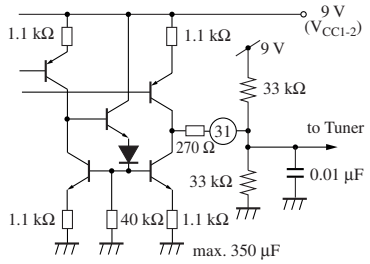
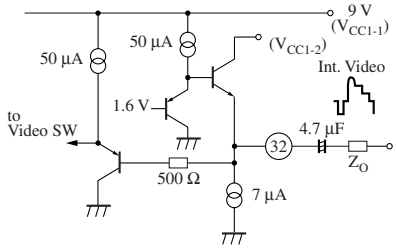
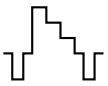
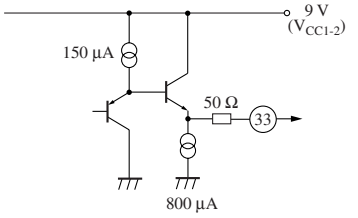
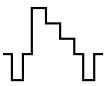
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
17		White Peak Detect Filter input pin • White gradation correction response characteristic is determined. When there is screen sag, make C→larger When screen response is slow, make C→smaller	DC
18	—	V_{CC2-1} (typ.5 V) • VIF, SIF circuit	DC 5 V
19 20		VIF input pin 1 VIF input pin 2 • VIF amp. input with balanced input • Input max.120 dBµ Input resistance: 1.2 kΩ (45.75 MHz) Input capacitance: 4.0 pF (45.75 MHz)	AC $f = f_P$ DC level approx. 2.7 V
21	—	GND • For VIF and SIF circuit	DC
22		RF AGC output pin • Collector open output • Recommended use range: 0 V to V_{CC1} (9 V) Maximum sink current min.: 1.5 mA	DC
23		SIF APC filter pin • Filter pin for APC circuit of SIF. • Deemphasis characteristic is changeable by the capacitor between pin and GND	DC approx. 2.5 V

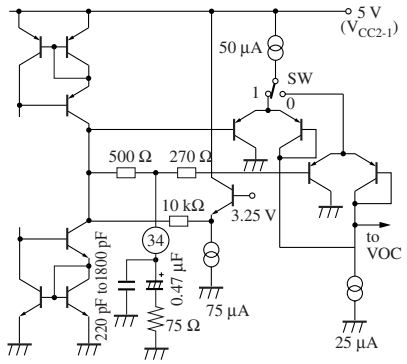
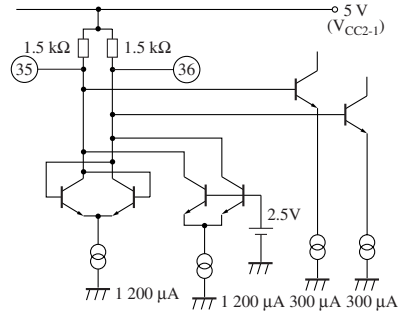
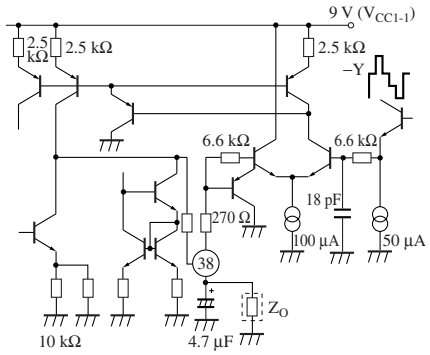
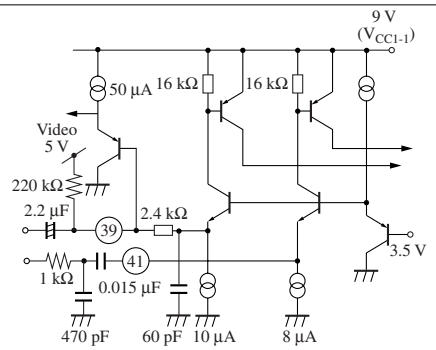
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
24		Audio output pin • DC fluctuates by internal/external changeover • Recommended use range: – 0.8 mA to + 0.8 mA	AC 0 kHz to 20 kHz DC approx. 3.9 V
25		External video input pin • Input pin for external video signal and DC cut input • Typical: 1 V[p-p] (max. 1.5 V[p-p]) • Z_O is 100 Ω or less	AC 1 V[p-p] (Composite)  DC approx. 1.6 V
26		Decoupling pin • S-curve in IC is wideband, but DC feedback is applied so that DC voltage of output signal becomes constant. • DC level (typ. 4.5 V), f_S→high: V_{26}→low • If C (4.7 µF) is too small, sound distortion tends to become larger at low frequency.	DC
27		External audio input pin • Input pin for external audio signal. DC cut input. • Adjust typical input level to internal sound level. • Input max. 7 V[p-p]	AC 0 kHz to 20 kHz
28		SIF signal input pin • Input max. 110 dBµ Blooming DC adjusting pin • White gradation correction curve and bias to determine absolute clip point are provided. (2.0 V to 4.5 V) • Recommended use range: 0 V to V_{CC1} (9 V)	AC $f = f_S$ DC approx. 2.3 V

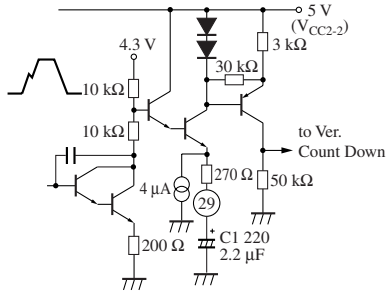
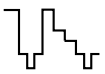
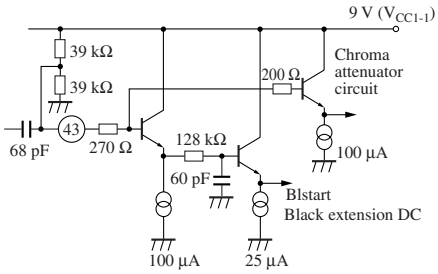
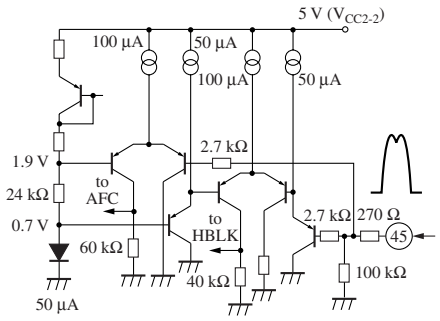
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
29		IF AGC filter pin • Pin for IF AGC filter. The current obtained from peak AGC circuit is smoothed by external capacitor. • Since response becomes faster when C goes smaller, hum characteristic will be improved. However, sag tends to appear easily.	DC approx. 2 V
30		Video output pin • INT.Video or EXT.Video selected by AV SW is outputted. • Recommended use range −3.2 mA to +0.4 mA	AC 2 V[p-p]  DC level approx. 4.2 V
31		AFT output pin • Offset of center voltage is adjusted by bus • When AFT defeat SW is turned on (0B = 00), V_{31} becomes a value determined by external resistance-divider. • µ of AFT is variable by impedance of externally attached resistor.	DC
32		Internal video input pin • Input pin for signal detected by VIF circuit (Internal video signal). • DC cut input Typical input: 1 V[p-p] (max. 1.5 V[p-p]) $Z_O \cong 280\ \Omega$	AC 1 V[p-p] (Composite)  DC level approx. 1.6 V
33		VIF detection output pin • Adjusted to center value by I^2C bus (Using upper 4-bit of 0 A) DC voltage becomes approx. 1 V at external video mode (04–D6 = 1) Recommended use range: −1.6 mA to + 0.8 mA	AC approx. 2.1 V[p-p] 

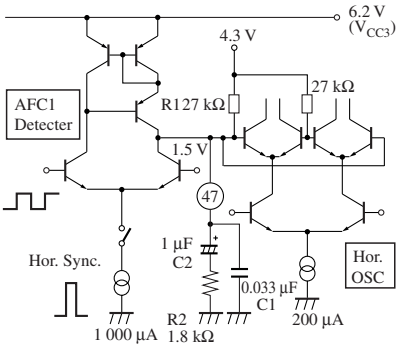
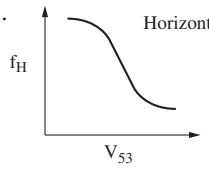
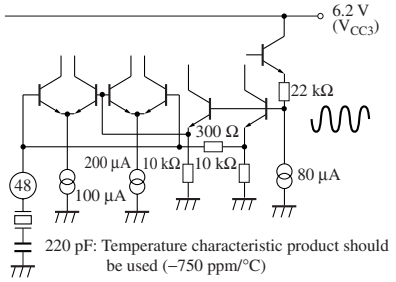
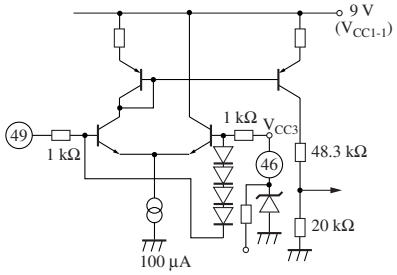
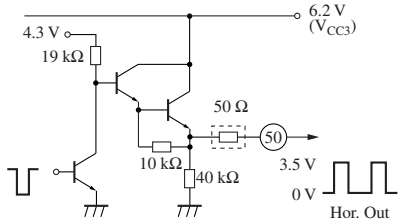
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
34		APC filter pin • Filter pin for VIF APC circuit. • Lock detection circuit for VCO is built in the IC inside to changeover the time constant for APC filter.	DC approx. 2.5 V
35 36		VIF oscillation pin • Oscillation coil is changed according to VIF frequency. • Allowable value of dispersion for coil resonance point is within 1%.	AC approx. 0.3 V[p-p] DC level approx. 3.9 V
37	—	V_{CC1-2} (typ.9 V) IF circuit	DC 9 V
38		Black level detection pin • Black level detection pin for black extension circuit • The most black Y-level except for blanking circuit is held. Black detection sensitivity drops when Z_O is made smaller, so that black detection becomes impossible unless a large black area.	DC approx. 5.1 V
39		Vertical sync. separation input pin Video input pin • Video signal input pin (Also composite video input) • Typical input: 2.0 V[p-p] • Sync. Top is clamped at 3.5 V • Video signal should be inputted at low impedance. (under 100 Ω)	AC 2.0 V[p-p] 

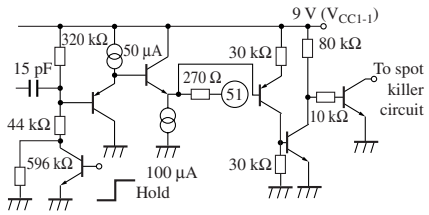
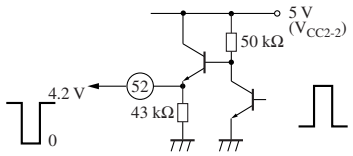
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
40		Vertical synchronizing signal clamp pin • Peak clamp pin for separating vertical sync. signal. • Integral amount of vertical sync signal itself has been determined by internal time constant. However, trigger application timing is determined by the selection of external constant C1.	AC $f = f_V$ 
41	—	Horizontal sync separation input pin • Internal circuit of pin 39 and 41 are the same. • When R→large, slice level becomes deeper (Weak to Sync compression). When R→ small, slice level becomes shallower (Weak to fluctuation such as Ver. Sag). • Sync. Top is clamped at 3.5 V.	AC 2 V[p-p] 
42	—	V_{CC2-2} (typ.5 V) For chroma, jungle circuit	DC 5 V
43		Chroma signal input pin Black extension start point adjusting pin • Pin 43 is chroma signal input pin, and black extension start point is adjusted by externally applied DC voltage. DC level: high ↔ low Start point: Shallow ↔ Deep Black extension effect: Small ↔ Large • Recommended use range: 0 V to V_{CC1} (9 V)	AC+DC Burst typ. 300 mV[p-p] DC typ. 4.5 V
44	—	GND • For video, chroma, jungle circuit	DC 0 V
45		FBP input pin • FBP input pin for horizontal blanking and AFC circuit • Threshold level HBLK: 0.7 V AFC: 1.9 V • A voltage input of 0 V or less is inhibited. • Recommended use range: 0 V to V_{CC2} (5 V)	AC FBP 
46	—	Horizontal stabilized power supply pin.	DC 6.2 V

■ Terminal Equivalent Circuits (continued)

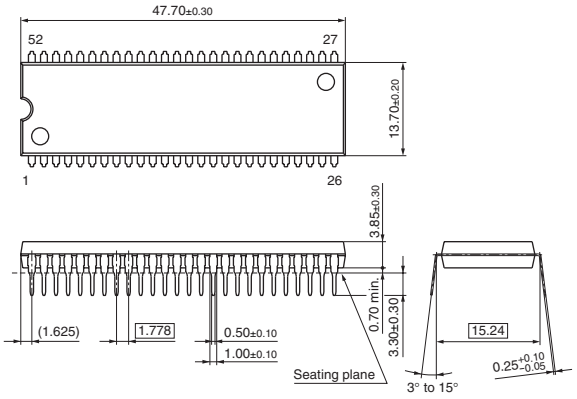
Pin No.	Equivalent circuit	Description	I/O
47		Horizontal AFC1 filter pin • The capacitor connected to pin 47 is charged and discharged after comparing the phase of horizontal synchronizing signal and pulse inside the IC. • R1, R2, C1 and C2 are lag lead filter for AFC1. 	DC typ. 4.3 V
48		Horizontal oscillation pin • Oscillation takes place at 32 × $f_H \cong 503$ kHz by ceramic oscillator. • Horizontal and vertical pulse are generated by count-down circuit inside the IC.	AC f = 32 f_H (approx. 500 kHz)
49		Overvoltage protection input pin • If increasing input pin voltage from 0 V at V_{REF} (pin 46) = 6.2 V; (1) Horizontal oscillation come to be out of synchronization: approx. 6.15 V (2) Blacked out: (1)+70 mV • Recommended use range: 0 V to V_{CC1} (9 V)	DC Normally 0 V
50		Horizontal pulse output pin • Duty cycle approx. 37% • Recommended use range: −6.4 mA to +0.1 mA	AC Pulse 

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
51		CW output pin / input pin for spot killer off. (Output amplitude 860 mV[p-p]) The pin also shares in Hold-down detection. • At normal: 6.1 V (DC) • At hold-down: 1.2 V (DC) • Apply 9 V(V_{CC1}) DC to turn off spot killer. Recommended use range: – 0.4 mA to + 0.1 mA 0 V to V_{CC1}	AC Approx. 830 mV[p-p]  f = 3.58 MHz
52		Vertical pulse output pin • Negative polarity, pulse width 6.25 H • Recommended use range: – 0.8 mA to + 0.1 mA	AC Pulse 

■ New Package Dimensions (Unit: mm)

• SDIP052-P-0600F (Lead-free package)



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