UMA1015M low power dual 1GHz frequency synthesizer

AN93016

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SUMMARY

This application note is a guide for designing a phase locked loop based on the Philips UMA1015M dual frequency synthesizer. The UMA1015M is a low power single chip solution to dual frequency synthesis in the range 50 MHz to 1100 MHz and is primarily intended for use in analog wireless communications equipment, such as 900 MHz cordless telephone, CT1, CT1+ and cellular radio telephone AMPS, TACS and NMT.

A basic loop filter design method is discussed. Following this procedure a dual synthesizer at 900 MHz is designed and measurement results are presented.

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1 INTRODUCTION TO UMA1015M DUAL SYNTHESIZER

1.1 General Description

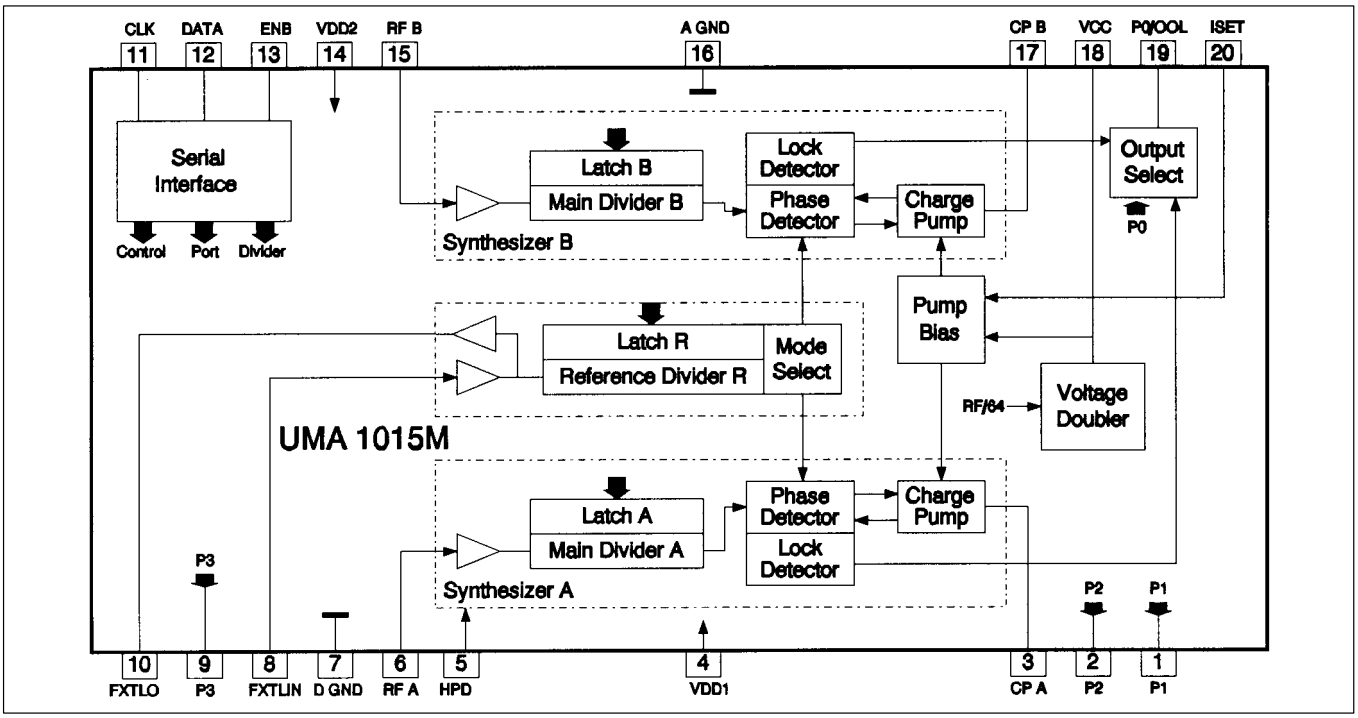


Figure 1. UMA1015M Dual Synthesizer for Mobile Radio Communications

The UMA1015M [1] is a low power dual frequency synthesizer for radio communications which operates in the 50 to 1100 MHz frequency range. Each synthesizer consists of a fully programmable main divider, a phase and frequency detector and a charge pump. There is a fully programmable reference divider common to both synthesizers which operates up to 35 MHz. The IC is programmed via a 3-wire serial bus which works up to 10 MHz. The programmable charge pump currents are fixed by an external resistance at pin I_{SET}. The BiCMOS device is designed to operate from 2.6 (3 Ni-Cd cells) to 5.5V. Each synthesizer can be powered down independently via the bus to save current. It is also possible to power down the chip via the pin HPD.

1.2 FEATURES

- Two synthesizers in one package
- Integrated prescalers for each synthesizer, 50 MHz to 1.1 GHz
- Reference divider common for both synthesizers, 3 MHz to 35 MHz
- Serial bus (3-line bus: data, clock, enable) for fast programming (f_{max} = 10 MHz)
- Wide, continuous and independent ranges of division ratios:

- 17 bits for each main divider (integer ratios between 512 and 131071)
- 12 bits common reference divider (integer ratios between 8 and 4095)
- In addition to the reference divider an extra divide by 2 block is selectable to set the reference frequency ratio between both synthesizers (1:1 or 1:2).

- Simple passive loop filter for typical applications
- Charge pump output current under bus control, set by external resistor, 0.1 .. 2.4 mA
- Operating voltage range 2.6 to 5.5 V for battery powered operation
- Low current consumption, 8.5 mA typically at 3 V.
- Independent power down modes for both synthesizers
- 4 multifunction output ports
  - (bus controlled, open drain, also active in power down mode)
- Programmable Out Of Lock detector/Output port (open drain)
  - (OOL synth. A, OOL synth. B, OOL synth. A or B, logic '1', logic '0')
- SSOP20 Package
- Buffered output of reference signal (open drain)
- Integrated voltage doubler for high phase detector output voltage

1.3 Typical Application Architecture

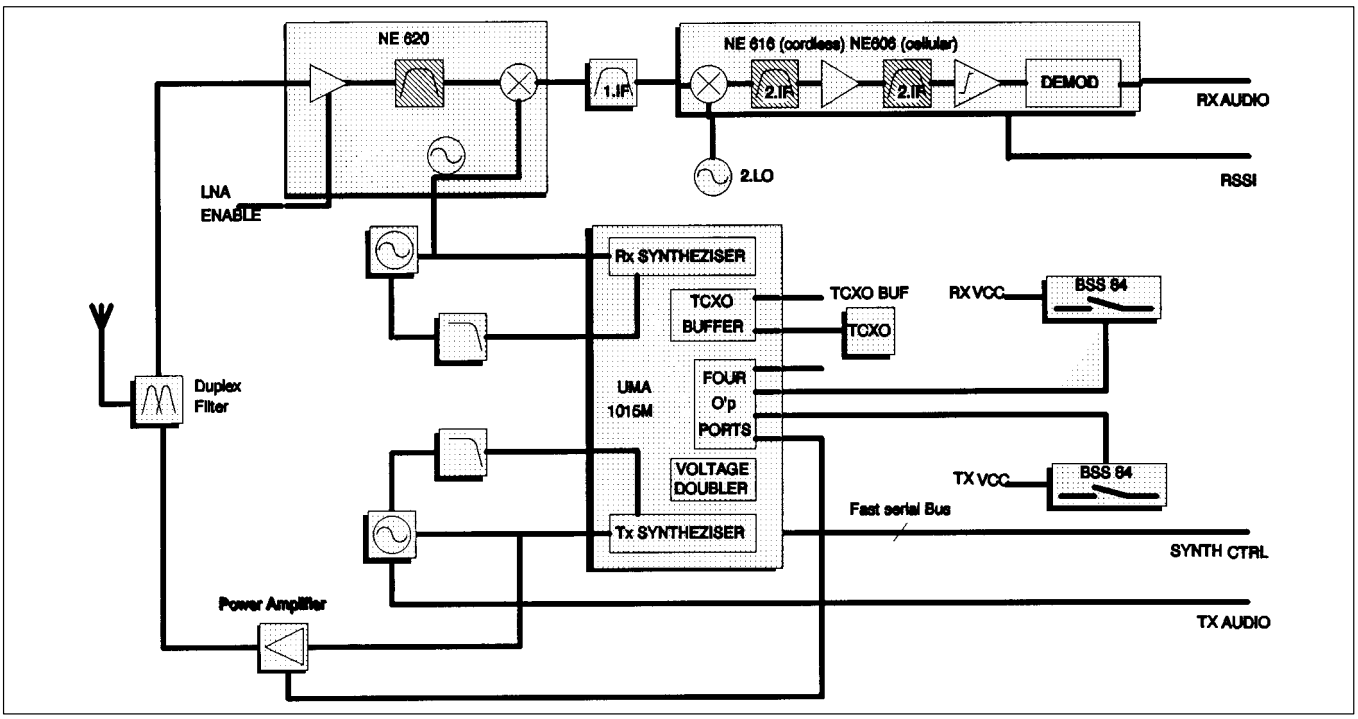


Figure 2. UMA1015M Dual Synthesizer in Typical Analog Transceiver Architecture

The UMA1015M dual synthesizer is processor controlled and notable for its flexibility in many different applications, e.g., CT1, CT1+, AMPS, TACS, NMT.

Figure 2 demonstrates the UMA1015M in an architecture commonly used in analog battery powered telecommunication equipment. The first local oscillator (LO) in the receive path and the carrier oscillator in the transmitter use PLL frequency synthesizers.

Four output ports allow processor control on miscellaneous functions in the transceiver, e.g. disable the transmit VCO or power amplifier.

The independent power down modes allow the transmit synthesizer to stand by while only the receiver periodically 'wakes up' to scan for incoming calls. When both synthesizers are in power down mode, the programmed data is retained in the synthesizer and current consumption is reduced to only 60 μA (maximum value).

For typical applications (900 MHz radio communications) a passive loop filter is sufficient, thus removing the need for operational amplifiers in the loop filter. The gain inside the loop is under bus control by switch-selecting the charge pump output current to either 12 or 24 times a value set by an external resistor at pin I_{SET}.

Programming the comparison frequency ratio select to 2:1 (as opposed to 1:1) allows optimized designs even for applications with half channel offset, such as CT1 and TACS. The comparison frequency may equal channel spacing in the receive synthesizer and half channel spacing in the transmit synthesizer.

In typical applications a temperature compensated reference oscillator will be used to provide the specified frequency stability. The reference input signal (pin 8, FXTLIN) is internally buffered and output to pin 10 (FXTLO). The buffered signal may be used as a

stable system clock or (after conversion) as the second local oscillator.

If a 9.6 MHz TCXO is used as a reference, a 1/8 divider is enough to generate a 1.2 MHz stable system clock for use in the Philips Cellular Chip Set [2].

The UMA1015M synthesizer features an on board voltage doubler. The primary use of the voltage doubler is in low voltage applications to generate VCO control voltages above the synthesizer supply voltage. The voltage doubler is enabled and disabled by programming the VDON bit via the bus. Programming the synthesizer into power down mode does not disable the voltage doubler. An external capacitor is required on pin VCC (pin 18) for smoothing. When the voltage doubler is enabled, thorough decoupling between synthesizer and VCO supply lines is necessary.

The P0/OOL signal can be used to switch the power amplifier enable line under control of the lock detect circuitry during normal 'conversation' mode to avoid false transmission if lock is unexpectedly lost. In other situations (for example when terminating a call) the processor can directly control the output of this pin by programming it to logic '1' or '0'.

Since the P0/OOL port is of open drain type, a wired-or configuration can be implemented to allow control of the transmitter to different devices, such as a micro controller. In a wired-or configuration, control of the transmitter is provided by a single line with controlling devices 'pulling low' to disable.

2 FUNDAMENTALS

2.1 Phase Lock Loop

Figure 3 depicts a generalized PLL block diagram.

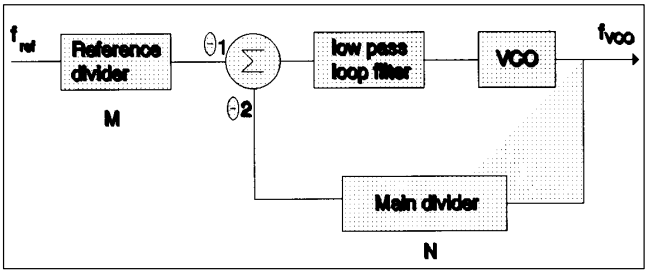


Figure 3. Main Components in Common PLL

The main parts in a common PLL are a phase detector, loop filter, voltage controlled oscillator, main divider and reference divider. In an in-lock situation the output frequency of the system is:

$$f_{VCO} = \frac{N}{M} \cdot f_{REF} \qquad (1.)$$

where f_{ref} = reference input frequency
f_{VCO} = VCO output frequency
M = reference divider division ratio
N = main divider division ratio

The inputs θ_2 and θ_1 to the phase detector are the comparison frequencies. The output of the phase detector is an error signal proportional to the difference in phase between the two input signals.

The keys for controlling the phase lock loop response are the time constants in the loop filter [3][4][5]. Frequency synthesis always involves PLL performance compromise: keeping loop bandwidth as wide as possible to reduce acquisition time and VCO noise, and at the same time suppressing reference frequency sidebands that can pass through wide bandwidths. But stability, being an absolute necessity, gets priority. The other two requirements, unfortunately, are inversely dependent and must be traded off against each other.

2.2 Phase comparator & charge pump

The two phase comparators in the UMA1015M dual synthesizer are sensitive to both phase and frequency. They react to small frequency differences between the inputs and have a highly linear response characteristic. The design responds to the full 360° range of phase inputs and control the charge pumps.

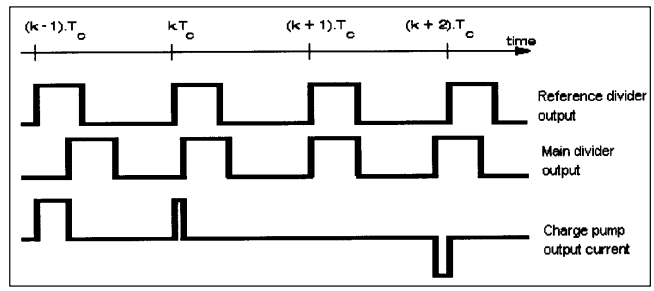


Figure 4. Timing Diagram

The phase comparator outputs are configured as charge pumps (current sources) so that the loop filters (integrators) can be designed with simple, passive components. The charge pumps drive the synthesizer loop filter to generate the VCO control voltages.

The operation principle of the phase detectors is depicted in figure 4. The comparison frequency f_c at the inputs of the phase comparator is typically the same as the system channel spacing. The phase comparison is performed once in each period of the reference signal. The duration between the comparisons is T_c, which is the reciprocal of f_c. Lower case letter k is an arbitrary index.

The charge pump outputs of the synthesizers are tri-state outputs. When in lock, i.e. when the phase error at the inputs of the phase comparator is zero, the charge pump output is in high impedance state. When the loop is unlocked the charge pump sources current pulses when the output of the reference divider is leading and sinks current pulses when lagging the main divider output. The duration of the pulses is proportional to the phase error. The sinking and sourcing pulses charge or discharge the capacitors in the loop filter.

To prevent cross talk between both synthesizers, the design of the chip assures that both charge pumps are never active simultaneously during normal operation.

The charge pump current (the 'height' of the positive or negative pulses in figure 4) is switch-selectable by software (bits CRA and CRB) and continuously adjustable via an external resistor.

The charge pump current is set by an external resistance R_{SET} at pin I_{SET}, where a temperature independent voltage of 1.2 volt is generated. R_{SET} should be between 12 kΩ and 60 kΩ to give an I_{SET} of 100 μA and 20 μA respectively. The charge pump current, I_{CP}, can be programmed for each synthesizer to be either (12 x I_{SET}) or (24 x I_{SET}) with the maximum being 2.4 mA.

Larger currents are used for fast switching. Smaller currents allow use of smaller capacitors but may make the system more susceptible to interferences and noise.

3 LOOP FILTER DESIGN

This chapter presents a loop filter design procedure in two parts:

- A basic design procedure yields approximate values for the main components.
- A PC based simulation program is used for analysis and optimization.

3.1 Basic Design Procedure

The basic design procedure yield approximate values for the components in the loop filter depicted in figure 5.

The procedure resorts to second-order loop approximations and describes the loop behavior in terms of its natural frequency f_n and damping ratio ζ. The natural frequency of the loop refers to the resonant frequency of the loop. The damping refers to the damping of this resonant frequency [3][4][5].

a: select basic loop and synthesizer parameters:

- output signal frequency, f_{VCO}, [Hz]
- VCO gain, K_{VCO}, [Hz/V]
- switching time, t_{sw}, [s]
- comparison frequency, f_{comp}, [Hz] (equals channel spacing or half channel spacing)
- loop damping factor, ζ , unitless (select ζ =0.707 for fastest switching, ζ =1 for low overshoot)
- charge pump output current, I_{CP}, [A]

b: calculate main division ratio and approximate natural frequency of loop from switching time requirement:

- main division ratio, $N = \frac{f_{VCO}}{f_{comp}}$ (2.)
- natural frequency, $f_n = \frac{2}{t_{SW}}$ (3.)

c: calculate resistor R_{SET} for setting charge pump output current

- resistor at I_{SET} pin, $R_{SET} = \frac{1.2 \cdot CRx}{I_{CP}}\ \Omega$ (4.)

where CRx = 24 if CRA/CRB bit is programmed to 1
CRx = 12 if CRA/CRB bit is programmed to 0

d: calculate approximate loop component values:

- main capacitor, $C_1 \approx K_{VCO} \cdot \frac{I_{CP}}{N \cdot (2\pi f_n)^2}$ (5.)
- damping resistor, $R_1 \approx 2 \cdot \zeta \sqrt{\frac{N}{K_{VCO} \cdot I_{CP} \cdot C1}}$ (6.)
- filter capacitor, $C_2 \approx \frac{C_1}{10}$ (7.)

The loop filter components calculated above are approximations and can be used as starting values for further analysis and optimization.

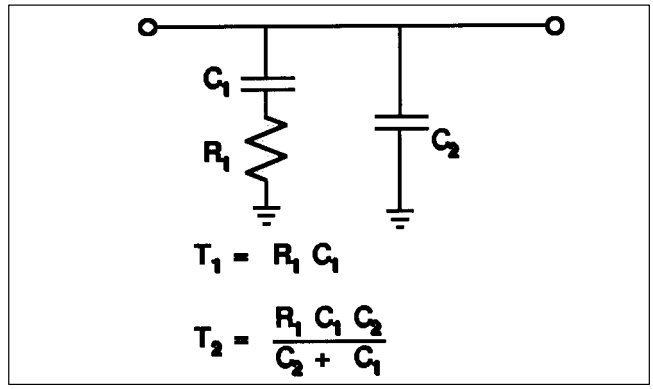


Figure 5. Second-Order Loop Filter

3.2 Analysis and Optimization

For analysis, optimization and worst case design of more complex filters, key loop parameters can be entered into a software analysis program to verify loop stability and switching time, for example SIMPATA [6]. Simpata is an interactive menu driven Phase Lock Loop design tool that runs on a personal computer and comes with a user manual. Among others the program can generate Bode Plots.

Figure 6 depicts a third order filter. The filter results from adding a low pass RC filter stage to the second order filter from the previous paragraph. The extra filter stage can reduce comparison frequency breakthrough spurs without slowing down the response of the loop.

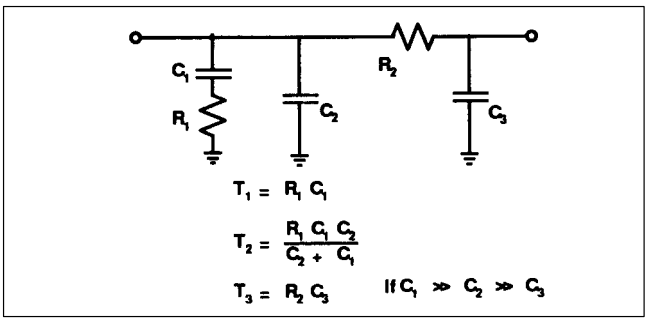


Figure 6. Third-Order Loop Filter

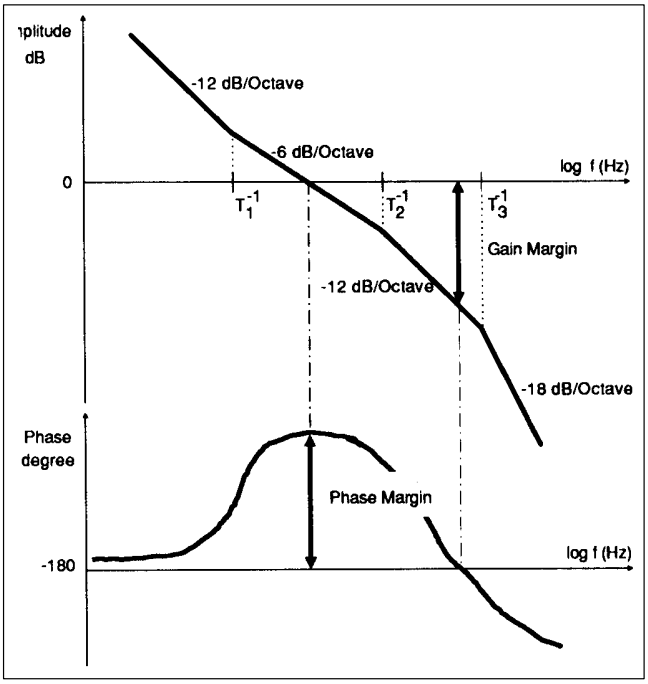


Figure 7. Bode Plot 4th-Order Open Loop Transfer Function Magnitude and Phase

A damping factor to control stability as in simpler second-order loops can not be readily defined in a higher-order loop. Instead, the phase margin becomes important.

The phase margin is easily evaluated and determined from the Bode plot. A Bode plot is a pair of graphs which displays the open loop transfer function magnitude and phase. In figure 7 shows Bode plot of a fourth order loop with third order filter and a pole in the origin due to the VCO.

The phase margin is defined as the difference between 180 and the phase of the open loop transfer function at the frequency where the logarithmic gain is 0 dB (gain cross over). The critical point for stability is a phase margin of 0 . The factor by which the system gain would have to be increased for the phase margin to reach the critical value of 0 is called the gain margin.

The time constants in the loop filter are the keys for controlling the loop performance and phase margin. The effects of different time constants can be evaluated from a Bode diagram. The reciprocal of the time constants of the loop filter in figure 6 are the breakpoints of the magnitude function in figure 7.

When increasing the time constant $T_3 = C_3.R_2$, the breakpoint T_3-^{1} will move left and the magnitude curve will start to roll off at a lower frequency. Therefore, the greater the time constant T_3, the better the comparison frequency breakthrough is suppressed. But increasing T_3 will force the point of inflection of the phase margin curve to move to the left as well, thus decreasing the phase margin and eventually making the system unstable.

Iteratively inspecting the Bode plot, adjusting the loop components and measuring performance, will yield a compromise between switching time and stability. Simulation programs may give reasonable approximations of PLL behavior, but their accuracy is always limited due to the fact that many practical imperfections and non linearities are not taken into account.

The phase margin should be between 30 and 70 for most applications. The larger the phase margin, the more stable the loop, and the slower the response.

A loop with a low phase margin is still stable but may exhibit other problems aside from outright oscillation. A low phase margin makes the transient response more oscillatory and requires very tight tolerances on all loop components, i.e. the phase margin must be positive over all variations in loop components.

A phase margin of 45° is often a good compromise between desired stability and the other generally undesired effects.

4 APPLICATION EXAMPLE

This chapter discusses the design and performance of the UMA1015M demo board.

The UMA1015M demo board demonstrates the UMA1015M dual synthesizer at frequencies in the AMPS (Advanced Mobile Phone System) cellular radio band. The circuit consists of two PLLs with 6 main parts: one temperature compensated crystal oscillator, one UMA1015M comprising two synthesizers, two loop filters and two VCOs.

Auxiliary functions are also demonstrated such as the output ports which can be programmed to power up/down the oscillators.

Circuit diagram and PCB layout are included in the appendix.

4.1 Loop filter design example

To accommodate for a fast receive synthesizer and a slower transmit synthesizer, the charge pump current I_{CP} to I_{SET} ratio is programmed to 12 for the transmitter and 24 for the receiver. On the demoboard the charge pumps currents are I_{CP} = 0.9 mA for the receiver (synthesizer A) and I_{CP} = 0.45 mA for the transmitter (synthesizer B).

Basic design procedure for AMPS receive synthesizer:

- VCO frequency, F_{VCO} = 920 MHz
- VCO gain, K_{VCO} = 11 MHz/V (from VCO specifications)
- Comparison frequency, F_{comp} = Channel spacing = 30 kHz (AMPS specification)
- Reference frequency, $F_{reference}$ = 9.6 MHz (arbitrarily, can have system advantage)

- switching time, t_s , 9 ms (indicative, for 10 MHz jump to within 1 kHz)
- I_{cp} , 0.9 mA, with CRA bit set to 1

Following the basic design procedure from paragraph 3.1 yields:

- main division ratio, $N = \frac{f_{VCO}}{f_{comp}} = \frac{918MHz}{30kHz} = 30,600$ (8.)
- natural frequency, $f_n = \frac{2}{t_{SW}}$

$$= \frac{2}{9 \cdot 10^{-3}} \approx 220Hz \quad (9.)$$

- resistor at pin I_{SET}: $\frac{1.2 \cdot CRx}{I_{CP}}$

$$= \frac{1.2 \cdot 24}{0.9 \cdot 10^{-3}} \approx 33k\Omega \quad (10.)$$

The main components in the loop filter are:

- main capacitor, $C_1 \approx K_{VCO} \cdot \frac{I_{CP}}{N \cdot (2\pi f_n)^2}$

$$= 11 \cdot 10^6 \cdot \frac{0.9 \cdot 10^{-3}}{30,600 \cdot (2\pi \cdot 220)^2} \approx 180nF \quad (11.)$$

- damping resistor, $R_1 \approx 2\,\zeta \sqrt{\frac{N}{K_{VCO} \cdot I_{CP} \cdot C_1}}$

$$= 2 \cdot 0.707 \sqrt{\frac{30,600}{11 \cdot 10^6 \cdot 0.9 \cdot 10^{-3} \cdot 180 \cdot 10^{-9}}}$$

$$= 5.8k\Omega \quad (12.)$$

- filter capacitor, $C_2 \approx \frac{C_1}{10} \approx 18nF$ (13.)

The above values for the main components in the receive synthesizer are only approximations as they are based on second order assumptions. For further optimization both a computer simulation program as well as practical experiments are used.

For trying out different component values in the loop filter, adjustable components can be used. The PLL performance can then be evaluated for various component values in the loop filter to find an optimum compromise of loop filter components with respect to the required performances.

Capacitors with leakage currents, such as electrolytic capacitors and capacitors with piezo or delay effects are not preferred because of higher reference breakthrough spurious responses.

For designing the demo board the main performance criteria for optimization were: fast switching, low residual FM and low comparison frequency breakthrough as measured with respectively a time domain analyzer, a frequency modulation analyzer and a spectrum analyzer.

During the optimization process, the software simulation program SIMPATA was used to verify the stability of the design. Figure 9 depicts the Bode plot of synthesizer A on the demo board. The loop gains falls at 6 dB/Octave at the gain cross over point. The requirement for basic loop stability is fulfilled since the phase margin is 52°.

The design procedure of the transmit synthesizer is similar to the above procedure for the receive synthesizer. The main difference is that in typical applications restrictions are imposed on the bandwidth of the loop filter of the transmit synthesizer. To allow audio modulation of the VCO, the loop filter bandwidth must be well below the lowest audio frequency, i.e. well below 300 Hz.

The loop filter components on the UMA1015M demoboard are summarized in Table 1.

Table 1. Design Parameters and Simulation Results UMA1015M Dual Synthesizer Demoboard

Parameter		Slow Transmit Synthesizer B	Fast Receive Synthesizer A
Loop filter components (reference Figure 8 below)		C_1 = 200nF	C_1 = 200nF
		C_2 = 33nF	C_2 = 15nF
		C_3 = 6.8nF	C_3 = 2.2nF
		R_1 = 10kΩ	R_1 = 6.8kΩ
		R_2 = 6.8kΩ	R_2 = 22kΩ
VCO	Gain, K_{VCO}	11MHz/V	11MHz/V
	VCO center frequency, F_{VCO}	836MHz	926MHz
	VCO frequency range	25MHz	25MHz
Comparison frequency ratio synthesizer A : B		ratio 1 : 1	
Comparison frequency, f_{comp}		30kHz	30kHz
Charge pump	Current I_{CP}	0.45mA	0.9mA
	R_{SET}	33kΩ	
	I_{SET} ratio, bits CRA, CRB	12	24
Reference	Frequency (TCXO)	9.6MHz	
	Division ratio	320	
Unity gain phase margin (simulated)		42°	52°
Gain margin at 180° phase margin (simulated)		24dB	23dB
Unity gain phase margin (simulated)		225Hz	330Hz

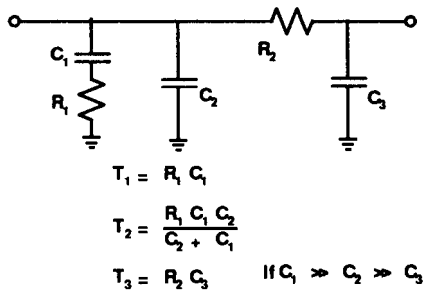


Figure 8. Loop Filter Components

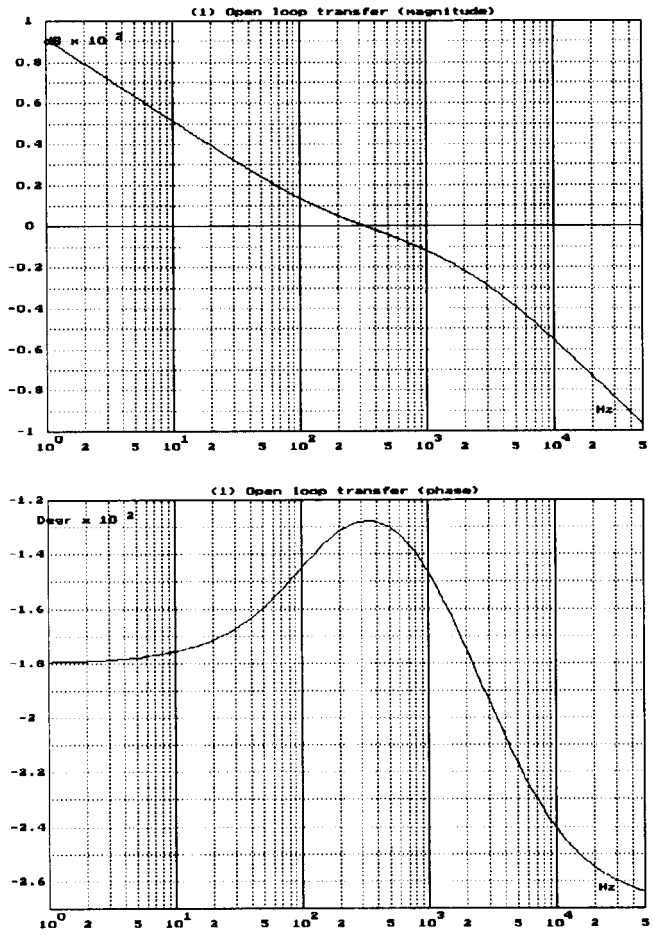


Figure 9. Simulated Bode Plot of 4th-Order Open Loop Transfer Function of Synthesizer A on UMA1015M Demoboard, Magnitude (above) and Phase (below) vs. Frequency

4.2 Performance of Design Example

This section describes the performance measured of the UMA1015M dual synthesizer demo board UMA1015M, designed in the previous paragraphs.

Important performance criteria for a frequency synthesizer are usually:

Close-in phase noise (i.e., noise level within the loop bandwidth relative to carrier)

Noise level at a specified distance from the carrier

Comparison breakthrough components

Switching time for specified frequency jump to within specified distance from target

Residual FM

Power consumption

It should be noted that these criteria can be traded off against each other to some extent to tailor overall performance, and that the performance described here is only one compromise between the various criteria. In general, the choice of a low loop bandwidth will improve the comparison frequency breakthrough and will filter out more of the close-in noise, but will result in a longer switching time. The use of a higher order filter can improve comparison frequency breakthrough with little effect on the noise or switching time. The noise floor at offsets significantly higher than the loop bandwidth is dominated by the VCO characteristics.

Table 2 summarizes the measurement results. Figures 10 to 12 show some measurement graphs from which the numbers in table 2 are read. During the recording of the measurement results, both synthesizers were enabled and locked.

Table 2. Results UMA1015M Dual Synthesizer Demoboard

Measurement results UMA1015M dual synthesizer demo board. Data are extracted from a limited number of engineering samples and do not indicate typical values. VCO supply voltage: 4.2V, both synthesizers enabled; UMA1015M supply voltage: 4.2V, room temperature.

Parameter		Fast Receive Synthesizer A	Slow Transmit Synthesizer B
VCO frequency range		914–939 MHz	824–849 MHz
Residual FM (CCITT weighted, RMS)		13.5 Hz RMS	8.5 Hz RMS
Comparison frequency breakthrough	at 30kHz	71 dBc	90 dBc
Switching time for frequency jump around center frequency to within 2.5kHz off the target frequency	30kHz (single channel)	2.6 ms	2.9 ms
	10MHz	6.2 ms	9.5 ms
	25MHz (maximum jump)	7.5 ms	10 ms
VCO noise level relative to carrier, at specified distance from carrier, normalized	120Hz (close-in)	–57 dBc/Hz	–57 dBc/Hz
	45kHz (adjacent channel)	–116 dBc/Hz	–116 dBc/Hz
Current consumption UMA1015M (Voltage doubler disabled)	Both synthesizers enabled	9.1 mA	
	Transmitter disabled; Receiver enabled	5.2 mA	
	Both synthesizers disabled	approx. 0.007 mA	

Figure 10 shows the transient response of synthesizer A for a 10 MHz frequency jump to within 2,5 kHz of the target to be 6.2 ms.

Figures 11 and 12 demonstrate the noise spectrum of synthesizer B with narrow (2 kHz) and wide (50 kHz) frequency span respectively. The markers in Figure 10 indicate the close-in noise to be 57 dB/Hz below carrier power level. Also from figure 10 the width of the noise plateau indicates that the loop band width is around 230 Hz, which is in accordance with design targets.

Figure 12 reveals an outstanding low comparison frequency (at 30 kHz) breakthrough of more then 90 dB below the carrier power level (below noise level). The low comparison frequency breakthrough allows a trade off of the comparison breakthrough against faster switching.

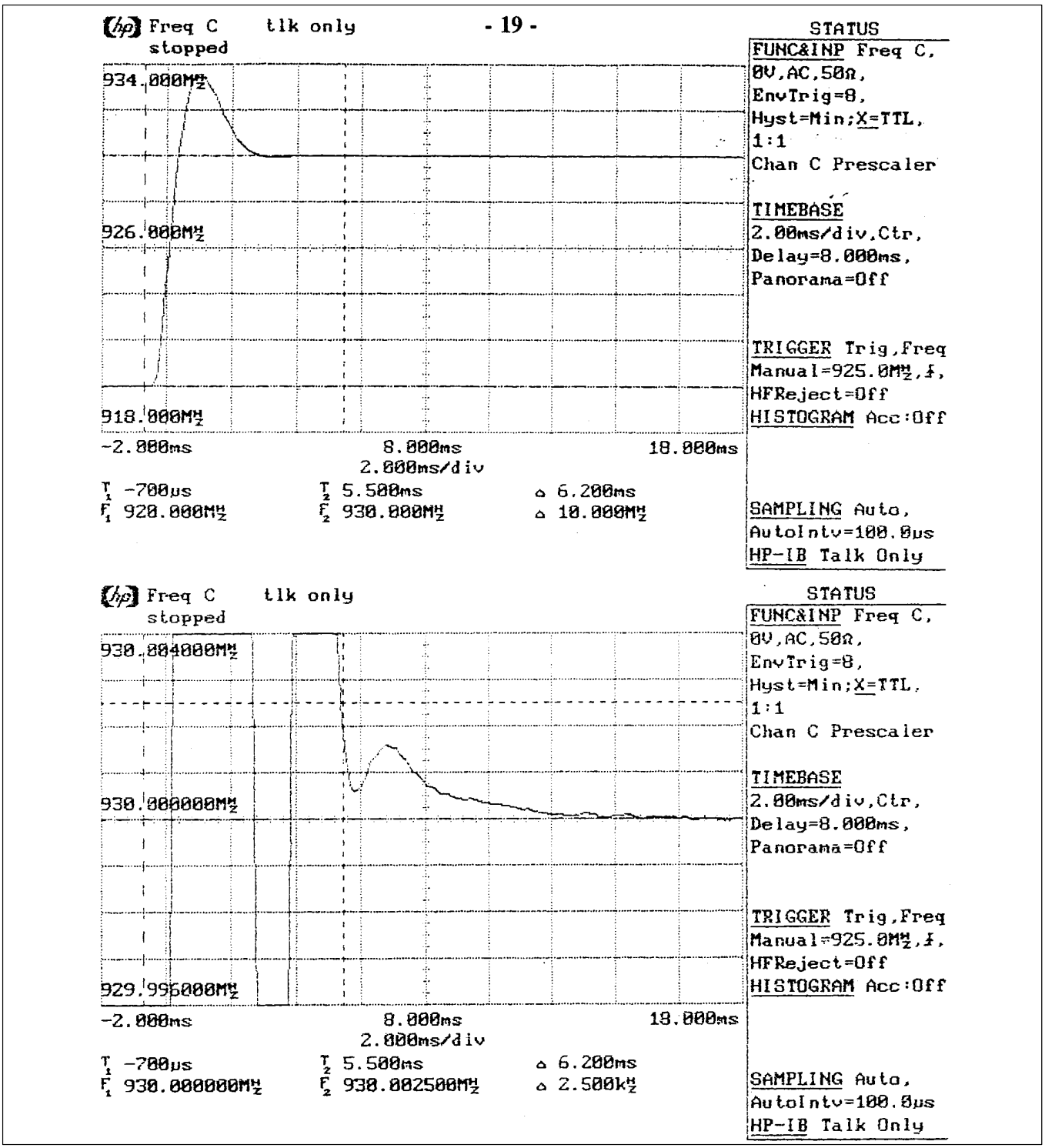


Figure 10. UMA1015M Demoboard, Transient Response Synthesizer A. 6.2ms for 10MHz Jump to Within 2.5kHz Off Target Frequency.

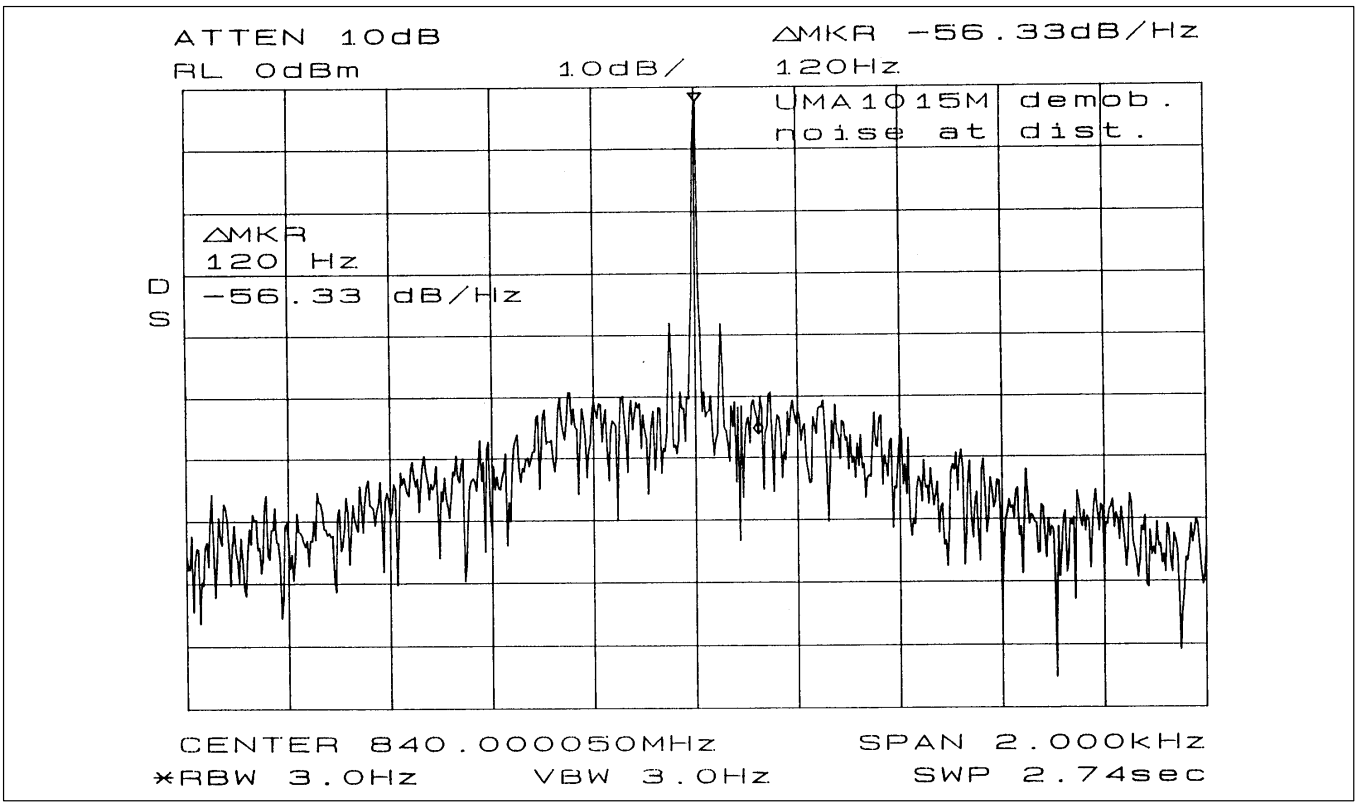


Figure 11. UMA1015M Demoboard, Frequency Spectrum Synthesizer B, 2kHz Span. Close-in Noise: 56dB/Hz Below Carrier.

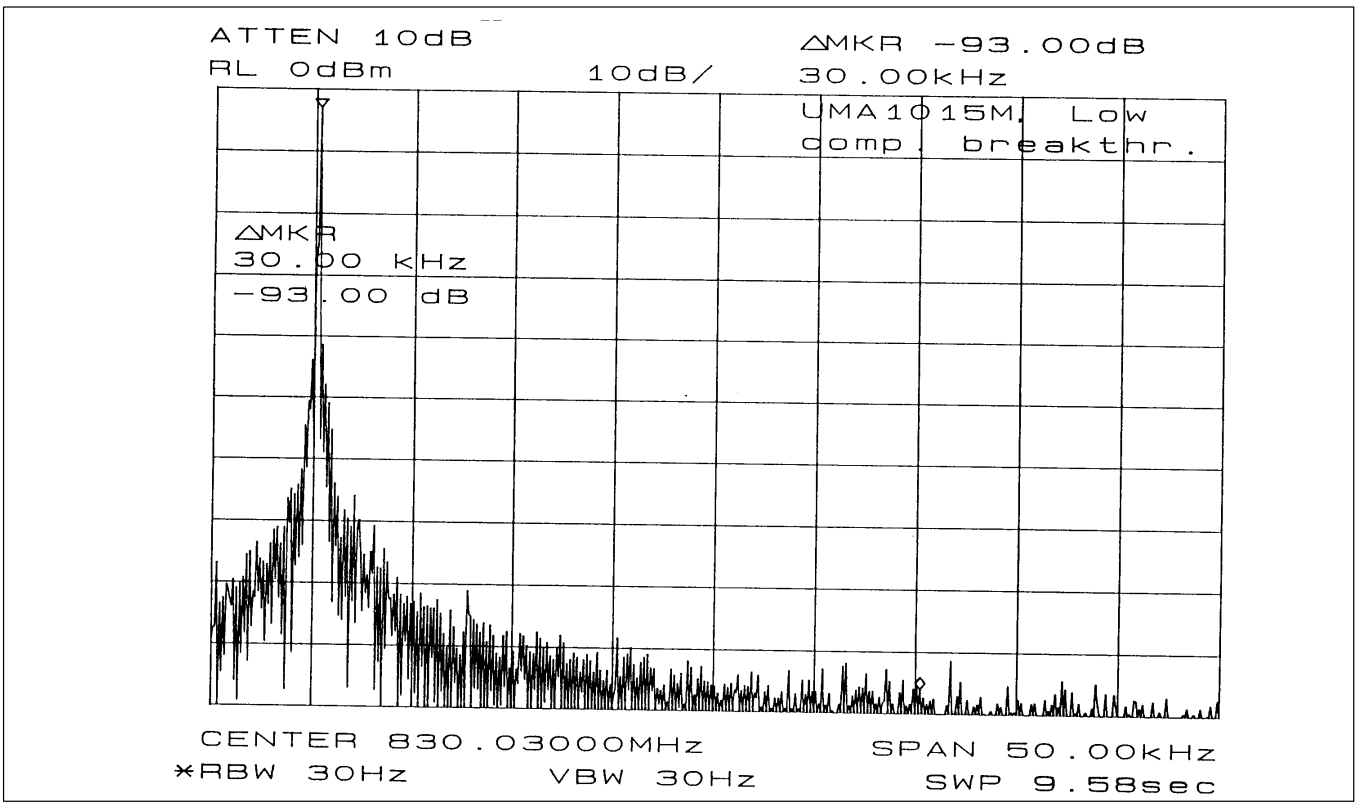


Figure 12. UMA1015M Demoboard, Frequency Spectrum Synth B, 50kHz Span. Low Comparison Breakthrough (below noise level)

5 FREQUENTLY ASKED QUESTIONS

Q. How to use the synthesizer with V_{DD} < 4.5V whereas pins DATA, CLK and ENB are at 5V logic?

A. A. Because of protection against electrostatic discharges, the input voltage for these logic pins can not be greater than V_{DD}+0.3V. An interface between the microcontroller and the synthesizer is then needed to reduce voltage at bus pins. A voltage divider is a simple and cheap solution to implement.

The design of this voltage divider (see below) involves performance compromise between the current consumption and the programming speed, which depend on R1, R2 and Cpar, a parasitic capacitance from the demo board.

A Technical Marketing Report (n° CTT94008) describes some measurements results : for different values of V_{DD} <4.5V, the current consumption and the programming speed are given.

Q. The example below shows a typical programming example of the UMA1015M with the following conditions :

– fxtal input frequency : 9.6 MHz

– Synthesizer A input frequency : 926.01 MHz

– Synthesizer A comparison frequency : 30 kHz

– Synthesizer B input frequency : 836.01 MHz

– Synthesizer B comparison frequency : 30 kHz

– Both synthesizers ON (sPDA = sPDB = 1)

– Out of lock indication from both synthesizer loops (OLA = OLB = 1)

– Charge pumps currents : $I_{CPA} = 24*I_{SET}$ (CRA = 1)

$I_{CPB} = 12*I_{SET}$ (CRB = 0)

– Voltage doubler disabled (VDON = 0)

Table 3. UMA1015M Register Data Allocations Expressed in Decimal and Hexadecimal

First In	Register Bit Allocation		Last In
dtl6	Data Field	dt10	Address
Test register (must be 0 if programmed)			0h
Control register = 0 0001 1100 0110 0000			1h
Synth A main divider coefficient = 30867d = 7893h			4h
Reference divider coefficient = 320 d = 140h			5h
Synth B main divider coefficient = 27867d = 6CDBh			6h

Table 4. UMA1015M Register Data Allocations Expressed in Binary

First In (MSB)			Data Field												Last In (LSB)	Address			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	0	0	0	1
0	0	1	1	1	1	0	0	0	1	0	0	1	0	0	1	1	0	1	0	0
0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	1	0	1
0	0	1	1	0	1	1	0	0	1	1	0	1	1	0	1	1	0	1	1	0

About Data Format

Special care has to be taken for correct programming when first applying power to the synthesizer.

The ENB signal should be held LOW and only taken HIGH after having programmed an appropriate register on first powering up. If this condition is not achieved, it may result in loading of random data from the serial bus shift register (programming register) into one of the synthesizers data registers/ addressed latches including the test register.

It should be noted that the test register does not normally need to be programmed. However, if it is programmed, all bits in the Data Field should be set to 0.

In case of random data being loaded into the test register, it is recommended to program a frame of zeros, on first powering up.

Q. How to use the TCXO output buffer stage to generate an harmonic of the crystal frequency?

A. The TCXO output is an open drain MOS output. The aim is to generate a signal at a multiple of the crystal input frequency. The most common method is to use a non-linear circuit, for instance a biased amplifier stage and to use a LC output circuit tuned to some multiple of the input frequency.

The following diagram is a proposal to obtain a third harmonic on pin fxtalo.

Q. About PCB layout considerations

Since careful PCB layout has a great impact on performances of RF circuitry, special attention should be paid when designing the frequency synthesizer layout.

To avoid crosstalk between synthesizers (A and B), the printed circuit board should have a solid ground plane on the non surface mount side (apart from isolated pads for non-grounded connections to leaded components). On the surface mount side of the board, the ground plane should be designed round each synthesizer, and underneath the integrated circuit so as to provide maximum isolation between two PLLs. A good number of plated-through holes must connect the two layers of the ground plane.

Power supply bypass capacitors (100 nF) in series with a small value resistor (12 Ω) should be located as close as possible to the device with short leads for pins 4 and 14.

Q. Out-of-lock indication

The Out-of-Lock functions works in such a way that :

– when $_e > T_{OOL}$ with $T_{OOL} = 80/ f_{RF}$, the OOL signal goes LOW

– for coming back into lock, $_e$ has to be smaller than T_{OOL} during 8 reference cycles. Then, the OOL signal goes HIGH again. This procedure is described on the following diagram.

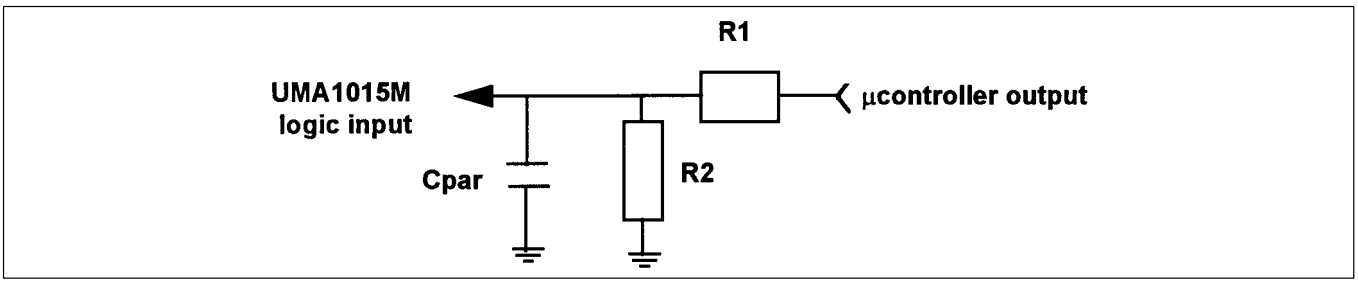


Figure 13. Out-Of-Lock Indication

6 REFERENCES

1. *Product Datasheet UMA1015M*, Philips Semiconductors, 22 June 1995.
2. Data Handbook 1993 *RF/Wireless Communications*, p. 851–895: Cellular Chip Set Design Guide, Philips Semiconductors 1993
3. Gardner, Floyd M., *Phaselock Techniques*, 2d ed., John Wiley & Sons, New York 1979
4. Rohde, Ulrich L., *Digital PLL Frequency synthesizers, Theory and Design*, Prentice–Hall, Englewood Cliffs, New Yersey 1983
5. Best, Roland E., *Phase–Locked Loops, Theory, design, and Applications*, 2d ed., McGraw–Hill, New York 1993, includes disk for PLL simulations
6. *SIMPATA*, PLL simulation program and manual, Philips CTT NatLab, Eindhoven, The Netherlands, 1992. Information or ordering: tel (+31)40–744212, fax (+31)40–744619
7. Technical Marketing Report (CTT94008),*Use the UMA1015M Synthesizer at V_{DD} under 4.5V with serial bus at 5V Logic* , Philips Semiconductors, 1994.

7 APPENDIX UMA1015M DEMOBOARD DATA SHEETS

UMA1015M demo board circuit diagram, PCB layout, component listings.

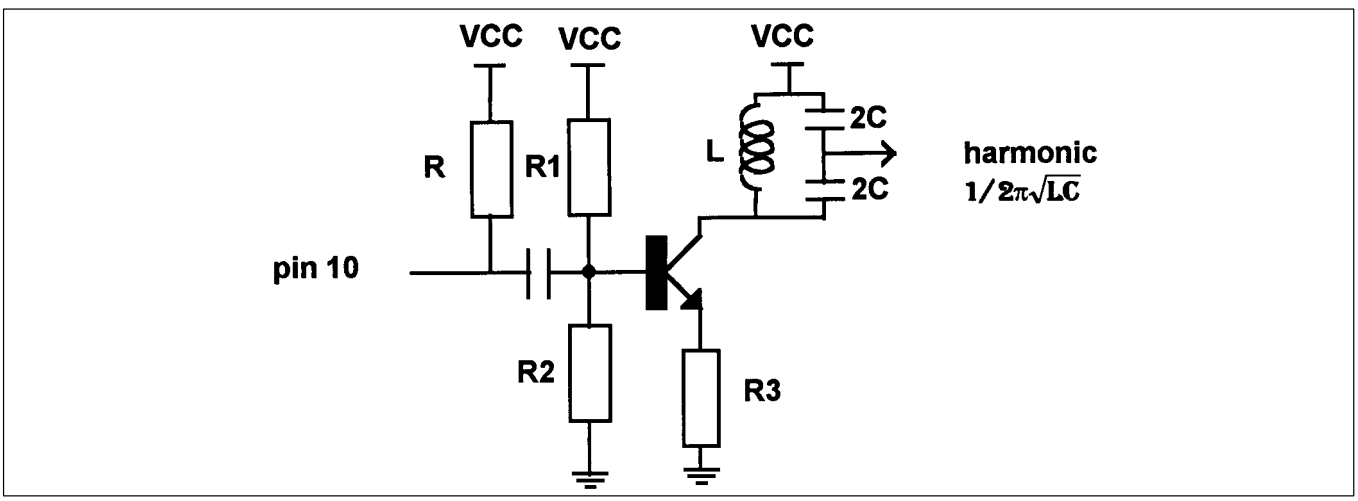


Figure 14.

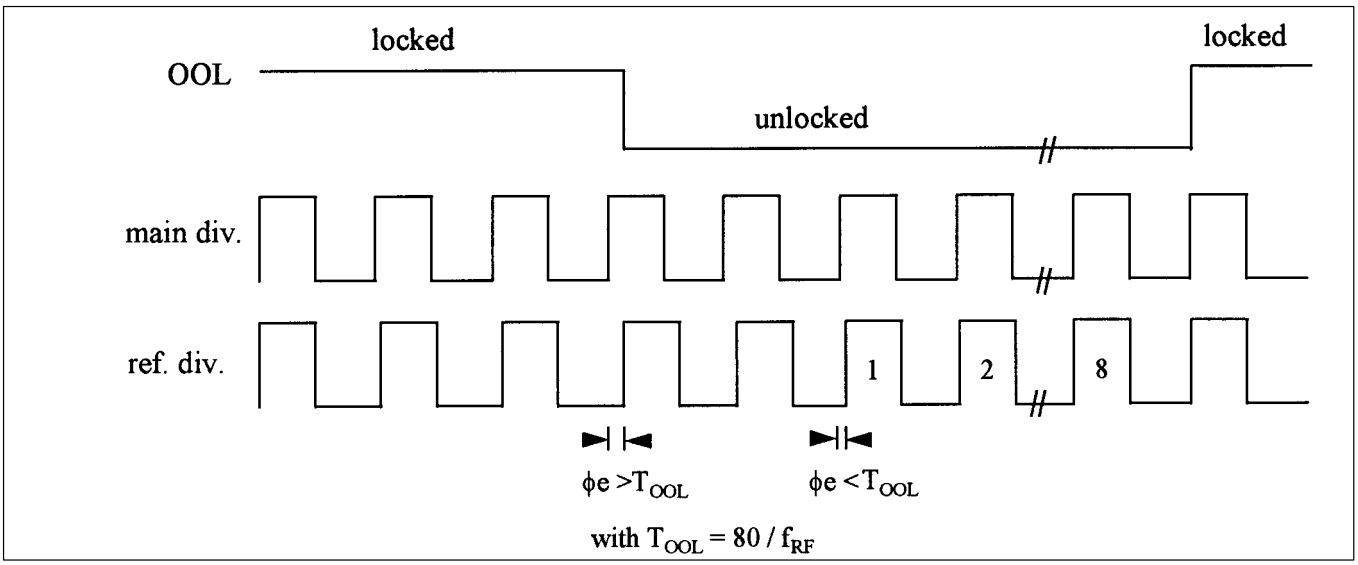

locked
locked
OOL
unlocked
main div.
ref. div.
1
2
8
φe >T_OOL
φe <T_OOL
with T_OOL = 80 / f_RF

Figure 15.

Appendix UMA1015M demo board data sheets

UMA1015M demo board circuit diagram, PCB lay-out, component listings.

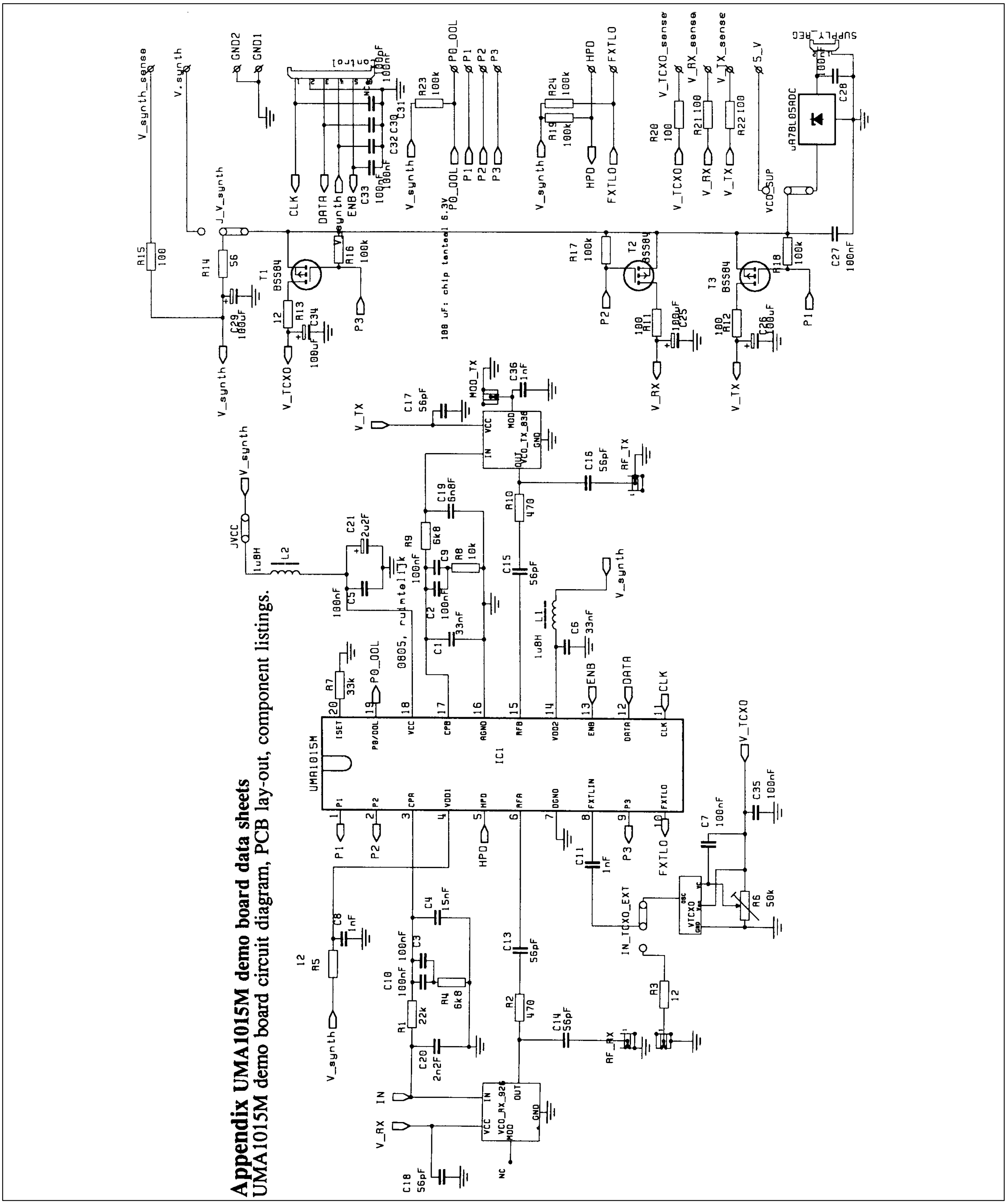


Figure 16.

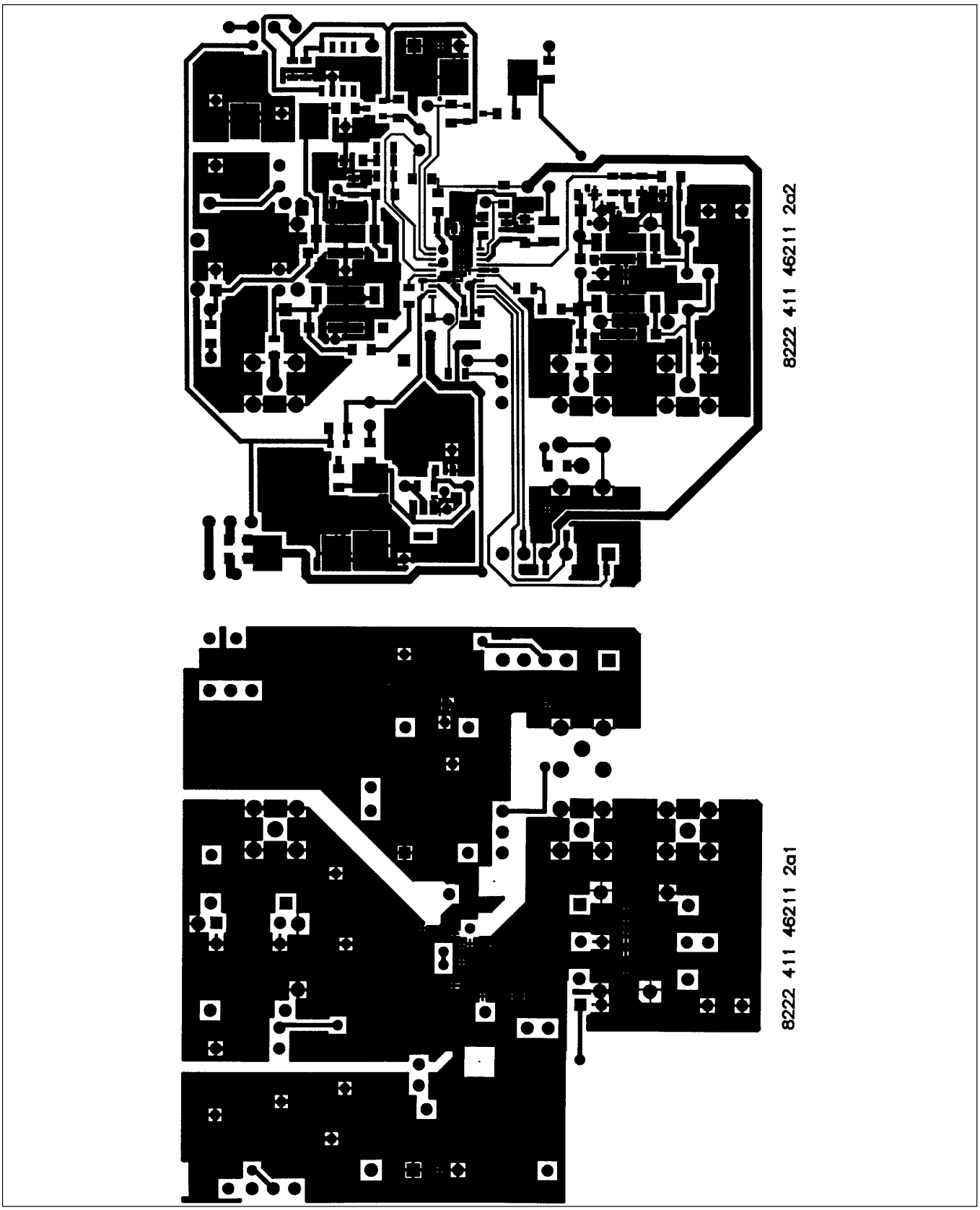


Figure 17.

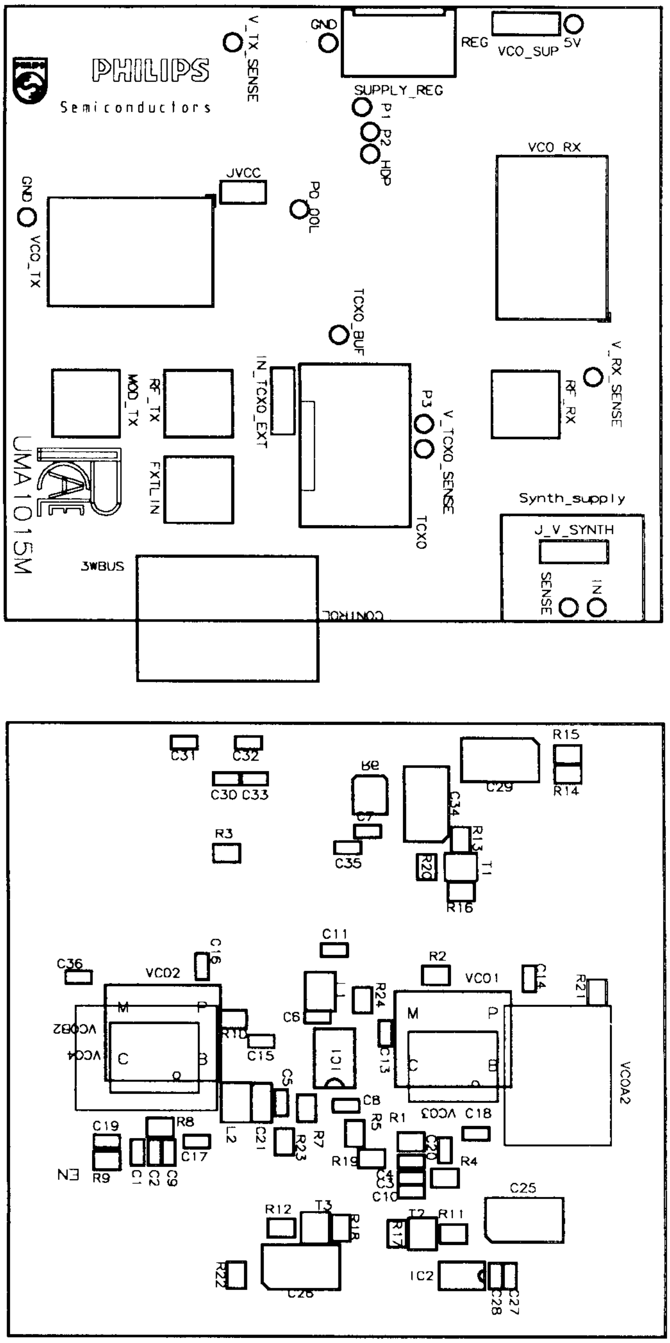
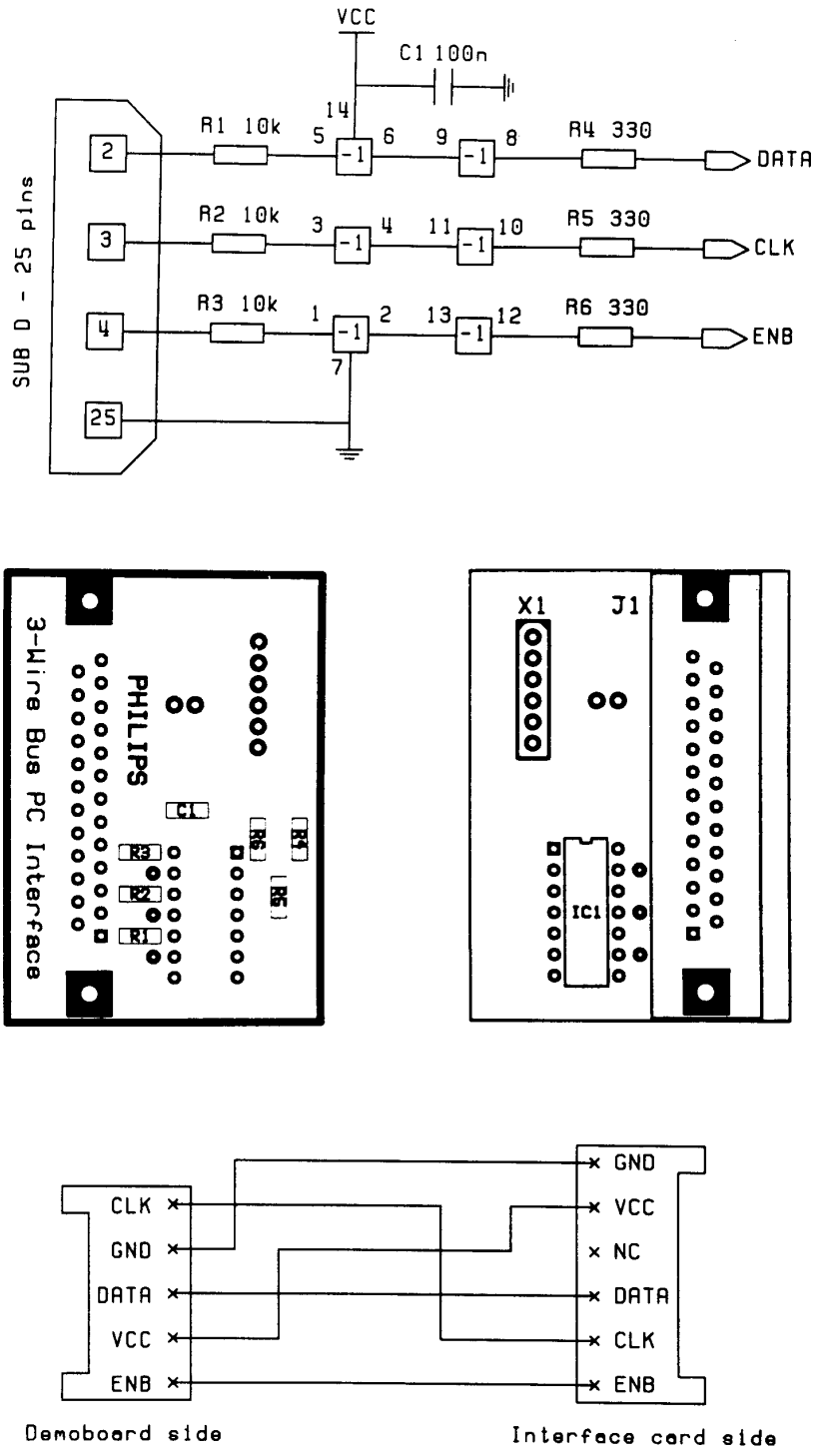

PHILIPS
Semiconductors
V_TX_SENSE
GND
REG
VCO_SUP
5V
SUPPLY_REG
P1
P2
HDP
VCO_RX
JVCC
GND
PD_OOL
VCO_TX
TCXO_BUF
V_RX_SENSE
IN_TCXO_EXT
MOD_TX
RF_TX
P3
V_TCXO_SENSE
RF_RX
FXTL_IN
Synth_supply
J_V_SYNTH
TCXO
UMA1015M
3WBUS
SENSE
IN
CONTROL
R15
C31
C32
C29
R14
C30 C33
C34
C7
R13
R3
C35
R20
T1
R16
C16
C11
C36
VCO2
R2
VCO1
C14
R21
M
P
R24
C6
R10
C15
C13
C
B
IC1
VCOA2
C5
C8
R1
C18
C19
R8
R5
L2
C21
R7
C20
R23
R19
R4
C17
R9
C1
C2
C9
C3
C4
C10
C25
R12
T3
R18
T2
R11
R17
R22
IC2
C28
C27
C26

Figure 18.



Interface card pcb layout and cable connection.

Figure 19.