Features

- **Operating Supply Range 3.0V to 3.6V**
- **Power Dissipation 1W Max**
- **Low-power Sleep Mode (<0.5 mW)**
- **RF Data Channel**
  - **Automatic Gain Control or Programmable Gain Mode**
  - **Wide Bandwidth VGA**
  - **VGA Accepts Inputs from 30–300 mV Peak-to-peak Differential (PPD), 60–600 mV_{PPD} or 110–1100 mV_{PPD}**
  - **Programmable Equalization via 7th-order Equiripple Filter with Programmable Symmetric Zeros**
  - **Programmable 5-to-1 Filter Cutoff Range**
  - **Data Slicer with DC Restore Circuit**
  - **Wide Frequency Range Clock Extraction**
  - **Frequency Synthesizer with Independent 7-bit M and 6-bit N Dividers, Better than 1% Resolution**
  - **Highly Programmable to Accommodate DVD (1–5X) and CD (6–30X)**
  - **Write Asymmetry Measurement for Adjusting Write-mode Power**
  - **Data Recovery Supports CLV, ZCLV, ZCAV Recording**
  - **Optional Internally-generated Timing for AGC and Timing Recovery**
- **Synthesizer Functions**
  - **Supports Wobble Clock Synthesis, Using Low-jitter PLL**
- **Servo Algebra and OPC Functions**
  - **45 MHz Bandwidth for Differential Phase Tracking Detector**
  - **Land and Groove Detector for DVD RAM**
  - **Supports One Beam Push/Pull Tracking Output**
  - **Supports One Beam Differential Phase Tracking**
  - **Supports Three-beam Push/Pull Tracking Output, Using E, F, G, H**
  - **Focus Error Signal Output**
  - **Focus OK Signal**
  - **Track Crossing Detection**
  - **Mirror Signal Output**
  - **Wobble Detection for DVD RAM, DVD-RW, DVD-R**
  - **Detects Tracking Error OK**
  - **Provides Sample and Hold Functions for CD and DVD OPC**
  - **Formats Pre-pit Data, Using Raw Pre-pit Information from AT78C1503**
- **Header Detection for DVD RAM**

Description

The AT78C1503 is a programmable DVD/CD channel responsible for servo algebra, gain control, equalization, bit detection and clock extraction for CD-ROM, DVD-ROM, DVD-R, DVD-RW and DVD-RAM formats. Programmable features allow data rates up to 5X DVD. Also, for DVD-RAM functionality, the channel serves the write path providing laser power control and pit asymmetry detection. Up to 2X DVD write speeds are supported for DVD-R, DVD-RW and DVD-RAM. The extracted wobble frequency is supplied to the AT78C1507 companion chip which in turn synthesizes the write clock.

The AT78C1507 is the companion chip to the AT78C1503 – DVD/CD Read Channel – and the AT78C1504 – DVD/CD Automatic Laser Power Controller. Working in conjunction with the read channel, the AT78C1507 is responsible for wobble clock synthesis for DVD-R and DVD-RAM formats. In addition, the two parts working together also support pre-pit data and clock recovery for the DVD-R format. Four separate inputs are provided to enable the AT78C1507 to perform tracking servo algebra, using just the outrigger photo detector signals (E, F, G, H for example) coming from the OPU. This extends the range of supported tracking servo algebra functions for the 1503-1507 combination. Lastly, OPC capability is supported for efficient writing of DVD-R, DVD-RAM and CD-R disks.

Based on CMOS technology, both the AT78C1503 and AT78C1507 operate from a single 3.3V supply and are fully programmable through serial interfaces for both CD and DVD modes.

DVD/CD Read Channel

AT78C1503
AT78C1507

Rev. 2054A–DVD–07/02

Figure 1. DVD System Block Diagram

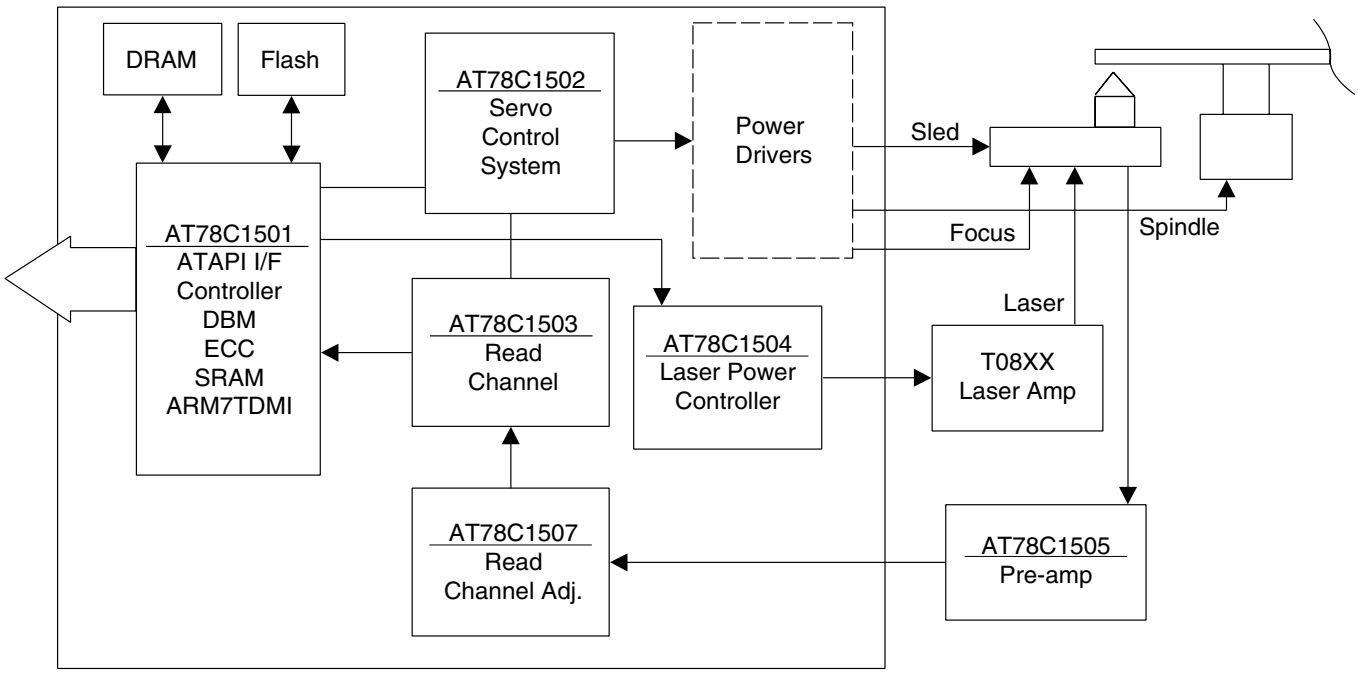

Figure 2. AT78C1503 Block Diagram

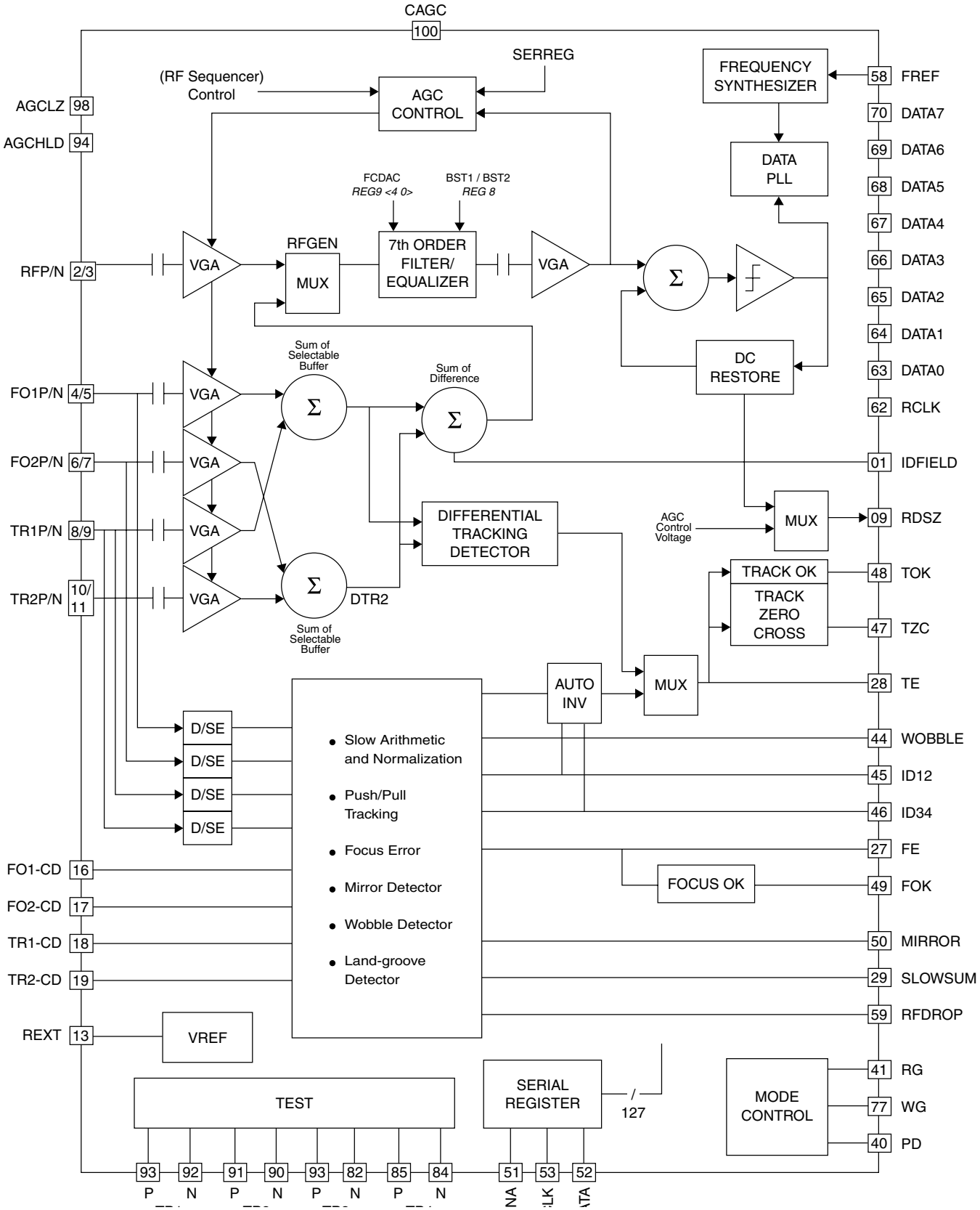

Figure 3. AT78C1503 Pin-out

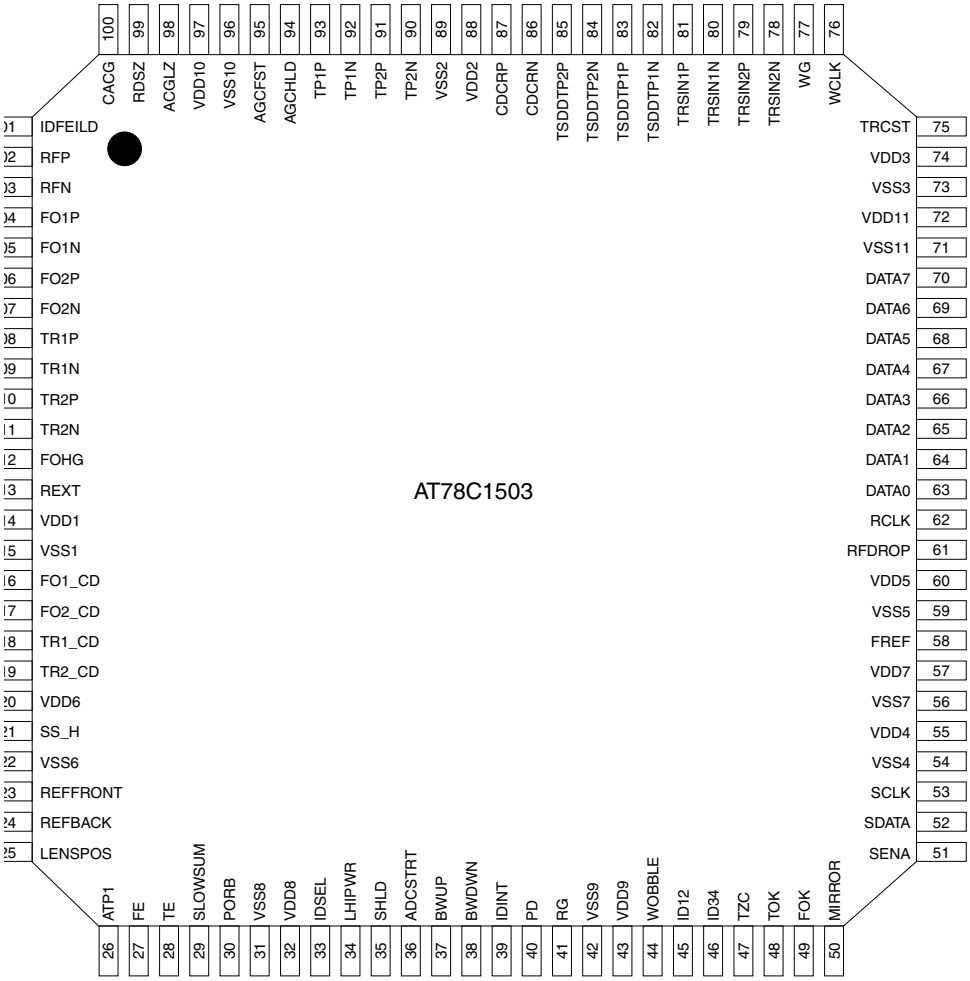

Table 1. AT78C1503 Pin List

Pin #	Pin Name	Type	Description
1	IDFIELD	Digital Output	Signal to Preamp to Drive ID Select
2	RFP	Analog Input	High-speed Signal Input
3	RFN	Analog Input	High-speed Signal Input
4	FO1P	Diff Input	Focus 1 Pos
5	FO1N	Diff Input	Focus 1 Neg
6	FO2P	Diff Input	Focus 2 Pos
7	FO2N	Diff Input	Focus 2 Neg
8	TR1P	Diff Input	Track 1 Pos
9	TR1N	Diff Input	Track 1 Neg
10	TR2P	Diff Input	Track 2 Pos
11	TR2N	Diff Input	Track 2 Neg

Table 1. AT78C1503 Pin List (Continued)

Pin #	Pin Name	Type	Description
12	FOHG	Digital Input	Focus High Gain
13	REXT	Passive	Passive for 0 TC Current Reference (16.5 K_, 1%)
14	VDD1	3.3V Supply	DPD, IBIAS
15	VSS1	0V Supply	DPD, IBIAS
16	FO1_CD	Analog Input	Focus 1, CD Input
17	FO2_CD	Analog Input	Focus 2, CD Input
18	TR1_CD	Analog Input	Track 1, CD Input
19	TR2_CD	Analog Input	Track 2, CD Input
20	VDD6	3.3V Supply	Slow Servo Analog
21	SS_H	Digital Input	Servo Sample and Hold
22	VSS6	0V Supply	Slow Servo Analog
23	REFFRONT	Input/Output	Servo Front-end Reference Level
24	REFBACK	Input/Output	Servo back-end Reference Level
25	LENSPOS	Analog Input	Lens Position Error Input
26	ATP1	Analog Output	Servo Analog Test Point
27	FE	Analog Output	Focus Error Output
28	TE	Analog Output	Tracking Error Output
29	SLOWSUM	Analog Output	Low-pass Filtered Sum of Photodetector Outputs
30	PORB	Digital Input	Power-on Reset, Bar (active-low)
31	VSS8	0V Supply	Servo DACs
32	VDD8	3.3V Supply	Servo DACs
33	IDSEL	Digital Input	ID Field Select
34	LHIPWR	Digital Input	Laser High Power
35	SHLD	Digital Input	Servo Hold
36	ADCSTRT	Digital Input	Start On-chip 6-bit ADC
37	BWUP	Digital Input	Bandwidth Up
38	BWDN	Digital Input	Bandwidth Down
39	IDINT	Digital Input	Mode Select of Sequencer
40	PD	Digital Input	Power-down
41	RG	Digital Input	User Data Read Gate
42	VSS9	0V Supply	Servo DAC Rings
43	VDD9	3.3V Supply	Servo DAC Rings
44	WOBBLE	Digital Output	Wobble Detect Output
45	ID12	Digital Output	ID Field 12 Detected
46	ID34	Digital Output	ID Field 34 Detected
47	TZC	Digital Output	Track Zero Crossing

Table 1. AT78C1503 Pin List (Continued)

Pin #	Pin Name	Type	Description
48	TOK	Digital Output	Track OK
49	FOK	Digital Output	Focus OK
50	MIRROR	Digital Output	Mirror Detect (ROM)/Mirror Field Detect (RAM)
51	SENA	Digital Input	Serial Data Enable; Must Be High to Read or Write Serial Registers
52	SDATA	Input/Output	Serial Data, Input (write data) or Output (read data)
53	SCLK	Digital Input	Serial Data Clock
54	VSS4	0V Supply	ESD Ring, Digital Ring
55	VDD4	3.3V Supply	ESD Ring, Digital Ring
56	VSS7	0V Supply	Slow Servo Digital, Synthesizer Dividers
57	VDD7	3.3V Supply	Slow Servo Digital, Synthesizer Dividers
58	FREF	Digital Input	Reference Clock Input to Synthesizer
59	VSS5	0V Supply	Digital I/O Supply
60	VDD5	3.3V Supply	Digital I/O Supply
61	RFDROP	Digital Output	RF Dropout Detected
62	RCLK	Digital Output	Recovered Clock Divided by 4 or 8
63	DATA0	Digital Output	Recovered Data Out, Bit 0 (last in time)
64	DATA1	Digital Output	Recovered Data Out, Bit 1
65	DATA2	Digital Output	Recovered Data Out, Bit 2
66	DATA3	Digital Output	Recovered Data Out, Bit 3
67	DATA4	Digital Output	Recovered Data Out, Bit 4
68	DATA5	Digital Output	Recovered Data Out, Bit 5
69	DATA6	Digital Output	Recovered Data Out, Bit 6
70	DATA7	Digital Output	Recovered Data Out, Bit 7 (first in time)
71	VSS11	0V Supply	Digital I/O Ring
72	VDD11	3.3V Supply	Digital I/O Ring
73	VSS3	0V Supply	TR CML, Synthesizer CML, DC Restore
74	VDD3	3.3V Supply	TR CML, Synthesizer CML, DC Restore
75	TRCST	Digital Input	Timing Recovery Coast
76	WCLK	Digital Output	Write Clock
77	WG	Digital Input	Write Gate (enables write clock)
78	TRSIN2N	Diff Input	Timing Recovery/Synthesizer Test Input
79	TRSIN2P	Diff Input	Timing Recovery/Synthesizer Test Input
80	TRSIN1N	Diff Input	Timing Recovery/Synthesizer Test Input
81	TRSIN1P	Diff Input	Timing Recovery/Synthesizer Test Input
82	TSDDTP1N	Test Output	TR/Detector/Phase Detector Test Input

Table 1. AT78C1503 Pin List (Continued)

Pin #	Pin Name	Type	Description
83	TSDDTP1P	Test Output	TR/Detector/Phase Detector Test Point
84	TSDDTP2N	Test Output	TR/Detector/Phase Detector Test Input
85	TSDDTP2P	Test Output	TR/Detector/Phase Detector Test Input
86	CDCRN	Diff Passive	Detector Duty Cycle Feedback Cap
87	CDCRP	Diff Passive	Detector Duty Cycle Feedback Cap
88	VDD2	3.3V Supply	RF Front-end Ring
89	VSS2	0V Supply	RF Front-end Ring
90	TP2N	Diff Output	Test Point 2 Output
91	TP2P	Diff Output	Test Point 2 Output
92	TP1N	Diff Output	Test Point 1 Output
93	TP1P	Diff Output	Test Point 1 Output
94	AGCHLD	Digital Input	AGC Hold Input
95	AGCFST	Digital Input	AGC Fast Recovery Input
96	VSS10	0V Supply	AGC, LPF
97	VDD10	3.3V Supply	AGC, LPF
98	AGCLZ	Digital Input	Low Z Control for AGC Input
99	RDSZ	Analog Output	AGC Cap/Detector Cap Voltage Outputs
100	CAGC	Passive	External Capacitor for AGC Loop

Table 2. Supply Pins

Supply Pin	Circuitry
VDD/SS1	DPD, IBIAS, RTRIM
VDD/SS2	RF Front-end Ring
VDD/SS3	TR & Synth CML, DC Restore, RF Dropout Analog
VDD/SS4	ESD & Digital Ring
VDD/SS5	Digital I/O Supply
VDD/SS6	Servo Analog
VDD/SS7	Servo, Synth and RF Dropout Digital, CMOSTPMUX, Serial Registers 1 and 3, Calibrator
VDD/SS8	Servo DACs
VDD/SS9	Servo DAC Rings
VDD/SS10	AGC, LPF
VDD/SS11	Digital I/O Ring

Figure 4. AT78C1507 Block Diagram – Wobble PLL and OPC Sample and Hold

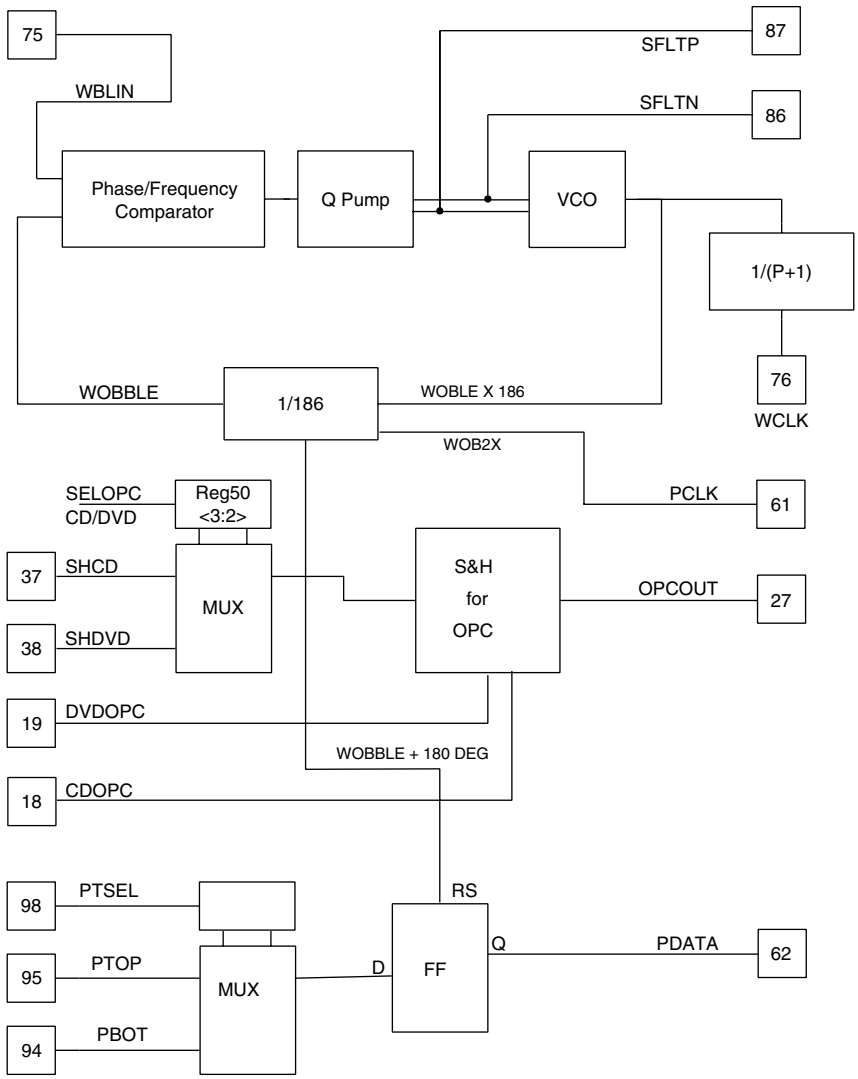

Figure 5. AT78C1507 – Tracking Error Path

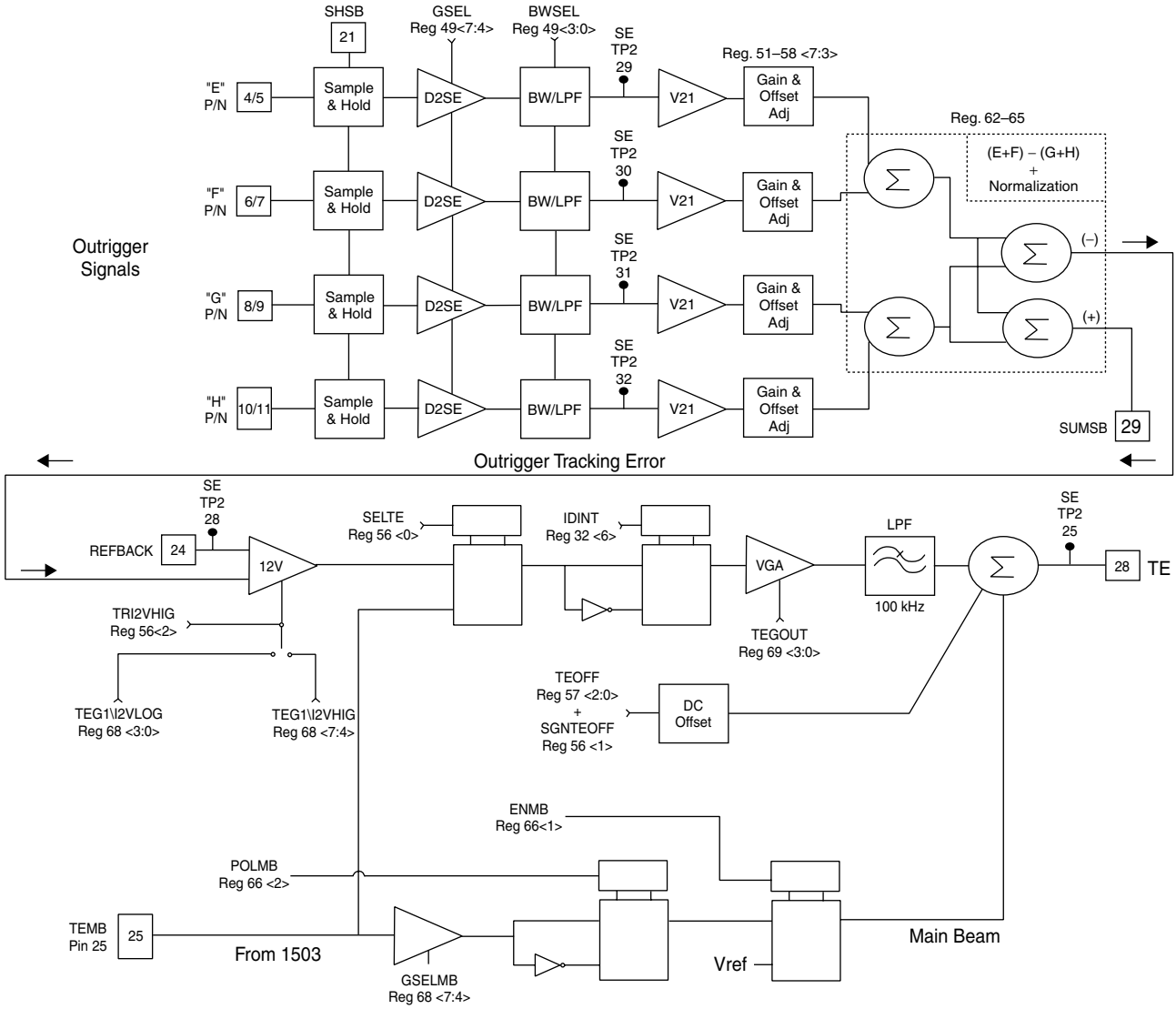

Figure 6. AT78C1507 Pin-out

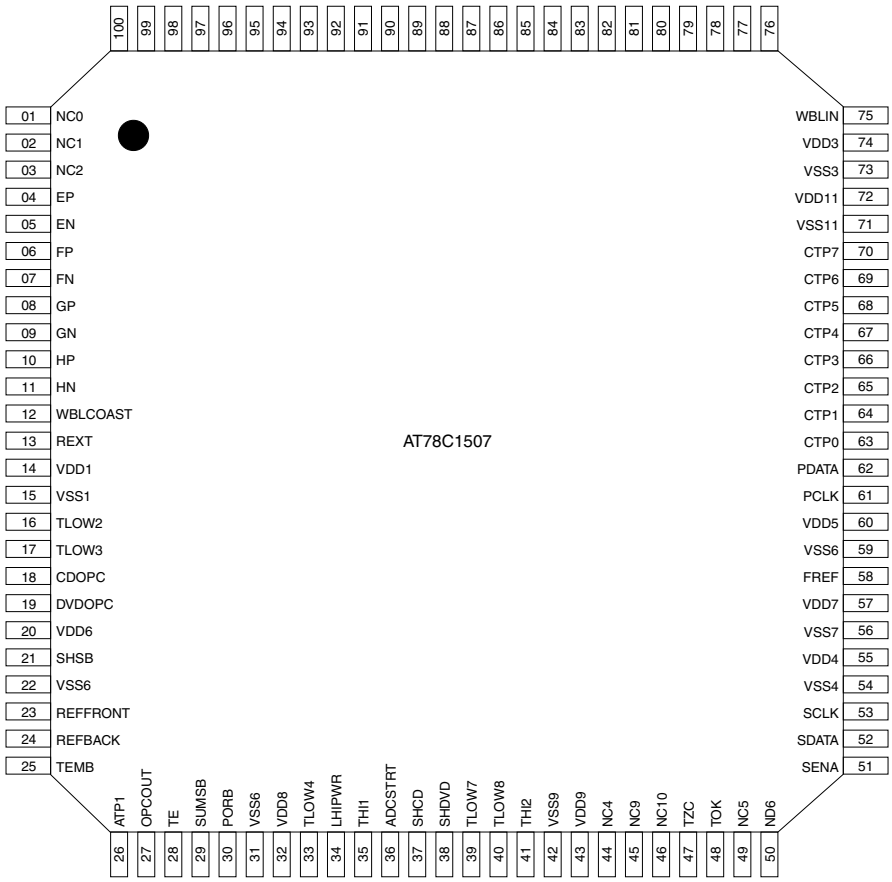

Table 3. AT78C1507 Pin List

Pin #	Pin Name	Type	Description
1	NC0	Digital Output	Not Used
2	NC1	Analog Input	Not Used
3	NC2	Analog Input	Not Used
4	EP	Diff Input	“E” Input Pos
5	EN	Diff Input	“E” Input Neg
6	FP	Diff Input	“F” Input Pos
7	FN	Diff Input	“F” Input Neg
8	GP	Diff Input	“G” Input Pos
9	GN	Diff Input	“G” Input Neg
10	HP	Diff Input	“H” Input Pos
11	HN	Diff Input	“H” Input Neg

Table 3. AT78C1507 Pin List (Continued)

Pin #	Pin Name	Type	Description
12	WBLCOAST	Digital Input	Coast Wobble Clock Synthesizer
13	REXT	Passive	16 K_, 1% Resistor to 0V Supply (for on-chip biasing)
14	VDD1	3.3V Supply	Power Supply
15	VSS1	0V Supply	Power Supply
16	TLOW2	0V	Tie-down to a 0V Supply
17	TLOW3	0V	Tie-down to a 0V Supply
18	CDOPC	Analog Input	CD Monitor Diode
19	DVDOPC	Analog Input	DVD Monitor Diode
20	VDD6	3.3V Supply	Power Supply
21	SHSB	Digital Input	Sample/Hold Control for E, F, G, H (1 = Sample, 0 = Hold)
22	VSS6	0V Supply	Power Supply
23	REFFRONT	Input/Output	Front-end Reference Voltage
24	REFBACK	Input/Output	Back-end Reference Voltage
25	TEMB	Analog Input	Tracking Error Main Beam from AT78C1503 (generated using A, B, C, D)
26	ATP1	Analog Output	Analog Test Point (single-ended)
27	OPCOUT	Analog Output	Sampled Monitor Diode Output
28	TE	Analog Output	Tracking Error Output
29	SUMSB	Analog Output	E + F + G + H
30	PORB	Digital Input	Power-on Reset, Bar (active-low)
31	VSS8	0V Supply	Power Supply
32	VDD8	3.3V Supply	Power Supply
33	TLOW4	0V	Tie-down to a 0V Supply
34	LHIPWR	Digital Input	Laser High Power
35	THI1	3.3V	Tie-up to a 3.3V Supply
36	ADCSTRT	Digital Input	Start on-chip 6-bit ADC
37	SHCD	Digital Input	Sample/Hold Control for CD Monitor Diode (1 = Sample, 0 = Hold)
38	SHDVD	Digital Input	Sample/Hold Control for DVD Monitor Diode (1 = Sample, 0 = Hold)
39	TLOW7	0V	Tie-down to a 0V Supply
40	TLOW8	0V	Tie-down to a 0V Supply
41	THI2	3.3V	Tie-up to a 3.3V Supply
42	VSS9	0V Supply	Power Supply
43	VDD9	3.3V Supply	Power Supply

Table 3. AT78C1507 Pin List (Continued)

Pin #	Pin Name	Type	Description
44	NC4	Digital Output	Not Used
45	NC9	Digital Output	Not Used
46	NC10	Digital Output	Not Used
47	TZC	Digital Output	Track Zero Crossing
48	TOK	Digital Output	Tracking Error OK
49	NC5	Digital Output	Not Used
50	NC6	Digital Output	Not Used
51	SENA	Digital Input	Serial Data Enable (must be high to read or write serial registers)
52	SDATA	Input/Output	Serial Data, Input (write data) or Output (read data)
53	SCLK	Digital Input	Serial Data Clock
54	VSS4	0V Supply	Power Supply
55	VDD4	3.3V Supply	Power Supply
56	VSS7	0V Supply	Power Supply
57	VDD7	3.3V Supply	Power Supply
58	FREF	Digital Input	Frequency Reference for Wobble Clock Synthesizer
59	VSS5	0V Supply	Power Supply
60	VDD5	3.3V Supply	Power Supply
61	PCLK	Digital Output	Pre-pit Clock
62	PDATA	Digital Output	Pre-pit Data
63	CTP0	Digital Output	Digital Test Point Out, Bit 0
64	CTP1	Digital Output	Digital Test Point Out, Bit 1
65	CTP2	Digital Output	Digital Test Point Out, Bit 2
66	CTP3	Digital Output	Digital Test Point Out, Bit 3
67	CTP4	Digital Output	Digital Test Point Out, Bit 4
68	CTP5	Digital Output	Digital Test Point Out, Bit 5
69	CTP6	Digital Output	Digital Test Point Out, Bit 6
70	CTP7	Digital Output	Digital Test Point Out, Bit 7
71	VSS11	0V Supply	Power Supply
72	VDD11	3.3V Supply	Power Supply
73	VSS3	0V Supply	Power Supply
74	VDD3	3.3V Supply	Power Supply
75	WBLIN	Digital Input	Raw Digital Wobble from AT78C1503
76	WCLK	Digital Output	Write Clock (synthesized wobble clock)
77	WCLKEN	Digital Input	Write Clock Enable

Table 3. AT78C1507 Pin List (Continued)

Pin #	Pin Name	Type	Description
78	TLOW9	0V	Tie-down to a 0V Supply
79	TLOW10	0V	Tie-down to a 0V Supply
80	TLOW11	0V	Tie-down to a 0V Supply
81	TLOW12	0V	Tie-down to a 0V Supply
82	TSDDTP1N	Test Output	Differential Analog/CML Test Point1 Neg
83	TSDDTP1P	Test Output	Differential Analog/CML Test Point1 Pos
84	TSDDTP2N	Test Output	Differential Analog/CML Test Point2 Neg
85	TSDDTP2P	Test Output	Differential Analog/CML Test Point2 Pos
86	SFILTN	Diff Passive	Wobble Synthesizer Filter Neg
87	SFILTP	Diff Passive	Wobble Synthesizer Filter Pos
88	VDD2	3.3V Supply	Power Supply
89	VSS2	0V Supply	Power Supply
90	TP2N	Diff Output	Not Used
91	TP2P	Diff Output	Not Used
92	TP1N	Diff Output	Not Used
93	TP1P	Diff Output	Not Used
94	PBOT	Digital Input	Bottom Pre-pit Detect from AT78C1503
95	PTOP	Digital Input	Top Pre-pit Detect from AT78C1503
96	VSS10	0V Supply	Power Supply
97	VDD10	3.3V Supply	Power Supply
98	PTSEL	Digital Input	Pre-pit Top Select (PTSEL = 1 selects input on pin PTOP; PTSEL = 0 selects input on PBOT)
99	NC7	Analog Output	Not Used
100	NC8	Passive	Not Used

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