Features

- **All-in-one Design**
  - **MIDI Control Processor**
  - **Synthesis**
  - **Compatible Effects: Reverb + Chorus**
  - **Programmable Spatial Effects for Four-channel Surround(1)**
  - **Four-band Stereo Equalizer**
- **State-of-the-art Synthesis Supplies Best Quality for Price**
  - **34-voice Polyphony + Effects**
  - **Up to 1 MB Wavetable/Firmware Support**
- **Synthesizer Chipset: ATSAM9713 + 8-Mbit ROM + 32K x 8 SRAM + DAC**
- **Hardware-programmable DAC Mode**
  - **I2S 16 to 20 bits**
  - **Japanese 16 bits**
- **Firmware/Sample Set Available for Turnkey Designs**
  - **8-Mbit GS® GMS960800B(2)**
  - **8-Mbit CleanWave® GMS970800B**
- **Typical Applications: Cost-sensitive Portable Karaoke/VCD Karaoke**
- **80-lead TQFP Package: Small Footprint, Easy Mounting**
- **Ideal for Battery Operation**
  - **Low Power**
  - **Power-down Mode**
  - **Wide Supply Voltage Range: 3V to 4.5V Core, 3V to 5.5V Periphery**

Notes: 1. Four-channel surround requires additional DAC.
2. GMS960800B with express permission of Roland Corporation. Special licensing conditions apply. Refer to warning on last page of this datasheet.

Sound Synthesis

ATSAM9713 Low-cost Integrated Synthesizer with Effects

Rev. 1712B-DRMSD–11/02

Description

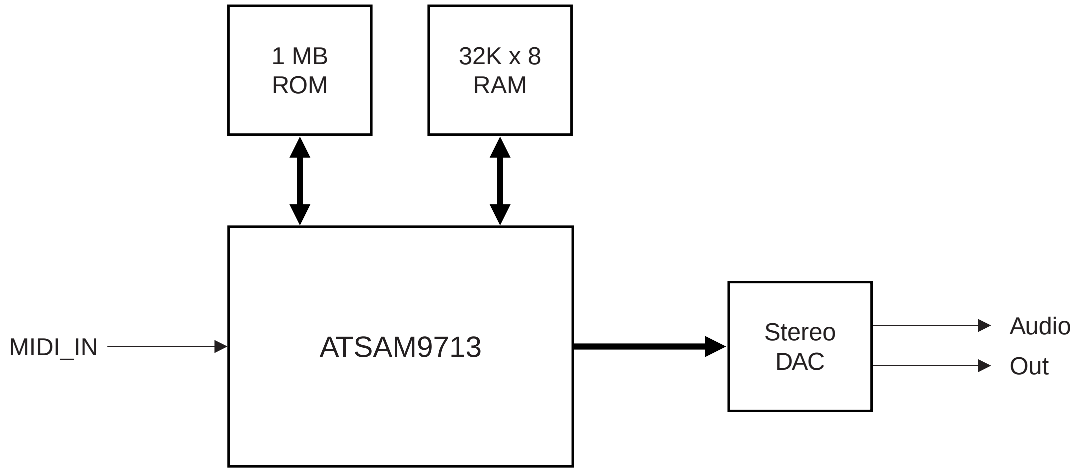
The highly integrated architecture of the ATSAM9713 combines a specialized high-performance RISC digital signal processor and a general-purpose 16-bit CISC control processor on a single chip. An on-chip memory management unit allows the digital signal processor and the control processor to share external ROM and RAM devices. The ROM bus width should be 16 bits while the SRAM can be selected to be 8 or 16 bits wide. When using an 8-bit SRAM, fast type (static cache) should be selected because two SRAM cycles will be completed in one ROM cycle duration.

Running at 300 million operations per second (MOPS), the digital signal processor supports high-quality PCM synthesis as well as most important functions like reverb, chorus, surround effect and equalizer. By adding an additional stereo DAC, four-channel audio surround can also be obtained.

The ATSAM9713 operates from a low-frequency 9.6 MHz typical crystal. A built-in PLL raises this frequency to a 38.4 MHz internal clock that controls the two processors. Care has been taken that output pin signals change only when necessary. This minimizes RFI (radio frequency interferences) and power consumption. Minimizing RFI is mostly important in order to comply with standards such as FCC, CSA and CE.

The core power supply for the ATSAM9713 should range from 3V to 4.5V; the periphery supports supply from 3V to 5.5V. Therefore, by selecting 3.3V ROM, SRAM and DAC, it is possible to develop low-power/low-voltage portable applications.

Figure 1. Typical Hardware Configuration



Pin Description

Pins by Function

Table 1. Power Supply Group

Pin Name	Pin Number	Type	Function
GND	5, 14, 21, 23, 36, 38, 57, 61, 62, 65, 74	PWR	Digital Ground All pins should be connected to a ground plane.
V_{CC}	1, 6, 13, 18, 22, 32, 56, 6480	PWR	Power Supply, 3V to 5.5V All pins should be connected to a VCC plane
V_{C3}	7, 17, 63	PWR	Core Power Supply, 3V to 4.5V All pins should be connected to nominal 3.3V. If 3.3V is not available, then V_{C3} can be derived from 5V by two 1N4148 diodes in series.

Table 2. Serial MIDI

Pin Name	Pin Number	Type	Function
MIDI_IN	15	IN	Serial TTL MIDI IN. All controls are received by this pin.

Table 3. External ROM/RAM Group

Pin Name	Pin Number	Type	Function
WA[18:0]	37, 39, 41 - 55, 58, 59	OUT	External ROM/RAM address for up to 512K words (8M bits) of memory. ROM memory holds firmware and PCM data. RAM memory holds working variables and effects delay lines.
WD[15:0]	66 - 73, 75 - 79, 2 - 4	I/O	External ROM/RAM data. Holds read data from ROM or RAM when $\overline{WOE}$ is low, writes data to RAM when $\overline{WWE}$ is low.
$\overline{WCS0}$	29	OUT	External ROM chip select, active low.
$\overline{WCS1}$	30	OUT	External RAM chip select, active low.
$\overline{WOE}$	31	OUT	External ROM/RAM output enable, active low.
$\overline{WWE}$	28	OUT	External RAM write, active low.
RBS	20	OUT	RAM byte select. Used as lower address from RAM when an 8-bit wide RAM is connected.

Note: Pin names exhibiting an overbar ($\overline{WOE}$ for example) indicate that the signal is active low.

Table 4. Digital Audio Group

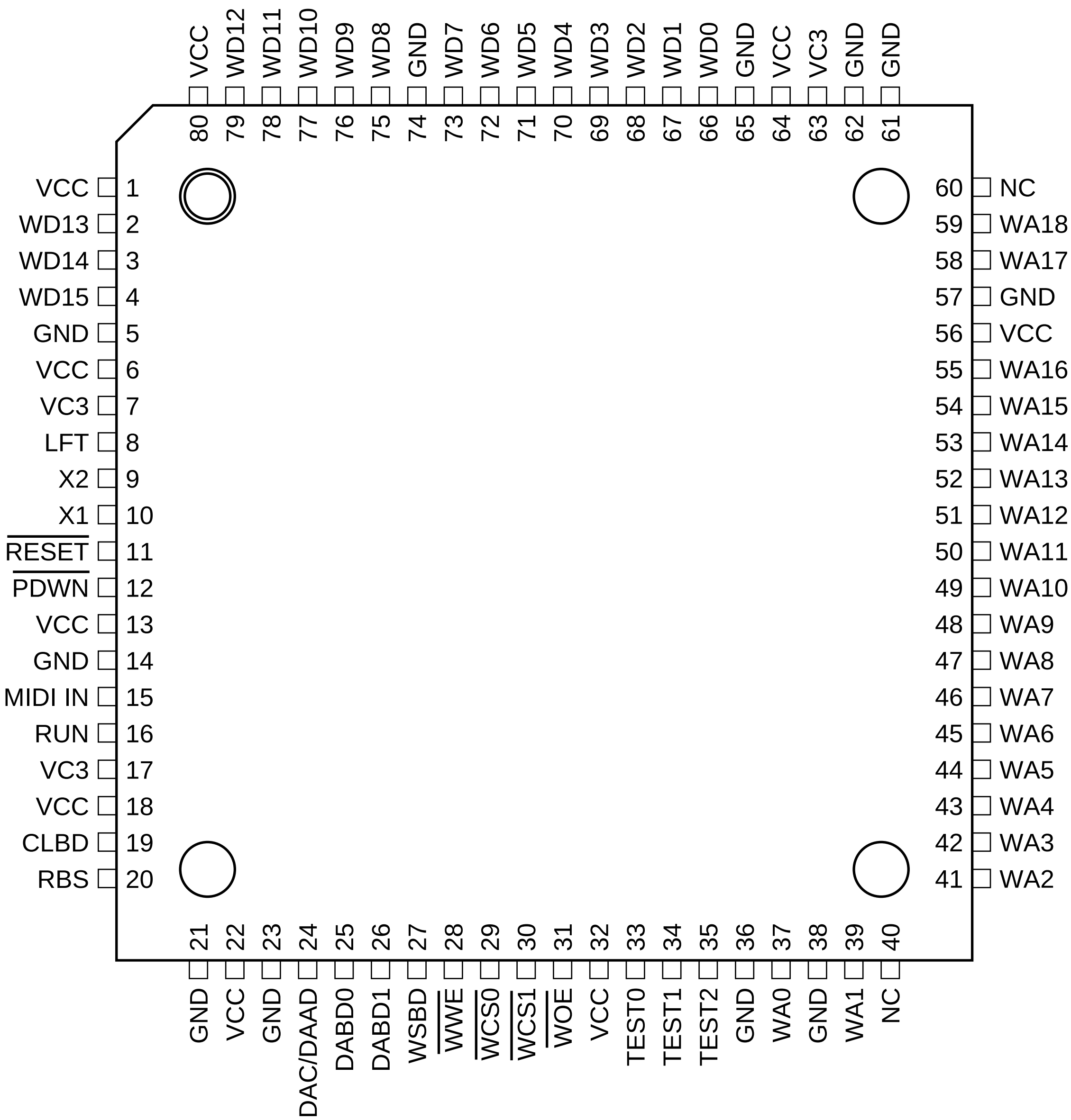
Pin Name	Pin Number	Type	Function
CLBD	19	OUT	Digital audio bit clock
WSBD	27	OUT	Digital audio left/right select
DABD0	25	OUT	Digital audio main stereo output
DABD1	26	OUT	Auxiliary digital stereo output. Reserved for surround effects.
DAC/DAAD	24	IN	DAC type: 0 = I2S 16 to 20 bits, 1 = Japanese 16 bits Can also be used as digital audio input if 32K x 16 RAM is connected.

Table 5. Miscellaneous Group

Pin Name	Pin Number	Type	Function
X1 X2	10, 9		9.6 MHz crystal connection. An external 9.6 MHz clock can also be used on X1 (3.3V input). X2 cannot be used to drive external circuits.
LFT	8		PLL external RC network
$\overline{\text{RESET}}$	11	IN	Reset input, active low. This is a Schmitt trigger input, allowing direct connection of an RC network.
$\overline{\text{PDWN}}$	12	IN	Power-down, active low. When power-down is active, then all output pins will be floated. The crystal oscillator will be stopped. To exit from power-down, $\overline{\text{PDWN}}$ should be high and $\overline{\text{RESET}}$ applied.
TEST[2:0]	33, 34, 35	IN	Test pins. Should be grounded.
RUN	16	OUT	When high, indicates that the synthesizer is up and running.

Pinout

Figure 2. ATSAM9713 Pinout in 80-lead TQFP Package



Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Ambient Temperature (Power Applied)................-40°C to + 85°C Storage Temperature..-65°C to + 150°C Voltage on any pin (except X1)......................-0.5V to V_{CC} + 0.5V V_{CC} Supply Voltage...-0.5V to + 6.5V. V_{C3} Supply Voltage..-0.5V t0 + 4.5V Maximum I_{OL} per I/O pin...10mA	*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Symbol	Parameter/Condition	Min	Typ	Max	Unit
V_{CC}	Supply Voltage(1)	3	3.3/5.0	5.5	V
V_{C3}	Supply Voltage	3	3.3	4.5	V
T_A	Operating Ambient Temperature	0		70	°C

Note: 1. When using 3.3V supply in a 5V environment, care must be taken that any pin voltage does not exceed V_{CC} + 0.5V. Pin X1 is powered by V_{C3} input. If X1 is driven by a 5V device, then a minimum series resistor is required (typ 330Ω).

DC Characteristics

Table 8. DC Characteristics (T_A = 25°C, V_{C3} = 3.3V ± 10%)

Symbol	Parameter/Condition	V_{CC}	Min	Typ	Max	Unit
V_{IL}	Low-level Input Voltage	3.3 5.0	-0.5 -0.5		1.0 1.7	V V
V_{IH}	High-level Input Voltage	3.3 5.0	2.3 3.3		V_{CC} + 0.5 V_{CC} + 0.5	V V
V_{OL}	Low-level Output Voltage I_{OL} = -3.2mA	3.3 5.0			0.45 0.45	V V
V_{OH}	High-level Output Voltage I_{OH} = 0.8mA	3.3 5.0	2.8 4.5			V V
I_{CC}	Power Supply Current (crystal freq. = 9.6 MHz)	3.3 5.0		70 25	90 35	mA mA
	Power-down Supply Current			70	100	µA

Timings

All timing conditions: T_A = 25°C, V_{CC} = 5V, V_{C3} = 3.3V, all outputs except X2 and LFT load capacitance = 30pF, crystal frequency or external clock at X1 = 9.6 MHz.

External ROM Timing

Figure 3. ROM Read Cycle

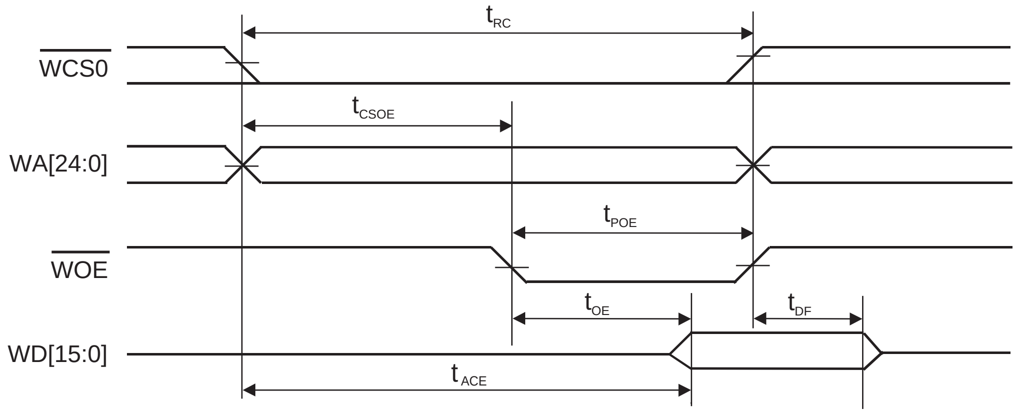


Table 9. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Read Cycle Time	130			ns
t_{CSOE}	Chip Select Low/Address Valid to $\overline{WOE}$ Low	45		80	ns
t_{POE}	Output Enable Pulse Width		78		ns
t_{ACE}	Chip Select/Address Access Time	125			ns
t_{OE}	Output Enable Access Time	70			ns
t_{DF}	Chip Select or $\overline{WOE}$ High to Input Data High-Z	0		50	ns

External RAM Timing

Figure 4. 16-bit SRAM Read Cycle

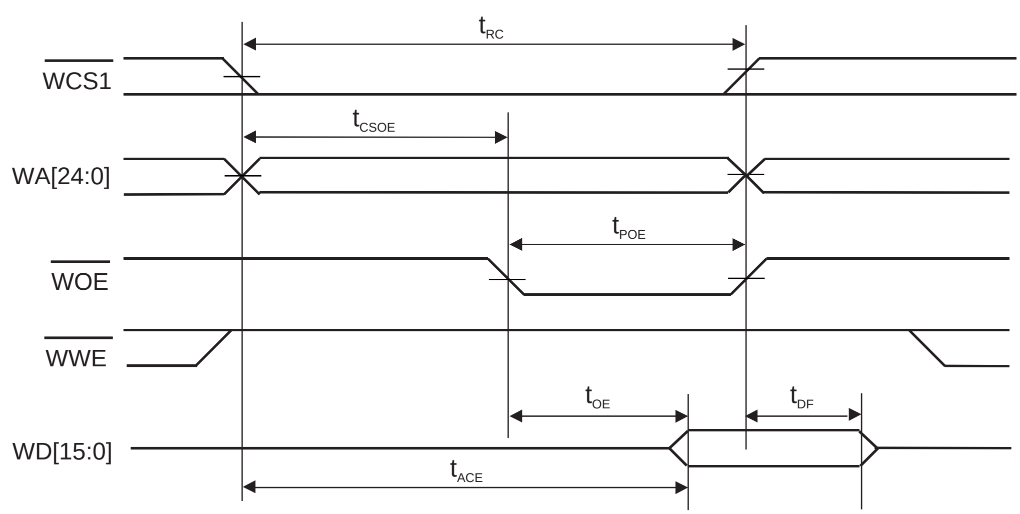


Figure 5. 16-bit SRAM Write Cycle

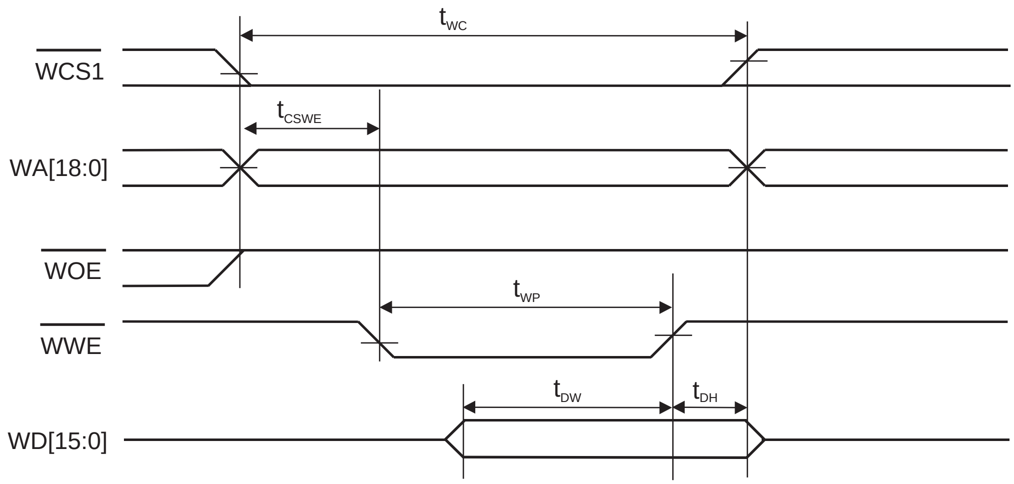


Table 10. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Read Cycle Time	130			ns
t_{CSOE}	Chip Select Low/Address Valid to $\overline{\text{WOE}}$ Low	45		80	ns
t_{POE}	Output Enable Pulse Width		78		ns
t_{ACE}	Chip Select/Address Access Time	125			ns
t_{OE}	Output Enable Access Time	70			ns
t_{DF}	Chip Select or $\overline{\text{WOE}}$ High to Input Data High-Z	0		50	ns
t_{WC}	Write Cycle Time	130			ns
t_{CSWE}	Write Enable Low from $\overline{\text{CS}}$ or Address or $\overline{\text{WOE}}$	40			ns
t_{WP}	Write Pulse Width		104		ns
t_{DW}	Data Out Setup Time	95			ns
t_{DH}	Data Out Hold Time	10			ns

Figure 6. 8-bit SRAM Read Cycle

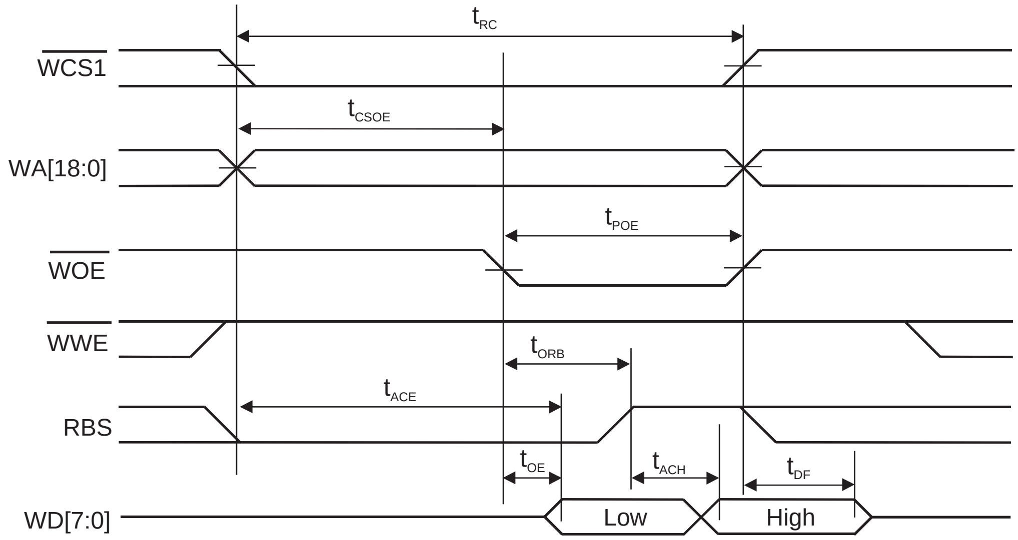


Figure 7. 8-bit SRAM Write Cycle

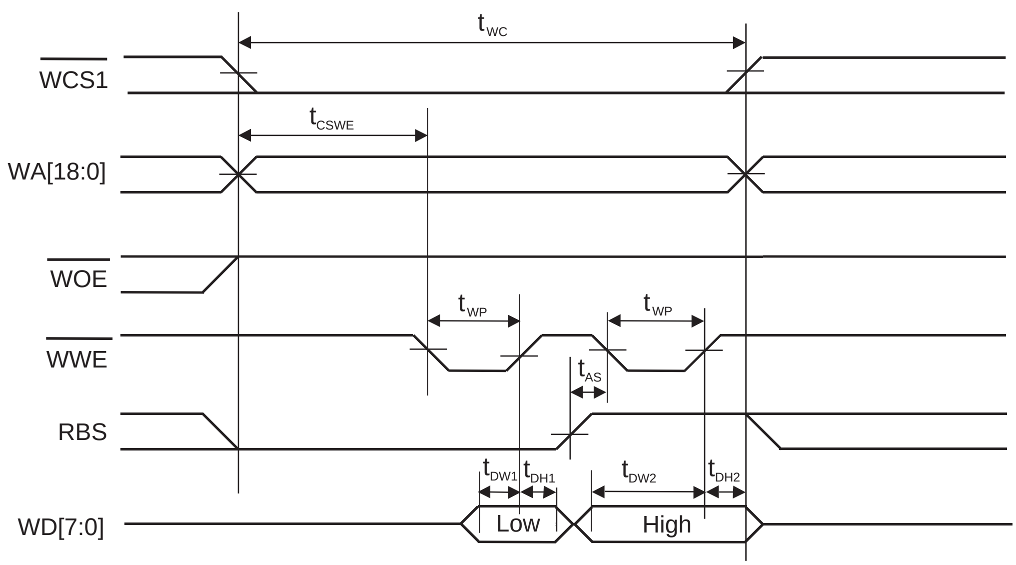
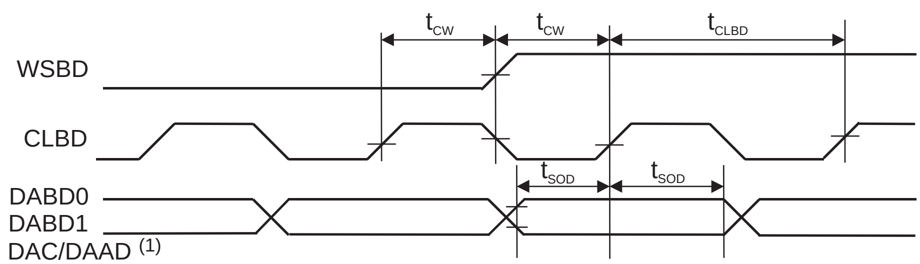


Table 11. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{RC}	Word Read Cycle Time	130			ns
t_{CSOE}	Chip Select Low/Address Valid to $\overline{WOE}$ Low	45		80	ns
t_{POE}	Output Enable Pulse Width		78		ns
t_{ACE}	Chip Select/Address Low Byte Access Time	70			ns
t_{OE}	Output Enable Low Byte Access Time	20			ns
t_{ORB}	Output Enable Low to Byte Select High		26		ns
t_{ACH}	Byte Select High Byte Access Time	45			ns
t_{DF}	Chip Select or $\overline{WOE}$ High to Input Data High-Z	0		50	ns
t_{WC}	Word Write Cycle Time	130			ns
t_{CSWE}	1st $\overline{WWE}$ Low from $\overline{CS}$ or Address or $\overline{WOE}$	40			ns
t_{WP}	Write (Low and High Byte) Pulse Width	20			ns
t_{DW1}	Data Out Low Byte Setup Time	25			ns
t_{DH1}	Data Out Low Byte Hold Time	20			ns
t_{AS}	RBS High to Second Write Pulse	8			ns
t_{DW2}	Data Out High Byte Setup Time	40			ns
t_{DH2}	Data Out High Byte Hold Time	10			ns

Digital Audio

Figure 8. Digital Audio Timing



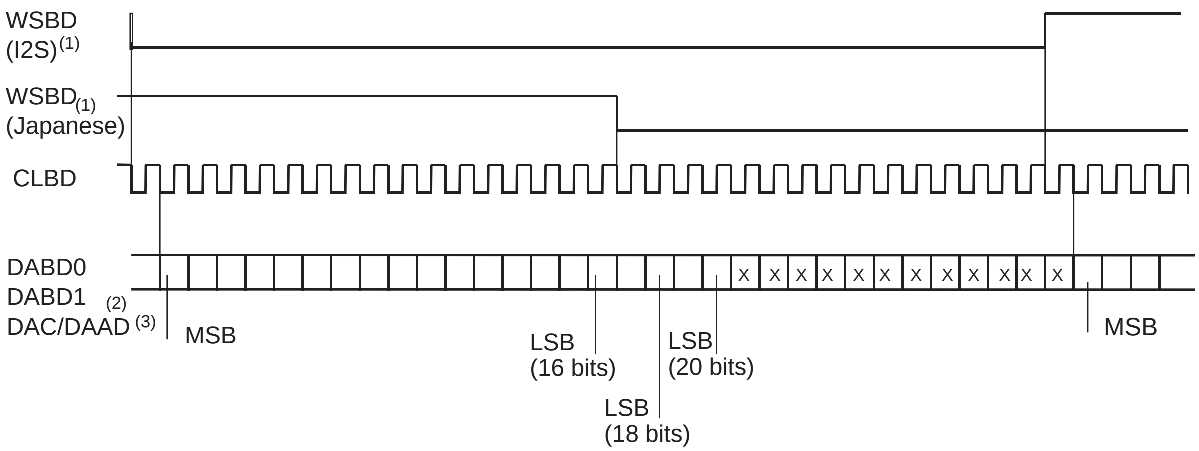
Note: 1. When used as audio in.

Table 12. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
t_{CW}	CLBD Rising to WSBD Change	200			ns
t_{SOD}	DABD Valid before/after CLBD Rising	200			ns
t_{CLBD}	CLBD Cycle Time		416.67		ns

Digital Audio Frame

Figure 9. Digital Audio Frame Format



Notes:
1. Selection between I2S and Japanese format is through pin DAC/DAAD in case of 32K x 8 SRAM.
2. Digital audio in is available only in case of 32K x 16 SRAM. In this case, DAAD is 16 bits only.
3. When used as audio in.

Reset and Power-down

During power-up, the $\overline{\text{RESET}}$ input should be held low until the crystal oscillator and PLL are stabilized, which can take about 20 ms. A typical RC/diode power-up network can be used.

After the low-to-high transition of $\overline{\text{RESET}}$, the following occurs:
- Synthesis enters an idle state
- The RUN output is set to zero
- Firmware execution starts from address 0100H in ROM space ($\overline{\text{WCS0}}$ low)

If $\overline{\text{PDWN}}$ is asserted low, then all I/Os and outputs will be floated and the crystal oscillator and PLL will be stopped. The chip enters a deep power-down sleep mode. To exit power-down, $\overline{\text{PDWN}}$ has to be asserted high, then $\overline{\text{RESET}}$ applied.

Recommended Board Layout

As for all HCMOS high-integration ICs, some rules of board layout should be followed for reliable device operation:
- GND, V_{CC}, V_{C3} distribution, decouplings

  All GND, V_{CC}, V_{C3} pins should be connected. GND and V_{CC} planes are strongly recommended below the ATSAM9713. The board GND and V_{CC} distribution should be in grid form. For 5V V_{CC} operation, if 3.3V is not available, V_{C3} can be connected to V_{CC} by two 1N4148 diodes in series. This guarantees a minimum voltage drop of 1.2V.

  Recommended V_{CC} decoupling is 0.1 µF at each corner of the IC with an additional 10 µF decoupling close to the crystal. V_{C3} requires a single 0.1 µF decoupling close to the IC.
- Crystal, LFT

  The paths between the crystal, the crystal compensation capacitors, the LFT filter R-C-R and the ATSAM9713 should be short and shielded. The ground return from the compensation capacitors and LFT filter should be the GND plane from ATSAM9713.

- Analog section

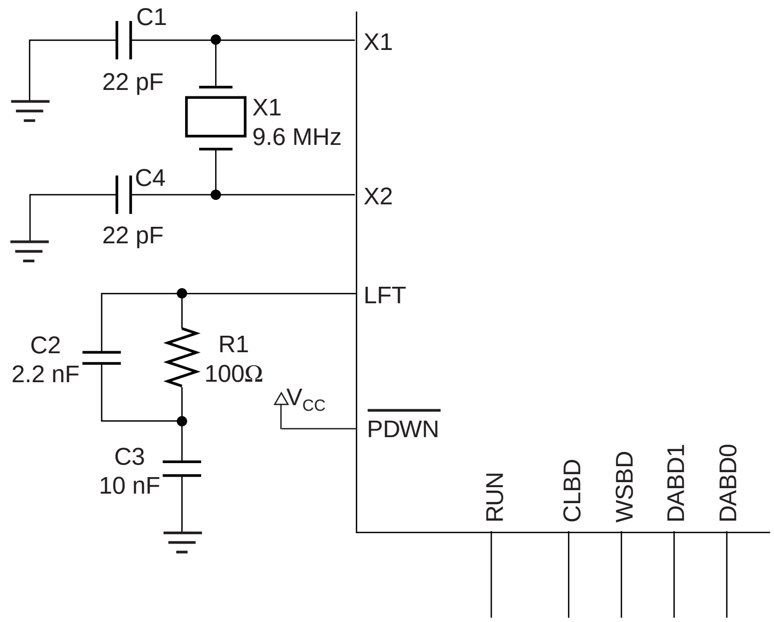
  A specific AGND ground plane should be provided, which connects by a single trace to the GND ground. No digital signals should cross the AGND plane. Refer to the codec vendor recommended layout for correct implementation of the analog section.

- Unused inputs

  Unused inputs should always be connected. A floating input can cause internal oscillation inside the IC, which can destroy the IC by dramatically increasing the power consumption. If you plan to use the power-down feature, care should be taken that no pin is left floating during power- down. Usually, a 1 MΩ ground return is sufficient.

Recommended Crystal Compensation and LFT Filter

Figure 10. Recommended Crystal Compensation and LFT FIlter Description



Note: The X2 output cannot be used to drive another circuit.

Mechanical Dimensions

Figure 11. 80-lead Thin Plastic Quad Flat Pack

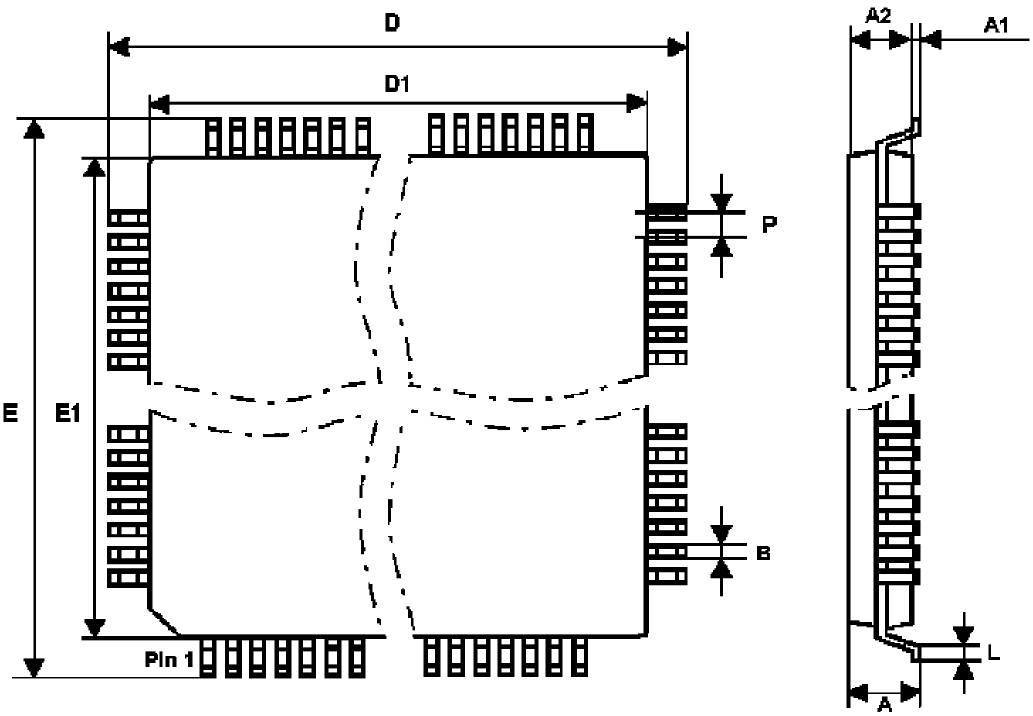


Table 13. Package Dimensions (in mm)

Dimension	Min	Typ	Max
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	15.90	16.00	16.10
D1	13.90	14.00	14.10
E	15.90	16.00	16.10
E1	13.90	14.00	14.10
L	0.45	0.60	0.75
P	–	0.65	–
B	0.22	0.32	0.38

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Warning: GMS960800B may not be installed in any musical instrument except electronic keyboards and synthesizers that have a sale price of less than $75 FOB. Using this product in the manufacture of musical instruments or selling this product for use in a musical instrument (other than the exceptions noted above) is a violation of the intellectual property rights of Roland Corporation and will result in liability for infringement.

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