Optical disc ICs

3-channel H-bridge type BTL driver and 1-channel reversible driver for CD-ROM drives

BA5998FP

The BA5998FP is a 4-channel driver for CD-ROM and CD player motors and actuators. Three of the 4 channels are H-bridge BTL drivers, and 1 is a reversible driver for loading motors. This IC also has an internal 5V regulator and 28-pin HSOP package, allowing for application miniaturization.

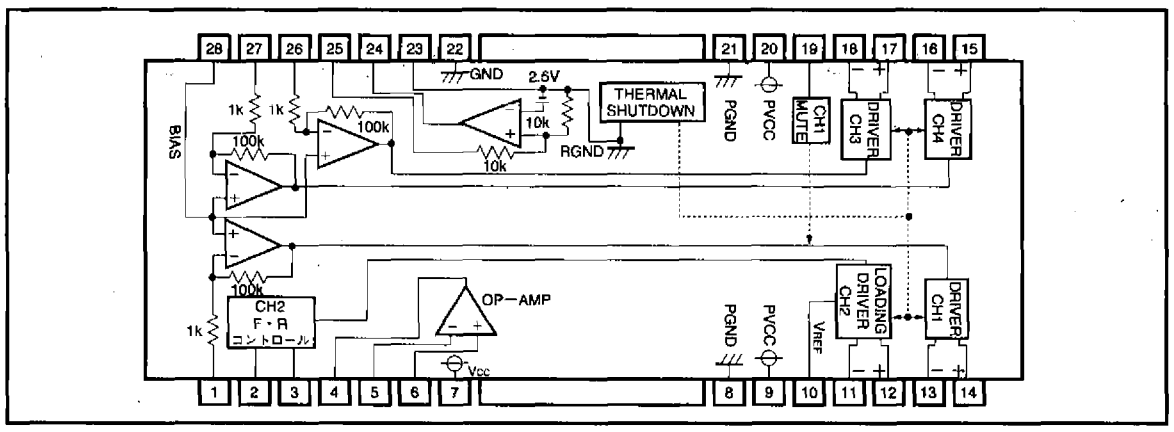
●Applications

CD-ROM drives and CD players

●Features

1) H-bridge BTL drivers (3 channels) and reversible driver (1 channel).
2) HSOP 28-pin package allows for miniaturization of applications.
3) Wide dynamic range.
4) Internal thermal shutdown circuit.
5) Gain is adjustable with an attached resistor.
6) Independence power supplies, for low-voltage operation and efficient drivers.
7) Standby mode when the preamplifier power supply is lowered.
8) CH1 output is muted when the mute pin voltage is raised above 2V.
9) Internal 5V regulator. (requires PNP transistor)
10) Internal standard operational amplifier. (reversible loading driver, CH2)
11) Four modes – forward, reverse, stop [free rotation] and brake – are output according to control logic input (two inputs).
12) Output voltage is set with the V_{REF} pin.

●Block diagram



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●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	18*1	V
Power dissipation	Pd	1.8*2	W
		2.9*3	
Operating temperature range	Topr	−35~85	℃
Storage temperature range	Tstg	−55~150	℃

*1 Applies to both VCCPRE and VCPOW.
*2 When mounted to a 70 × 70 × 1.6 mm glass epoxy board with less than 3% copper foil
*3 When mounted to a 70 × 70 × 1.6 mm glass epoxy board with less than 60% copper foil

●Recommended operating conditions (Allow for power dissipation when setting supply voltage)

Parameter	Symbol		Min.	Typ.	Max.	Unit
Power supply voltage	VCCPRE (Pre Vcc)	When regulator used	6.0	—	14.0	V
		When regulator not used *1	5.5	—	14.0	V
	VCCPOW (CH1,2 Power Vcc)		5.5	—	14.0	V
	VCCPOW (CH3,4 Power Vcc)		1.5	—	14.0	V

*1 Pins 24 and 25 may be left open when the regulator is not used.

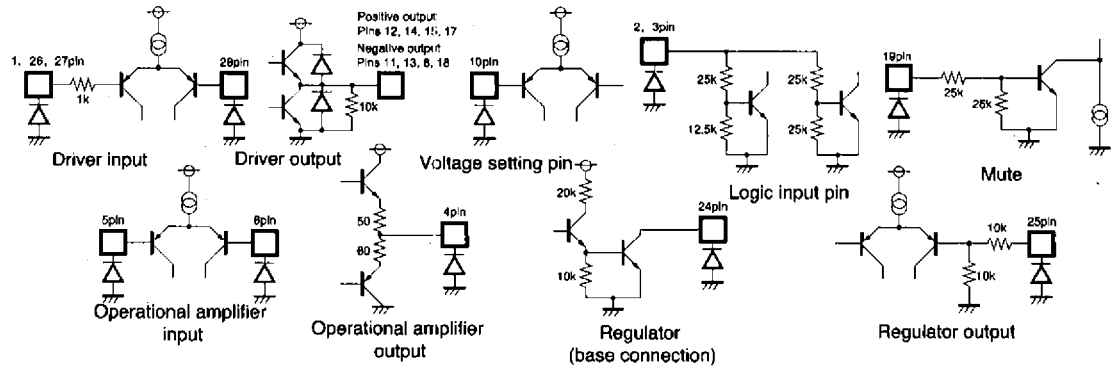
●Pin description

Pin No.	Name	Function
1	VIN1	Channel 1 input
2	FIN	Input of channel 2 forward control signal
3	RIN	Input of channel 2 reverse control signal
4	OPOUT	Operational amplifier output
5	OPIN−	Operational amplifier negative input
6	OPIN+	Operational amplifier positive input
7	VCCPRE	Predrive Vcc
8	PGND	Power ground (channels 1 and 2)
9	VCCPOW	Power Vcc (channels 1 and 2)
10	VREF	High level voltage for channel 2 output
11	VO2−	Channel 2 negative output
12	VO2+	Channel 2 positive output
13	VO1−	Channel 1 negative output
14	VO1+	Channel 1 positive output

Pin No.	Name	Function
15	VO4+	Channel 4 positive output
16	VO4−	Channel 4 negative output
17	VO3+	Channel 3 positive output
18	VO3−	Channel 3 negative output
19	MUTE1	Channel 1 mute
20	VCCPOW	Power Vcc (channels 3 and 4)
21	PGND	Power ground (channels 3 and 4)
22	GND	Predrive ground
23	RGND	Regulator ground
24	REGB	Connect to base of attached PNP transistor
25	REGOUT	5 V output (Note 3)
26	VIN3	Channel 3 input
27	VIN4	Channel 4 input
28	BIAS	Bias input

Notes:1. "Driver positive output" and "driver negative output" indicate polarity relative to input. (For example, pin 14 is HIGH when pin 1 input is HIGH.)
2. Pin 23 is the ground pin for the regulator and internal voltage source and so must be connected to a ground even if the regulator is not used.
3. Attach a transistor collector.

●Input / output circuits



●Electrical characteristics (Unless otherwise noted, Ta=25℃, V_{CCPRE}=V_{CCPOW}=8V, BIAS=2.5V, V_{REF}=2.5V, R_L=8V, R_L=8Ω, R_{IN}=33kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement Circuit
Circuit current 1 (Vcc PRE)	I_{Q1}	3.5	6.5	9.5	mA	Input open	Fig.1
Circuit current 2 (Vcc POW)	I_{Q2}	—	—	10	μA	Input open	Fig.1
Standby current	I_{ST}	—	—	1	μA	V_{CCPRE}=OFF, V_{CCPOW}=4V	Fig.1
⟨CH1, CH3, CH4⟩							
Input voltage, offset	V_{OI}	−5	0	5	mV		Fig.1
Output voltage, offset	V_{OO}	−5	0	5	mV		Fig.1
Dead zone	V_{DB}	5	13	20	mV	Total for positive and negative	Fig.1
Max. output amplitude	V_{OM}	5.0	5.4	—	V	V_{IN}=±2.5V	Fig.1
Voltage gain	G_{VC}	4.5	7.5	10.5	dB	V_{IN}=±0.5V	Fig.1
Positive/negative volt.gain differential	ΔG_{VC}	−1.5	0	1.5	dB		Fig.1
Mute-on voltage	V_{MON}	2.0	—	—	V	CH1only	Fig.1
Mute-off voltage	V_{MOFF}	—	—	0.5	V	CH1only	Fig.1
⟨Loading driver CH2⟩							
Input voltage, high level	V_{IH}	4.0	—	—	V		Fig.1
Input voltage, low level	V_{IL}	—	—	0.5	V		Fig.1
Input current, high level	I_{IH}	—	290	450	μA		Fig.1
Input current, low level	I_{IL}	−2.0	—	+2.0	μA		Fig.1
Vref pin leak output current	I_{REF}	—	0.02	1.0	μA	Forward or reverse mode	Fig.1
Output saturation voltage	V_{CE}	—	1.4	2.1	V	Sum of top and bottom invalid voltage when Io = 100 mA, Vref = 5 V output transistor	Fig.1
Output voltage 1	V_{OUT1}	4.8	5.05	5.3	V	Forward mode I_O=0mA	Fig.1
Output voltage 2	V_{OUT2}	−5.3	−5.05	−4.8	V	Reverse mode I_O=0mA	Fig.1
Output voltage 3	V_{OUT3}	−50	0	50	mV	Break mode I_O=100mA	Fig.1
Output voltage 4	V_{OUT4}	−50	0	50	mV	Stop mode	Fig.1
Output load variation	ΔV_{OUT}	—	170	270	mV	*1	Fig.1
⟨5 V regulator⟩							
Output voltage	V_{REG}	4.75	5.00	5.25	V	I_L=100mA	Fig.2
Output load variation	ΔV_{RL}	−50	0	10	mV	I_L=0~200mA	Fig.2
Supply voltage variation	ΔV_{VCC}	−10	0	60	mV	(V_{CC}=6~14V) I_L=100mA	Fig.2
Drop voltage	V_{DIF}	—	0.3	0.6	V	V_{CC}=4.7V,I_L=200mA*2	Fig.2
Vreg amplifier output current	I_{REG}	8	20	—	mA	Vcc = 4.7 V, 3 V impressed *3	Fig.2
⟨Operational amplifier⟩							
Offset voltage	V_{OFOP}	−5	0	5	mV		Fig.2
Input bias current	I_{BOP}	—	—	300	nA		Fig.2
Output voltage, high level	V_{OHOP}	6.5	7.2	—	V		Fig.2
Output voltage, low level	V_{OLOP}	—	—	1.8	V		Fig.2
Output drive current (sink)	I_{SINK}	10	40	—	mA	50Ω at Vcc	Fig.2
Output drive current (source)	I_{SOURCE}	10	40	—	mA	50Ω at GND	Fig.2
Open loop voltage gain	G_{VO}	—	72	—	dB	V_{IN}=−75dBV, 1kHz	Fig.2
Slew rate	SR	—	1	—	V/μS		Fig.2

◎Not designed for radiation resistance.

*1 "Output load variation" refers to the difference in voltage between 200 mA source and 100 mA source from HIGH level output pin in forward or reverse mode, and the difference in voltage between 200 mA sink and 100 mA sink from LOW level output pin in forward or reverse mode.

*2 When power transformer satisfies characteristic Vsat≦ 0.2 V at 200 mA (Ic).

*3 Pin 5 = open

●Measurement circuit

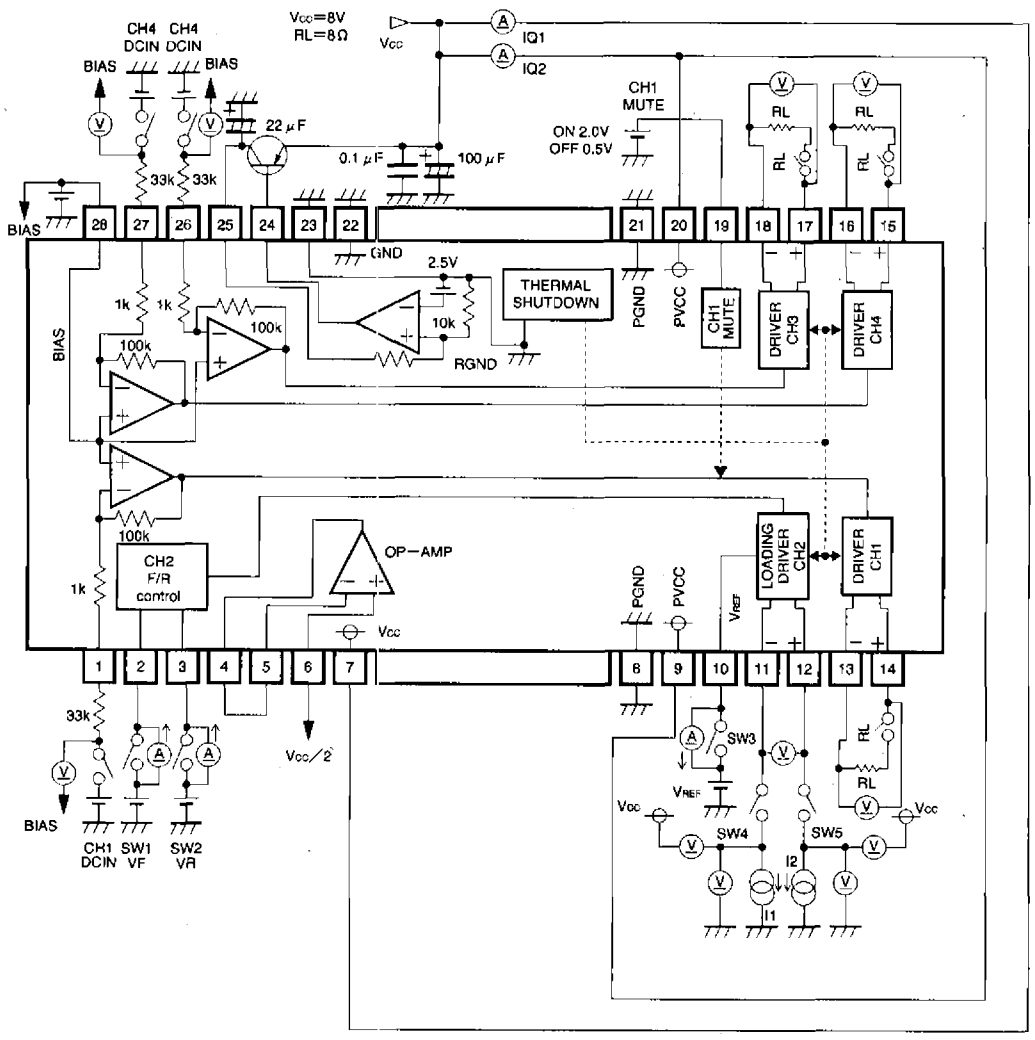


Fig. 1

●Measurement circuit

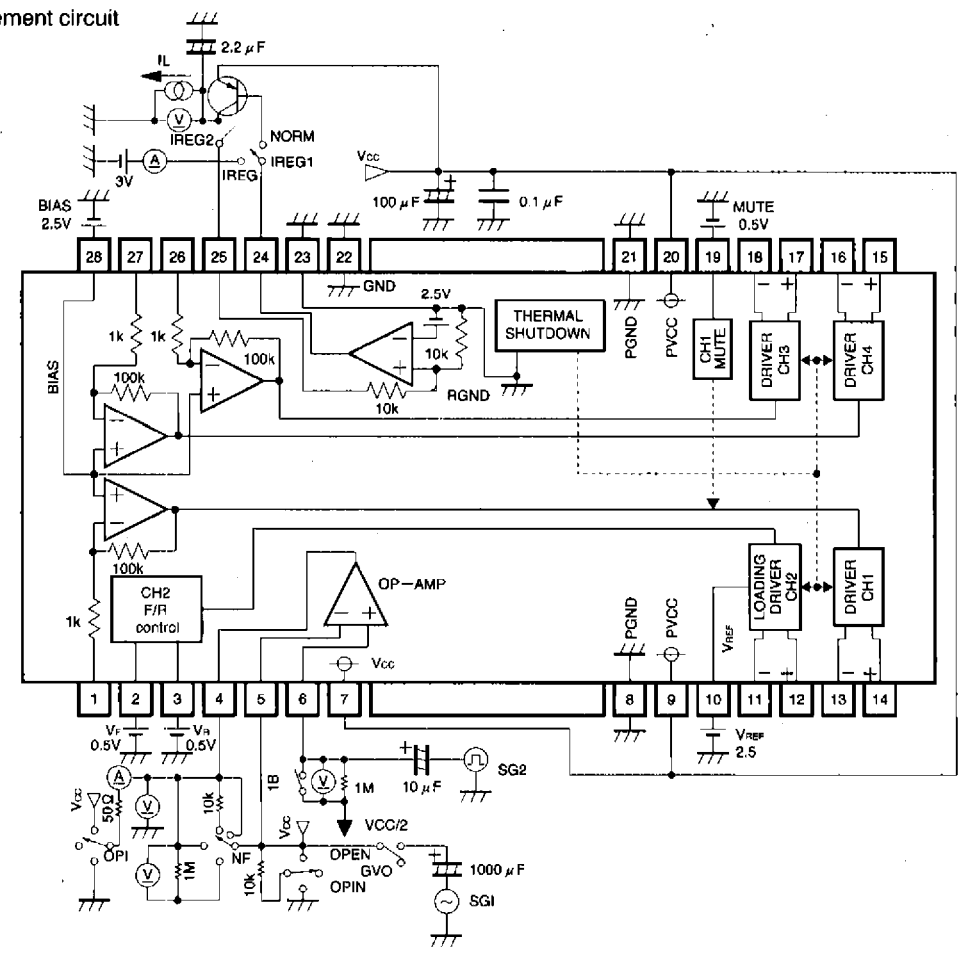


Fig. 2

●Circuit operation

1. Driver

Inputs to the IC are the focus tracking error signal from the servo preamplifier and the control signal from the motor. The input signals normally center on 2.5V and switch polarity depending on voltage size relative to the bias voltage. When polarity is switched, power transistors Q1 and Q4 or Q2 and Q3 turn on. Power transistor Q1 or Q3, whichever is turned on, is driven by the full wave rectified signal and the level shifted signal, and supplies current to the load. When there is no input, both output pins are at the GND level.

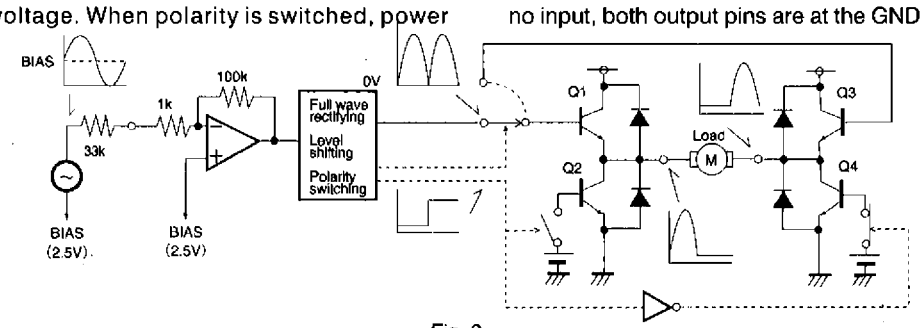


Fig. 3

2. Forward/reverse control block

The IC outputs the forward, reverse, stop (free rotation) or brake mode in accordance with the two control logic inputs.

〈Forward and reverse modes〉

An output voltage twice that of the reference voltage is generated.

〈Stop mode〉

Each pin changes to the high impedance state.

〈Brake mode〉

Each pin outputs 0V.

Logic input and output states

F_{IN}	R_{IN}	OUT (+)	OUT (−)	Mode
H	L	H	L	Forward
L	H	L	H	Reverse
H	H	L	L	Brake
L	L	OPEN	OPEN	Stop

・Normal voltage is not output when the reference voltage is below 1.0V or above $V_{CC}/2-1.0V$. When using the modes below, pass through the stop mode first in order to prevent current penetration. Stop mode times are as follows.

Mode	Stop mode time
Brake → forward/reverse	3 μs or more
Forward ⇄ Reverse	3 μs or more

3. Regulator

This is a typical series regulator that generates a reference voltage internally. A PNP low saturation transistor must be connected.

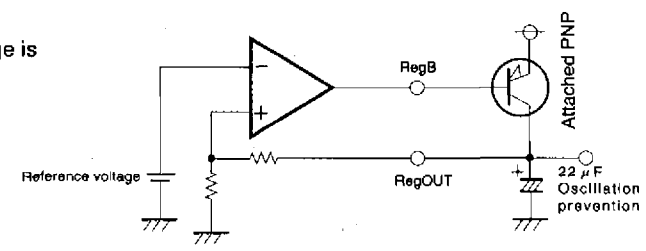


Fig. 4

4. Operational amplifier

A standard 4558 type.

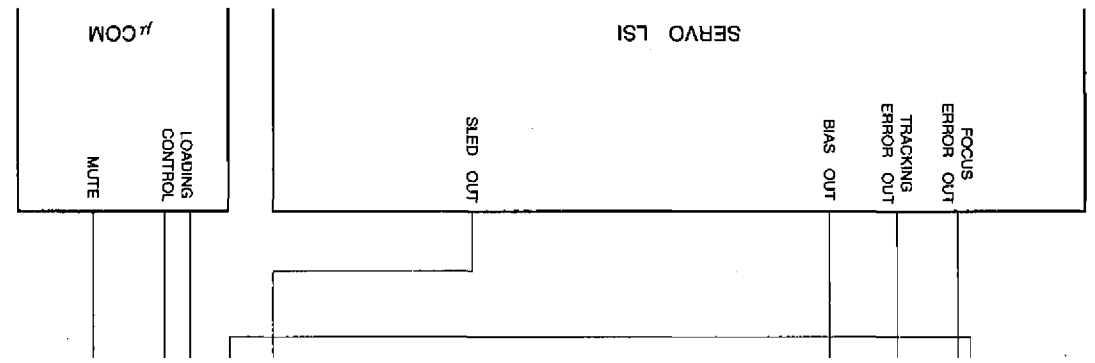
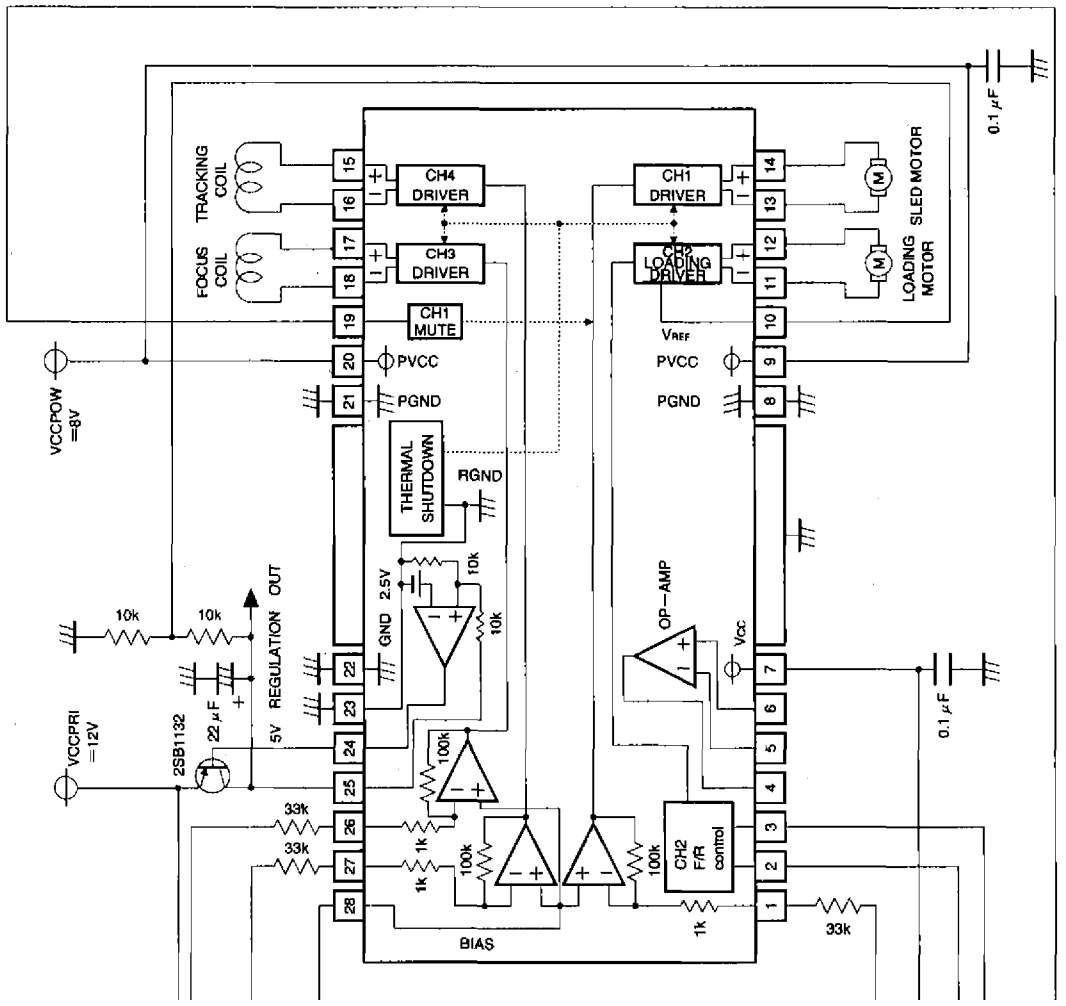

SERVO LSI
SLED OUT
BIAS OUT
TRACKING ERROR OUT
FOCUS ERROR OUT
μCOM
MUTE
LOADING CONTROL

Fig. 5

●Application example



●Operation notes

1. The BA5998FP has an internal shutdown circuit. The output current is muted when the chip temperature exceeds 175℃ (typically).
2. If the mute pin (19 pin) voltage is opened or lowered below 0.5V, the mute pin operates continuously. When the mute pin voltage changes to the HIGH level (above 2V), CH1 output (13, 14 pin) is muted.
3. The bias pin (28 pin) is muted when lowered below 1.4V (typically). Make sure it stays above 1.6V during normal use.
4. All four driver output channels are muted during thermal shutdown, muting and a drop in bias pin voltage. No other components are muted.
5. Dead zone width is determined as follows :
   Dead zone width=input resistance×0.2 μA
   A dead zone like that defined by the above equation occurs when gain is changed. For example, when the attached input resistor is 33kΩ :
   Dead zone width=V_{DB}=(33k+1k)×0.2 μ=6.8mV (one side).
   Thus, total dead zone width for positive and negative is 13.6mV.
6. Be sure to connect the IC to a 0.1 μF bypass capacitor to the power supply, at the base of the IC.
7. Connect the radiating fin to an external ground.
8. The capacitor between regulator output (24 pin) and GND also serves to prevent oscillation of the IC, so select one with good temperature characteristics.
9. Set input resistance to keep input current from exceeding 400 μA.

●Electrical characteristic curves

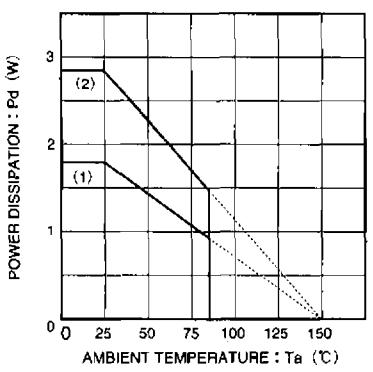


Fig. 6 Thermal derating curve

(1) When mounted to a 70 × 70 × 1.6 mm glass epoxy board with less than 3% copper foil
(2) When mounted to a 70 × 70 × 1.6 mm glass epoxy board with less than 60% copper foil

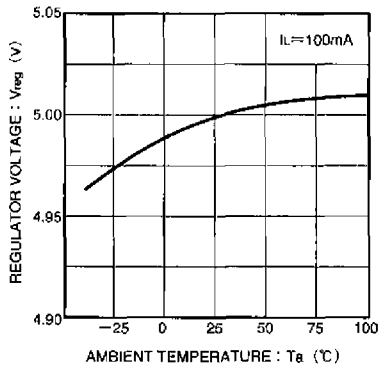


Fig. 7 Regulator voltage vs. temperature

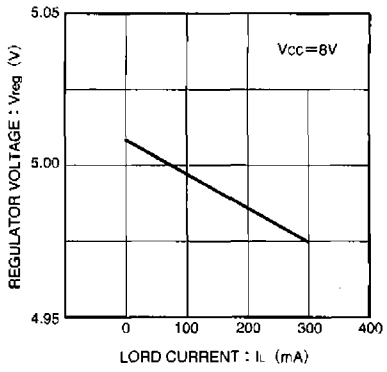


Fig. 8 Load current vs. regulator voltage

●Electrical characteristic curves

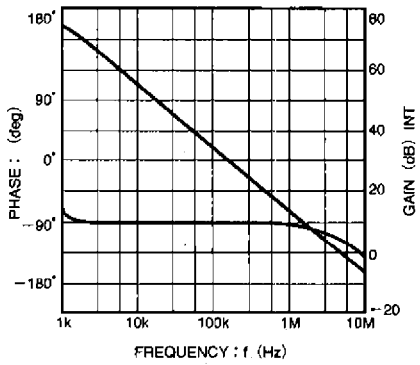


Fig. 9 Operational amplifier vs. open loop characteristics

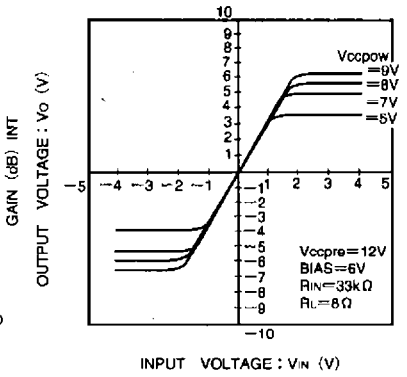


Fig. 10 Driver I/O characteristics (variable VCCPOW)

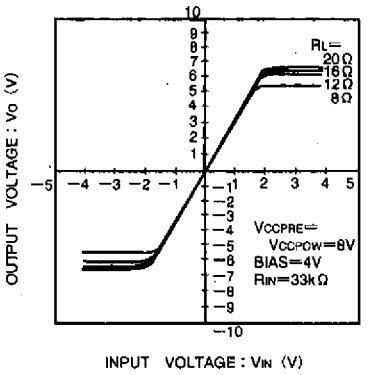


Fig. 11 Driver I/O characteristics (variable load)

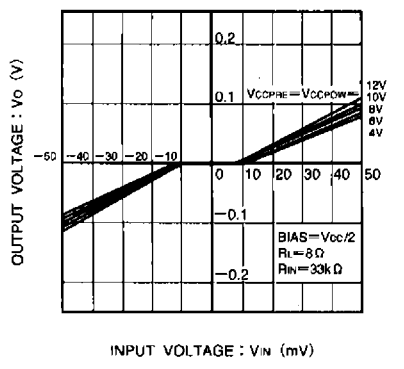


Fig. 12 Dead zone I/O characteristics

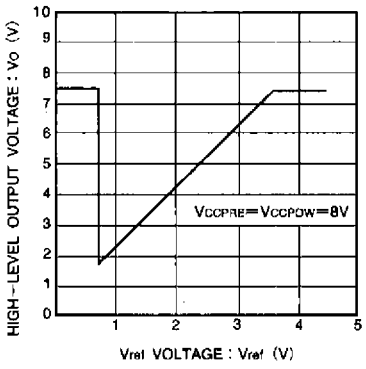


Fig. 13 Reference voltage vs. output voltage

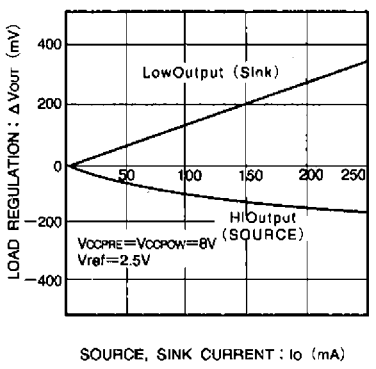
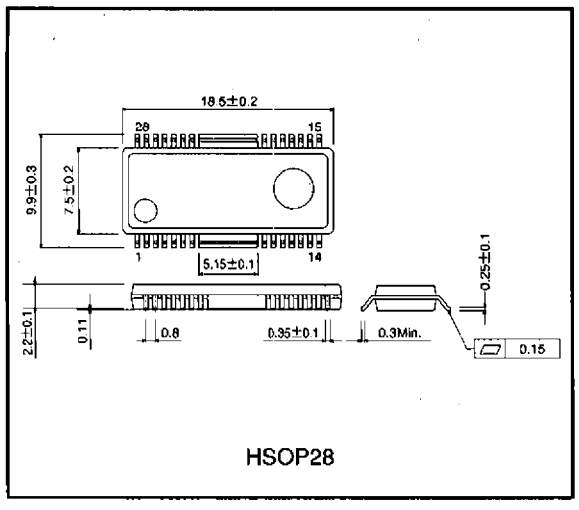


Fig. 14 Current (source and sink) vs. output voltage variation

●External dimensions (Units: mm)



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