Fluorescent display tube level meter driver, 12-point × 2 channel, VU scale, bar display

BA6810F

The BA6810F is a two-channel, 12-point fluorescent display tube driver for VU-scale bar-level meters.
It uses a dynamic-drive system and has both AC and DC inputs. The AC input mode has a peak hold circuit. The IC features a power-on mute, and the output block can directly drive fluorescent display tubes, so few external components are required, allowing cost and space savings while improving reliability. The grid output duty cycle is 1/8.

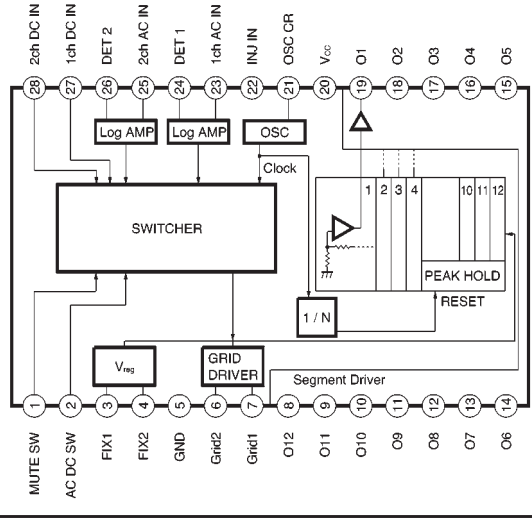
●Applications

Level meters for all types of AV equipment

●Features

1) Uses dynamic-drive system to display two 12-point channels. 28-pin SOP package.
2) AC and DC inputs provided. Switching function allows two-mode display.
3) Upper 8 points have peak hold function in AC mode (two seconds typ.).
4) Power-on mute function.
5) Forced-mute function.
6) Terminal for meter sensitivity adjustment provided (adjustment with one terminal is possible).
7) I^2L injector current terminal provided.
8) Square root compression amplifier built in.
9) Dynamic-drive system reduces the power dissipation of the fluorescent display tube power supply.

●Block diagram



●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V_{CC}	7.0	V
Power dissipation	P_d	550*	mW
Operating temperature	Topr	−20～+70	℃
Storage temperature	Tstg	−55～+125	℃
Output voltage	$V_{CC}+V_{EE}$	36	V

* Reduced by 5.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions

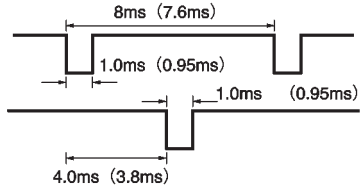
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	—	5.5	V

●Electrical characteristics (unless otherwise noted, Ta = 25°C and V_{CC} = 5.0V)

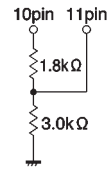
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent power supply current	I_{CC}	—	12	17	mA	R_{inj}=750Ω
〈1 / 2 divider amplifier〉 *1						
Quiescent output voltage	V_{OQ}	—	—	100	mV	I_{IN}=0, R_L=47kΩ
Input resistance	R_{IN}	2.3	3.3	4.3	kΩ	—
Output voltage	V_O	750	1000	1250	mV	I_{IN}=−100μA, R_L=47kΩ
Maximum input current	$I_{IN\ Max.}$	—	—	2	mA	—
Crosstalk	C.T.	—	70	120	mV	V_{IN}=2.4V_{rms}, f=1kHz, R_L=47Ω
Output voltage difference between channels	ΔVo	—	0	±120	mV	V_{IN}=−100μA
Output voltage linearity	ΔV / Δ1	500	680	850	mV	I_{IN}=−10～−100μA
〈DC input〉						
DC input resistance	R_{INDC}	35.5	51	66.5	kΩ	—
〈Mute circuit〉						
Mute pin input resistance	R_{INMU}	35.5	51	66.5	kΩ	—
Mute pin threshold	V_{thmu}	2.2	2.5	2.8	V	—
〈Oscillator〉						
Oscillator frequency	f	1.79	2.1	2.42	kHz	C_1=0.01μF, R_1=47kΩ
〈Drive output circuits for grid and FIP〉						
Peak hold time *2	t_{hold}	—	2.0	—	s	Oscillator frequency = 2.0kHz
Output duty cycle	duty	—	1 / 8	—	—	Oscillator frequency = 2.0kHz *3
Grid output low level voltage	V_{gl}	—	0.4	0.8	V	I_L5mA, R_{inj}=750Ω
Grid output leakage current	I_{gleak}	—	—	10	μA	V_{CE}=5V
Segment output high level voltage	V_{OH}	3.7	4.0	—	V	I_L=2mA, R_{inj}=750Ω
Segment output leakage current	I_{OLEAK}	—	—	10	μA	V_{EE}=−31V
Mute time at power on	t_{mute}	—	1	—	s	Oscillator frequency = 2.0kHz
AC / DC switching input resistance	R_{INAD}	35.5	51	66.5	kΩ	—
AC / DC switching input threshold *4	V_{th}	2.2	2.5	2.8	V	—
〈Comparator〉						
AC comparator level 12	V_{C12AC}	8.5	10	12	dB	Has peak hold *5
AC comparator level 11	V_{C11AC}	5.5	7	8.5	dB	Has peak hold *5
AC comparator level 10	V_{C10AC}	3.0	4	5.5	dB	Has peak hold *5
AC comparator level 9	V_{C9AC}	1.0	2	3.0	dB	Has peak hold *5
AC comparator level 8	V_{C8AC}	—	0	—	dB	Has peak hold *5
AC comparator level 7	V_{C7AC}	−3.0	−2	−1.0	dB	Has peak hold *5
AC comparator level 6	V_{C6AC}	−5.5	−4	−3.0	dB	Has peak hold *5
AC comparator level 5	V_{C5AC}	−8.5	−7	−5.5	dB	Has peak hold *5
AC comparator level 4	V_{C4AC}	−15	−10	−8.5	dB	No peak hold
AC comparator level 3	V_{C3AC}	−25	−20	−15	dB	No peak hold
AC comparator level 2	V_{C2AC}	−35	−30	−25	dB	No peak hold
AC comparator level 1	V_{C1AC}	−55	−40	−35	dB	No peak hold
AC sensitivity *6	V_{INAC}	250	400	630	mVrms	AC comparator 8 on level

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Conditions
DC comparator level 12	V_{C12DC}	2.22	2.49	2.75	V	∗7
DC comparator level 11	V_{C11DC}	1.91	2.13	2.36	V	—
DC comparator level 10	V_{C10DC}	1.51	1.80	2.05	V	—
DC comparator level 9	V_{C9DC}	1.29	1.63	1.95	V	—
DC comparator level 8	V_{C8DC}	1.10	1.46	1.81	V	—
DC comparator level 7	V_{C7DC}	0.99	1.31	1.63	V	—
DC comparator level 6	V_{C6DC}	0.87	1.18	1.49	V	—
DC comparator level 5	V_{C5DC}	0.72	0.98	1.24	V	—
DC comparator level 4	V_{C4DC}	0.56	0.82	1.08	V	—
DC comparator level 3	V_{C3DC}	0.29	0.44	0.59	V	—
DC comparator level 2	V_{C2DC}	0.12	0.22	0.32	V	—
DC comparator level 1	V_{C1DC}	0.04	0.09	0.15	V	—
Maximum grid output current	$I_{OMax.}$	5	—	—	mA	V_{OL}=0.8V, R_{inj}=750Ω
Maximum segment output current	$I_{OMax.}$	2	—	—	mA	V_{OH}=3.7V, R_{inj}=750Ω
Comparator level reference point voltage	V_{CO}	1.98	2.2	2.42	V	∗8
Rch and Lch dispersion	R / L	−1.0	0	+1.0	dB	∗9

∗1 The attack and recovery times of the CR smoothing circuit connected to pins 3 and 5 can be changed by using different values for the resistor and capacitor. The sag of the CR circuit discharge will influence the comparator level to a certain extent.
∗2 Peak hold is available for the levels of comparators 5 to 12 in AC mode. Peak hold is not available for DC mode.
∗3 The grid output duty cycle (pins 13 and 14) is shown in the duty timing diagram (for an oscillator frequency of 2kHz). The values in parentheses are typical values for component values of C = 0.01 μF and R = 47kΩ.



∗4 When the input switch level is "H", AC input is selected, and when it is "L", DC is selected.
∗5 The ratings given in the table for AC comparator levels are after 0dB adjustment has been performed. Adjust using the voltage on pin 10.
∗6 The AC sensitivity ratings are for when the circuit connected to pins 10 and 11 is as shown in the diagram on the right. Ratings related to AC input are for when the input is from an oscillator with an output impedance of 600Ω.
∗7 There is no chance that the segments will light out of order or light simultaneously. The DC sensitivity ratings are for when the circuit connected to pins 10 and 11 is as shown in the diagram on the right. Therefore, the level will change somewhat after 0dB adjustment with AC input.
∗8 Pin 10 voltage when the 8th segment lights for an input of AC400mVrms.
∗9 When the pin 10 and 11 conditions are the same as for item 6), the ratio of the R and L channel AC input voltages referred to the L channel when the 8th point lights.



●Measurement circuit

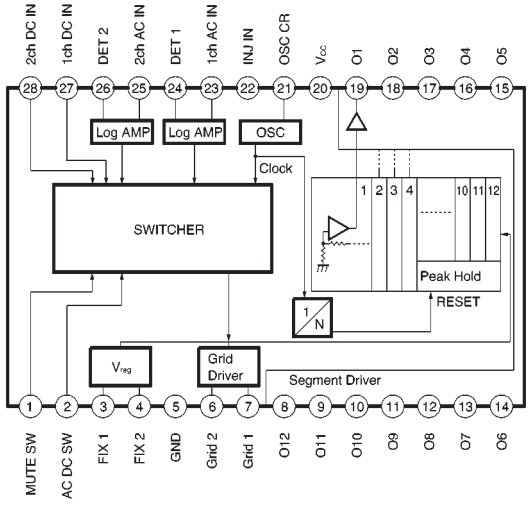


Fig. 1

●Application example

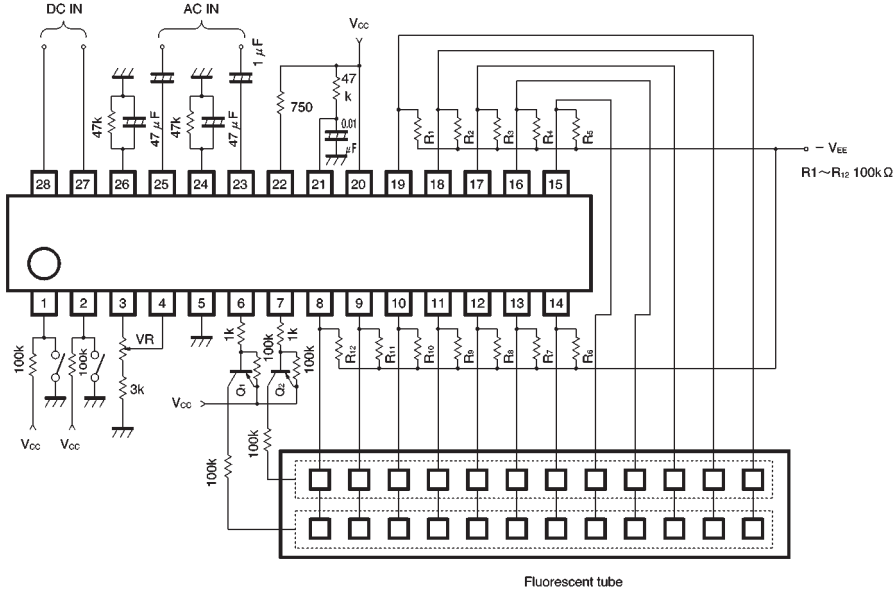


Fig. 2

●Circuit operation

(1) Input block

The AC input pins are pins 23 and 25, and the DC input pins are pins 27 and 28. Pin 2 is used to switch between the AC and DC inputs. When the input to pin 2 is “H”, AC input is selected (pins 23 and 25). Therefore, by using pin 2 to switch between the AC and DC modes, the IC can do two jobs, using one fluorescent tube. For example, pins 23 and 25 can be used for audio signal input, and pins 27 and 28 can be used as the input for the signal meter output from a tuner (DC).

(2) Peak hold circuit

The BA6810F features a peak hold circuit that temporarily holds peak signal levels in AC input mode.

The peak hold function can be used with the upper 8 points (5 to 12). The peak hold time depends on the oscillator frequency. It is 2 sec. (typ.) for an oscillator frequency of 2kHz.

(3) MUTE function

The display can be turned off by driving the MUTE terminal “H”.

(4) Meter sensitivity adjustment terminal

Connect a potentiometer of about 10kΩ, and adjust it so that the 8th point lights when the for an AC input of 400mV$_{rms}$. The dispersion between left and right channels is ±1.0dB.

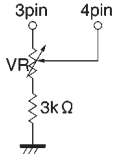


Fig. 3

(5) Grid output

The pin 6 and 7 grid outputs are open-collector NPN transistors. The logic is active low (the fluorescent tube lights when the output is “L”), so connect two PNP transistors Q_1 and Q_2 as shown in the application example circuit to drive the fluorescent tubes (see Fig. 4).

(6) Segment output block

Pins 8 to 19 are the segment outputs. The output circuits are open-collector PNP transistors. When grid 1 is “L”, the ch1 level is output (pin 23 or 27 input level), and when grid 2 is “L”, the ch2 level is output (pin 25 or 28 input level). Refer to Fig. 5.

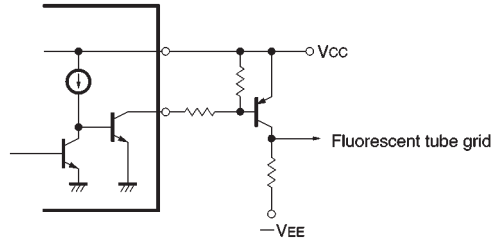


Fig. 4

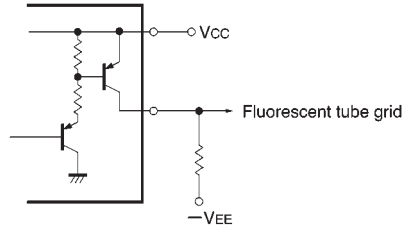


Fig. 5

(7) Grid and segment output timing chart.

The grid and segment output timing is shown in Fig. 6.

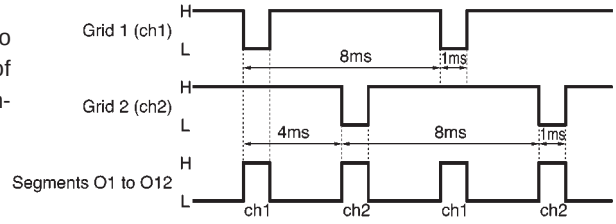


Fig. 6

(8) Attack and recovery times

The output response characteristic for AC input signals is set by pins 24 and 26. The comparator level may change somewhat due to the sag of the CR circuit discharge.

(9) Oscillator frequency

The resistor and capacitor connected to pin 21 determine the oscillator frequency. The oscillator frequency (f_{osc}) and grid output period (T) are related as follows:

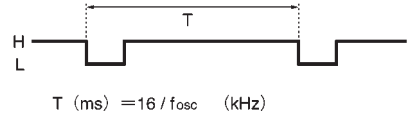


Fig. 7

●Electrical characteristics curves

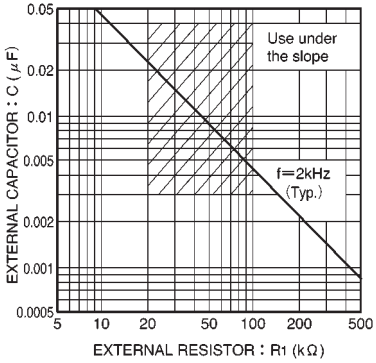


Fig. 8 Value of external components for oscillator

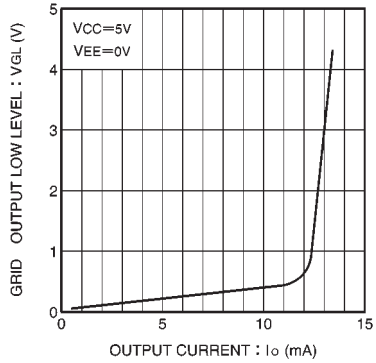


Fig. 9 Grid low level output vs. output current

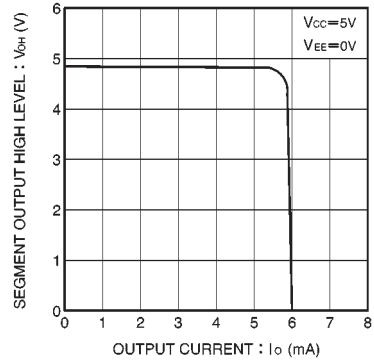


Fig. 10 Segment high level output vs. output current

●External dimensions (Units: mm)