Synchronization signal processor for high definition displays

BA7078AF

The BA7078AF is a synchronization signal processing LSI chip designed for multiscan high-definition displays. It generates a synchronization signal and clamp pulse for three types of input signals: separate synchronization, composite synchronization, and synchronization on video.

●Application

CRT displays

●Features

1) Operates on a single 5V power supply, with low power consumption.
2) Synchronization signal existence and polarity detec-tion output.
3) Adjustable clamp pulse width, allowing for the selec-tion of front or back editing.
4) Vertical synchronization separation is based on hori-zontal frequency tracking, for separation starting at 1H.
5) Minimal attached components.

●Absolute maximum ratings (Ta = 25°C)

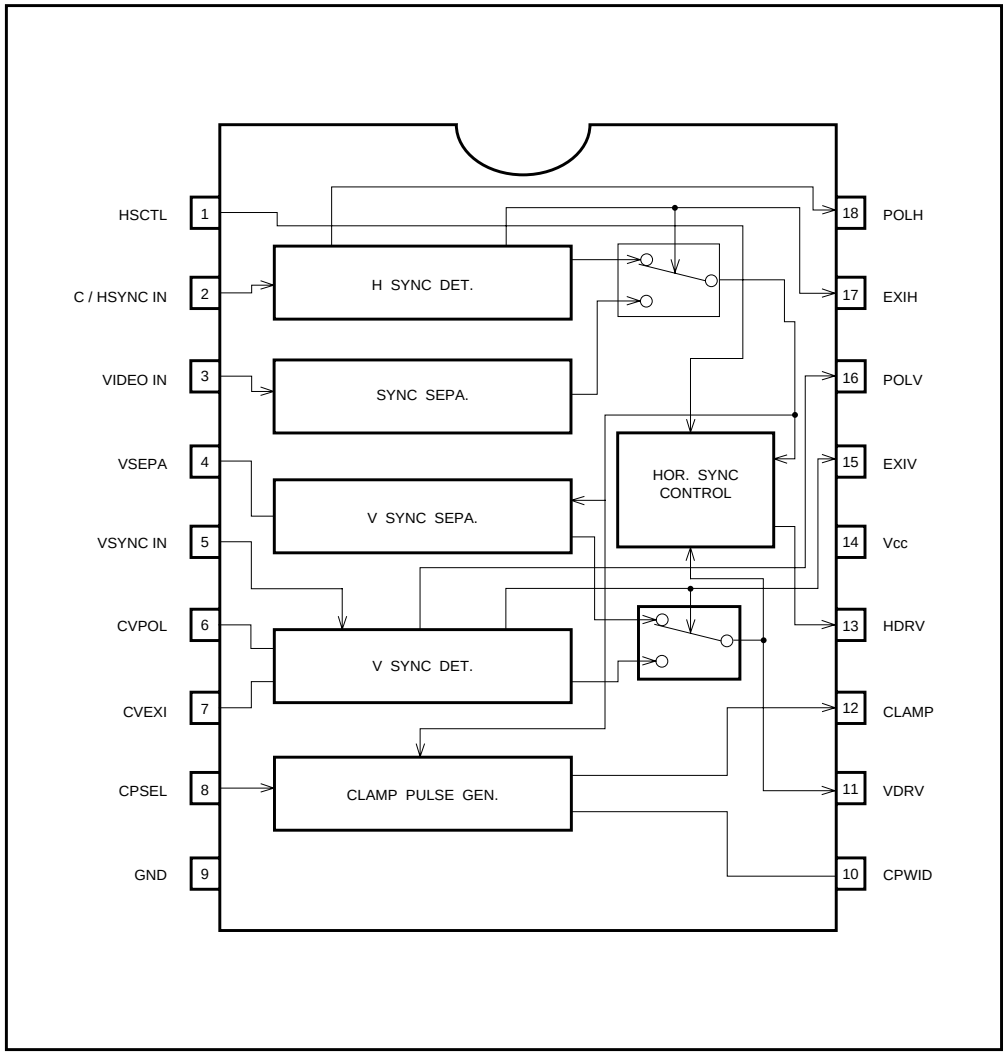
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	7.0	V
Power dissipation	Pd	450	mW
Operating temperature	Topr	−25〜+75	°C
Storage temperature	Tstg	−55〜+125	°C

∗ Reduced by 4.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V

●**Block diagram**

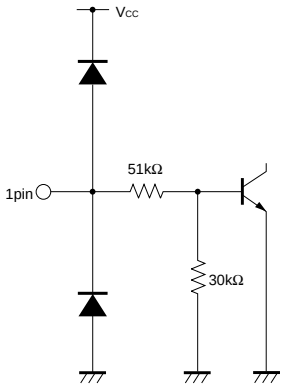


●Pin descriptions

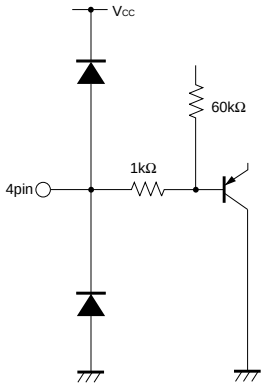
Pin No.	Pin name	Functions	
1	HSCTL	HDRV output	Used to select whether to output the VDRV section of the HDRV output signal. High : VDRV section of HDRV is output Low : VDRV section of HDRV is not output
2	C / HSYNC IN	Composite sync / H SYNC input	Input either the composite synchronization signal or the horizontal synchronization signal. Input is clamped, and is initiated by capacitor coupling.
3	VIDEO IN	SYNC ON VIDEO input	Inputs the SYNC ON VIDEO signal(green). Input is sink chip clamped. Input is initiated by capacitor coupling.
4	VSEPA	f-V conversion	Converts the horizontal synchronization signal frequency into a voltage. The voltage generated is proportional to the frequency of the horizontal synchronization signal. Attach a 0.56μF capacitor between the ground pins.
5	VSYNC IN	V SYNC input	Inputs the vertical synchronization signal.
6	CVPOL	Vertical polarity integration	Integrates the vertical synchronization signal polarity detection circuit. Attach a 1.5μF capacitor between this pin and the ground.
7	CVEXI	Vertical existence integration	Integrates the vertical synchronization signal existence detection circuit. Attach a 1μF capacitor between this pin and the ground.
8	CPSEL	Setting the clamp position	Used to set the clamp pulse generation position to either the front or back edge of HSYNC High : The front edge is the generation position Open : Composite / H SYNC IN : The front edge is the generation position VIDEO IN : The back edge is the generation position Low : The back edge is the generation position
9	GND	Ground	–
10	CPWID	Setting the clamp pulse width	Sets the clamp pulse width according to the attached time constant. Attach a resistor between this pin and V_{CC} and, a capacitor between this pin and GND. When R = 3.9kΩ and C = 100pF, pulse width is approximately 400 ns. Set the resistor to register an abnormality at 1kΩ.
11	VDRV	VDRV output	Outputs the vertical synchronization signal. The output signal has positive polarity.
12	CLAMP	Clamp output	Outputs the clamp pulse generated from the vertical synchronization signal. The output signal has a positive polarity.
13	HDRV	HDRV output	Outputs the clamp pulse generated from the horizontal synchronization signal. The output signal has positive polarity.
14	V_{CC}	Power supply	–
15	EXIV	Vertical existence output	Indecates whether the vertical synchronization signal exists. For the output logic, refer to the separate table.
16	POLV	Vertical polarity output	Indicates the polarity of the vertical synchronization signal. For the output logic, refer to the separate table.
17	EXIH	Horizontal existence output	Indicates whether the horizontal synchronization signal exists. For the output logic, refer to the separate table.
18	POLH	Horizontal polarity output	Indicates the polarity of the horizontal synchronization signal. For the output logic, refer to the separate table.

●Input / output circuits

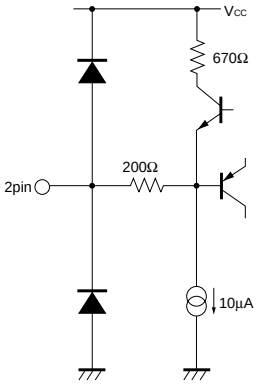
HSCTL



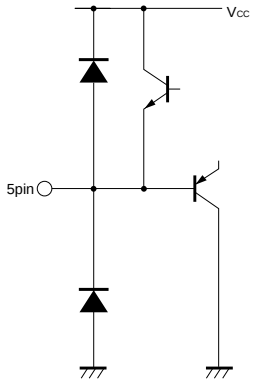
VSEPA



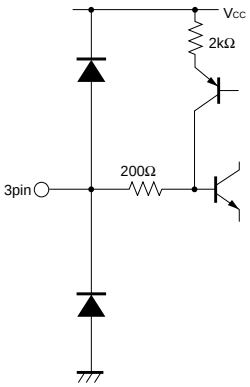
C / HSYNC IN



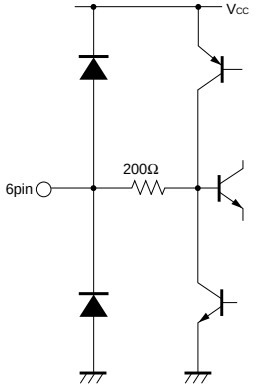
VSYNC IN



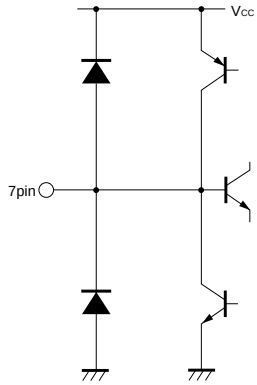
VIDEO IN



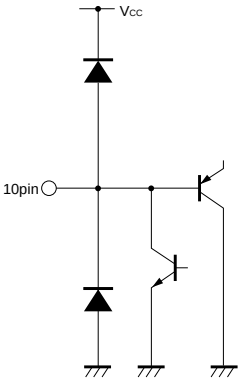
CVPOL



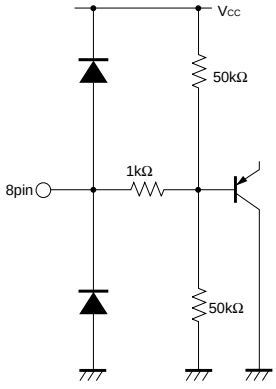
CVEXI



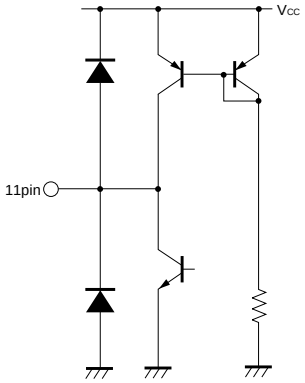
CPWID



CPSEL

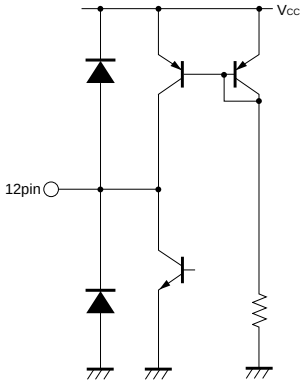


VDRV

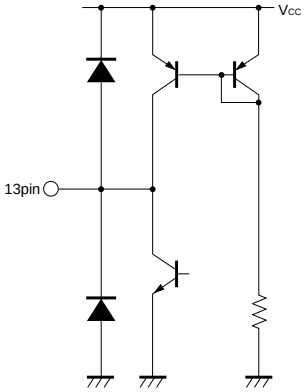


GND

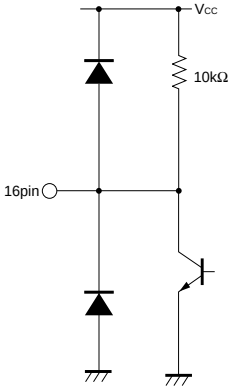
CLAMP



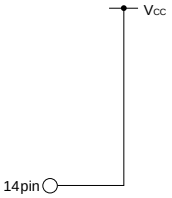
HDRV



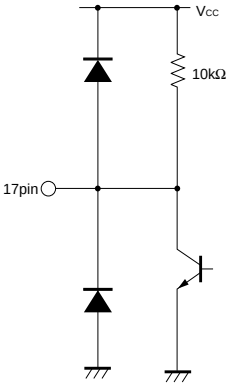
POLV



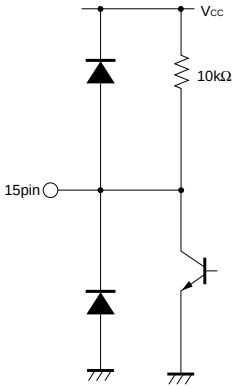
Vcc



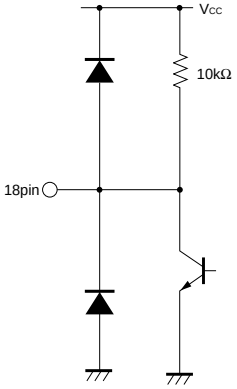
EXIH



EXIV



POLH



●**Electrical characteristics** (unless otherwise noted, V_{CC} = 5V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage	V_{CC}	4.5	5.0	5.5	V	
Quiescent current	I_{CC}	21	30	39	mA	
VDRV output voltage "H"	V VDH	4.5	5.0	–	V	
VDRV output voltage "L"	V VDL	–	0.2	0.5	V	
VDRV output current "L"	I VDL	8	–	–	mA	
VDRV rising delay time	trdVD	–	280	450	ns	VSYNC IN
HDRV output voltage "H"	V HDH	4.5	5.0	–	V	
HDRV output voltage "L"	V HDL	–	0.2	0.5	V	
HDRV output current "L"	I HDL	8	–	–	mA	
HDRV rising delay time (1)	trdHD1	–	65	115	ns	C / HSYNC IN
HDRV rising delay time (2)	trdHD2	–	95	145	ns	VIDEO IN
CLAMP output voltage "H"	V CPH	4.5	5.0	–	V	
CLAMP output voltage "L"	V CPL	–	0.2	0.5	V	
CLAMP output current "L"	I CPL	8	–	–	mA	
CLAMP rising delay time (1)	trdCP1	–	75	125	ns	front edge
CLAMP rising delay time (2)	trdCP2	–	95	145	ns	back edge
Synchronization detection output voltage "H"	V DH	4.5	5.0	–	V	
Synchronization detection output voltage "L"	V DL	–	0.2	0.5	V	
Synchronization detection output current "L"	I DL	3	–	–	mA	
Synchronization detection output impedance	Z oD	7	10	13	kΩ	
Minimum synchronization separation level	V SMin.	–	–	0.2	V_{P-P}	
HSCTL "H" level threshold voltage	V tHSH	2.5	–	–	V	
HSCTL "L" level threshold voltage	V tHSL	–	–	1.5	V	
CPSEL "H" level threshold voltage	V tCPH	3.8	–	–	V	
CPSEL "L" level threshold voltage	V tCPL	–	–	1.2	V	

●**Synchronization signal detection chart**

INPUT		OUTPUT			
Composite / HSYNC	VSYNC	EXIH	EXIV	POLH	POLV
H. COMP (Positive)	No signal	H	L	L	L
	Positive	H	H	L	L
	Negative	H	H	L	H
H. COMP (Negative)	No signal	H	L	H	L
	Positive	H	H	H	L
	Negative	H	H	H	H
No signal	No signal	L	L	L	L
	Positive	L	H	L	L
	Negative	L	H	L	H

●Relationship between INPUT to OUTPUT

INPUT			OUTPUT		
Composite / HSYNC	VSYNC	VIDEO	HDRV	VDRV	CLAMP
–	–	○	VIDEO	VIDEO	VIDEO
○	–	○	CS	CS	CS
–	○	○	VIDEO	VS	VIDEO
○	○	○	CS	VS	CS
–	–	–	–	–	–
○	–	–	CS	CS	CS
–	○	–	–	VS	–
○	○	–	CS	VS	CS

Explanation of symbol ○: Signal Input ―: No Signal

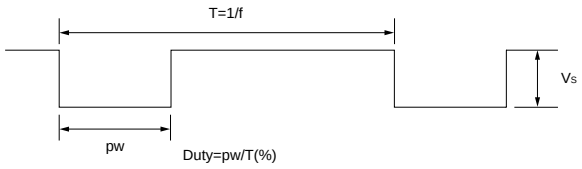
●Input signal range

Parameter	Vert. separate sync	Hor. separate sync	Composite sync	Sync on Video
Polarity	Posi. / Neg.	Posi. / Neg.	Posi. / Neg.	Neg.
Amplitude (Sync) : Vs	1.0~5.0V_{P-P}	1.0~5.0V_{P-P}	1.0~5.0V_{P-P}	0.2~0.6V_{P-P}
(Video) : Vv				0~2.1V_{P-P}
Vert. sync frequency range : fV	40~200Hz	–	40~200Hz	40~200Hz
Vert. sync pulse width range : pwV	8.0µs~Duty35%	–	＊1HMin.~400µs	＊1HMin.
Hor. sync frequency range : fH	–	15k~200kHz	15k~200kHz	15k~200kHz
Hor. sync pulse width range : pwH	–	94ns~Duty35%	94ns~Duty30%	Duty30% Max.

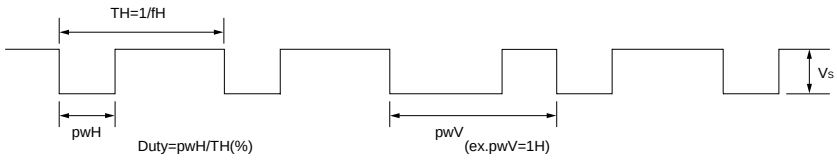
＊1H = 1 / fH

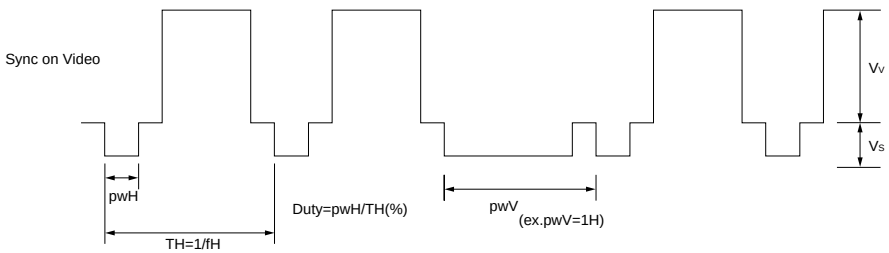
●Input signal waveform

Vert. / Hor.separate sync



Composite sync





●**Measurement circuit**

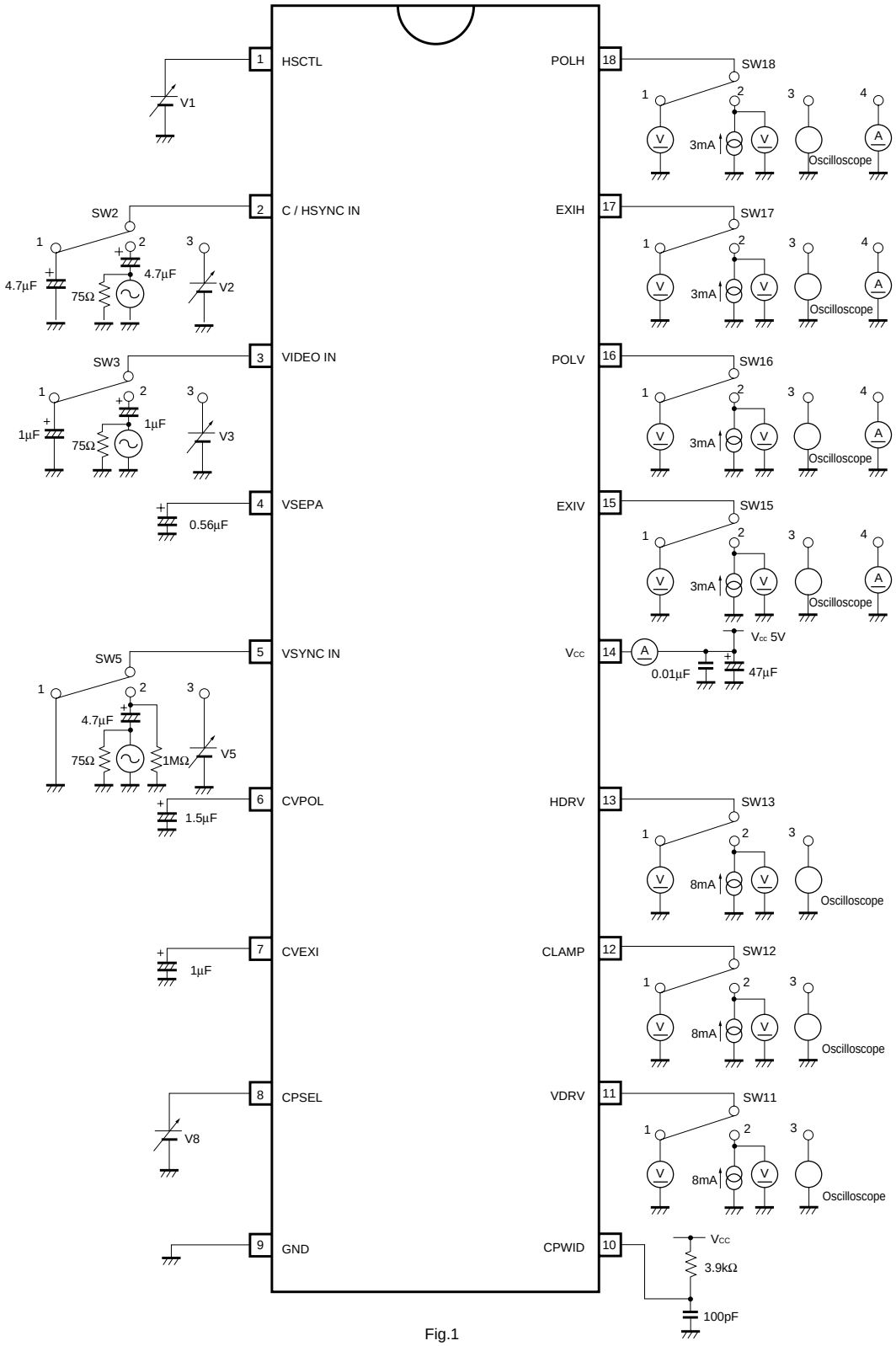


Fig.1

●Conditions for measurement of electrical characteristics

Parameter	Switch condition									
	2	3	5	11	12	13	15	16	17	18
Quiescent current	1	1	1	1	1	1	1	1	1	1
VDRV output voltage "H"	1	1	3	1	1	1	1	1	1	1
VDRV output voltage "L"	1	1	3	1	1	1	1	1	1	1
VDRV output current "L"	1	1	3	2	1	1	1	1	1	1
VDRV rising delay time	1	1	2	3	1	1	1	1	1	1
HDRV output voltage "H"	3	1	1	1	1	1	1	1	1	1
HDRV output voltage "L"	3	1	1	1	1	1	1	1	1	1
HDRV output current "L"	3	1	1	1	1	2	1	1	1	1
HDRV rising delay time (1)	2	1	1	1	1	3	1	1	1	1
HDRV rising delay time (2)	1	2	1	1	1	3	1	1	1	1
CLAMP output voltage "H"	2	1	1	1	3	1	1	1	1	1
CLAMP output voltage "L"	2	1	1	1	3	1	1	1	1	1
CLAMP output current "L"	3	1	1	1	2	1	1	1	1	1
CLAMP rising delay time (1)	2	1	1	1	3	1	1	1	1	1
CLAMP rising delay time (2)	1	2	1	1	3	1	1	1	1	1
POLH output voltage "H"	2	1	1	1	1	1	1	1	1	1
POLH output voltage "L"	2	1	1	1	1	1	1	1	1	1
POLH output current "L"	3	1	1	1	1	1	1	1	1	2
POLH output impedance	3	1	1	1	1	1	1	1	1	4
EXIH output voltage "H"	2	1	1	1	1	1	1	1	1	1
EXIH output voltage "L"	1	1	1	1	1	1	1	1	1	1
EXIH output current "L"	3	1	1	1	1	1	1	1	2	1
EXIH output impedance	3	1	1	1	1	1	1	1	4	1
POLV output voltage "H"	1	1	2	1	1	1	1	1	1	1
POLV output voltage "L"	1	1	2	1	1	1	1	1	1	1
POLV output current "L"	1	1	3	1	1	1	1	2	1	1
POLV output impedance	1	1	3	1	1	1	1	4	1	1
EXIV output voltage "H"	1	1	2	1	1	1	1	1	1	1
EXIV output voltage "L"	1	1	1	1	1	1	1	1	1	1
EXIV output current "L"	1	1	3	1	1	1	2	1	1	1
EXIV output impedance	1	1	3	1	1	1	4	1	1	1
Minimum synchronization separation level	1	2	1	1	1	3	1	1	1	1
HSCTL "H" level threshold voltage	2	1	2	1	1	3	1	1	1	1
HSCTL "L" level threshold voltage	2	1	2	1	1	3	1	1	1	1
CPSEL "H" level threshold voltage	1	2	1	1	3	3	1	1	1	1
CPSEL "L" level threshold voltage	2	1	1	1	3	3	1	1	1	1

●**Application example**

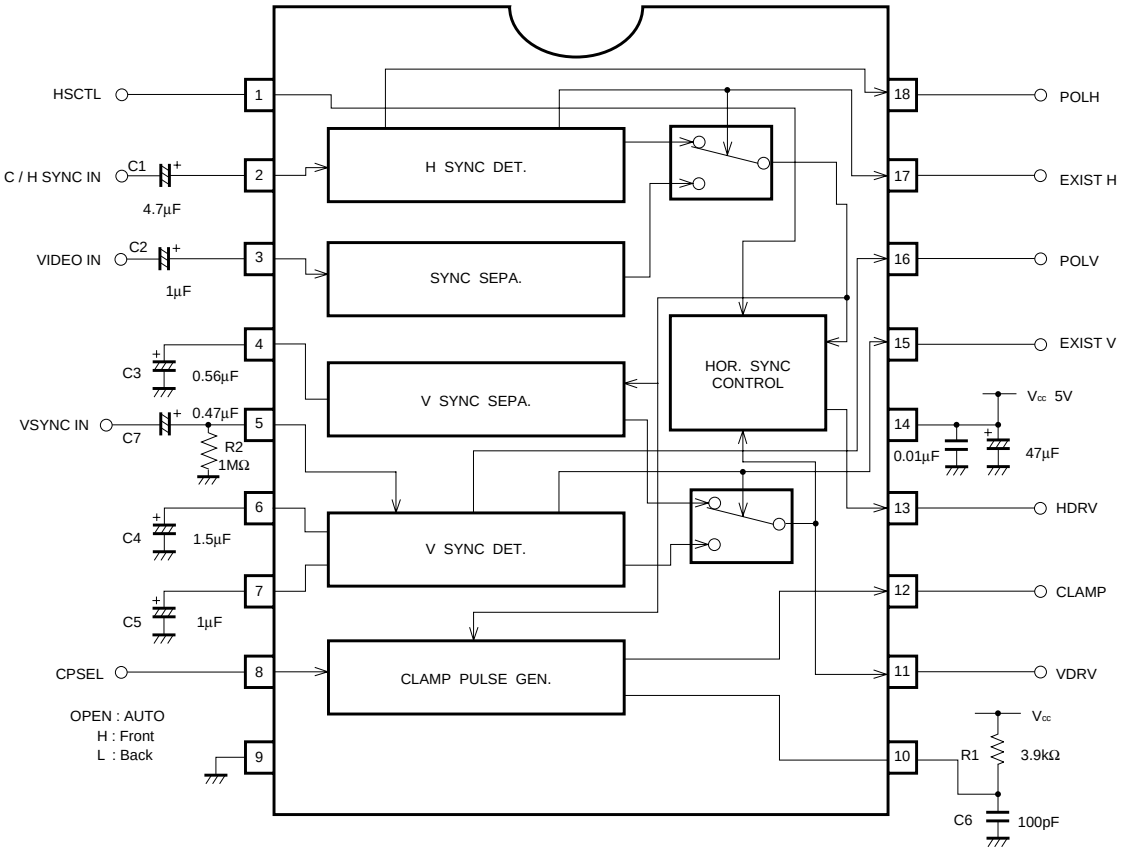
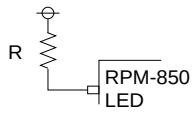


Fig.2

●Attached components

R : The resistor for limiting the LED current.
Use the resistor of not less than 1W.



C1 : 47μF Coupling capacitor for C / H SYNC IN
A low capacitance increases the size of the input pin waveform's sag.

C2 : 1μF Coupling capacitor for VIDEO IN
A low capacitance increase the size of the input pin waveform's sag.

C3 : 0.56μF Conversion capacitor for f-V
A low capacitance increase the size of the ripple of the f-V conversion voltage. A large capacitance is not a problem, but will delay the reaction speed.

C4 : 1.5 μF Capacitor for POLH (detection of the vertical synchronization signal's polarity)
The minimum capacitance is determined as follows:
The internal hysteresis comparator does not react when the duty of minimum frequency synchronization (fV = 40Hz, T = 25ms) is 50%.
CMin. = 16μ × T [F]
A large capacitance is not a probrem, built will deray the reaction speed.

C5 : 1μF Capacitor for EXIH (detection of the vertical synchronization signal's existance)
The minimum capacitance is determined as follows:
The internal hysteresis comparator does not react at the minimum frequency synchronization (fV = 40Hz, T = 25ms)
CMin. = 16μ × T [F]
A large capacitance is not a problem, but will deray the reaction speed.

C6 : 100pF Constant for setting the clamp pulse width

C7 : 0.47μF Coupling capacitor for VSYNC IN
A low capacitance increases the size of the input pin waveform's sag.

R1 : 3.9kΩ A low resistance results in a narrow clamp pulse width. Set no lower than 1kΩ.

R2 : 1MΩ Discharge current setting resistor for CLAMP IN

●Electrical characteristic curves

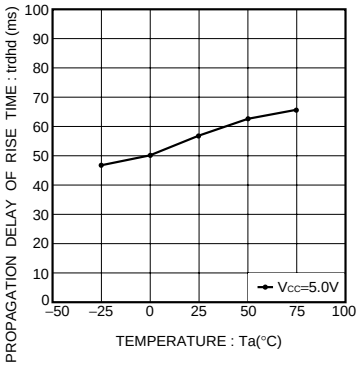


Fig.3 C / HSYNC IN-HDRV
Rising delay time vs.
temperature

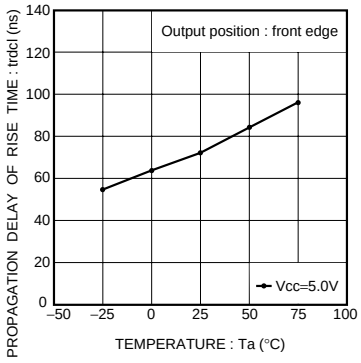


Fig.4 C / HSYNC IN-CLAMP
Rising delay time vs.
temperature

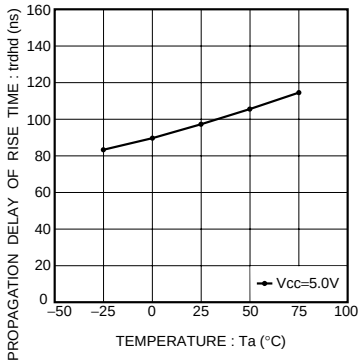


Fig.5 VIDEO IN–HDRV
Rising delay time vs.
temperature

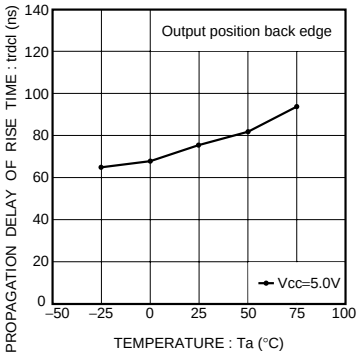


Fig.6 VIDEO IN-CLAMP
Rising delay time vs.
temperature

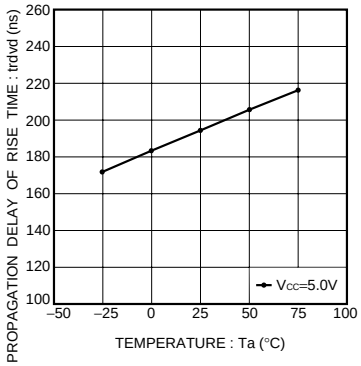


Fig.7 VSYNC IN-VDRV
Rising delay time vs.
temperature

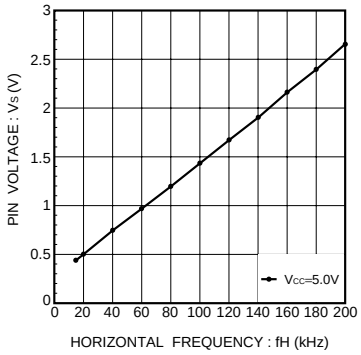
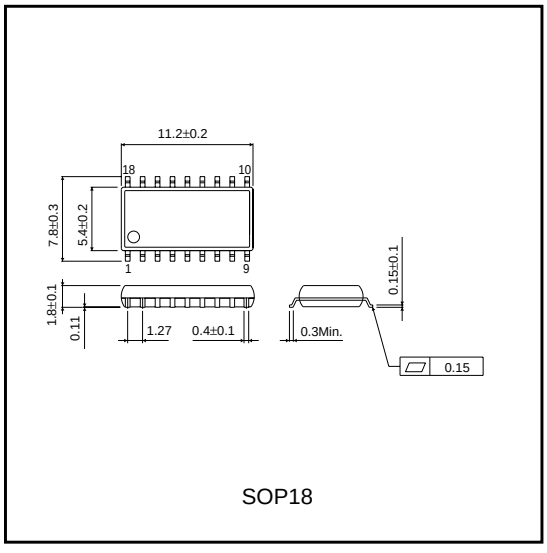


Fig.8 VSEPA horizontal
frequency vs.
pin voltage

●External dimensions (Units : mm)



SOP18