1.5A, Singe Input, Single Cell Switchmode Li-Ion Battery Charger with Power Path Management and I²C Interface

Check for Samples: bq24270, bq24271

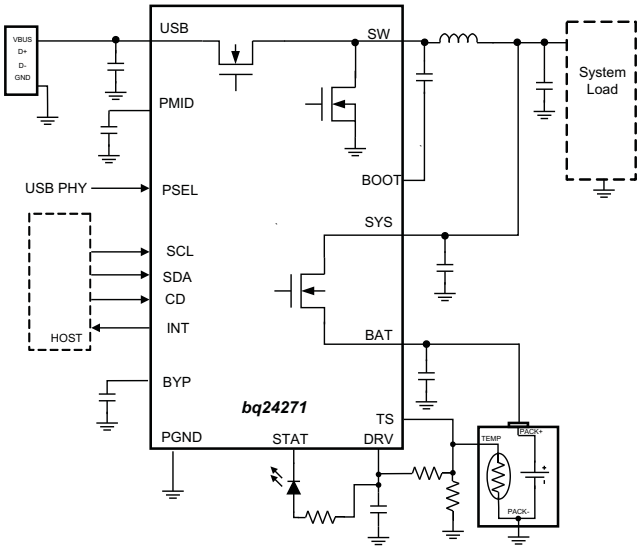
FEATURES

- High-Efficiency Switch Mode Charger with Separate Power Path Control
  - Make a GSM Call with a Deeply Discharged Battery or No Battery
  - Instantly Start up the System from a Deeply Discharged Battery or No Battery
- Highly Integrated Battery N-Channel MOSFET Controller for Power Path Management
  - 20 V input rating, with 6.5 V Overvoltage Protection (OVP)
  - Integrated FETs for Up to 1.5 A Charge Rate
- Safe and Accurate Battery Management Functions
  - 0.5% Battery Regulation Accuracy
  - 10% Charge Current Accuracy
- Charge Parameters Programmed Using I²C ™Interface
  - Charge Voltage, Current, Termination Threshold, Input Current Limit, V_{INDPM} Threshold
- Voltage-based, NTC Monitoring Input
  - JEITA Compatible
- Thermal Regulation Protection for Output Current Control
- BAT Short-Circuit Protection
- Soft-Start Feature to Reduce Inrush Current
- Thermal Shutdown and Protection
- Available in Small 2.8 mm x 2.8 mm 49-ball WCSP or 4 mm x 4 mm QFN-24 Packages

APPLICATIONS

- Handheld Products
- Portable Media Players
- Portable Equipment
- Netbook and Portable Internet Devices

APPLICATION SCHEMATIC



DESCRIPTION

The bq24270 and bq24271 are highly integrated single cell Li-Ion battery charger and system power path management devices targeted for space-limited, portable applications with high capacity batteries. The single cell charger has several input current limits which allow operation from either a USB port or higher power input supply (i.e. AC adapter or wireless charging input) for a versatile solution.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The power path management feature allows the bq24270 and bq24271 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. This allows for proper charge termination and timer operation. The system voltage is regulated to the battery voltage but will not drop below 3.5 V. This minimum system voltage support enables the system to run with a defective or absent battery pack and enables instant system turn-on even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. This enables the use of a smaller adapter. The charge parameters are programmable using the I^2C interface

The battery is charged in three phases: precharge, fast charge constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded. Additionally, a voltage-based battery pack thermistor monitoring input (TS) is included that monitors battery temperature for safe charging The TS function for bq24270 and bq24271 are JEITA compatible.

ORDERING INFORMATION

PART NUMBER(1) (2)	USB OVP	$\overline{CE}$ bit Default	USB Detection	Safety and WD Timers	NTC Monitoring	$V_{BATSHRT}$ or $I_{BATSHRT}$	Package
bq24270YFFR	6.5 V	0 (Charge Enabled)	D+, D-	Yes	JEITA	3 V 50 mA	WCSP
bq24270YFFT	6.5 V	0 (Charge Enabled)	D+, D-	Yes	JEITA	3 V 50 mA	WCSP
bq24270RGER	6.5 V	0 (Charge Enabled)	D+, D-	Yes	JEITA	3 V 50 mA	RGE
bq24270RGET	6.5 V	0 (Charge Enabled)	D+, D-	Yes	JEITA	3 V 50 mA	RGE
bq24271YFFR	6.5 V	0 (Charge Enabled)	PSEL	Yes	JEITA	3 V 50 mA	WCSP
bq24271YFFT	6.5 V	0 (Charge Enabled)	PSEL	Yes	JEITA	3 V 50 mA	WCSP
bq24271RGER	6.5 V	0 (Charge Enabled)	PSEL	Yes	JEITA	3 V 50 mA	RGE
bq24271RGET	6.5 V	0 (Charge Enabled)	PSEL	Yes	JEITA	3 V 50 mA	RGE

(1) The YFF and RGE packages are available in the following options:
R - taped and reeled in quantities of 3,000 devices per reel.
T - taped and reeled in quantities of 250 devices per reel

(2) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage range (with respect to VSS)	USB	–2	20	V
	PMID, BYP, BOOT	–0.3	20	V
	SW	–0.7	12	V
	SDA, SCL, SYS, BAT, STAT, BGATE, DRV, TS, D+, D-, INT, PSEL, CD	–0.3	7	V
BOOT to SW		–0.3	7	V
Output current (continuous)	SW		4.5	A
	SYS		3.5	A
Input current (continuous)	USB		1.75	A
Output sink current	$\overline{STAT}$		10	mA
	INT		1	mA
Operating free-air temperature range		-40	85	°C
Junction temperature, T_J		-40	125	°C
Storage temperature, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		bq24270 and bq24721		UNITS
		YFF (48 PINS)	RGE (24 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	49.8	32.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	30.5	
θ_{JB}	Junction-to-board thermal resistance	1.1	3.3	
ψ_{JT}	Junction-to-top characterization parameter	1.1	0.4	
ψ_{JB}	Junction-to-board characterization parameter	6.6	9.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	2.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

PARAMETER(1)		MIN	MAX	UNITS
V_{USB}	USB voltage range	4.2	18	V
	USB operating range	4.2	6	
I_{USB}	Input current USB input		1.5	A
I_{SYS}	Output Current from SW, DC		3	A
I_{BAT}	Charging		1.5	A
	Discharging, using internal battery FET		2.5	
T_J	Operating junction temperature range	0	125	ºC

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BOOT or SW pins. A tight layout minimizes switching noise.

ELECTRICAL CHARACTERISTICS

Circuit of Figure 3, $V_{(UVLO)} < V_{(USB)} < V_{(OVP)}$ AND $V_{(USB)} > V_{(BAT)}+V_{(SLP)}$, T_J = 0°C–125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(USB)}$	Supply current for control	$V_{(UVLO)} < V_{(USB)} < V_{(OVP)}$ AND $V_{(USB)} > V_{(BAT)}$ + $V_{(SLP)}$ PWM switching			15		mA
		$V_{(UVLO)} < V_{(USB)} < V_{(OVP)}$ AND $V_{(USB)} > V_{(BAT)}+V_{(SLP)}$ PWM NOT switching				5	
		0°C < T_J < 85°C, High-Z Mode				175	µA
$I_{(BAT)}$	Leakage current from BAT to the supply	0°C< T_J < 85°C, $V_{(BAT)}$ = 4.2 V, $V_{(USB)}$ = 0 V				5	µA
	Battery discharge current in High Impedance mode (BAT, SW, SYS)	0°C< T_J < 85°C, $V_{(BAT)}$ = 4.2 V, $V_{(USB)}$ = 5 V or 0 V, SCL, SDA = 0 V or 1.8 V, High-Z Mode				55	µA
POWER PATH MANAGEMENT							
$V_{SYS(REG)}$	System regulation voltage	$V_{(BAT)} < V_{(MINSYS)}$		3.6	3.7	3.82	V
		Battery FET turned off		V_{BATREG} + 1.5%	V_{BATREG} + 3%	V_{BATREG} + 4.17%	
$V_{(MINSYS)}$	Minimum system regulation voltage	$V_{(BAT)} < V_{(MINSYS)}$, Input current limit or $V_{(INDPM)}$ active		3.4	3.5	3.62	V
$V_{(BSUP1)}$	Enter supplement mode threshold	$V_{(BAT)}$ > 2.5 V			V_{BAT} – 30mV		V
$V_{(BSUP2)}$	Exit supplement mode threshold	$V_{(BAT)}$ > 2.5 V			V_{BAT} – 10mV		V
I_{LIM}	Current limit, discharge or supplement mode	Current monitored in internal FET only			7		A
$t_{DGL(SC1)}$	Deglitch time, SYS short circuit during discharge or supplement mode	Measured from ($V_{(BAT)}$ – $V_{(SYS)}$) = 300 mV to BAT = high-impedance			250		µs
$t_{REC(SC1)}$	Recovery time, SYS short circuit during discharge or supplement mode				60		ms
	Battery range for BGATE and supplement mode operation			2.5		4.5	V
BATTERY CHARGER							
$R_{ON(BAT-SYS)}$	Internal battery charger MOSFET on-resistance	Measured from BAT to SYS, $V_{(BAT)}$ = 4.2 V	YFF pkg		37	57	mΩ
			RGE pkg		50	70	
$V_{(BATREG)}$	Charge voltage	Operating in voltage regulation, Programmable Range		3.5		4.44	V
	Voltage regulation accuracy	T_A = 25°C		-0.5%		.5%	
				-1%		1%	
$I_{(CHARGE)}$	Fast charge current range	$V_{(BATHSRT)}$ ≤ $V_{(BAT)}$ < $V_{BAT(REG)}$ programmable range		550		1500	mA
	Fast charge current accuracy	0°C to 125°C		-10%		10%	
$V_{(BATSHRT)}$	Battery short circuit threshold	100 mV hysteresis		2.9	3	3.1	V
$I_{(BATSHRT)}$	Battery short circuit current	$V_{(BAT)} < V_{(BATSHRT)}$			50.0		mA
$t_{DGL(BATSHRT)}$	Deglitch time for battery short to fast charge transition				32		ms
I_{TERM}	Termination charge current	$I_{(TERM)}$ = 50 mA		-35%		35%	
		$I_{(TERM)}$ ≥ 100 mA		-15%		15%	
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2-mV over-drive, t_{RISE}, t_{FALL} = 100 ns			32		ms
$V_{(RCH)}$	Recharge threshold voltage	Below $V_{(BATREG)}$			120		mV
$t_{DGL(RCH)}$	Deglitch time	$V_{(BAT)}$ falling below $V_{(RCH)}$, t_{FALL} = 100 ns			32		ms
$V_{(DETECT)}$	Battery detection voltage	During battery detection source cycle			3.3		V
		During battery detection sink cycle			3		
$I_{(DETECT)}$	Battery detection current before charge done (sink current)	Termination enabled (EN_TERM = 1)			2.5		mA
$t_{(DETECT)}$	Battery detection time	Termination enabled (EN_TERM = 1)			250		ms
V_{IH}	PSEL, CD input high logic level			1.3			V
V_{IL}	PSEL, CD input low logic level					0.4	V

ELECTRICAL CHARACTERISTICS (continued)

Circuit of Figure 3, $V_{(UVLO)} < V_{(USB)} < V_{(OVP)}$ AND $V_{(USB)} > V_{(BAT)}+V_{(SLP)}$, T_J = 0°C–125°C and T_J = 25°C for typical values (unless otherwise noted)

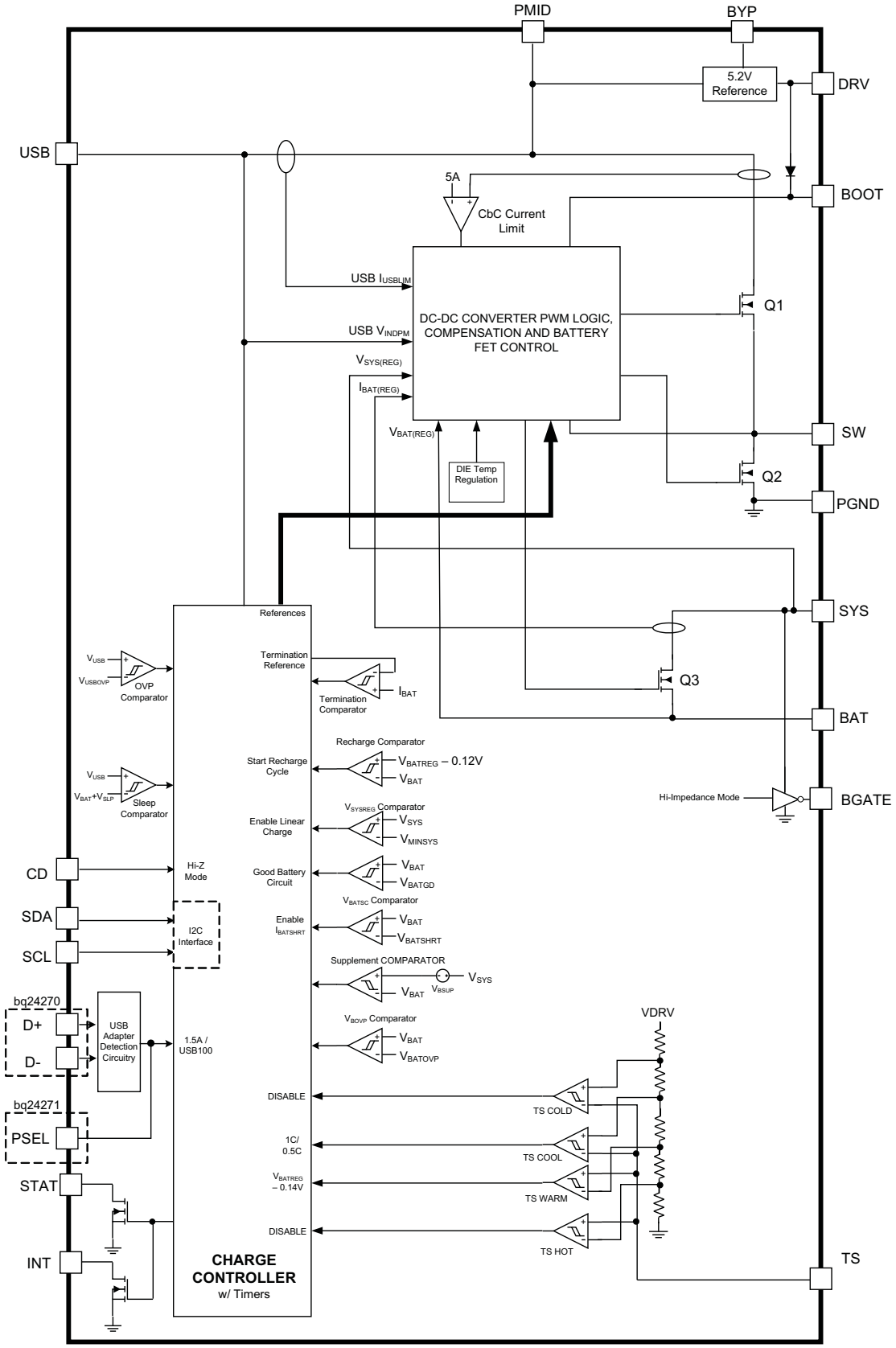
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENT LIMITING							
$I_{(USBLIM)}$	Input current limit threshold (USB input)	USB charge mode, $V_{(USB)}$ = 5 V, DC Current pulled from SW	$I_{(USBLIM)}$ = USB100	90	95	100	mA
			$I_{(USBLIM)}$ = USB500	400	475	500	
			$I_{(USBLIM)}$ = USB150	135	142.5	150	
			$I_{(USBLIM)}$= USB900	800	850	900	
			$I_{(USBLIM)}$ = USB800	700	750	800	
			$I_{(USBLIM)}$= 1.5A	1250	1400	1500	
$V_{(IN\_DPM)}$	Input based DPM threshold range	Charge mode, programmable via I^2C		4.2		4.76	V
	$V_{(IN\_DPM)}$ threshold Accuracy			–2%		2%	
VDRV BIAS REGULATOR							
$V_{(DRV)}$	Internal bias regulator voltage	$V_{(USB)}$ > 5.45 V		5	5.2	5.45	V
$I_{(DRV)}$	DRV Output current			10			mA
$V_{(DO\_DRV)}$	DRV Dropout voltage ($V_{(USB)}$ – $V_{(DRV)}$)	$I_{(USB)}$ = 1A, $V_{(USB)}$ = 5 V, $I_{(DRV)}$ = 10 mA				450	mV
STATUS OUTPUT ($\overline{STAT}$, INT)							
V_{OL}	Low-level output saturation voltage	I_O = 10 mA, sink current				0.4	V
I_{IH}	High-level leakage current	$V_{\overline{CHG}}$ = $V_{\overline{PG}}$ = 5 V				1	mA
PROTECTION							
$V_{(UVLO)}$	IC active threshold voltage	$V_{(USB)}$ rising		3.6	3.8	4	V
$V_{UVLO(HYS)}$	IC active hysteresis	$V_{(USB)}$ falling from above $V_{(UVLO)}$		120	150		mV
$V_{(SLP)}$	Sleep-mode entry threshold, V_{USB}-V_{BAT}	2 V ≤ $V_{(BAT)}$ ≤ $V_{(BATREG)}$, V_{USB} falling		0	40	100	mV
$V_{(SLP\_EXIT)}$	Sleep-mode exit hysteresis	2 V ≤ $V_{(BAT)}$ ≤ $V_{(BATREG)}$		40	100	175	mV
	Deglitch time for supply rising above V_{SLP} + V_{SLP_EXIT}	Rising voltage, 2-mV over drive, t_{RISE} = 100 ns			30		ms
	Bad source detection threshold				V_{IN_DPM} – 80 mV		V
	Deglitch on bad source detection				32		ms
V_{OVP}	Input supply OVP threshold voltage	USB, $V_{(USB)}$ Rising		6.3	6.5	6.7	V
$V_{OVP(HYS)}$	V_{OVP} hysteresis	Supply falling from $V_{(OVP)}$			100		mV
$V_{(BOVP)}$	Battery OVP threshold voltage	$V_{(BAT)}$ threshold over $V_{(OREG)}$ to turn off charger during charge		1.025 × V_{BATREG}	1.05 × V_{BATREG}	1.075 × V_{BATREG}	V
	VB_{OVP} hysteresis	Lower limit for $V_{(BAT)}$ falling from above $V_{(BOVP)}$			1		% of V_{BATREG}
$V_{BAT(UVLO)}$	Battery UVLO threshold voltage	$V_{(BAT)}$ rising, 100 mV hysteresis			2.5		V
I_{LIMIT}	Cycle by Cycle current limit	$V_{(SYS)}$ shorted		4.1	4.9	5.6	A
$T_{SHUTDWN}$	Thermal trip				165		°C
	Thermal hysteresis				10		°C
T_{REG}	Thermal regulation threshold	Charge current begins to cut off			120		°C
	Safety timer accuracy			–20%		20%	
PWM							
	Internal top reverse blocking MOSFET on-resistance	$I_{(IN\_LIMIT)}$ = 500 mA, Measured from $V_{(USB)}$ to PMIDU			95	175	mΩ
	Internal top N-channel Switching MOSFET on-resistance	Measured from PMIDU to SW			100	175	mΩ
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND			65	115	mΩ
f_{OSC}	Oscillator frequency			1.35	1.50	1.65	MHz
D_{MAX}	Maximum duty cycle				95%		
D_{MIN}	Minimum duty cycle			0%			

ELECTRICAL CHARACTERISTICS (continued)

Circuit of Figure 3, $V_{(UVLO)} < V_{(USB)} < V_{(OVP)}$ AND $V_{(USB)} > V_{(BAT)}+V_{(SLP)}$, T_J = 0°C–125°C and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY-PACK NTC MONITOR						
V_{HOT}	High temperature threshold	$V_{(TS)}$ falling	29.7	30	30.5	$\%V_{DRV}$
$V_{HOT(HYS)}$	Hysteresis on high threshold	$V_{(TS)}$ rising		1		
V_{WARM}	High temperature threshold	$V_{(TS)}$ falling	37.9	38.3	39.6	$\%V_{DRV}$
$V_{WARM(HYS)}$	Hysteresis on high threshold	$V_{(TS)}$ rising		1		
V_{COOL}	Low temperature threshold	$V_{(TS)}$ rising	56	56.5	56.9	$\%V_{DRV}$
$V_{COOL(HYS)}$	Hysteresis on low threshold	$V_{(TS)}$ falling		1		
V_{COLD}	Low temperature threshold	$V_{(TS)}$ rising	59.5	60	60.4	$\%V_{DRV}$
$V_{COLD(HYS)}$	Hysteresis on low threshold	$V_{(TS)}$ falling		1		
TS_{OFF}	TS Disable threshold	$V_{(TS)}$ rising, 2% $V_{(DRV)}$ Hysteresis	70		73	$\%V_{DRV}$
$t_{DGL(TS)}$	Deglitch time on TS change			50		ms
D+/D- Detection (bq24270)						
V_{D+_SRC}	D+ Voltage Source		0.5	0.6	0.7	V
I_{D+_SRC}	D+ Connection Check Current Source		7		14	µA
I_{D-_SINK}	D- Current Sink		50	100	150	µA
I_{D_LKG}	Leakage Current into D+/D-	D-, switch open	–1		1	µA
		D+, switch open	–1		1	µA
V_{D+_LOW}	D+ Low Comparator Threshold		0.8			V
V_{D-_LOW}	D- Low Comparator Threshold		250		400	mV
R_{D-_DWN}	D- Pulldown for Connection Check		14.25		24.8	kΩ
BATGD Operation						
V_{BATGD}	Good Battery threshold		3.6	3.8	3.9	V
	Deglitch for good battery threshold	$V_{(BAT)}$ rising to HIGH-Z mode, DEFAULT Mode Only		32		ms
I^2C Compatible Interface						
V_{IH}	Input high threshold level	$V_{(PULL-UP)}$ = 1.8 V, SDA and SCL	1.3			V
V_{IL}	Input low threshold level	$V_{(PULL-UP)}$ = 1.8 V, SDA and SCL			0.4	V
V_{OL}	Output low threshold level	I_L = 10 mA, sink current			0.4	V
I_{BIAS}	High-Level leakage current	$V_{(PULL-UP)}$ = 1.8 V, SDA and SCL			1	µA
$t_{WATCHDOG}$	Watchdog Timer timeout		30			s

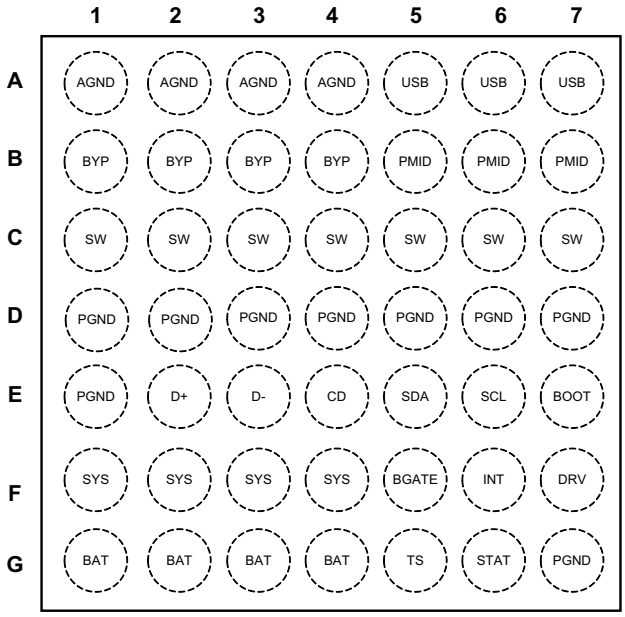
BLOCK DIAGRAM



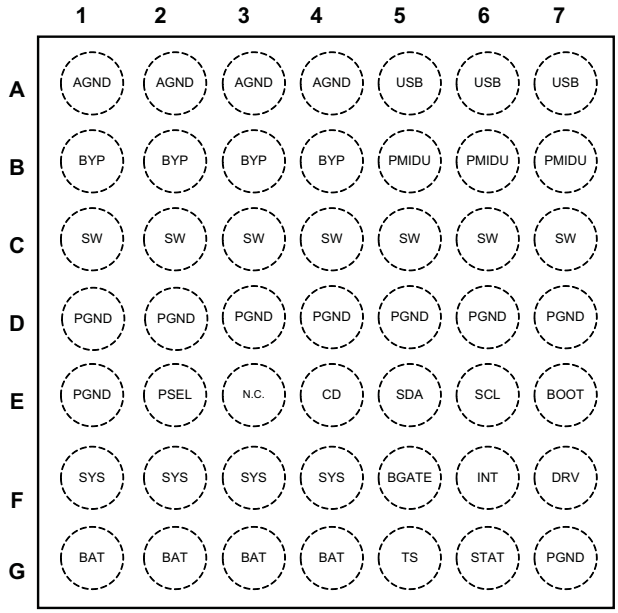
PIN CONFIGURATION

49-Ball 2.78 mm x 2.78 mm WCSP

bq24270 (Top View)

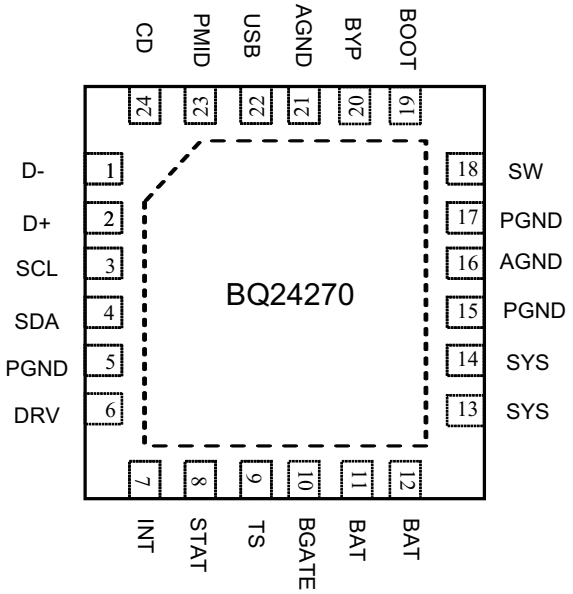


bq24271 (Top View)

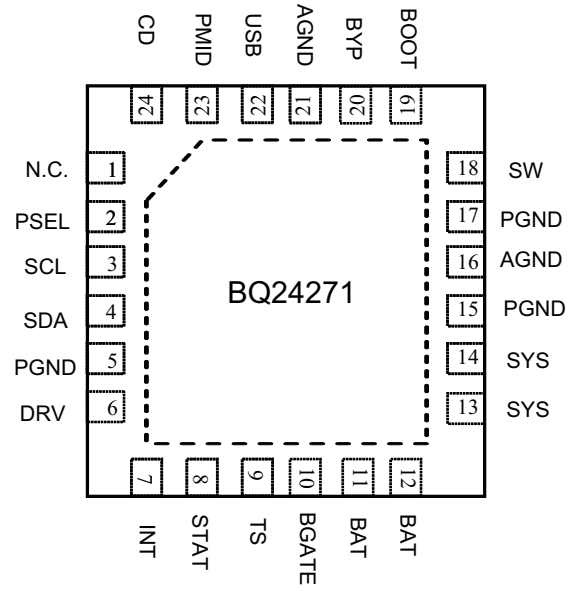


24-Pin RGE

bq24270 (Top View)



bq24271 (Top View)



PIN FUNCTIONS

PIN NAME	PIN NO. bq24270		PIN NO. bq24271		I/O	DESCRIPTION
	YFF	RGE	YFF	RGE		
AGND	A1-A4	16, 21	A1-A4	16, 21	I	Ground terminal. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
USB	A5-A7	22	A5-A7	22	I	USB Input Power Supply. USB is connected to the external DC supply (AC adapter or USB port). Bypass USB to PGND with at least a 1 µF ceramic capacitor.
BYP	B1-B4	20	B1-B4	20	O	Bypass for internal supply. Bypass BYP to GND with at least a 0.1 µF ceramic capacitor.
PMID	B5-B7	23	B5-B7	23	O	Reverse Blocking MOSFET and High Side MOSFET Connection Point for USB Input. Bypass PMID to GND with at least a 4.7µF ceramic capacitor. Use caution when connecting an external load to PMID. The PMID output is not current limited. Any short on PMID will result in damage to the IC.
SW	C1-C7	18	C1-C7	18	O	Inductor Connection. Connect to the switched side of the external inductor.
PGND	D1-D7, E1, G7	5, 15, 17	D1-D7, E1, G7	5, 15, 17	–	Ground terminal. Connect to the thermal pad (for QFN only) and the ground plane of the circuit.
D+	E2	2	–	–	I	D+ and D- Connections for USB Input Adapter Detection. When a charge cycle is initiated by the USB input, and a short is detected between D+ and D-, the USB input current limit is set to 1.5 A. If a short is not detected, the USB100 mode is selected.
D-	E3	1	–	–	I	
CD	E4	24	E4	24	I	IC Hardware Disable Input. Drive CD high to place the bq24270 and bq24271 in high-z mode. Drive CD low for normal operation.
SDA	E5	4	E5	4	I/O	I2C Interface Data. Connect SDA to the logic rail through a 10 kΩ resistor.
SCL	E6	3	E6	3	I	I2C Interface Clock. Connect SCL to the logic rail through a 10 kΩ resistor.
BOOT	E7	19	E7	19	I	High Side MOSFET Gate Driver Supply. Connect a 0.01 µF ceramic capacitor (voltage rating > 10 V) from BOOT to SW to supply the gate drive for the high side MOSFETs.
PSEL	–	–	E2	2	I	USB Source Detection Input. Drive PSEL high to indicate a USB source is connected to the USB input. When PSEL is high, the IC starts up with a 100mA input current limit for USB. Drive PSEL low to indicate that an AC Adapter is connected to the USB input. When PSEL is low, the IC starts up with a 1.5 A input current limit for USB.
SYS	F1-F4	13, 14	F1-F4	13,14	I/O	System Voltage Sense and Charger FET Connection. Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with 10 µF.
BGATE	F5	10	F5	10	O	External Discharge MOSFET Gate Connection. BGATE drives an external P-Channel MOSFET to provide a very low resistance discharge path. Connect BGATE to the gate of the external MOSFET. BGATE is low in high impedance mode and when no input is connected.
INT	F6	7	F6	7	O	Status Output. INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 128 µs pulse is sent out as an interrupt for the host. INT is enabled /disabled using the EN_STAT bit in the control register. Connect INT to a logic rail through a 100 kΩ resistor to communicate with the host processor.
DRV	F7	6	F7	6	O	Gate Drive Supply. DRV is the bias supply for the gate drive of the internal MOSFETs. Bypass DRV to PGND with a 1 µF ceramic capacitor. DRV may be used to drive external loads up to 10 mA. DRV is active whenever the input is connected and $V_{USB} > V_{UVLO}$ and $V_{USB} > (V_{BAT} + V_{SLP})$
BAT	G1-G4	11, 12	G1-G4	11, 12	I/O	Battery Connection. Connect to the positive terminal of the battery. Additionally, bypass BAT to GND with a 1µF capacitor.
TS	G5	9	G5	9	I	Battery Pack NTC Monitor. Connect TS to the center tap of a resistor divider from DRV to GND. The NTC is connected from TS to GND. The TS function provides 4 thresholds for JEITA compatibility. TS faults are reported by the I2C interface. See the NTC Monitor section for more details on operation and selecting the resistor values.

PIN FUNCTIONS (continued)

PIN NAME	PIN NO. bq24270		PIN NO. bq24271		I/O	DESCRIPTION
	YFF	RGE	YFF	RGE		
STAT	G6	8	G6	8	O	Status Output. STAT is an open-drain output that signals charging status and fault interrupts. STAT pulls low during charging. STAT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 128 µs pulse is sent out as an interrupt for the host. STAT is enabled /disabled using the EN_STAT bit in the control register. Connect STAT to a logic rail using an LED for visual indication or through a 10 kΩ resistor to communicate with the host processor.
Thermal PAD	—	Pad	—	Pad	-	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device.

TYPICAL APPLICATION CIRCUIT

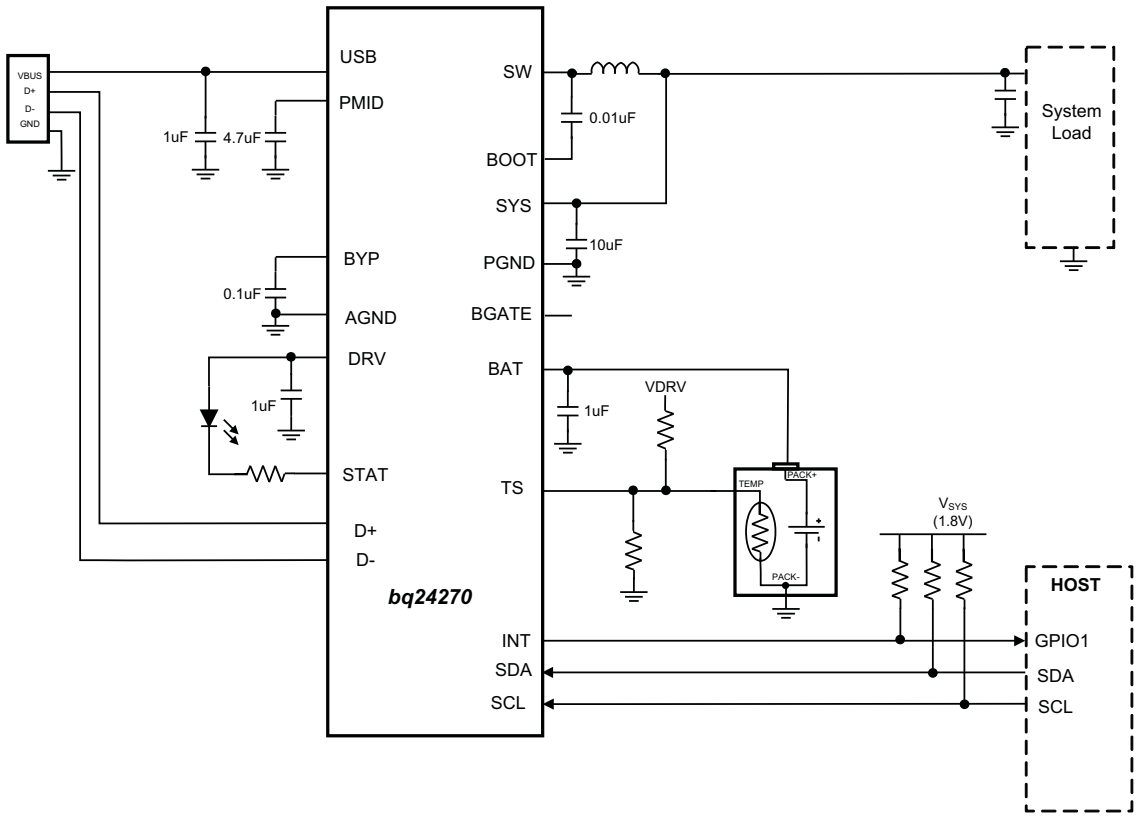


Figure 1. Typical Application Circuit– bq24270, Shown with No External Discharge FET

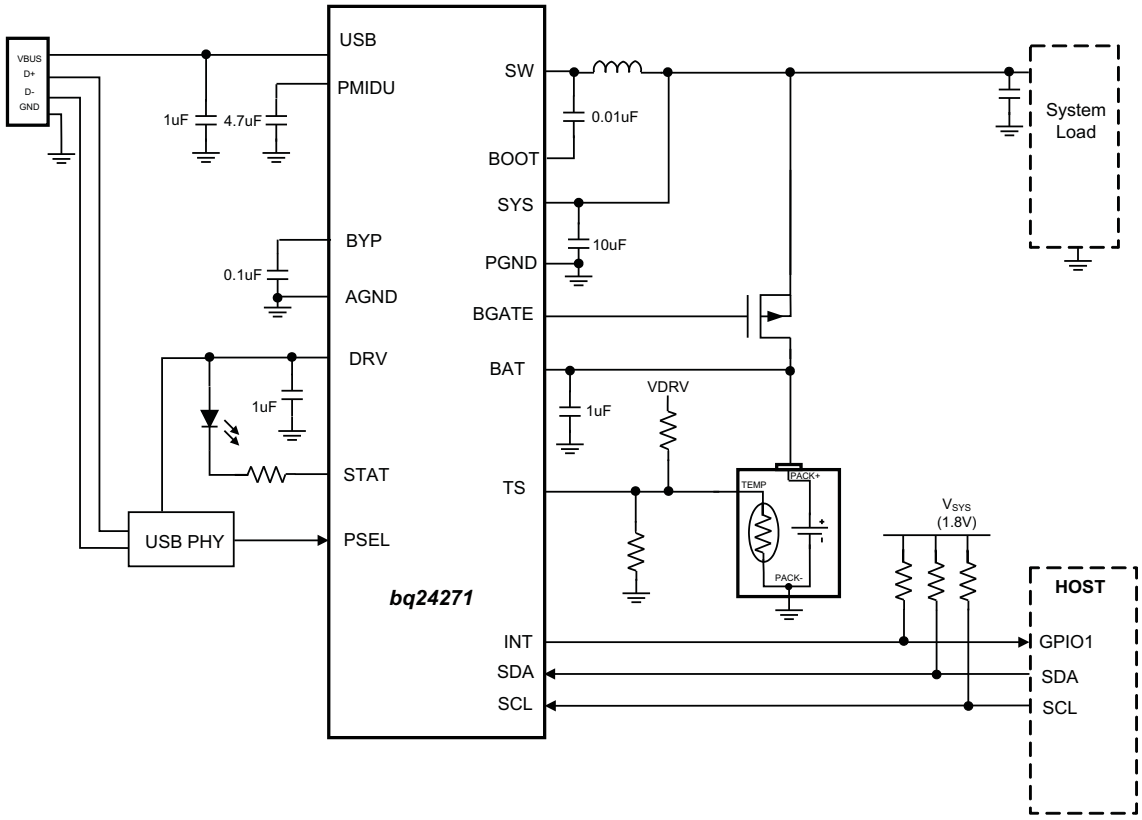


Figure 2. Typical Application Circuit – bq24271, Shown with External Discharge FET

DETAILED DESCRIPTION

The bq24270 and bq24271 are highly integrated single cell Li-Ion battery chargers and system power path management devices targeted for space-limited, portable applications with high capacity batteries. The single-input, single cell charger operates from either a USB port or alternate power source (i.e. wall adapter or wireless power input) for a versatile solution.

The power path management feature allows the bq24270 and bq24271 to power the system from a high efficiency DC to DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. This allows for proper charge termination and enables the system to run with a defective or absent battery pack. Additionally, this enables instant system turn-on even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. This enables the use of a smaller adapter. The charge parameters are programmable using the I^2C interface.

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded.

Charge Mode Operation

Charge Profile

The internal battery MOSFET is used to charge the battery. When the battery is above the MINSYS voltage, the internal FET is on to maximize efficiency and the PWM converter regulates the charge current into the battery. When battery is less than MINSYS, the SYS is regulated to $V_{SYS(REG)}$ and battery is charged using the battery FET to regulate the charge current. There are 5 loops that influence the charge current:

- Constant current loop (CC)
- Constant voltage loop (CV)
- Thermal-regulation loop
- Minimum system-voltage loop (MINSYS)
- Input-voltage dynamic power-management loop ($V_{(IN-DPM)}$)

During the charging process, all five loops are enabled and the one that is dominant takes control. The bq24270 supports a precision Li-Ion or Li-Polymer charging system for single-cell applications. The Dynamic Power Path Management (DPPM) feature regulates the system voltage to a minimum of V_{MINSYS}, so that startup is enabled even for a missing or deeply discharged battery. Figure 3shows a typical charge profile including the minimum system output voltage feature.

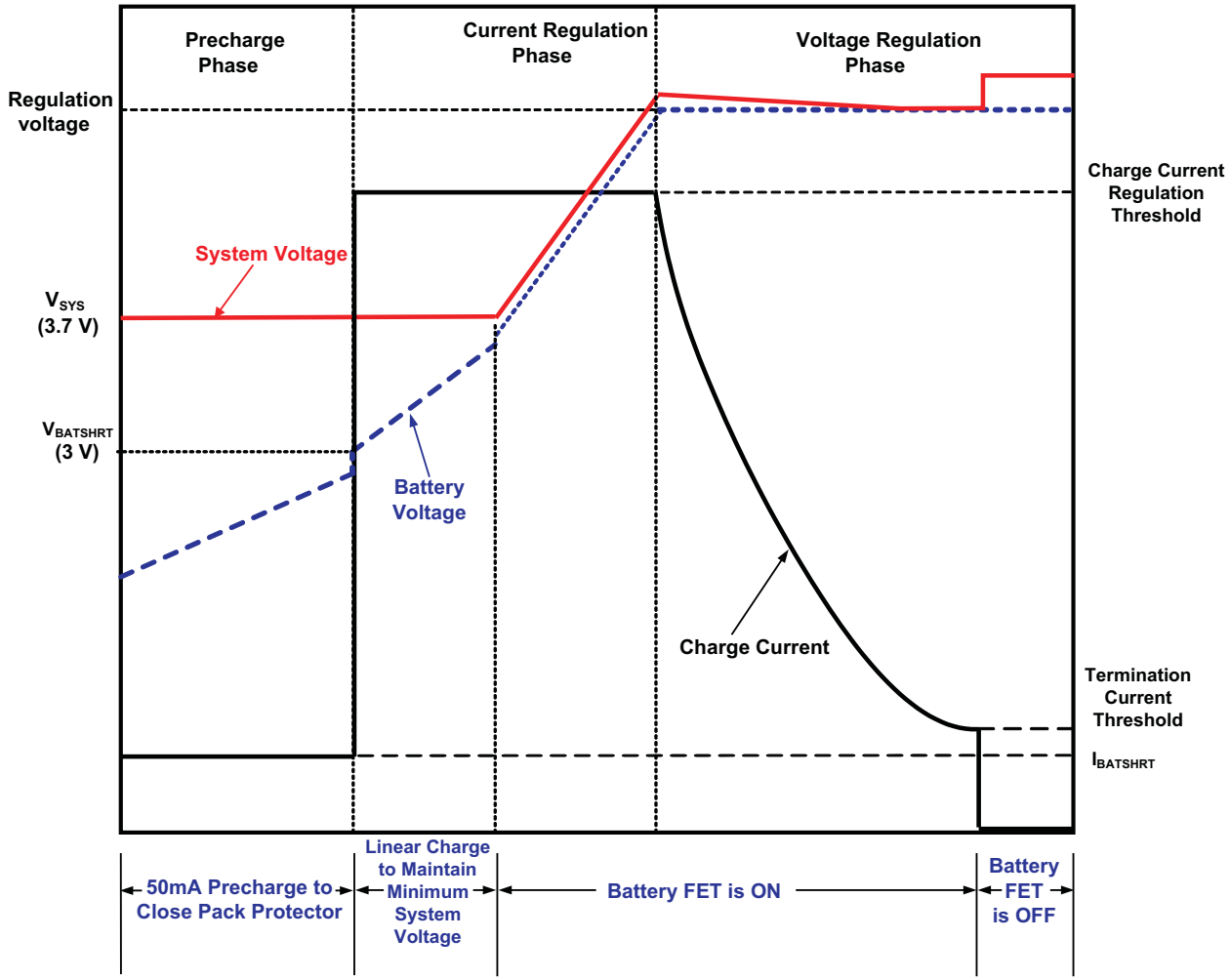


Figure 3. Typical Charging Profile of bq24270 and bq24271

PWM Controller in Charge Mode

The bq24270 and bq24271 provide an integrated, fixed-frequency 1.5 MHz voltage-mode controller to power the system and supply the charge current. The voltage loop is internally compensated and provides enough phase margin for stable operation, allowing the use of small ceramic capacitors with low ESR. The input scheme for the devices prevents battery discharge when the supply voltages are lower than V_{BAT}. The high-side N-MOSFET (Q1) switches to control the power delivered to the output. The DRV LDO provides a supply for the gate drive for the low side MOSFET, while a bootstrap circuit (BST) with an external bootstrap capacitor is used to boost up the gate drive voltage for Q1.

The input is protected by a cycle-by-cycle current limit that is sensed through the internal sense MOSFETs for Q1. The threshold for the current limit is set to a nominal 5-A peak current. The input also uses an input current limit that limits the current from the power source

Battery Charging Process

When the battery is deeply discharged or shorted ($V_{(BAT)} < V_{(BATSHRT)}$) the bq24270 and bq24271 apply $I_{BATSHRT}$ to close the pack protector switch and bring the battery voltage up to acceptable charging levels. During this time, the battery FET is linearly regulated and the system output is regulated to $V_{SYS(REG)}$. Once the battery rises above $V_{(BATSHRT)}$, the charge current is regulated to the value set in the I^2C register. The battery FET is linearly regulated to maintain the system voltage at $V_{SYS(REG)}$. Under normal conditions, the time spent in this region is a short percentage of the total charging time, so the linear regulation of the charge current does not affect the

overall charging efficiency for long. If the die temperature does heat up, the thermal regulation circuit reduces the charge current to maintain a die temperature less than 125°C. If the current limit for the SYS output is reached (limited by the input current limit, or $V_{(IN\_DPM)}$), the SYS output drops to the $V_{(MINSYS)}$ output voltage. When this happens, the current is reduced to provide the system with all the current that is needed while maintaining the minimum system voltage. If the charge current is reduced to 0 mA, pulling further current from SYS causes the output to fall to the battery voltage and enter supplement mode (see the Dynamic Power Path Management section for more details

Once the battery is charged enough to where the system voltage begins to rise above $V_{SYS(REG)}$ (approximately 3.5 V), the battery FET is turned on fully and the battery is charged with the full programmed charge current set by the I^2C interface, $I_{(CHARGE)}$. The slew rate for fast charge current is controlled to minimize the current and voltage over-shoot during transient. The charge current is regulated to $I_{(CHARGE)}$ until the battery is charged to the regulation voltage. Once the battery voltage is close to the regulation voltage, $V_{(BATREG)}$, the charge current is tapered down as shown in Figure 3 while the SYS output remains connected to the battery. The voltage regulation feedback occurs by monitoring the battery-pack voltage between the BAT and PGND pins. The $V_{(BATREG)}$ is targeted for single-cell voltage batteries and has an adjustable regulation voltage (3.5 V to 4.44 V) programmed using the I^2C interface

The devices monitor the charging current during the voltage regulation phase. Once the termination threshold, $I_{(TERM)}$, is detected and the battery voltage is above the recharge threshold, the devices terminate charge and turn off the battery charging FET and enters battery detection. If a battery is detection (See the Battery Detection section), the devices enter charge done. The system output is regulated to the $V_{SYS(REG)}$ and supports the full current available from the input and the battery supplement mode is available (see the Dynamic Power Path Management section for more details). The termination current level is programmable. To disable the charge current termination, the host sets the charge termination bit (TE) of charge control register to 0, see the to I^2C section for details.

1. The battery voltage falls below the $V_{(BATREG)}$- $V_{(RCH)}$ threshold.
2. $V_{(USB)}$ toggle
3. $\overline{CE}$ bit toggle or RESET bit is set
4. Hi-Z bit toggle

Battery Detection

When termination conditions are met, a battery detection cycle is started. During battery detection, $I_{(DETECT)}$ is pulled from $V_{(BAT)}$ for $t_{(DETECT)}$ to verify there is a battery. If the battery voltage remains above $V_{(DETECT)}$ for the full duration of $t_{(DETECT)}$, a battery is determined to present and the IC enters “Charge Done”. If $V_{(BAT)}$ falls below $V_{(DETECT)}$, a “Battery Not Present” fault is signaled and battery detection continues. The next cycle of battery detection, the bq24270 and bq24271 turn on $I_{(BATSHRT)}$ for $t_{(DETECT)}$. If $V_{(BAT)}$ rises to $V_{(DETECT)}$, the current source is turned off and after $t_{(DETECT)}$, the battery detection continues through another current sink cycle. Battery detection continues until charge is disabled or a battery is detected. Once a battery is detected, the fault status clears and a new charge cycle begins. Battery detection is not run when termination is disabled.

Dynamic Power Path Management

The bq24270 and bq24271 feature a SYS output that powers the external system load connected to the battery. This output is active whenever a source is connected to USB or BAT. The following sections discuss the behavior of SYS with a source connected to the supply or a battery source only.

Input Source Connected

When a valid input source is connected, the buck converter turns on to power the load on SYS. The STAT/INT show an interrupt with 128 µs pulse to tell the host that something has changed. The FAULT bits read normal, and the Supply Status register shows that a new supply is connected. The $\overline{CE}$ bit (bit 1) in the control register (0x02) determines whether a charge cycle is initiated. By default, the bq24270 and bq24271 ($\overline{CE}$ = 0) enable a charge cycle when a valid input source is connected. When the $\overline{CE}$ bit is 1 and a valid input source is connected, the battery FET is turned off and the SYS output is regulated to the $V_{SYS(REG)}$ programmed by the $V_{(BATREG)}$ threshold in the I^2C register. A charge cycle is initiated when the $\overline{CE}$ bit is written to a 0.

When the $\overline{CE}$ bit is a 0 and a valid source is connected to USB, the buck converter starts up and a charge cycle is initiated. When $V_{(BAT)}$ is high enough that $V_{(SYS)}$ is > $V_{SYS(REG)}$, the battery FET is turned on and the SYS output is connected to BAT. If the SYS voltage falls to $V_{SYS(REG)}$, it is regulated to that point to maintain the system output even with a deeply discharged or absent battery. In this mode, the SYS output voltage is regulated by the buck converter and the battery FET linearly regulates the charge current into the battery. The current from the supply is shared between charging the battery and powering the system load at SYS. The dynamic power path management (DPPM) circuitry of the devices monitor the current limits continuously and if the SYS voltage falls to the $V_{(MINSYS)}$ voltage, it adjusts charge current to maintain the minimum system voltage and supply the load on SYS. If the charge current is reduced to zero and the load increases further, the devices enter battery supplement mode. During supplement mode, the battery FET is turned on and the battery supplements the system load.

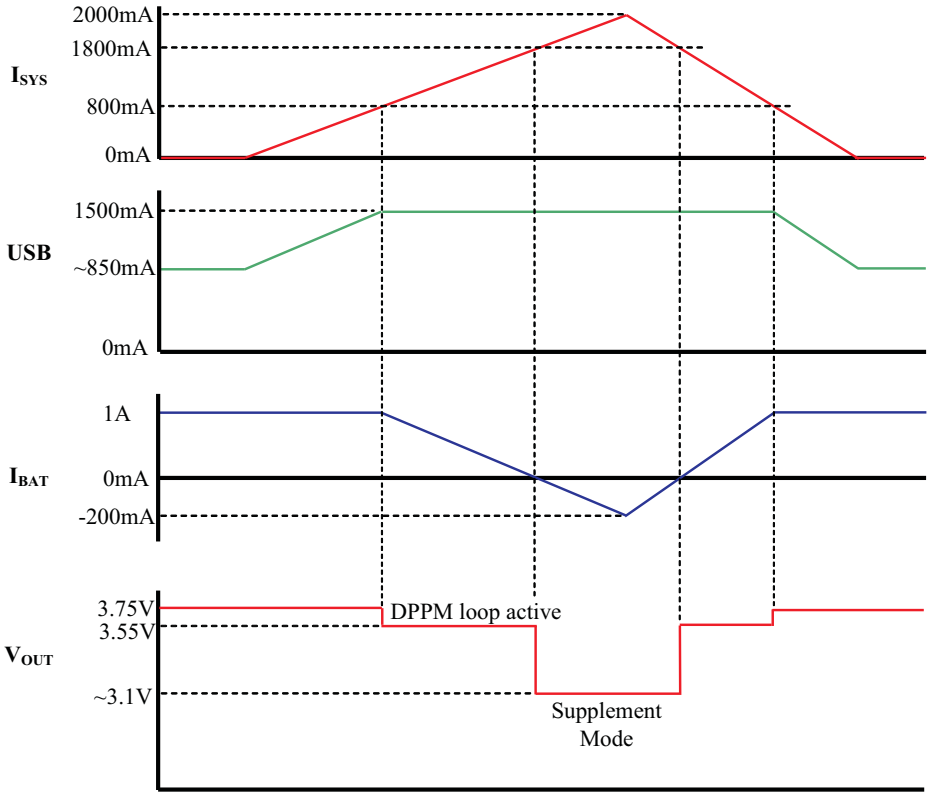


Figure 4. Example DPPM Response ($V_{(Supply)}$ = 5 V, $V_{(BAT)}$ = 3.1 V, 1.5 A Input Current Limit)

$V_{BAT(REG)}$ should never be programmed less than $V_{(BAT)}$. If the battery is ever 5% above the regulation threshold, the battery OVP circuit shuts the PWM converter off and the battery FET is turned on to discharge the battery to safe operating levels. Battery OVP errors are shown in the I^2C status registers.

Battery Only Connected

When a battery voltage > $V_{(BATUVLO)}$ is connected with no input source, the battery FET is turned on similar to supplement mode. In this mode, the current is not regulated; however, there is a short circuit current limit. If the short circuit limit is reached, the battery FET is turned off for the deglitch time. After the deglitch time, the battery FET is turned on to test and determine if the short has been removed. If it has not, the FET turns off and the process repeats until the short is removed. This process is to protect the internal FET from over current. If an external FET is used for discharge, the body diode prevents the load on SYS from being disconnected from the battery. If the battery voltage is less than $V_{(BATUVLO)}$, the battery FET (Q3) remains off and BAT is high-impedance. This prevents further discharging deeply discharged batteries.

Battery Discharge FET (BGATE)

The bq24270 and bq24271 contain a MOSFET driver to drive an external discharge FET between the battery and the system output. This external FET provides a low impedance path when supplying the system from the battery. Connect BGATE to the gate of the external discharge MOSFET. BGATE is on under the following conditions:

1. No valid input supply connected.
2. 2. HZ_MODE = 1

DEFAULT Mode

DEFAULT mode is used when I^2C communication is not available. DEFAULT mode is entered in the following situations:

1. When the charger is enabled and $V_{(BAT)}$ < 3.6 V before I^2C communication is established.
2. When the watchdog timer expires without a reset from the I^2C interface and the safety timer has not expired.
3. When the devices comes out of any fault condition (sleep mode, OVP, faulty adapter mode, etc.) before I^2C communication is established.

In default mode, the I^2C registers are reset to the default values. The 27 min safety timer is reset and starts when DEFAULT mode is entered. The default value for $V_{(BATREG)}$ is 3.6V, and the default value for $I_{(CHARGE)}$ is 1 A. The input current limit for the USB input is determined by the D+ and D- detection (bq24270) or PSEL (bq24271). Default mode is exited by programming the I^2C interface. Once I^2C communication is established, PSEL has no effect on the USB input. Note that if termination is enabled and charging has terminated, a new charge cycle is NOT initiated when entering DEFAULT mode.

Safety Timer and Watchdog Timer

At the beginning of charging process, the bq24270 and bq24271 start the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, charging is halted and the $\overline{CE}$ bit is written to a “1”. The length of the safety timer is selectable using the I^2C interface. A single 128 µs pulse is sent on the STAT and INT outputs and the STATx bits of the status registers are updated in the I^2C. The $\overline{CE}$ bit must be toggled in order to clear the safety timer fault. The safety timer duration is selectable using the TMR_X bits in the Safety Timer Register/ NTC Monitor register. Changing the safety timer duration resets the safety timer. If the safety timer expires, charging is disabled ($\overline{CE}$ changed to a “1”). This function prevents continuous charging of a defective battery if the host fails to reset the safety timer.

In addition to the safety timer, the devices contain a watchdog timer that monitors the host through the I^2C interface. Once a read/write is performed on the I^2C interface, a 30-second timer ($t_{WATCHDOG}$) is started. The 30-second timer is reset by the host using the I^2C interface. This is done by writing a “1” to the reset bit (TMR_RST) in the control register. The TMR_RST bit is automatically set to “0” when the 30-second timer is reset. This process continues until battery is fully charged or the safety timer expires. If the 30-second timer expires, the IC enters DEFAULT mode where the default register values are loaded, the safety timer restarts at 27 minutes and charging continues. The I^2C may be accessed again to reinitialize the desired values and restart the watchdog timer as long as the 27 minute safety timer has not expired. The watchdog timer flow chart is shown in Figure 5.

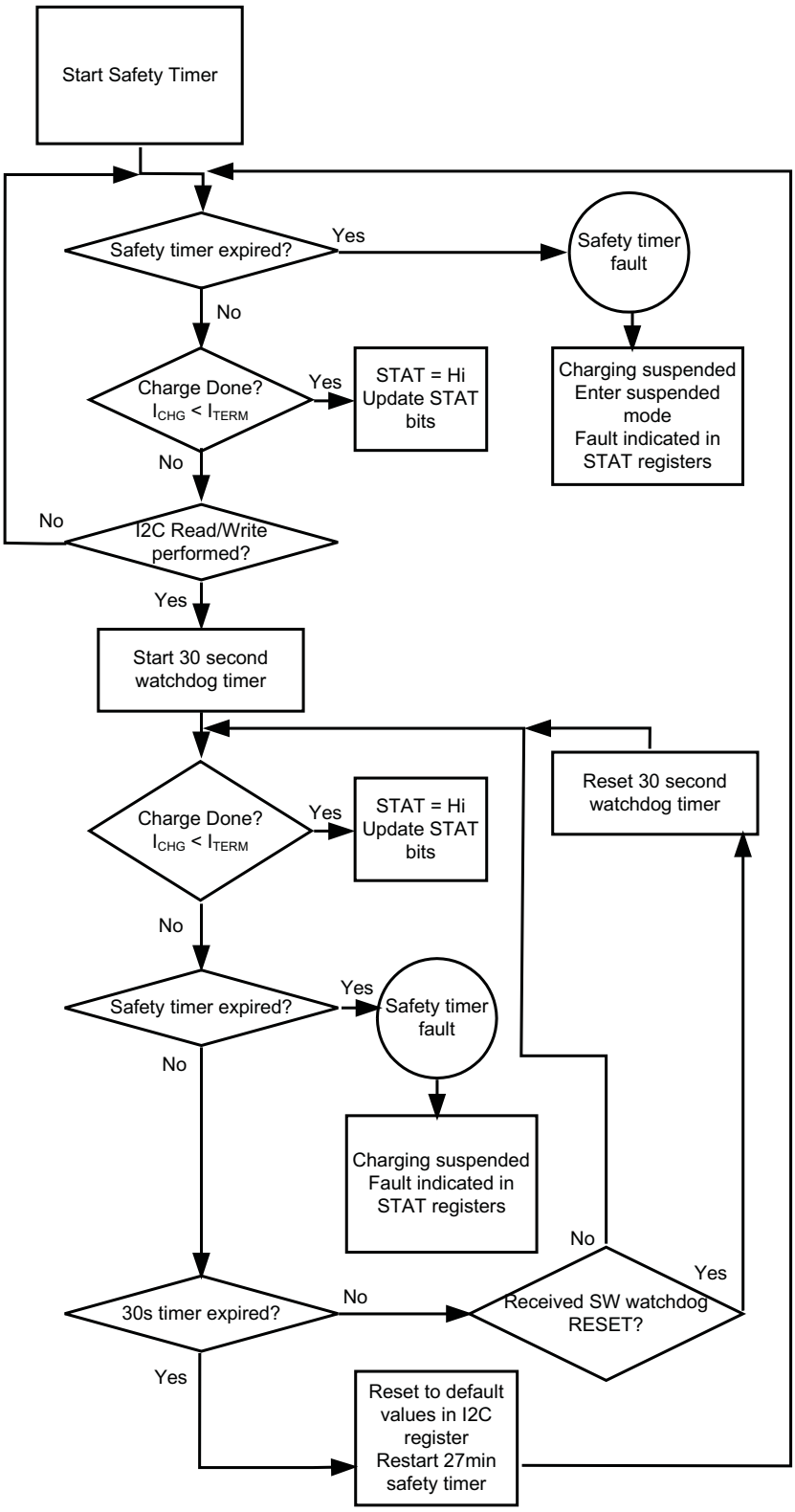


Figure 5. The Watchdog Timer Flow Chart for bq24270 and bq24271

D+ and D- Based Adapter Detection for the USB Input (D+ and D-, bq24270)

The bq24270 contains a D+ and D– based adapter detection circuit that is used to program the input current limit for the USB input during DEFAULT mode. D+ and D– detection is only performed in DEFAULT mode unless forced by the D+ and D– EN bit in host mode.

By default the USB input current limit is set to 100 mA. When USB is asserted the bq24270 performs a charger source identification to determine if it is connected to an SDP (USB port) or CDP and DCP (dedicated charger). When the detection is initiated, the first step is the connection detection as described in BC1.2. This step detects when the D+ and D- lines are connected to the bq24270. Once this connection is made, the circuit moves to the Primary Detection. If the connection detection has not completed within 500 ms, the D+ and D- detection selects 100 mA for the unknown input source. The primary detection complies with the method described in BC1.2. During primary detection, the D+ and D- lines are tested to determine if the port is an SDP or CDP and DCP. If a CDP and DCP is detected the input current limit is increased to 1.5 A, if an SDP is detected the current limit remains at 100 mA, until changed via the I^2C interface. Secondary detection is not performed.

Automatic detection is performed only if $V_{(D+)}$ and $V_{(D–)}$ are less than 0.6 V to avoid interfering with the USB transceiver which may also perform D+ and D- detection when the system is running normally. However, D+ and D– can be initiated at any time by the host by setting the D+ and D– EN bit in the Control/Battery Voltage Register to 1. After detection is complete the D+ and D– EN bit is automatically reset to 0 and the detection circuitry is disconnected from the D+ and D- pins to avoid interference with USB data transfer. When a command is written to change the input current limit in the I^2C, this overrides the current limit selected by D+/D- detection.

USB Input Current Limit Selector Input (PSEL, bq24271)

The bq24271 contains a PSEL input that is used to program the input current limit for USB during DEFAULT mode. Drive PSEL high to indicate a USB source is connected to the USB input and program the 500 mA current limit for USB. Drive PSEL low to indicate that an AC Adapter is connected to the)USB input. When PSEL is low, the IC starts up with a 1.5 A current limit for USB. Once an I^2C write is done, PSEL has no effect on the input current limit until the watchdog timer expires.

Hardware Chip Disable Input (CD)

The bq24270 and bq24271 contain a CD input that is used to disable the IC and place the devices into high-impedance mode. Drive CD low to enable charge and enter normal operation. Drive CD high to disable charge and place the devices into high-impedance mode. Driving CD resets the safety timer.

LDO Output (DRV)

The bq24270 and bq24271 contain a linear regulator (DRV) that is used to supply the internal MOSFET drivers and other circuitry. Additionally, DRV supplies up to 10mA external loads to power the STAT LED or the USB transceiver circuitry. The maximum value of the DRV output is 5.45 V so it ideal for protecting voltage sensitive USB circuits from high voltage fluctuations in the supply. The LDO is on whenever a supply is connected to the USB input of the bq24270 and bq24271. The DRV is disabled under the following conditions:

1. $V_{(USB)} < UVLO$
2. $V_{(USB)} < V_{SLP}$
3. Thermal Shutdown
4. OTG_LOCK bit set to '1'

External NTC Monitoring (TS)

The I^2C interface allows the user to implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. Additionally, the bq24270 and bq24271 provide a flexible, voltage based TS input for monitoring the battery pack NTC thermistor. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. The devices enable the user to implement the JEITA. The JEITA specification is shown in Figure 6.

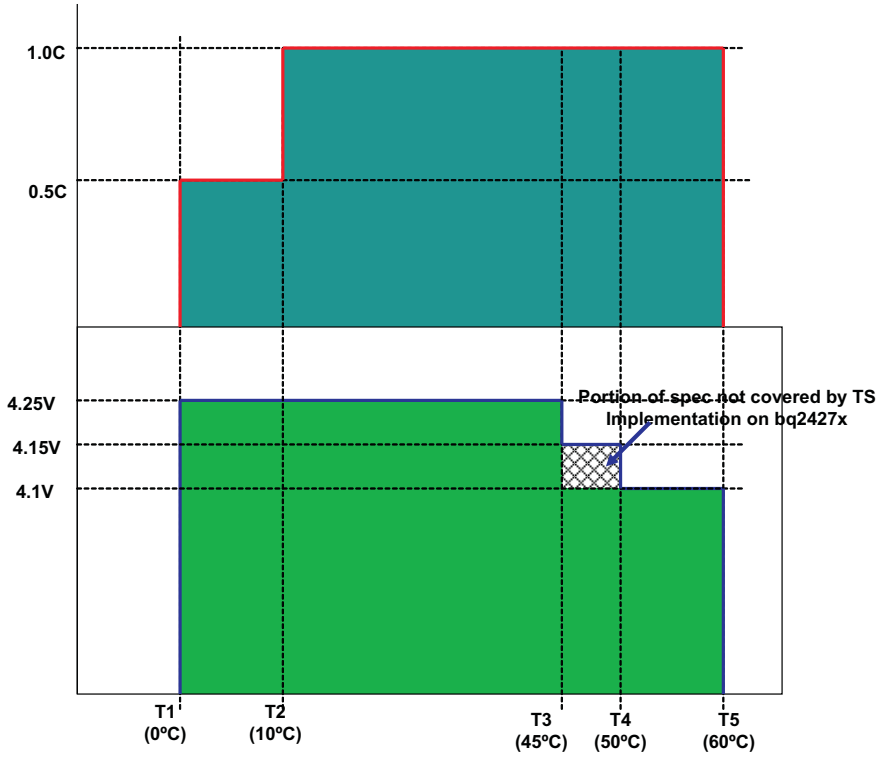


Figure 6. Charge Current/Voltage During TS Conditions

To satisfy the JEITA requirements, four temperature thresholds are monitored; the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < T_{NTC} < 10°C) the warm battery threshold (45°C < T_{NTC} < 60°C) and the hot battery threshold (T_{NTC} > 60°C).). These temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds. Charging is suspended and timers are suspended when V_{TS} < V_{HOT} or V_{TS} > V_{COLD}. When V_{HOT} < V_{TS} , V_{WARM} the battery regulation voltage is reduced by 140 mV from the programmed regulation threshold. When V_{COOL} < V_{TS} < V_{COLD}, the charging current is reduced to half of the programmed charge current.

The TS function is voltage based for maximum flexibility. Connect a resistor divider from DRV to GND with TS connected to the center tap to set the threshold. The connections are shown in Figure 7. The resistor values are calculated using the following equations:

$$RLO = \frac{V_{DRV} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{DRV}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{DRV}}{V_{COLD}} - 1\right]} \quad (1)$$

$$RHI = \frac{\frac{V_{DRV}}{V_{COLD}} - 1}{\frac{1}{RLO} + \frac{1}{RCOLD}} \quad (2)$$

Where:

V_{COLD} = 0.6 x V_{DRV}

V_{HOT} = 0.3 v V_{DRV}

Where RHOT is the NTC resistance at the hot temperature and RCOLD is the NTC resistance at cold temperature.

For the bq24270 and bq24271, the WARM and COOL thresholds are not independently programmable. The COOL and WARM NTC resistances for a selected resistor divider are calculated using the following equations:

$$RCOOL = \frac{RLO \times 0.564 \times RHI}{RLO - RLO \times 0.564 - RHI \times 0.564} \quad (3)$$

$$RWARM = \frac{RLO \times 0.383 \times RHI}{RLO - RLO \times 0.383 - RHI \times 0.383} \quad (4)$$

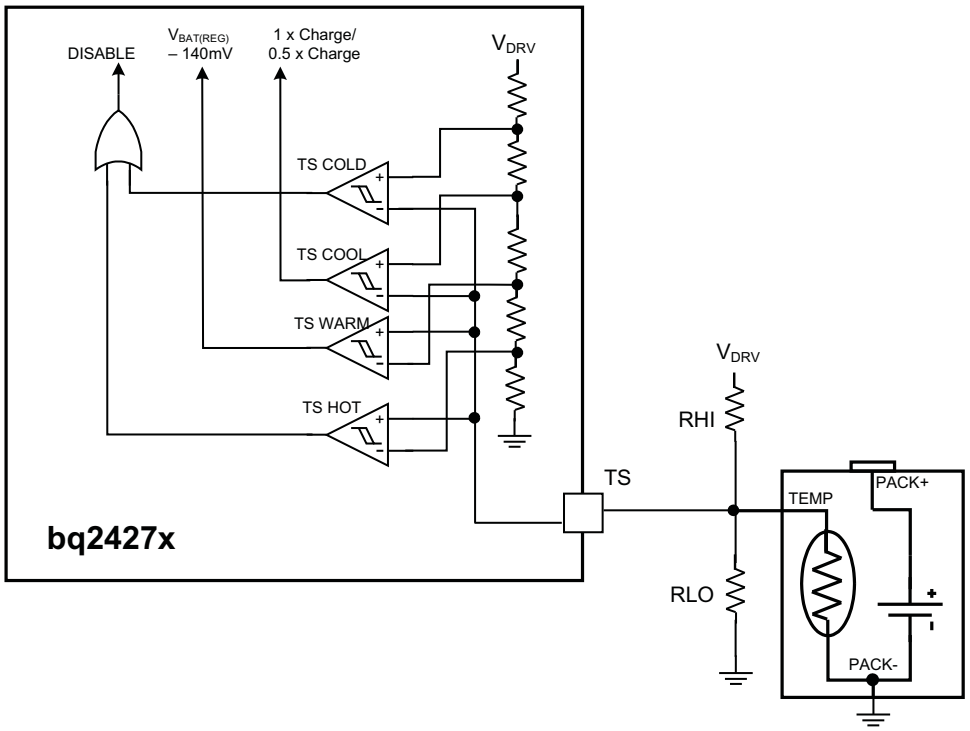


Figure 7. TS Circuit

If the TS function is not used, connect TS to DRV directly to disable the feature. Additionally, the TS function can be disabled in the I^2C by writing to the EN_TS bit. When the TS is disabled, the status registers always read "Normal".

Thermal Regulation and Protection

During the charging process, to prevent the IC from overheating, bq24270 and bq24271 monitor the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, T_{REG}. The charge current is reduced to zero when the junction temperature increases about 10°C above T_{REG}. Once the charge current is reduced, the system current is reduced while the battery supplements the load to supply the system. This may cause a thermal shutdown of the devices if the die temperature rises too high. At any state, if T_J exceeds T_{SHTDWN}, the devices suspend charging and disables the buck converter. During thermal shutdown mode, PWM is turned off, and the timers are suspended, and a single 128 µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. A new charging cycle begins when T_J falls below T_{SHTDWN} by approximately 10°C.

Input Voltage Protection in Charge Mode

Sleep Mode

The bq24270 and bq24271 enter the low-power sleep mode if the voltage on $V_{(USB)}$ falls below sleep-mode entry threshold, $V_{(BAT)}$ + $V_{(SLP)}$, and $V_{(VBUS)}$ is higher than the undervoltage lockout threshold, V_{UVLO}. This feature prevents draining the battery during the absence of $V_{(USB)}$. When $V_{(USB)} < V_{(BAT)} + V_{(SLP)}$, the devices turn off the PWM converter, turn on the battery FET, drive BGATE to GND, send a single 128 µs pulse on the STAT and INT outputs, and update the STATx and FAULT_x bits in the status registers. Once $V_{(USB)} > V_{(BAT)} + V_{(SLP)}$, the STATx and FAULT_x bits are cleared and the devices initiate a new charge cycle.

Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage deceases. Once the supply drops to V_{IN_DPM} (default 4.2 V), the input current limit is reduced down to prevent further supply droop. When the IC enters this mode, the charge current is lower than the set value and the DPM_STATUS bit is set (Bit 5 in Register 05H). This feature ensures IC compatibility with adapters with different current capabilities without a hardware change. Figure 8 shows the V_{IN-DPM} behavior to a current limited source. In this figure, the input source has a 750 mA current limit and the charging is set to 750 mA. The SYS load is then increased to 1.2 A.

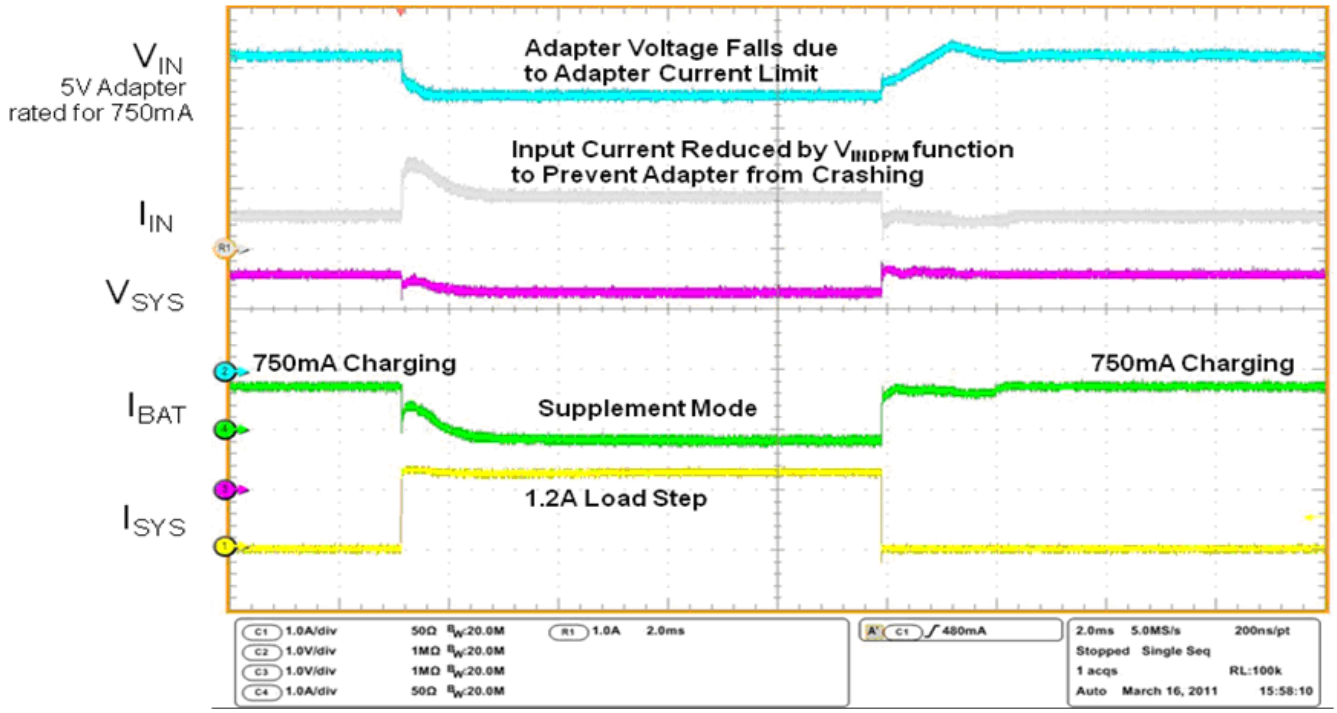


Figure 8. bq24270 V_{IN-DPM}

Bad Source Detection

When a source is connected to USB, the bq24270 and bq24271 run a Bad Source Detection procedure to determine if the source is strong enough to provide some current to charge the battery. A current sink is turned on (30 mA) for 32 ms. If the source is valid after the 32 ms ($V_{(BAD\_SOURCE)} < V_{(USB)} < V_{(OVP)}$), the buck converter starts up and normal operation continues. If the supply voltage falls below $V_{(BAD\_SOURCE)}$ during the detection, the current sink shuts off for 2s and then retries. The detection circuits retries, a single 128 µs pulse is sent on the STAT and INT outputs, and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated in the I^2C. The detection circuits retries continuously until either a new source is connected to the other input or a valid source is detected after the detection time. If during normal operation the source falls to $V_{(BAD\_SOURCE)}$, the devices turn off the PWM converter, turn on the battery FET and BGATE, send a single 128 µs pulse on the STAT and INT outputs, and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated in the I^2C. Once a good source is detected, the STATx and FAULT_x bits are cleared and the devices return to normal operation

Input Overvoltage Protection

The bq24270 and bq24271 provide overvoltage protection on the input that protects downstream circuitry. The built-in input overvoltage protection to protect the devices and other components against damage from overvoltage on the input supply (Voltage from $V_{(USB)}$ or V_{IN} to PGND). During normal operation, if $V_{(USB)} > V_{(OVP)}$, the devices turn off the PWM converter, turns the battery FET and BGATE on, sends a single 128 µs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers and the battery and supply status registers are updated in the I^2C. Once the OVP fault is removed, the STATx and FAULT_x bits are cleared and the devices return to normal operation.

Charge Status Outputs (STAT, INT)

The STAT output is used to indicate operation conditions for bq24270 and bq24271. STAT is pulled low during charging when EN_STAT bit in the control register (0x02h) is set to “1”. When charge is complete or disabled, STAT is high impedance. When a fault occurs, a 128-µs pulse (interrupt) is sent out to notify the host. The status of STAT during different operation conditions is summarized in Table 1. STAT drives an LED for visual indication or can be connected to the logic rail for host communication. The EN_STAT bit in the control register (00H) is used to enable/disable the charge status for STAT. The interrupt pulses are unaffected by EN_STAT and will always be shown. The INT output is identical to STAT and is used to interface with a low voltage host processor

Table 1. STAT Pin Summary

Charge State	STAT and INT behavior
Charge in progress and EN_STAT=1	Low
Other normal conditions	High-Impedance
Status Changes: Supply Status Change (plug in or removal), safety timer fault, watchdog expiration, sleep mode, battery temperature fault (TS), battery fault (OVP or absent), thermal shutdown	128-µs pulse, then High Impedance

The bq24270 and bq24271 contain a good battery monitor circuit that places the devices into high-z mode if the battery voltage is above the BATGD threshold while in DEFAULT mode. This function is used to enable compliance to the battery charging standard that prevents charging from an un-enumerated USB host while the battery is above the good battery threshold. If the devices are in HOST mode, it is assumed that USB host has been enumerated and the good battery circuit has no effect on charging.

SERIAL INTERFACE DESCRIPTION

The bq24270 and bq24271 use an I^2C compatible interface to program charge parameters. I^2C is a 2-wire serial interface developed by Philips Semiconductor (see I^2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The devices work as a slave and support the following data transfer modes, as defined in the I^2C Bus Specification: standard mode (100 kbps) and fast mode (400 kbps). The interface adds flexibility to the battery charging solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as battery voltage remains above 2.5 V (typical). The I^2C circuitry is powered from $V_{(BUS)}$ when a supply is connected. If the $V_{(BUS)}$ supply is not connected, the I^2C circuitry is powered from the battery through BAT. The battery voltage must stay above 2.5 V with no input connected in order to maintain proper operation

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The devices only support 7-bit addressing. The 7-bit address is defined as ‘1101011’ (6Bh).

F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 9. All I^2C - compatible devices should recognize a start condition.

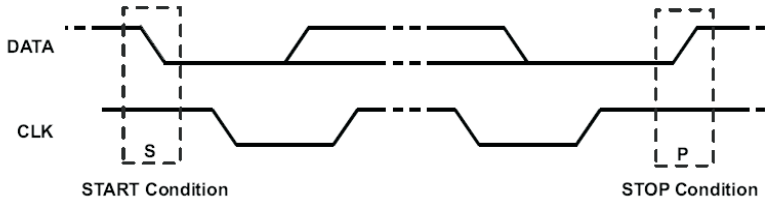


Figure 9. START and STOP Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 10). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 11) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

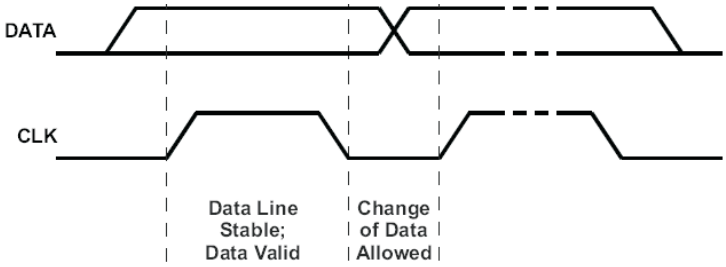


Figure 10. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 12). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs sending a STOP condition to prevent the slave I^2C logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section result in FFh being read out.

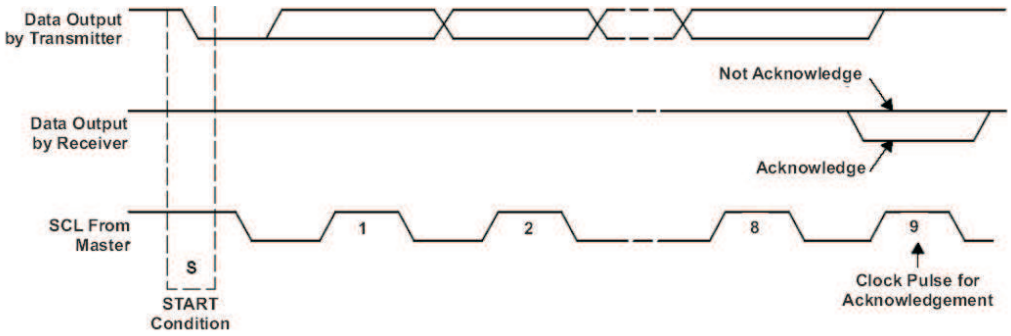


Figure 11. Acknowledge on the I^2C Bus

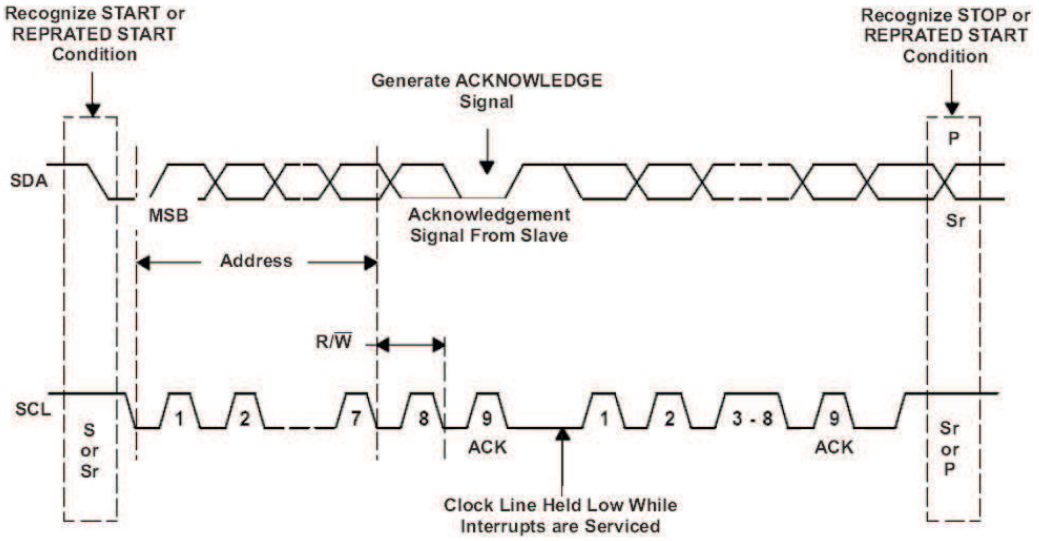


Figure 12. Bus Protocol

REGISTER DESCRIPTION

Status and Control Register (READ/WRITE)

Memory location: 00, Reset state: 0xxx 0xxx

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	TMR_RST	Read/Write	Write: TMR_RST function, write “1” to reset the watchdog timer (auto clear) Read: Always 0
B6	STAT_2	Read only	000- No Valid Source Detected 001- NA 010- USB Ready 011-NA 100- Charging from USB 101- Charge Done 110- NA 111- Fault
B5	STAT_1	Read only	
B4	STAT_0	Read only	
B3	NA	Read/Write	NA
B2	FAULT_2	Read only	000-Normal 001- Thermal Shutdown 010- Battery Temperature Fault 011- Watchdog Timer Expired (bq24270/1 only) 100- Safety Timer Expired (bq24270/1 only) 101- NA 110- USB Supply Fault 111- Battery Fault
B1	FAULT_1	Read only	
B0(LSB)	FAULT_0	Read only	

Battery and Supply Status Register (READ/WRITE)

Memory location: 01, Reset state: xxxx 0xxx

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	NA	Read Only	NA
B6	NA	Read Only	NA
B5	USBSTAT1	Read Only	00-Normal 01-Supply OVP 01-Weak Source Connected (No Charging) 11- $V_{USB} < V_{UVLO}$
B4	USBSTAT0	Read Only	
B3	OTG_LOCK	Read/Write	0 – No OTG supply present. Use USB input as normal. 1 – OTG supply present. Lockout USB input for charging. (default 0)
B2	BATSTAT1	Read Only	00-Battery Present and Normal 01-Battery OVP 10-Battery Not Present 11- NA
B1	BATSTAT0	Read Only	
B0 (LSB)	EN_NOBATOP	Read/ Write	0-Normal Operation 1-Enables No Battery Operation when termination is disabled (default 0)

OTG_LOCK Bit (USB Lockout)

The OTG_LOCK bit is used to prevent any charging from USB. For systems using OTG supplies, it is not desirable to charge from an OTG source. Doing so would mean draining the battery by allowing it to effectively charge itself. Write a “1” to OTG_LOCK to lock out the USB input. Write a “0” to OTG_LOCK to return to normal operation. The watchdog timer must be reset while in USB_LOCK to maintain the USB lockout state. This prevents the USB input from being permanently locked out for cases where the host loses I^2C communication with OTG_LOCK set (i.e. discharged battery from OTG operation). See the Safety Timer and Watchdog Timer section for more details.

EN_NOBATOP (No Battery Operation with Termination Disabled

The EN_NOBATOP bit is used to enable operation when termination is disabled and no battery is connected. This is useful for cases where the PA is connected to the BAT pin and it desired to do a calibration in the factory. For this application, the TE bit (Bit 2 in Register 0x02h) should be set to a “0” to disable termination and the EN_NOBATOP should be set to a “1”. This feature should not be used during normal operation as it disables the BATOVP and the reverse boost protection circuits.

Control Register (READ/WRITE)

Memory location: 02, Reset state: 1000 1100

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	RESET	Write only	Write: 1-Reset all registers to default values 0-No effect Read: always get “1”
B6	IUSB_LIMIT_2	Read/Write	000-USB2.0 host with 100mA current limit 001-USB3.0 host with 150mA current limit 010 – USB2.0 host with 500mA current limit 011 – USB host/charger with 800mA current limit 100 – USB3.0 host with 900mA current limit 101 – USB host/charger with 1500mA current limit 110 -111 – NA (default 000(1))
B5	IUSB_LIMIT_1	Read/Write	
B4	IUSB_LIMIT _0	Read/Write	
B3	EN_STAT	Read/Write	1-Enable STAT output to show charge status, 0-Disable STAT output for charge status. Fault interrupts are still show even when EN_STAT = 0. (default 1)
B2	TE	Read/Write	1-Enable charge current termination, 0-Disable charge current termination (default 1)
B1	$\overline{CE}$	Read/Write	1-Charger is disabled 0-Charger enabled (default 0)

BIT	NAME	Read/Write	FUNCTION
B0 (LSB)	HZ_MODE	Read/Write	1-High impedance mode 0-Not high impedance mode (default 0)

RESET Bit

The RESET bit in the control register (0x02h) is used to reset all the charge parameters. Write “1” to RESET bit to reset all the registers to default values and place the bq24270 and bq24271 into DEFAULT mode and turn off the watchdog timer. The RESET bit is automatically cleared to zero once the devices enter DEFAULT mode.

$\overline{CE}$ Bit (Charge Enable

The $\overline{CE}$ bit in the control register (0x02h) is used to disable or enable the charge process. A low logic level (0) on this bit enables the charge and a high logic level (1) disables the charge. When charge is disabled, the SYS output regulates to VSYS(REG) and battery is disconnected from the SYS. Supplement mode is still available if the system load demands cannot be met by the supply. BGATE is high impedance when $\overline{CE}$ is high.

HZ_MODE Bit (High Impedance Mode Enable

The HZ_MODE bit in the control register (0x02h) is used to disable or enable the high impedance mode. A low logic level (0) on this bit enables the IC and a high logic level (1) puts the IC in a low quiescent current state called high impedance mode. When in high impedance mode, the converter is off and the battery FET and BGATE are on. The load on SYS is supplied by the battery.

Control/Battery Voltage Register (READ/WRITE)

Memory location: 03, Reset state: 0001 0100

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	VBREG5	Read/Write	Battery Regulation Voltage: 640mV (default 0)
B6	VBREG4	Read/Write	Battery Regulation Voltage: 320mV (default 0)
B5	VBREG3	Read/Write	Battery Regulation Voltage: 160mV (default 0)
B4	VBREG2	Read/Write	Battery Regulation Voltage: 80mV (default 1)
B3	VBREG1	Read/Write	Battery Regulation Voltage: 40mV (default 0)
B2	VBREG0	Read/Write	Battery Regulation Voltage: 20mV (default 1)
B1	NA	Read/Write	NA
B0(LSB)	D+/D-_EN	Read/Write	0—Normal state, D+/D- Detection done 1—Force D+/D- Detection. Returns to “0” after detection is done. (default 0)

Charge voltage range is 3.5 V—4.44 V with the offset of 3.5V and step of 20mV (default 3.6V).

Vender, Part, Revision Register (READ only)

Memory location: 04, Reset state: 0100 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	Vender2	Read only	Vender Code: bit 2 (default 0)
B6	Vender1	Read only	Vender Code: bit 1 (default 1)
B5	Vender0	Read only	Vender Code: bit 0 (default 0)
B4	PN1	Read only	For I^2C Address 6Bh: 00: bq24270 and bq24271 01 – 11: Future product spins
B3	PN0	Read only	
B2	Revision2	Read only	000: Revision 1.0 001:Revision 1.1 010: Revision 2.0 011:Revision 2.1 100:Revision 2.2 101: Revision 2.3 110-111: Future Revisions
B1	Revision1	Read only	
B0(LSB)	Revision0	Read only	

Battery Termination and Fast Charge Current Register (READ/WRITE)

Memory location: 05, Reset state: 0011 0010

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	NA	Read/Write	NA
B6	I_{CHRG3}	Read/Write	Charge current: 600 mA— (default 0)
B5	I_{CHRG2}	Read/Write	Charge current: 300 mA—(default 1)
B4	I_{CHRG1}	Read/Write	Charge current: 150 mA— (default 1)
B3	I_{CHRG0}	Read/Write	Charge current: 75 mA (default 0)
B2	I_{TERM2}	Read/Write	Termination current sense voltage: 200 mA (default 0)
B1	I_{TERM1}	Read/Write	Termination current sense voltage: 100 mA (default 1)
B0(LSB)	I_{TERM0}	Read/Write	Termination current sense voltage: 50 mA (default 0)

Charge current sense offset is 550 mA and default charge current is 1000 mA

Termination threshold offset is 50 mA and default termination current is 150 mA

V_{IN-DPM} Voltage and DPPM Status Register

Memory location: 06, Reset state: xx00 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	MINSYS_STATUS	Read Only	1—Minimum System Voltage mode is active (low battery condition) 0—Minimum System Voltage mode is not active
B6	DPM_STATUS	Read Only	1—V_{IN-DPM} mode is active 0—V_{IN-DPM} mode is not active
B5	$V_{INDPM2(USB)}$	Read/Write	USB input V_{IN-DPM} voltage: 320mV (default 0)
B4	$V_{INDPM1(USB)}$	Read/Write	USB input V_{IN-DPM} voltage: 160mV (default 0)
B3	$V_{INDPM0(USB)}$	Read/Write	USB input V_{IN-DPM} voltage: 80mV (default 0)
B2	NA	Read/Write	NA
B1	NA	Read/Write	NA
B0(LSB)	NA	Read/Write	NA

V_{IN-DPM} voltage offset is 4.20 V and default V_{IN-DPM} threshold is 4.20 V

Safety Timer and NTC Monitor Register (READ/WRITE)

Memory location: 07, Reset state: 1001 1xxx

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	2XTMR_EN	Read/Write	1 – Timer slowed by 2x when in thermal regulation, input current limit, V_{IN_DPM} or DPPM 0 – Timer not slowed at any time (default 0)
B6	TMR_1	Read/Write	Safety Timer Time Limit – 00 – 27 minute fast charge 01 – 6 hour fast charge 10 – 9 hour fast charge 11 – Disable safety timers (default 00)
B5	TMR_2	Read/Write	
B4	NA	Read/Write	NA
B3	TS_EN	Read/Write	0 – TS function disabled 1 – TS function enabled (default 1)
B2	TS_FAULT1	Read only	TS Fault Mode: 00— Normal, No TS fault 01— TS temp < T_{COLD} or TS temp > T_{HOT} (Charging suspended) 10— T_{COOL} > TS temp > T_{COLD} (Charge current reduced by half, bq24270 only) 11— T_{WARM} < TS temp < T_{HOT} (Charge voltage reduced by 140 mV, bq24270 only)
B1	TS_FAULT0	Read only	
B0(LSB)	LOW_CHG	Read/ Write	0 – Charge current as programmed in Register 0x05
			1 – Charge current is half programmed value in Register 0x05 (default 0)

LOW_CHG Bit (Low Charge Mode Enable)

The LOW_CHG bit is used to reduce the charge current from the programmed value. This feature is used by systems where battery NTC is monitored by the host and requires a reduced charge current setting or by systems that need a “preconditioning” current for low battery voltages. Write a “1” to this bit to charge at half of the programmed charge current. Write a “0” to this bit to charge at the programmed charge current.

APPLICATION INFORMATION

Output Inductor and Capacitor Selection Guidelines

When selecting an inductor, several attributes must be examined to find the right part for the application. First, the inductance value should be selected. The bq24270 and bq24271 are designed to work with 1.5 µH to 2.2 µH inductors. The chosen value will have an effect on efficiency and package size. Due to the smaller current ripple, some efficiency gain is reached using the 2.2 µH inductor, however, due to the physical size of the inductor, this may not be a viable option. The 1.5 µH inductor provides a good tradeoff between size and efficiency.

Once the inductance has been selected, the peak current must be calculated in order to choose the current rating of the inductor. Use Equation 5 to calculate the peak current.

$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{\%_{RIPPPLE}}{2}\right) \quad (5)$$

The inductor selected must have a saturation current rating less than or equal to the calculated I_{PEAK}. Due to the high currents possible with the devices, a thermal analysis must also be done for the inductor. Many inductors have 40°C temperature rise rating. This is the DC current that will cause a 40°C temperature rise above the ambient temperature in the inductor. For this analysis, the typical load current may be used adjusted for the duty cycle of the load transients. For example, if the application requires a 1.5 A DC load with peaks at 2.5 A 20% of the time, a Δ40°C temperature rise current must be greater than 1.7 A:

$$I_{TEMPRISE} = I_{LOAD} + D \times (I_{PEAK} - I_{LOAD}) = 1.5\ A + 0.2 \times (2.5\ A - 1.5\ A) = 1.7\ A \quad (6)$$

The devices provide internal loop compensation. Using this scheme, the bq24270 is stable with 10 µF to 200 µF of local capacitance. The capacitance on the SYS rail can be higher if distributed amongst the rail. To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 10µF and 47µF is recommended for local bypass to SYS.

PCB Layout Guidelines

It is important to pay special attention to the PCB layout. Figure 13 provides a sample layout for the high current paths of the bq24270 and bq24271.

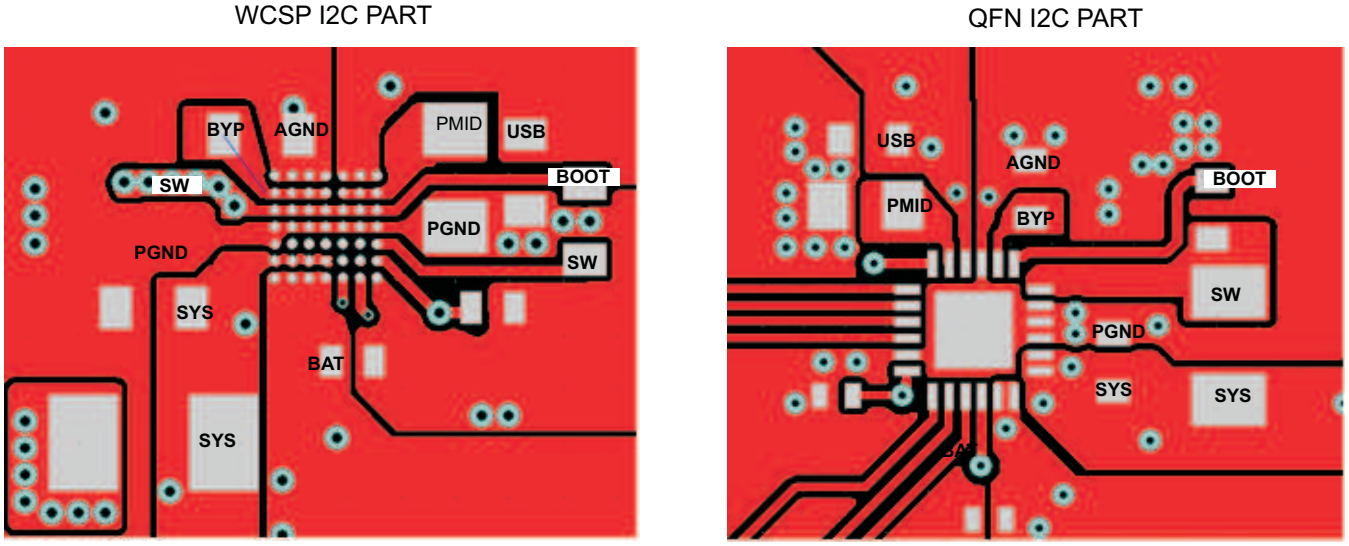
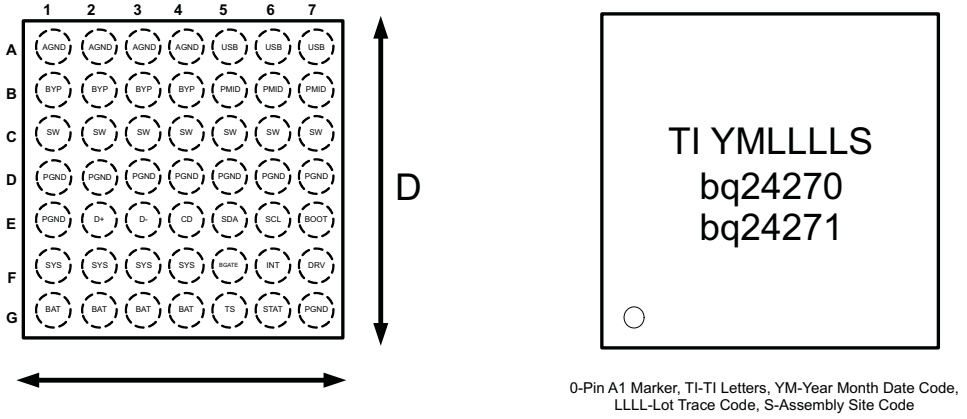


Figure 13. Recommended bq24270 and bq24271 PCB Layout

The following provides some guidelines:

- To obtain optimal performance, the power input capacitors, connected from the PMID input to PGND, must be placed as close as possible to the bq24270 and bq24271
- Place 4.7 µF input capacitor as close to PMID pin and PGND pin as possible to make high frequency current loop area as small as possible. Place 1µF input capacitor GNDs as close to the respective PMID cap GND and PGND pins as possible to minimize the ground difference between the input and PMID.
- The local bypass capacitor from SYS to GND should be connected between the SYS pin and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin.
- Place all decoupling capacitor close to their respective IC pin and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components). It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.
- The high-current charge paths into USB, BAT, SYS and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET.
- For high-current applications, the balls for the power paths should be connected to as much copper in the board as possible. This allows better thermal performance as the board pulls heat away from the IC.

PACKAGE SUMMARY



0-Pin A1 Marker, TI-TI Letters, YM-Year Month Date Code, LLLL-Lot Trace Code, S-Assembly Site Code

CHIP SCALE PACKAGING DIMENSIONS

The devices are available in a 49-bump chip scale package (YFF, NanoFree™). The package dimensions are:

- D – 2.78mm ± 0.05mm
- E – 2.78mm ± 0.05mm

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ24270RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BQ 24270	Samples
BQ24270RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BQ 24270	Samples
BQ24270YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24270	Samples
BQ24270YFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24270	Samples
BQ24271RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24271	Samples
BQ24271RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24271	Samples
BQ24271YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24271	Samples
BQ24271YFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24271	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

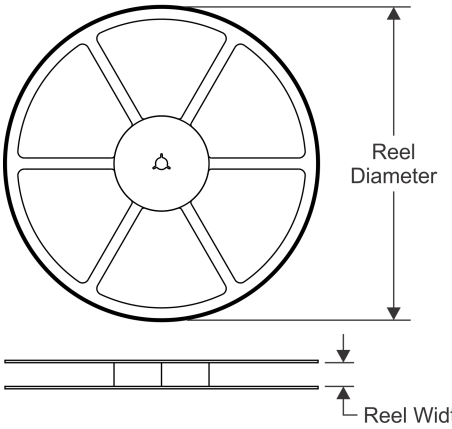
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

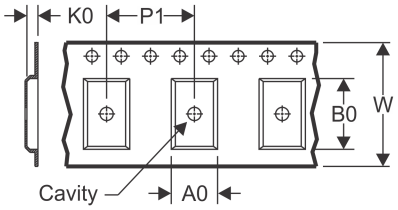
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

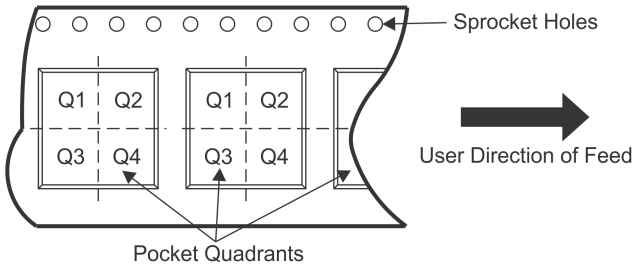


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

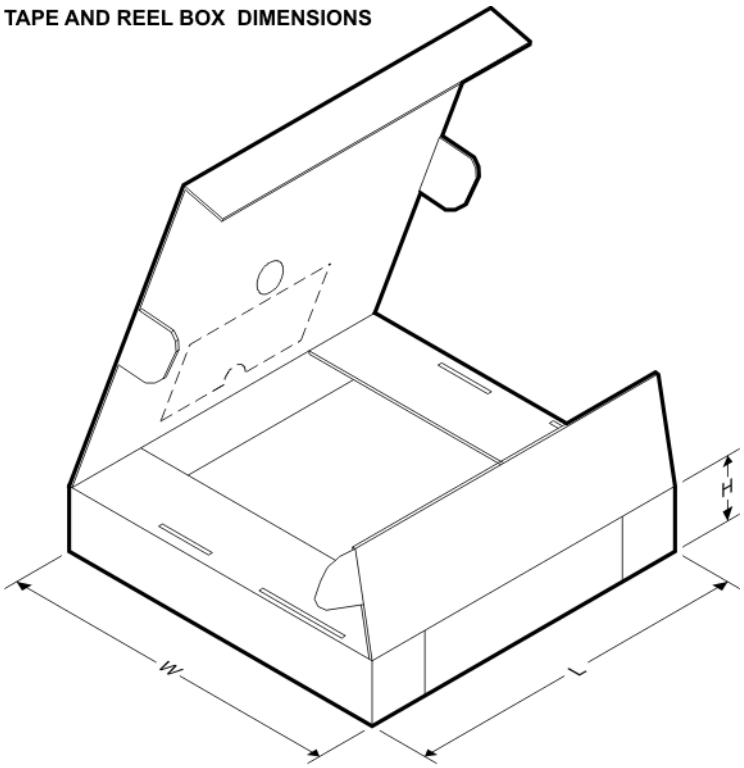
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24270RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24270RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24270YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24270YFFT	DSBGA	YFF	49	250	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24271RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24271RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24271YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24271YFFT	DSBGA	YFF	49	250	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1

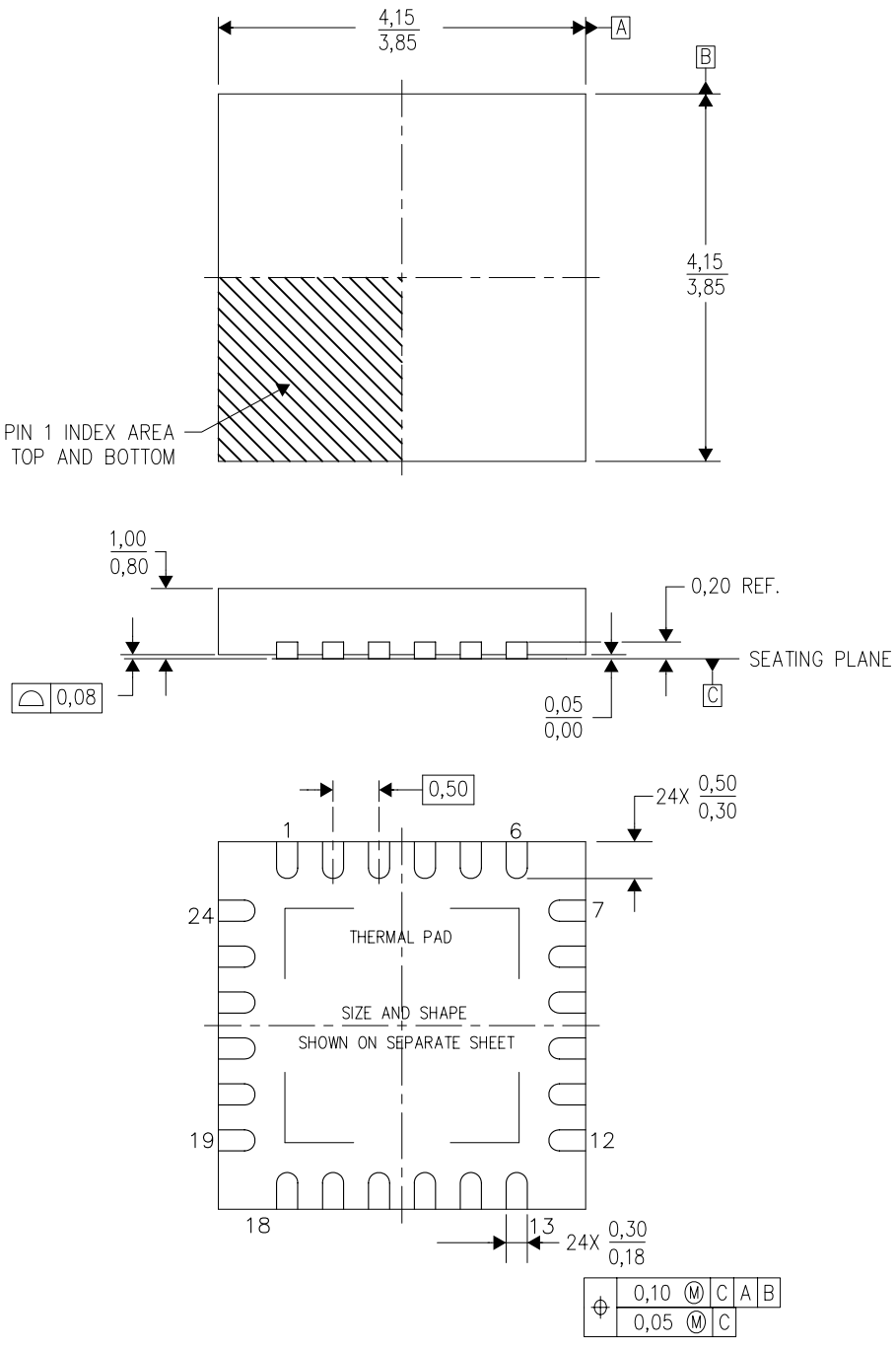
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24270RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24270RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24270YFFR	DSBGA	YFF	49	3000	210.0	185.0	35.0
BQ24270YFFT	DSBGA	YFF	49	250	210.0	185.0	35.0
BQ24271RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24271RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24271YFFR	DSBGA	YFF	49	3000	210.0	185.0	35.0
BQ24271YFFT	DSBGA	YFF	49	250	210.0	185.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

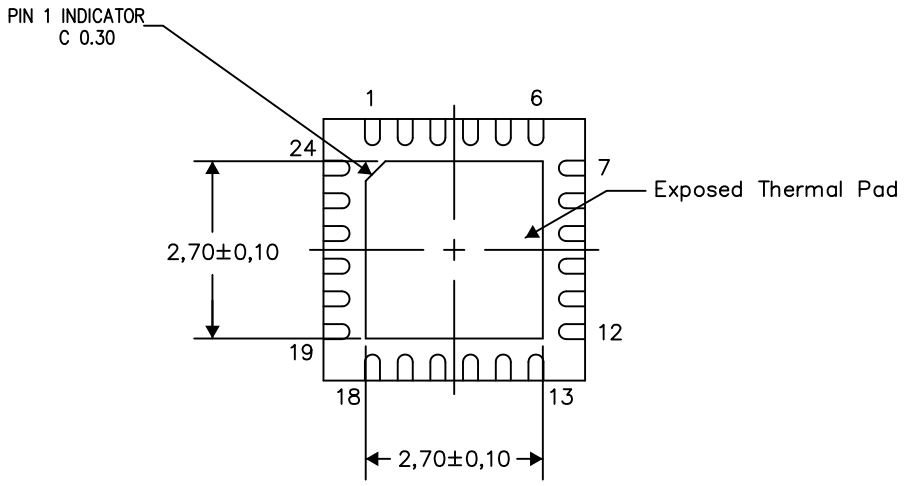
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



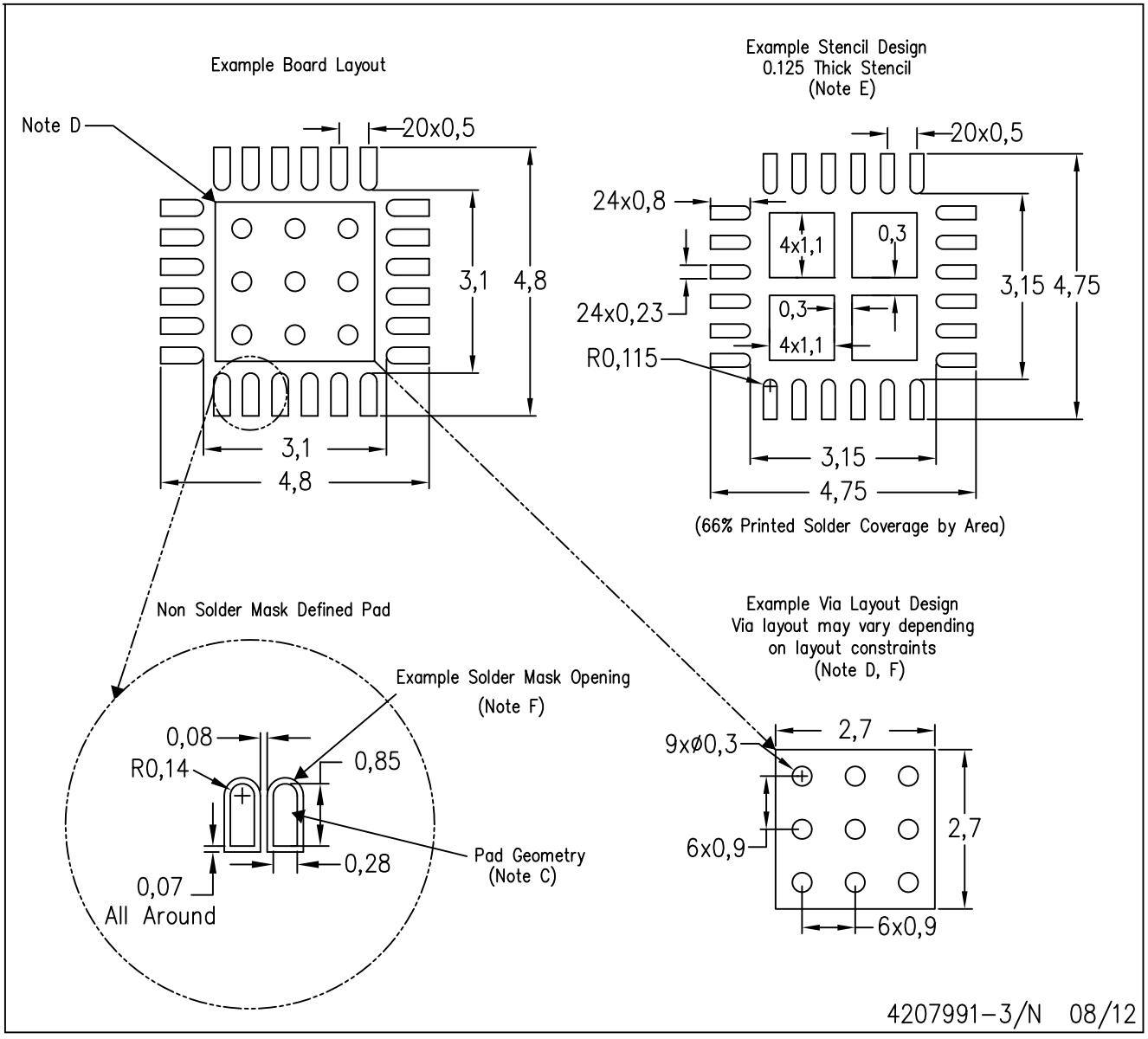
Bottom View

Exposed Thermal Pad Dimensions

4206344–4/AB 09/12

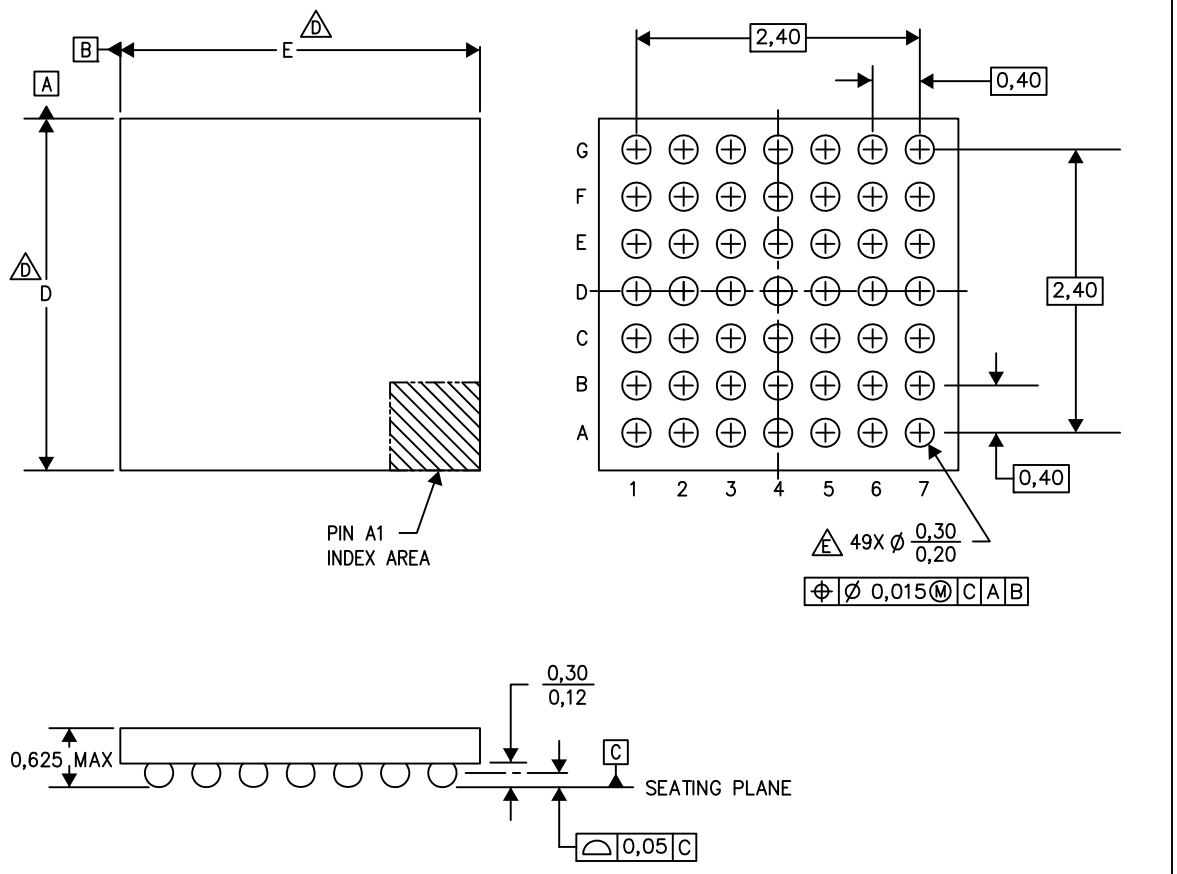
NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
7 x 7 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

NanoFree is a trademark of Texas Instruments

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