◇PRODUCT　256×8 bit Electrically Erasable PROM (based on Serial Presence Detect)

◇PART NUMBER　BR34L02FV-W

◇DESCRIPTION　The BR34L02FV-W is a 2k bit EEPROM memory with write-protect function having independent rewrite inhibit area, developed for a DIMM that uses syncronous DRAM memory, and a RIMM that uses RAMBUS DRAM memory. This is a memory IC that reads ID in order for the Plug & Play feature to operate.

◇APPLICATION　General purpose

◇FEATURES
- 256k registers × 8 bits serial architecture
- Single power supply (1.8V～5.5V)
- Two wire serial interface
- Page Write Function(16byte)
- Write Protect Mode
  Write Protect 1(Onetime Rom)　: 00h～7Fh
  Write Protect 2(Hardwire WP PIN) : 00h～FFh
- Low Power consumption
  Write　(5V) : 1.2mA (Typ.)
  Read　(5V) : 0.2mA (Typ.)
  Standby (5V) : 0.1μA(Typ.)
- DATA security
  Write protect feature (WP pin)
  Inhibit to WRITE at low Vcc
- Small package ------ SSOP-B8pin
- High reliability fine pattern CMOS technology
- Endurance : 1,000,000 erase/write cycles
- Data retention : 40 years
- Filtered inputs in SCL·SDA for noise suppression
- Initial data FFh in all address

◇ABSOLUTE MAXIMUM RATING (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.3～6.5	V
Power Dissipation	Pd	300 (SSOP-B8) *	
Storage Temperature	Tstg	-65～125	℃
Operating Temperature	Topr	-40～85	℃
Terminal Voltage	—	-0.3～Vcc+0.3	V

* Degradation is done at 3.0mW/℃ for operation above 25℃

◇RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	1.8～5.5	V
Input Voltage	VIN	0～Vcc	V

◇DC OPERATING CHARACTERISTICS (Unless otherwise specified Ta=-40～85℃, Vcc=1.8～5.5V)

Parameter	Symbol	Specification			Unit	test condition
		min.	typ.	max.		
"H" Input Voltage1	VIH1	0.7Vcc	—	—	V	2.5V≦Vcc≦5.5V
"L" Input Voltage1	VIL1	—	—	0.3Vcc	V	2.5V≦Vcc≦5.5V
"H" Input Voltage2	VIH2	0.8Vcc	—	—	V	1.8V≦Vcc＜2.5V
"L" Input Voltage2	VIL2	—	—	0.2Vcc	V	1.8V≦Vcc＜2.5V
"L" Output Voltage1	VOL1	—	—	0.4	V	IOL=3.0mA, 2.5V≦Vcc≦5.5V, (SDA)
"L" Output Voltage2	VOL2	—	—	0.2	V	IOL=0.7mA, 1.8V≦Vcc＜2.5V, (SDA)
Input Leakage Current 1	ILI 1	-1	—	1	μA	VIN=0V～Vcc
Input Leakage Current 2	ILI 2	-1	—	15	μA	VIN=0V～Vcc (WP)
Output Leakage Current	ILO	-1	—	1	μA	VOUT=0V～Vcc
Operating Current	ICC1	—	—	2.0	mA	Vcc=5.5V,fSCL=400kHz,tWR=5ms Byte Write Page Write Write Protect
	ICC2	—	—	0.5	mA	Vcc=5.5V,fSCL=400kHz Random Read Current Read Sequential Read
Standby Current	ISB	—	—	2.0	μA	Vcc=5.5V,SDA・SCL=Vcc A0,A1,A2=GND,WP=GND

○ This product is not designed for protection against radioactive rays.

◇DIMENSION

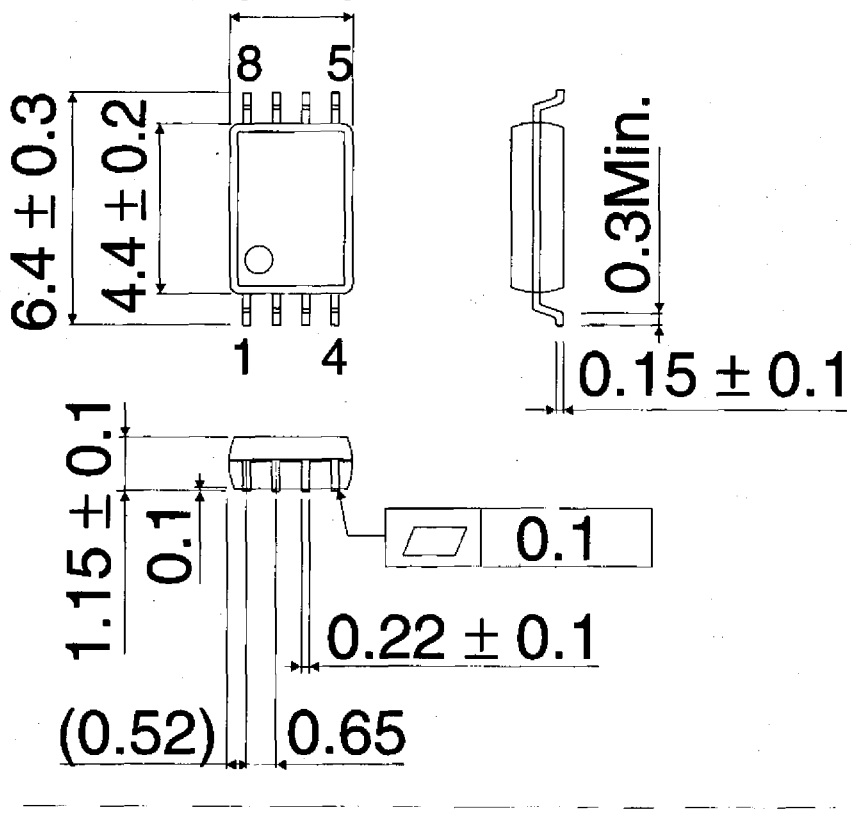


Fig.-1(a) PHYSICAL DIMENSION (SSOP-B8) (Unit : mm)

◇BLOCK DIAGRAM

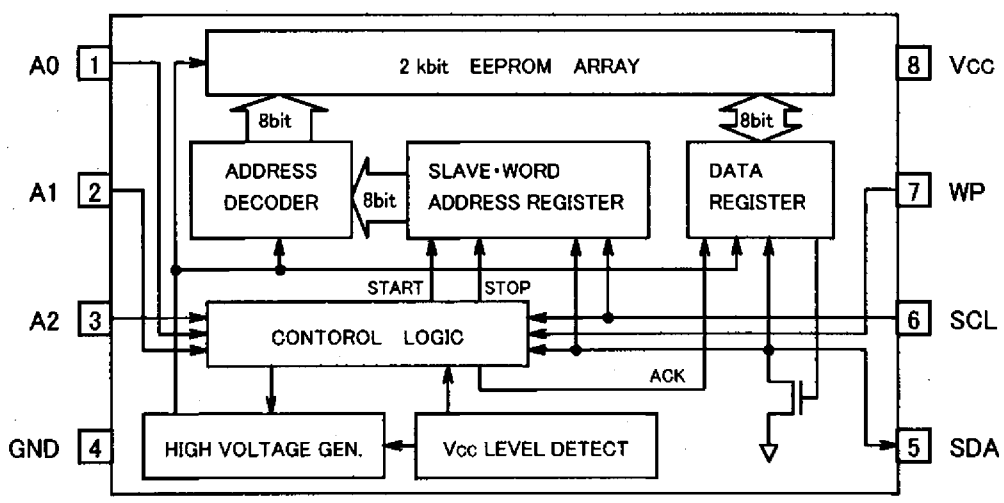


Fig.-2 BLOCK DIAGRAM

◇PIN CONFIGURATION

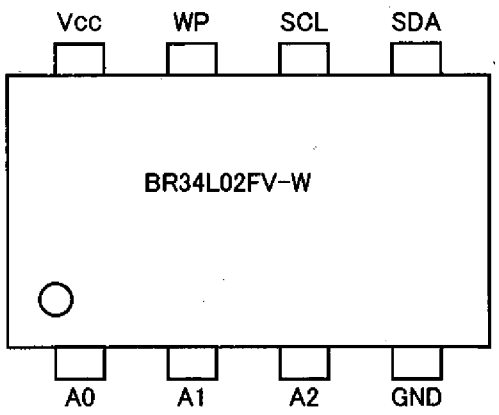


Fig.-3 PIN LAYOUT

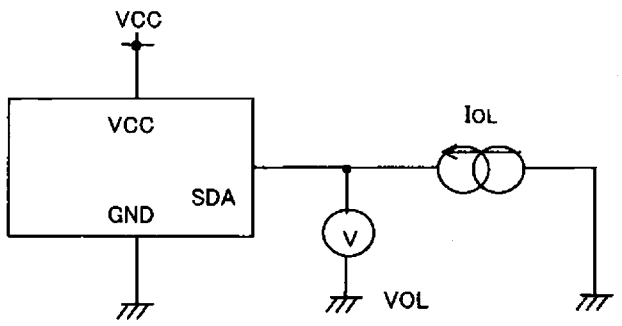
◇PIN NAME

PIN NAME	I/O	FUNCTIONS
Vcc	—	Power Supply
GND	—	Ground (0V)
A0,A1,A2	IN	Slave Address Set.
SCL	IN	Serial Clock Input
SDA	IN/OUT	Slave and Word Address, Serial Data Input, Serial Data Output *1
WP	IN	Write Protect Input *2

*1 An open drain output requires a pull-up resister.

*2 WP Pin has a Pull-Down resister. Please be left unconnected or connect to GND when WP feature is not in use.

◇TEST CIRCUIT



OUTPUT ="L"

Fig-4 "L" OUTPUT VOLTAGE TEST CIRCUIT

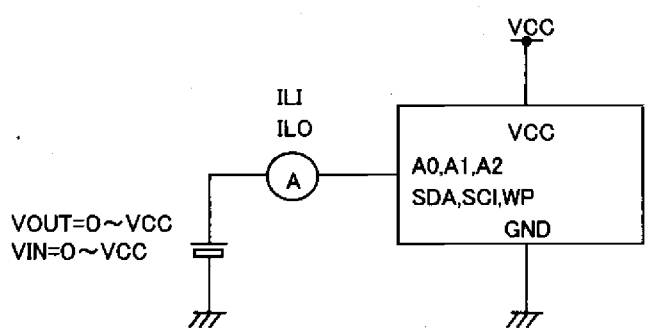


Fig-5 INPUT/OUTPUT CURRENT TEST CIRCUIT

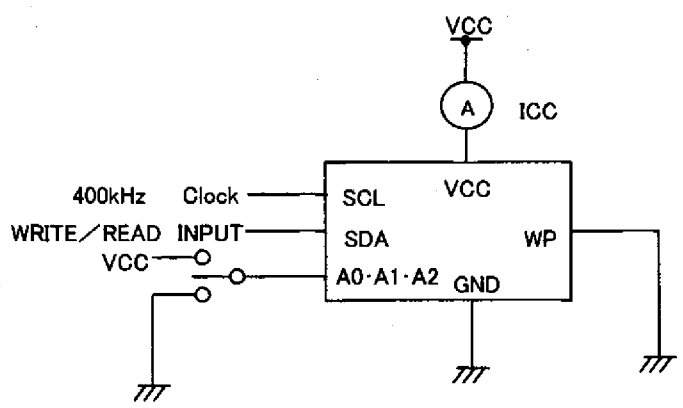


Fig-6 POWER CONSUMPTION TEST CIRCUIT

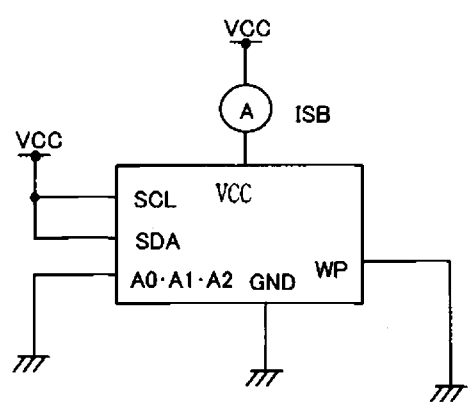


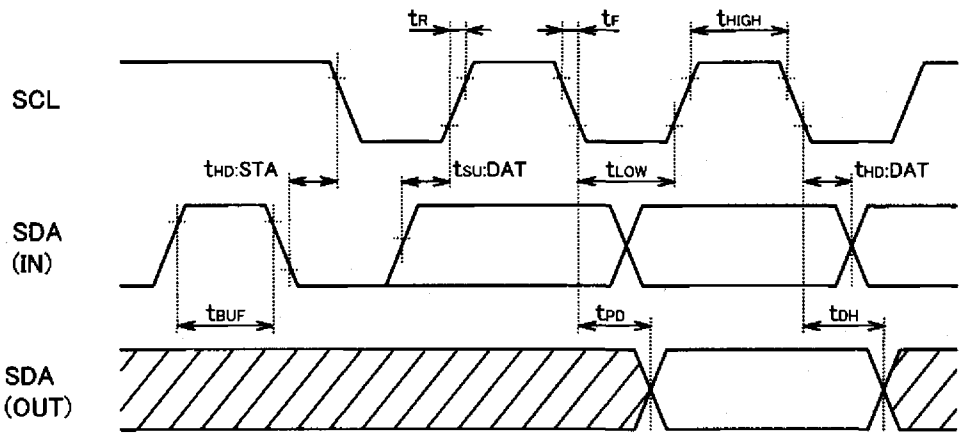
Fig-7 STANDBY CURRENT VOLTAGE TEST CIRCUIT

◇AC OPERATING CHARACTERISTICS (Unless otherwise specified Ta=-40～85℃, Vcc=1.8～5.5V)

Parameter	Symbol	FAST-MODE 2.5≦Vcc≦5.5V			STANDARD-MODE 1.8≦Vcc≦5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fSCL	—	—	400	—	—	100	kHz
Data Clock High Period	tHIGH	0.6	—	—	4.0	—	—	μs
Data Clock Low Period	tLOW	1.2	—	—	4.7	—	—	μs
SDA and SCL Rise Time ※1	tR	—	—	0.3	—	—	1.0	μs
SDA and SCL Fall Time ※1	tF	—	—	0.3	—	—	0.3	μs
Start Condition Hold Time	tHD:STA	0.6	—	—	4.0	—	—	μs
Start Condition Setup Time	tSU:STA	0.6	—	—	4.7	—	—	μs
Input Data Hold Time	tHD:DAT	0	—	—	0	—	—	ns
Input Data Setup Time	tSU:DAT	50	—	—	50	—	—	ns
Output Data Delay Time	tPD	0.1	—	0.9	0.2	—	3.5	μs
Output Data Hold Time	tDH	0.1	—	—	0.2	—	—	μs
Stop Condition Setup Time	tSU:STO	0.6	—	—	4.7	—	—	μs
Bus Free Time	tBUF	1.2	—	—	4.7	—	—	μs
Write Cycle Time	tWR	—	—	5	—	—	5	ms
Noise Spike Width (SDA and SCL)	tI	—	—	0.1	—	—	0.1	μs
WP Hold Time	tHD:WP	0	—	—	0	—	—	ns
WP Setup Time	tSU:WP	0.1	—	—	0.1	—	—	μs
WP High Period	tHIGH:WP	1.0	—	—	1.0	—	—	μs

※1:Not 100% TESTED

◇SYNCHRONOUS DATA TIMING



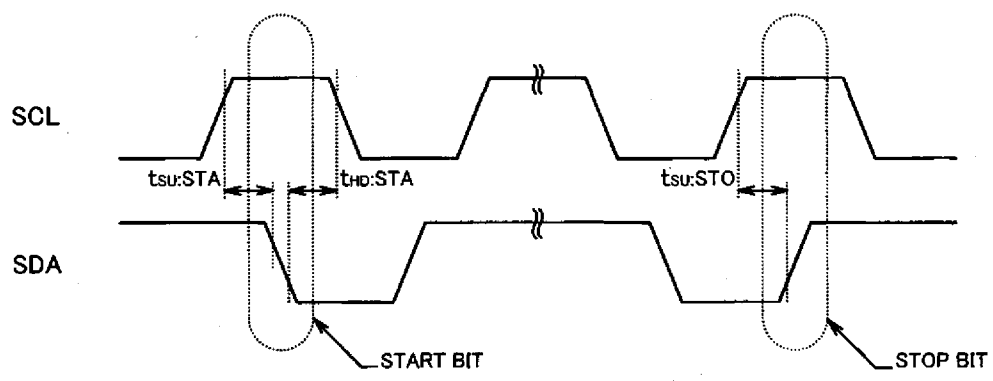


Fig.-8 SYNCHRONOUS DATA TIMING

○SDA data is latched into the chip at the rising edge of SCL clock.
○Output date toggles at the falling edge of SCL clock.

◇WRITE CYCLE TIMING

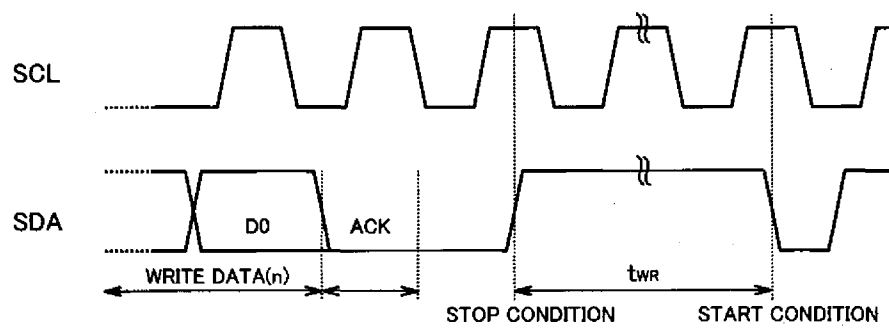


Fig.-9 WRITE CYCLE TIMING

◇WP TIMING

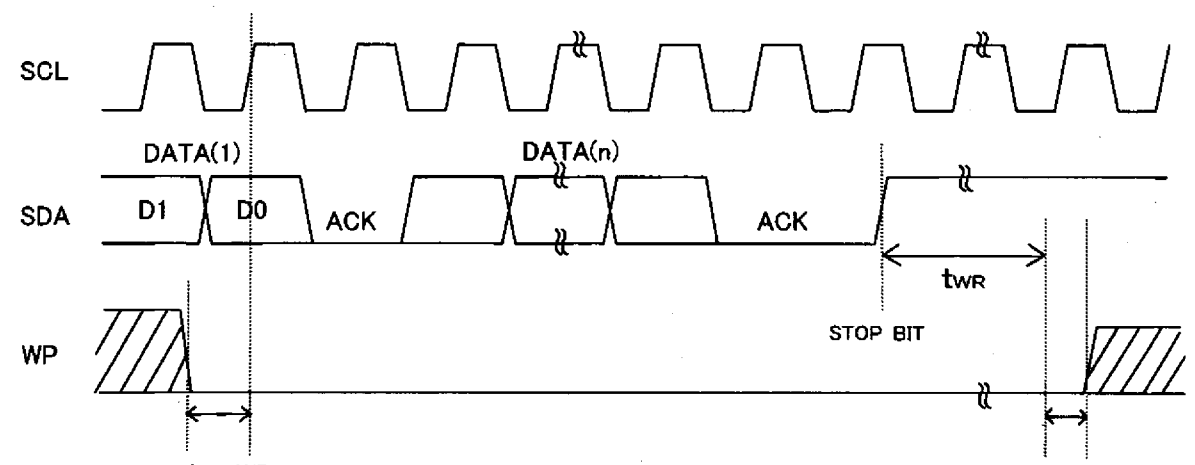


Fig-10(a) WP TIMING OF THE WRITE OPERATION

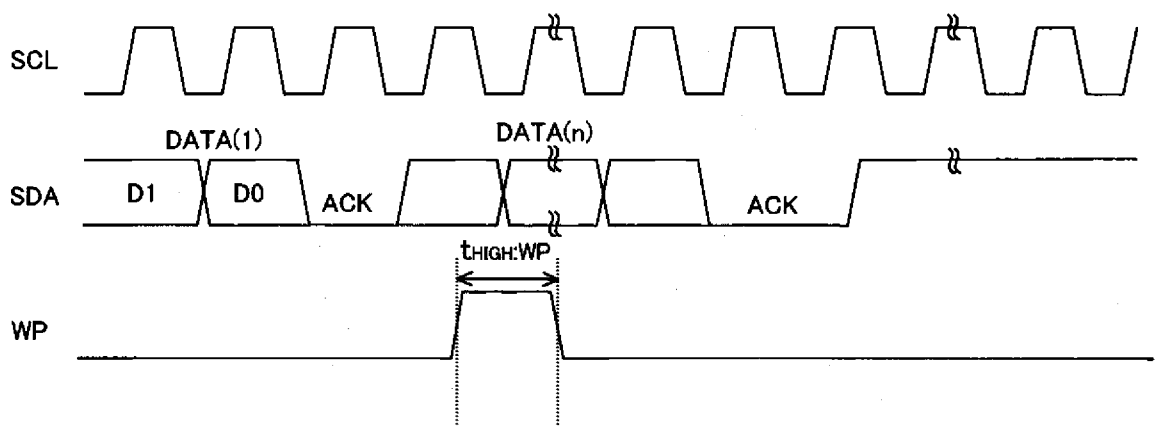


Fig-10(b) WP TIMING OF THE WRITE CANCEL OPERATION

○For the WRITE operation, WP must be "LOW" during the period of time from the rising edge of the clock which takes in D0 of first byte until the end of t_{WR}. (See Fig-10(a))
During this period, WRITE operation is canceled by setting WP "HIGH".(See Fig-10(b))

○In the case of setting WP "HIGH" during t_{WR}, WRITE operation is stopped in the middle and the data of accessing address is not guaranteed. Please write correct data again in the case.

◇DEVICE OPERATION

○START CONDITION (RECOGNITION OF START BIT)

・All commands are proceeded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH.

・The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

(See Fig-8 SYNCHRONOUS DATA TIMING)

○STOP CONDITION (RECOGNITION OF STOP BIT)

・All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH.

(See Fig-8 SYNCHRONOUS DATA TIMING)

○NOTICE ABOUT WRITE COMMAND

・In the case that stop condition is not excuted in WRITE mode, transfered data will not be written in a memory

○DEVICE ADDRESSING

・Following a START condition, the master output the device address to be accessed. The most significant four bits of the slave address are the "device type indentifier," For the device this is fixed as "1010."
(In access to WP resister, this code use "0110".)

・The next three bit (device address) identify the specified device on the bus. The device address is defined by the state of A0,A1 and A2 input pins. This IC works only when the device address inputted from SDA pin correspond to the state of A0, A1 and A2 input pins. Using this address scheme, up to eight devices may be connected to the bus. The last bit of the stream (R/$\overline{W}$···READ/$\overline{WRITE}$) determines the operation to the performed.

R/$\overline{W}$=0	WRITE (including word address input of Random Read)
R/$\overline{W}$=1	READ

Device Type	Device Address				
1 0 1 0	A2	A1	A0	R/$\overline{W}$	Access to Memory
0 1 1 0	A2	A1	A0	R/$\overline{W}$	Access to Write Protect Resister

○WRITE PROTECT COMMAND

・Write Protect Command is to cancel any write command which access to the address 00～7Fh.
Write Protect Resister can be written for once.(Onetime Rom)
Once this command is excuted, the data is protected forever.

○WRITE PROTECT PIN(WP)

・When WP pin set to Vcc (H level), write protect is set for 256words (all address).
When WP pin set to GND (L level), it is enable to write 256words (all address).
If permanent protection is done by Write Protect command, lower half area (00～7Fh address) is inhibited writing regardless of WP pin state.
WP pin has a Pull-Down resister. Please be left unconnected or connect to GND when WP feature is not in use.

○ACKNOWLEDGE

- Acknowledge is a software convention used to indicate successful data transfers. The transmitter device will release the bus after transmitting eight bits. (When inputting the slave address in the write or read operation, transmitter is μ-COM. When outputting the data in the read operation, it is this device.)
- During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that the eight bits of data has been received. (When inputting the slave address in the write or read operation, receiver is this device. When outputting the data in the read operation, it is μ-COM.)
- The device will respond with an Acknowledge after recognition of a START condition and its slave address (8bit).
- In the WRITE mode, the device will respond with an Acknowledge, after the receipt o feach subsequent 8-bit word (word address and write data).
- In the READ mode, the device will transmit eight bit of data, release the SDA line, and monitor the line for an Acknowledge.
- If an Acknowledge is detected, and no STOP condition is generated by the master, the device will continue to transmit the data. If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode. (See Fig-11 ACKNOWLEDGE RESPONSE FROM RECEIVER)

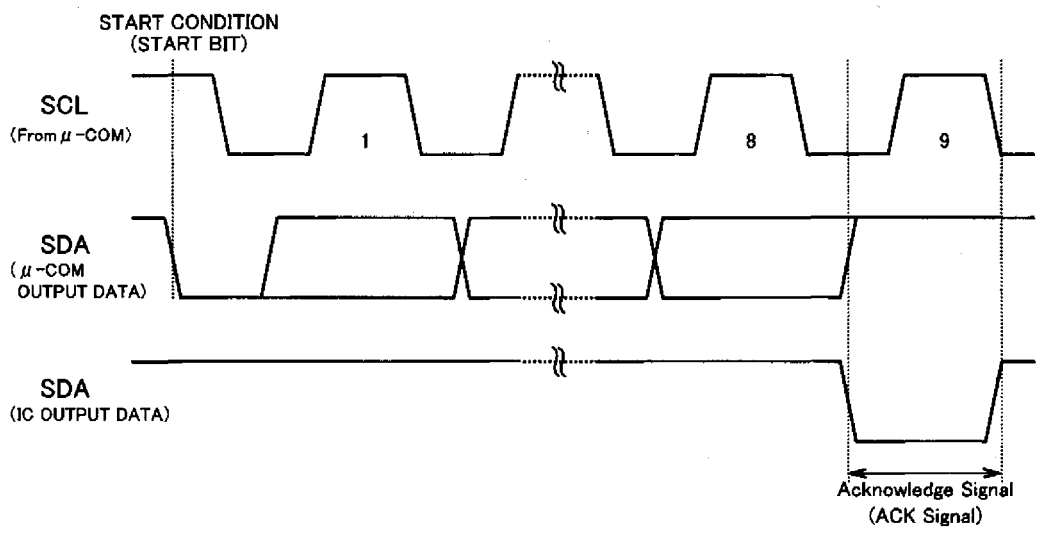


Fig.-11 ACKNOWLEDGE RESPONSE FROM RECEIVER

◇BYTE WRITE

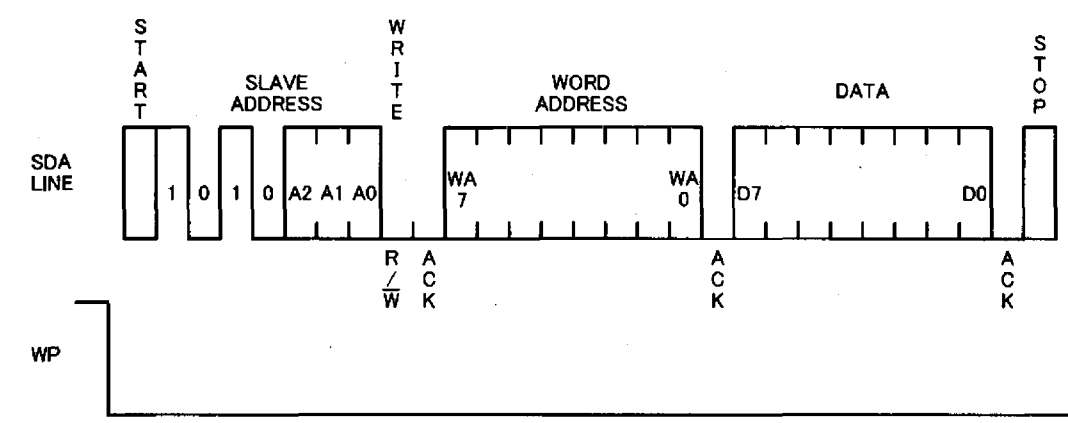


Fig.-12 BYTE WRITE CYCLE TIMING

○By using this command, the data is programed into the indicated word address.
○When the master generates a STOP condition, the device begins the internal write cycle to the nonvolatile memory array.

◇ PAGE WRITE

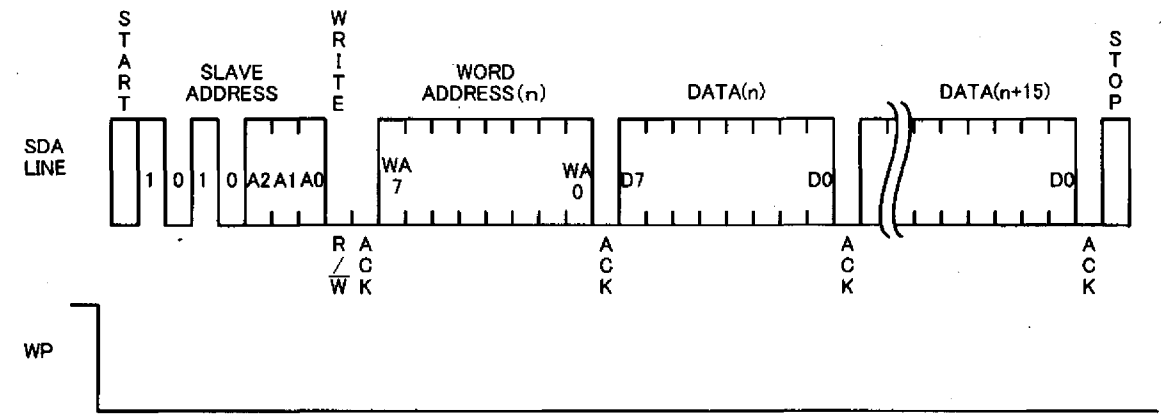


Fig.-13 PAGE WRITE CYCLE TIMING

○ This device is capable of sixteen byte Page Write operation.
○ When two or more byte data are inputted, the four low order address bits are internally incremented by one after the receipt of each word. The four higher order bits of the address(WA7～WA4) remain constant.
○If the master transmits more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previous transmitted data will be overwritten.

◇CURRENT READ

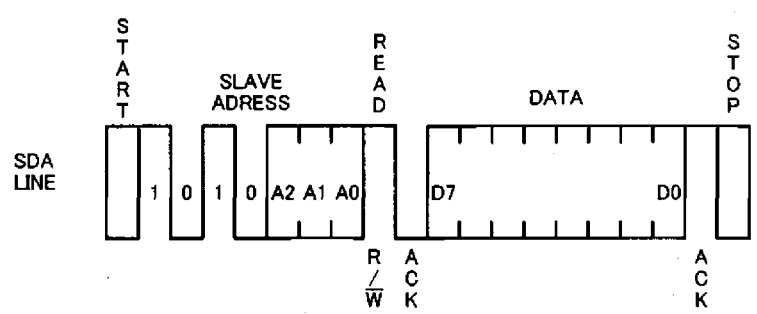


Fig.-14 CURRENT READ CYCLE TIMING

○In case that the previous operation is Random or Current Read (which includes Sequential Read respectively), the internal address counter is increased by one from the last accessed address (n). Thus Current Read outputs the data of the next word address (n+1).
If the last command is Byte or Page Write, the internal address counter stays at the last address (n). Thus Current Read outputs the data of the word address (n).

○If an Acknowledge is detected, and no STOP condition is generated by the master (μ-COM), the device will continue to transmit the data. [It can transmit all data (2kbit 256word)]

○If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition befere returning to the standby mode.

NOTE) If an Acknowledge is detected with "Low" level, not "High" level, command will become Sequential Read. So the device transmits the next data, Read is not terminated. In the case of terminating Read, input Acknowledge with "High" always, then input stop condition.

◇RANDOM READ

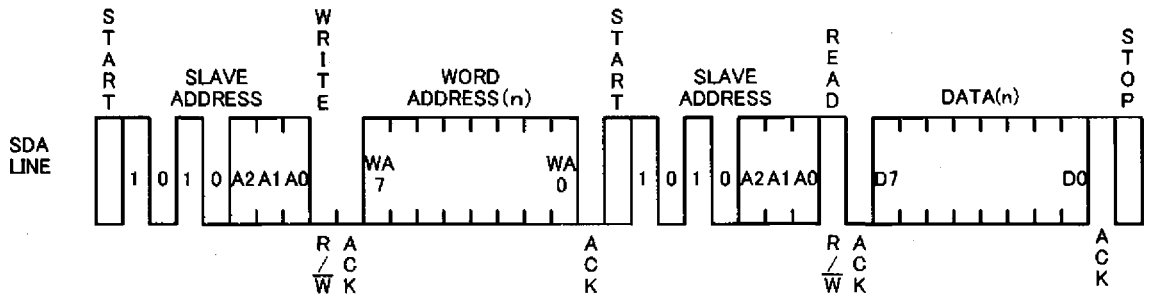


Fig.-15 RANDOM READ CYCLE TIMING

○Random Read operation allows the master to access any memory location indicated word address.

○If an Acknowledge is detected, and no STOP condition is generated by the master (μ-COM),the device will continue to transmit the data. [It can transmit all data (2kbit 256word)]

○If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition befere returning to the standby mode.

NOTE) If an Acknowledge is detected with "Low" level, not "High" level, command will become Sequential Read. So the device transmits the next data, Read is not terminated. In the Case of terminating Read, input Acknowledge with "High" always, then input stop condition.

◇SEQENTIAL READ

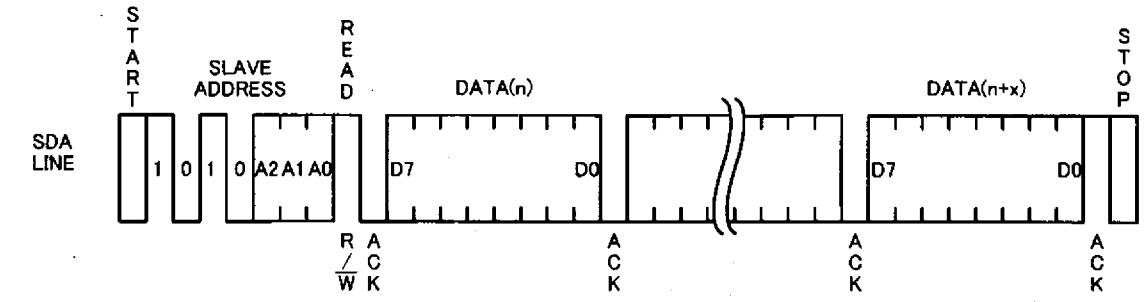


Fig.-16 SEQUENTIAL READ CYCLE TIMING
(Current Read)

○If an Acknowledge is detected, and no STOP condition is generated by the master (μ-COM), the device will continue to transmit the data. [It can transmit all data (2kbit 256word)]
○If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode.
○The Sequential Read operation can be performed with both Current Read and Random Read.

NOTE) If an Acknowledge is detected with "Low" level, not "High" level, command will become Sequential Read. So the device transmits the next data, Read is not terminated. In the case of terminating Read, input Acknowledge with "High" always, then input stop condition.

◇WRITE PROTECT

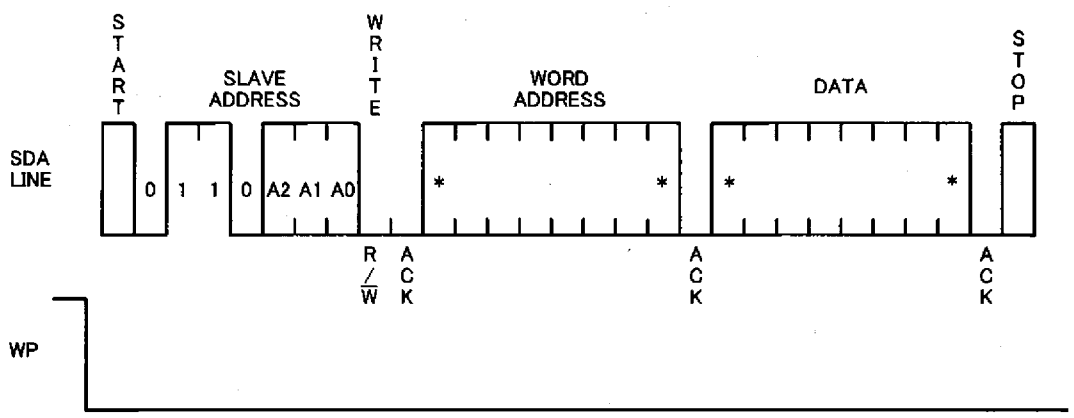


Fig-17 WRITE PROTECT CYCLE TIMING

○Using this command, writing is inhibited in lower half area. (00h～7Fh address) If Write Protect Command is excuted, cannot cancel the protection permanently. (Onetime Rom)
○This Command is cancelled, if Write Protect Command is already excuted.
○During this command, please be left WP unconnected or connect WP to GND.
○This command need the period of t_{WR} after stop condition just like Byte or Page Write command. During the t_{WR}, next command is ignored.

◇APPLICATION

1) WP EFFECTIVE TIMING

WP is fixed to "H" or "L" usually . But in case of controlling WP to cancel the write command, please pay attention to 「WP effective timing」 as follows.

During write command input , write command is canceled by controlling WP "H" within the WP cancellation effective period.

The period from the start condition to the rising edge of the clock which take in DO of the data (the first byte of the data for Page Write) is the cancellation invalid period. WP input is don't care during the period. Setup time for rising edge of the SCL which takes in DO must be more than 100ns.

The period from the rising edge of SCL which takes in DO to the end of internal write cycle (tWR) is the cancellation effective period. In case of setting WP to "H" during tWR, WRITE operation is stopped in the middle and the data of accessing address is not guaranteed, so that write correct data again please.

It is not necessary waiting tWR (5msmax.) after stopping command by WP, because the device is stand by state.

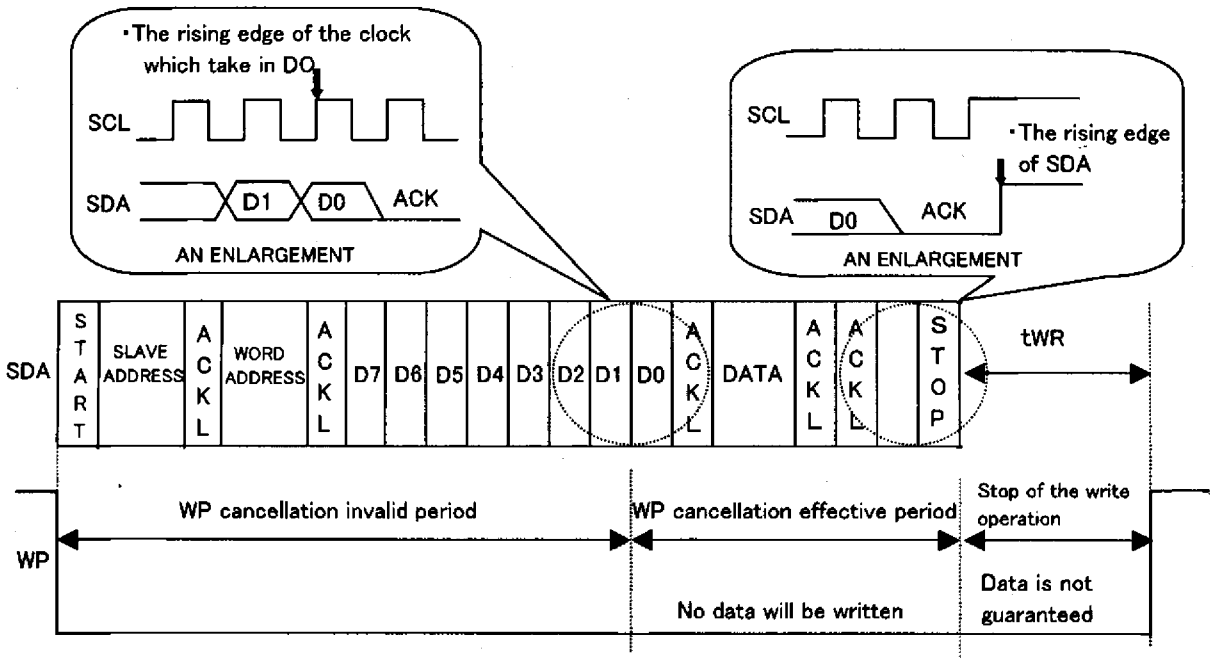


Fig1. WP EFFECTIVE TIMING

2)SOFTWARE RESET

Please execute software reset in case that the device is an unexpected state after power up and/or the command input need to be reset.

There are some kinds of software reset. Here we show three types of example as follows.

During dummy clock, please release SDA bus (tied to Vcc by pull up resistor) .

During that time, the device may pull the SDA line LOW for acknowledge or outputting or read data.

If the master controls the SDA line HIGH, it will conflict with the device output LOW then it makes a current overload. It may cause instantaneous power down and may damage the device.

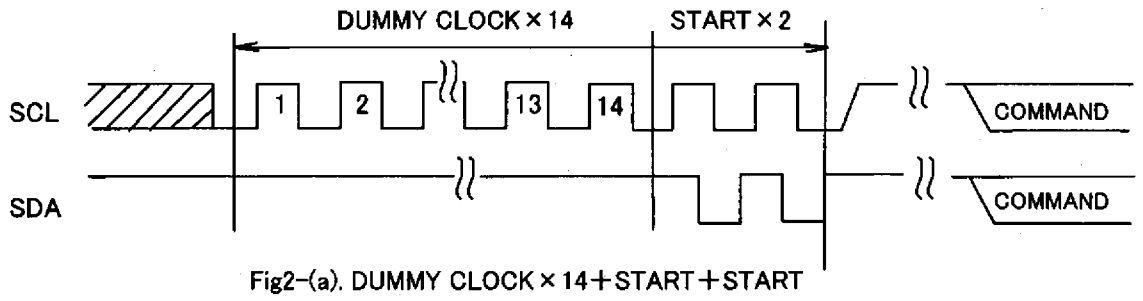


Fig2-(a). DUMMY CLOCK × 14+START+START

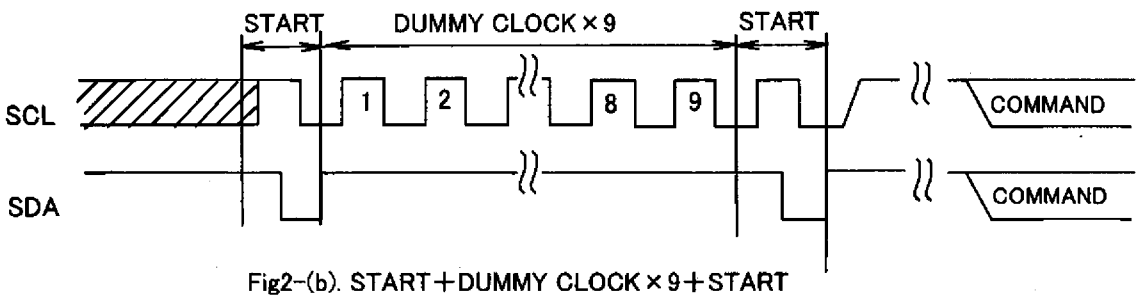


Fig2-(b). START+DUMMY CLOCK × 9+START

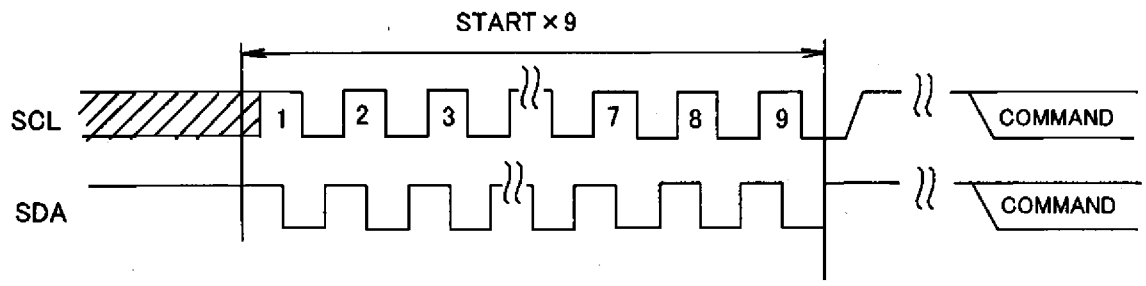


Fig2-(c). START × 9

※COMMAND starts with start condition.

3)ACKNOWLEDGE POLLING

Since the device ignore all input commands during the internal write cycle, no ACK will be returned. When the master send the next command after the write command, if the device returns the ACK, it means that the program is completed. If no ACK is returned, it means that the device is still busy.

By using Acknowledge polling, the waiting time is minimized less than t_{WR}=5ms.

In case of operating Write or Current Read right after Write, first, send the slave address (R/$\overline{W}$ is "HIGH" or "LOW" respectively). After the device returns the ACK, continue word address input or data output respectively.

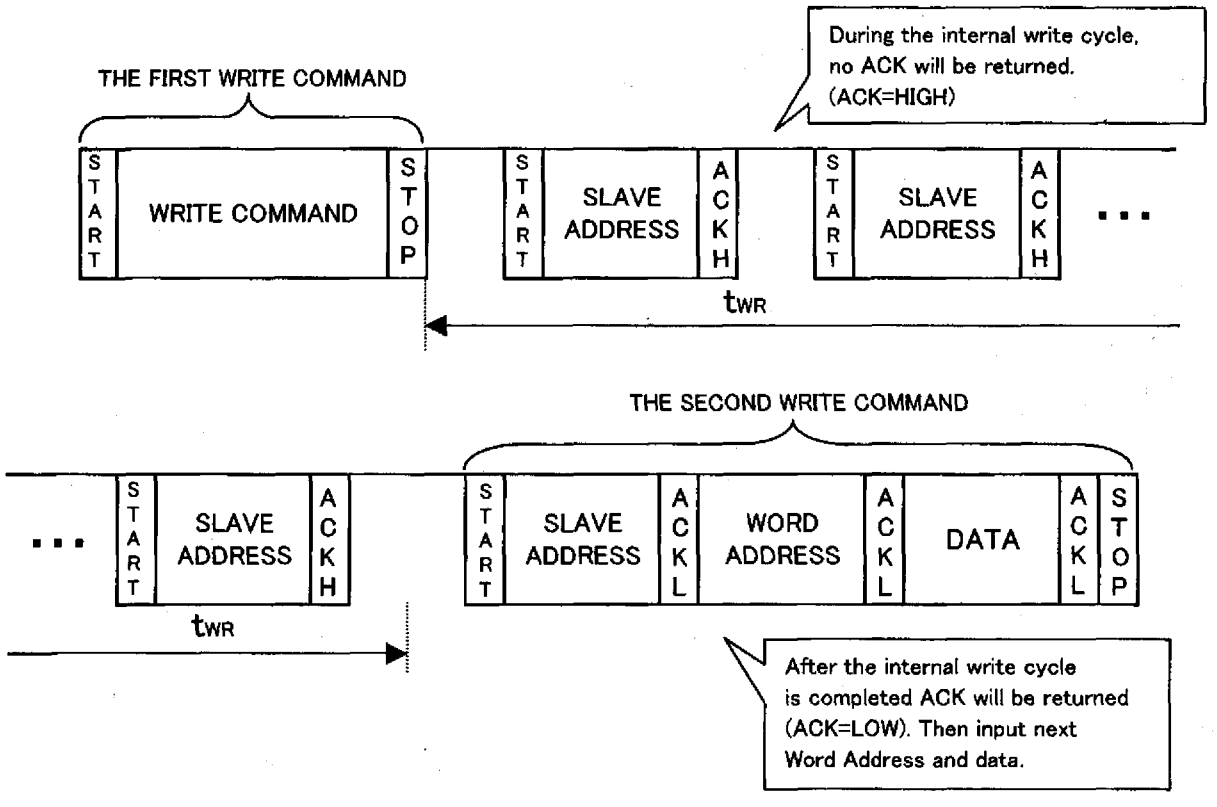


Fig3. SUCCESSIVE WRITE OPERATION BY ACKNOWLEDGE POLLING

4)COMMAND CANCELLATION BY START AND STOP CONDITION

During a command input, it is canceled by the successive inputs of start condition and stop condition.(Fig4)

But during ACK or data output, the device may output the SDA line LOW. In such cases, operation of start and stop condition is impossible, so that the reset can't work. Execute the software reset in the cases. (See Page2)

Operating the command cancel by start and stop condition during the command of Random Read or Sequential Read or Current Read, internal address counter is not confirmed.

Therefore operation of Current Read after this is not valid. Operate a Random Read in this case.

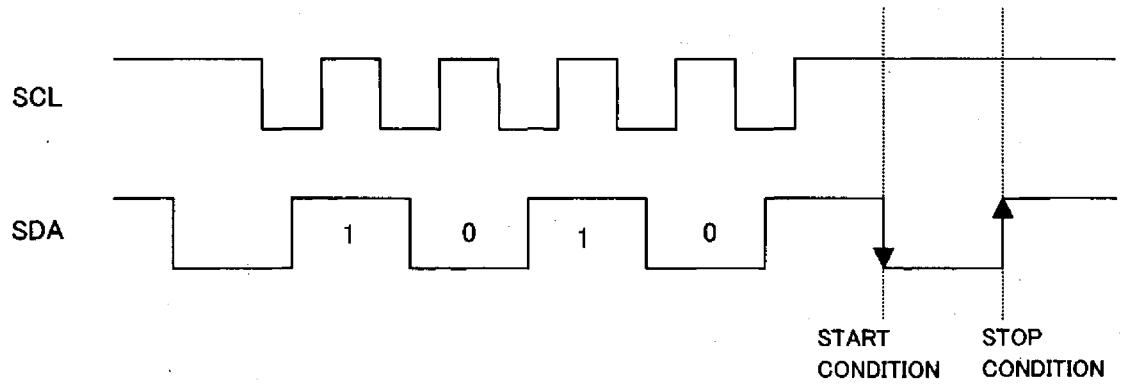


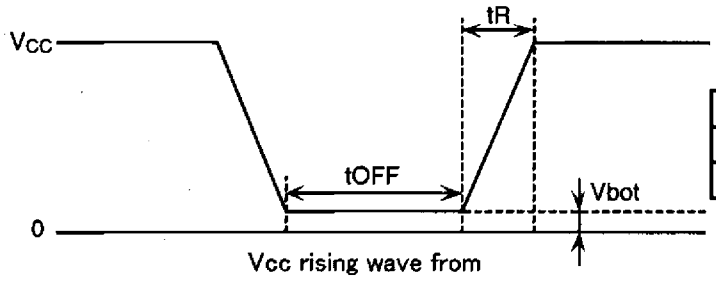
Fig4. COMMAND CANCELLATION BY START AND STOP CONDITION DURING THE INPUT OF SLAVE ADDRESS

5)NOTES FOR POWER SUPPLY

Vcc rises through the low voltage region in which internal circuit of IC and the controller are unstable, so that device may not work properly due to an incomplete reset of internal circuit.
To prevent this, the device has the feature of P.O.R. and LVCC.
In the case of power up, keep the following conditions to ensure functions of P.O.R and LVCC.

1. It is necessary to be "SDA='H'" and "SCL='L' or 'H'".

2. Follow the recommended conditions of tR, tOFF, Vbot for the function of P.O.R. during power up.



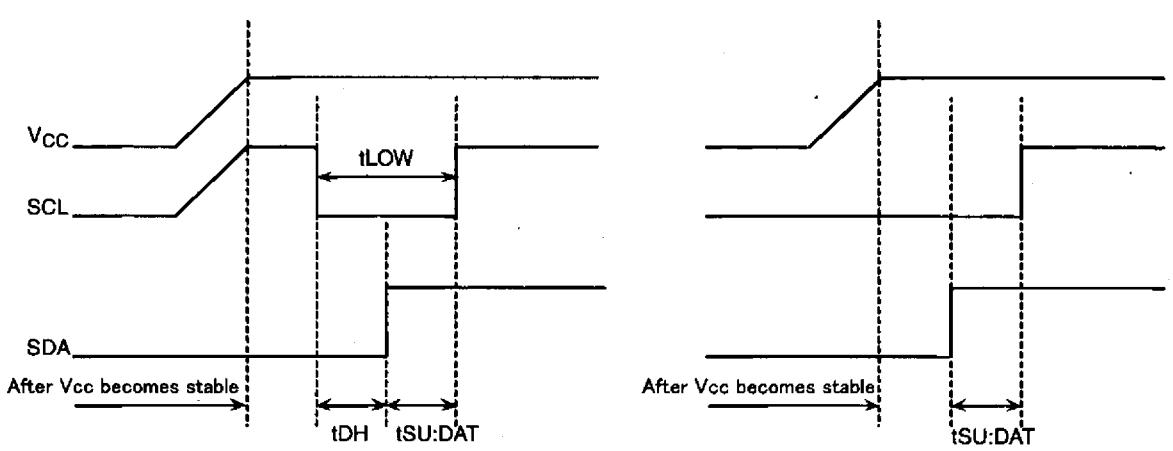
Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

3. Prevent SDA and SCL from being "Hi-Z".

In case that condition 1. and/or 2. cannot be met, take following actions.

A) Unable to keep condition 1.(SDA is "LOW" during power up.)
→Control SDA ,SCL to be "HIGH" as figure below.



a) SCL='H' and SDA='L'

b) SCL='L' and SDA='L'

B) Unable to keep condition 2.
→After power becomes stable, execute software reset. (See page 2)

C) Unable to keep both conditions 1 and 2.
→Follow the instruction A first, then the instruction B.

○LVCC CIRCUIT

LVCC circuit inhibit write operation at low voltage, and prevent an inadvertent write. Below the LVCC voltage(Typ.=1.2V), write operation is inhibited.

6) I/O CIRCUIT

○PULL UP RESISTER OF SDA PIN

The pull up resister is needed because SDA is NMOS open drain. Decide the value of this resister (Rpu) properly, by considering V_{IL}, I_L characteristics of a controller which control the device and V_{OH}, I_{OL} characteristics of the device. If large R_{PU} is chosen, clock frequency need to be slow. In case of small R_{PU}, the operating current increases.

○MAXIMUM OF R_{PU}

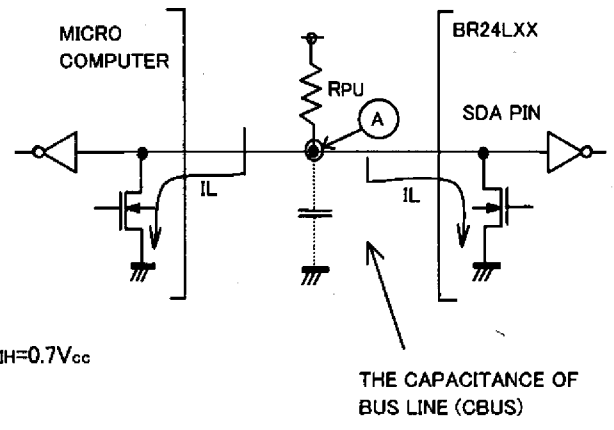
Maximum of R_{PU} is determined by following factor.

①SDA rise time determined by R_{PU} and the capacitance of bus line(CBUS) must be less than T_R. And the other timing must keep the conditions of AC spec.

②When SDA bus is HIGH, the voltage Ⓐ of SDA bus determined by a total input leak(I_L) of the all devices connected to the bus and R_{PU} must be enough higher than input HIGH level of a controller and the device, including noise margin 0.2Vcc.

$$V_{cc} - I_L R_{PU} - 0.2V_{cc} \geqq V_{IH}$$

$$\therefore\ R_{PU} \leqq \frac{0.8V_{cc} - V_{IH}}{I_L}$$



Examples: When V_{cc}=3V I_L=10μA V_{IH}=0.7V_{cc}

According to ②

$$R_{PU} \leqq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

○THE MINIMUM VALUE RPU

The minimum value of R_{PU} is determined by following factors.

①Meet the condition that V_{OLMAX}=0.4V, I_{OLMAX}=3mA when the device output low on SDA line.

$$\frac{V_{CC}-V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{V_{CC}-V_{OL}}{I_{OL}}$$

②V_{OLMAX}(=0.4V) must be lower than the input LOW level of the controller and the EEPROM including recommended noise margin(0.1Vcc).

$$V_{OLMAX} \leqq V_{IL} - 0.1V_{CC}$$

Examples: Vcc=3V, V_{OL}=0.4V, I_{OL}=3mA, the V_{IL} of the controller and the EEPROM is V_{IL}=0.3Vcc、

According to ①

$$R_{PU} \geqq \frac{3-0.4}{3\times10^{-3}}$$

$$\geqq 867\ [\Omega]$$

and

V_{OL}=0.4[V]

V_{IL} =0.3×3

=0.9[V]

so that condition② is met

○PULL UP RESISTER OF SCL PIN

In the case that SCL is controlled by CMOS output, the pull up resister of SCL is not needed. But in the case that there is a timing at which SCL is Hi-Z, connect SCL to Vcc with pull up resister. Several ～ several dozen kΩ is recommended as a pull up resister, which is considered with the driving ability of the output port of the controller.

7)CONNECTIONS OF A0, A1, A2, WP PIN

○CONNECTIONS OF DEVICE ADDRESS PIN(A0, A1, A2)

The state of device address PIN are compared with the device address send by the master, then one of the devices which are connected to the identical bus is selected. Pull up or down these pins, or connect them to Vcc or GND.

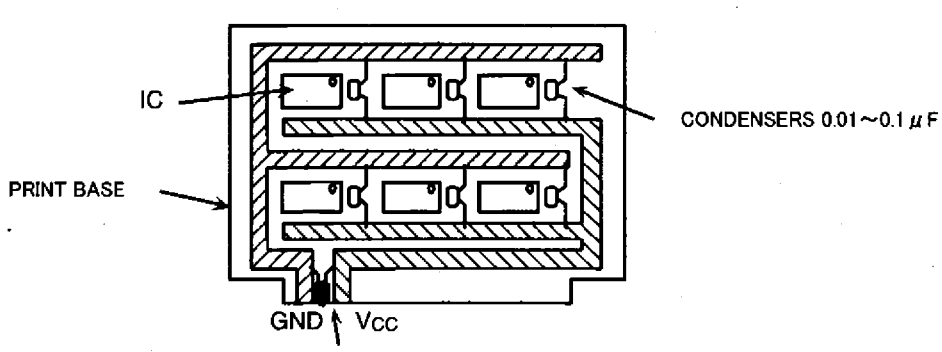
○CONNECTIONS OF WP PIN

The WP input allows or inhibits write operations. When WP is HIGH, only READ is available and WRITE to any address is inhibited. Both Read and Write are available when WP is LOW.
In the case that the device is used as a ROM, it is recommended that WP is pulled up or connected to Vcc. In the case that both READ and WRITE are operated, WP pin must be pulled down or connected to GND, controlled, or be left unconnected. (WP has a pull down resister. So it is allowed to be left unconnect)

8) NOTES FOR NOISE ON Vcc

○ABOUT BYPASS CONDENSER

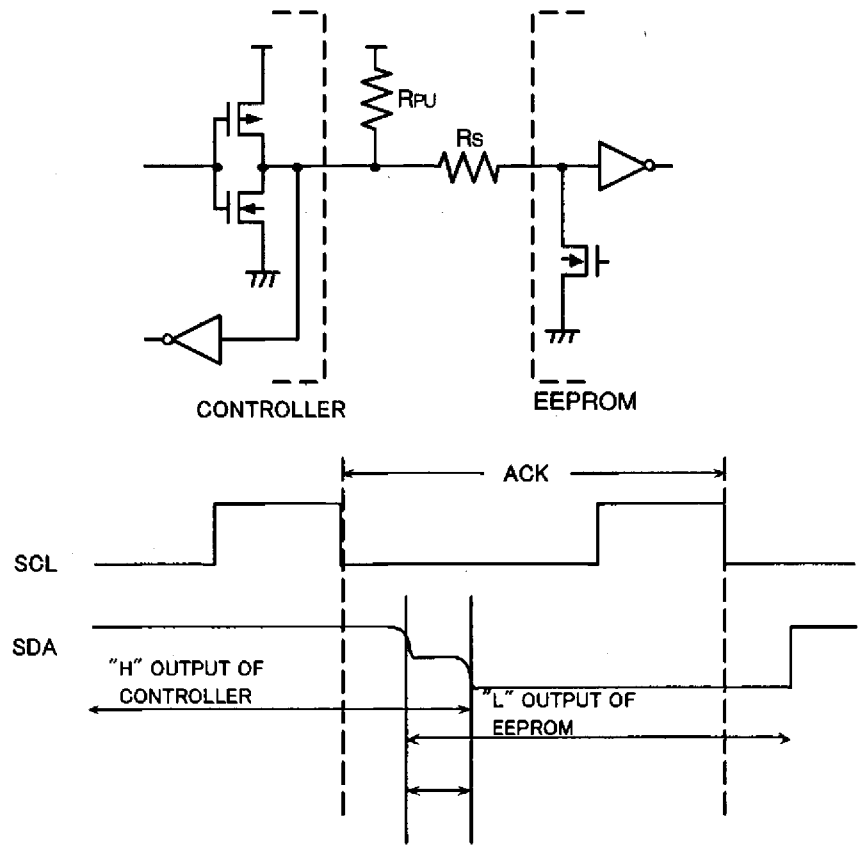
Noise and surges on power line may cause the abnormal function. It is recommended that the bypass condensers(0.1 μF) are attached on the Vcc and GND line beside the device. The attachment of bypass condensers on the board near by connector is also recommended.



9) THE NOTICE ABOUT THE CONNECTION OF CONTROLLER

○ABOUT RS

The open drain interface is recommended for SDA port in I²CBUS. But, in the case that Tri-state CMOS interface is applied to SDA, insert a series resister Rs between SDA pin of the device and a pull up resister RPU. It limits the current from PMOS of controller to NMOS of EEPROM.
Rs also protects SDA pin from surges. therefore, Rs is able to be used though SDA port is open drain.



The "H" output of controller and the "L" output of EEPROM may cause current overload to SDA line.

○THE MAXIMUM VALUE OF Rs

The maximum value of Rs is determined by following factors.

①SDA rise time determined by R_{PU} and the capacitance of bus line(CBUS) of SDA must be less than t_R. And the other timing must also keep the conditions of the AC timing.

②When the device outputs LOW on SDA line, the voltage of the bus Ⓐ determined by R_{PU} and Rs must be lower than the inputs LOW level of the controller, including recommended noise margin(0.1Vcc).

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

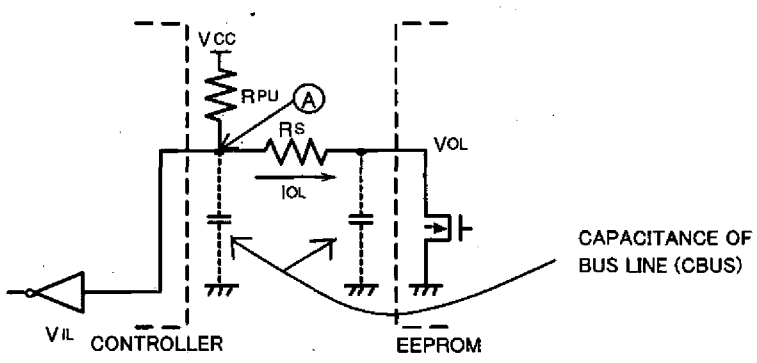
$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Examples: When Vcc=3V, V_{IL}=0.3Vcc, V_{OL}=0.4V, R_{PU}=20kΩ

According to②

$$R_S \leqq \frac{0.3\times 3-0.4-0.1\times 3}{1.1\times 3-0.3\times 3} \times 20\times 10^3$$

$$\leqq 1.67[k\Omega]$$

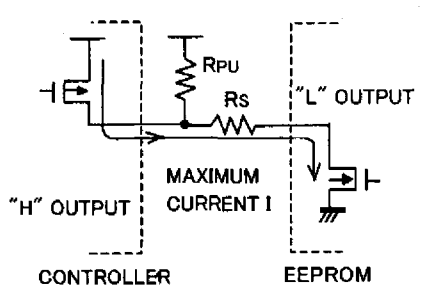


○THE MINIMUM VALUE OF Rs

The minimum value of Rs is determined by the current overload due to the conflict on the bus.
The current overload may cause noises on the power line and instantaneous power down.
The following conditions must be met, where I is the maximum permissible current.
The maximum permissible current depends on Vcc line impedance and so on. It need to be less than 10mA for EEPROM.

$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{V_{CC}}{I}$$



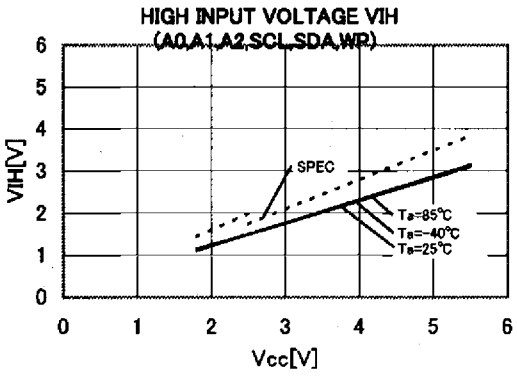
Examples: When Vcc=3V、I=10mA

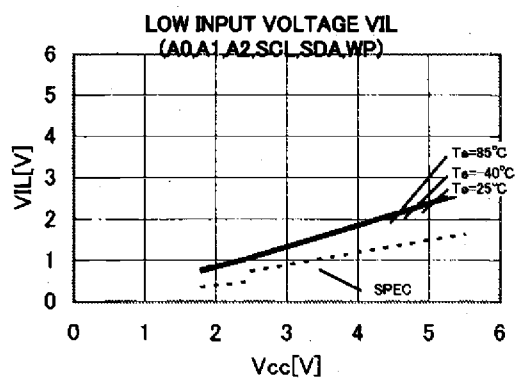
$$R_S \geqq \frac{3}{10\times 10^{-3}}$$

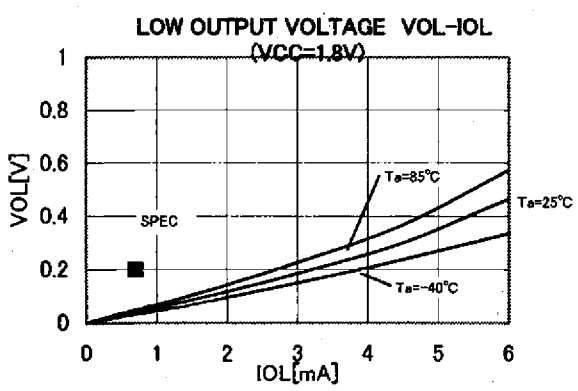
$$\geqq 300[\Omega]$$

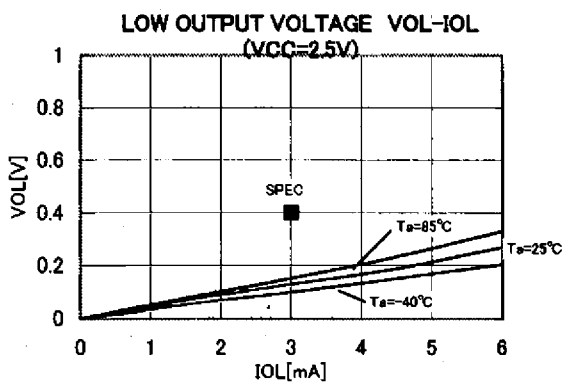
10) THE SPECIAL CHARACTER DATA

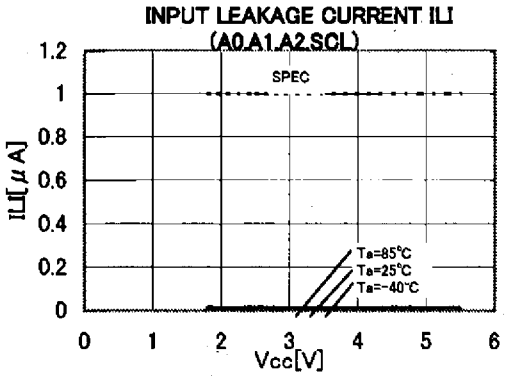
The following characteristic data are typ value.

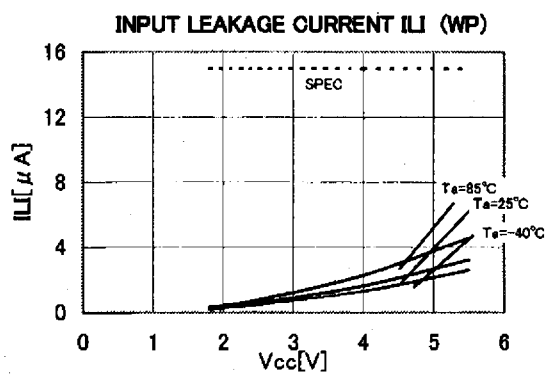


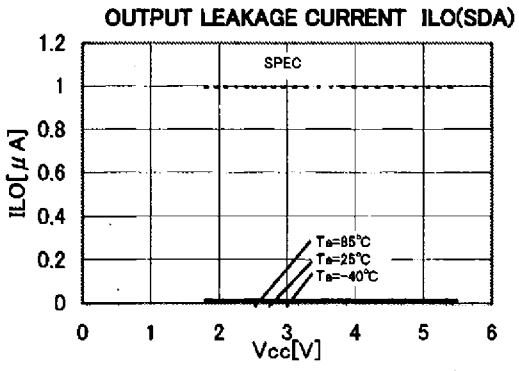


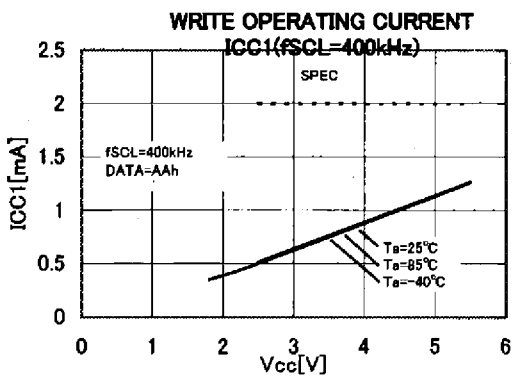


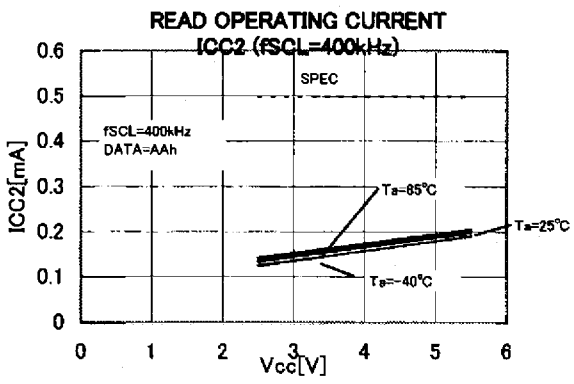


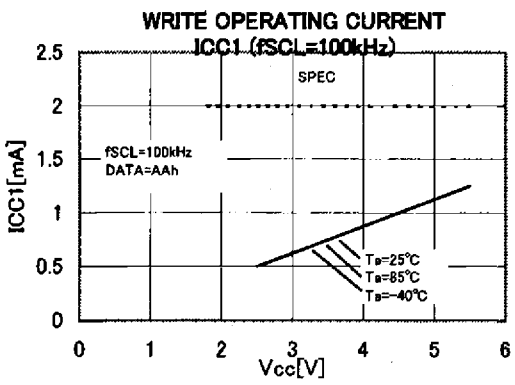


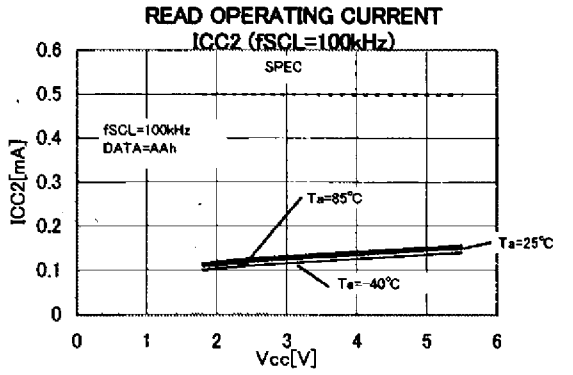


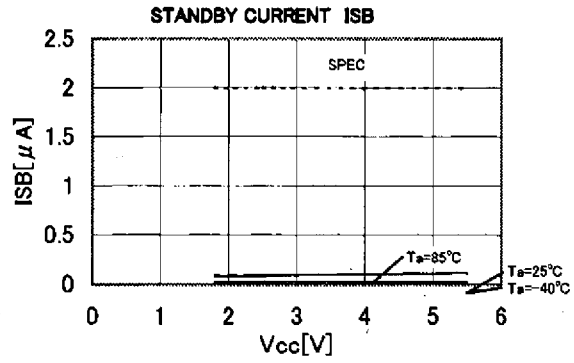


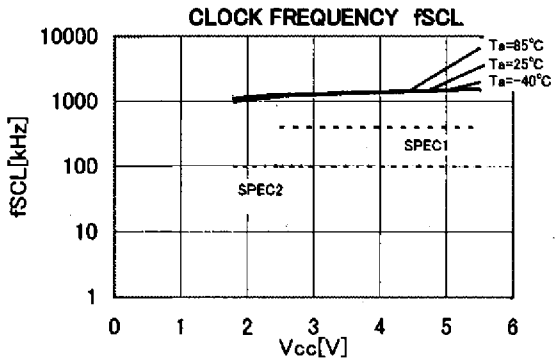






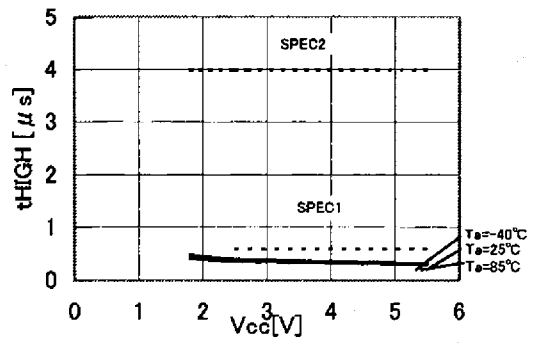




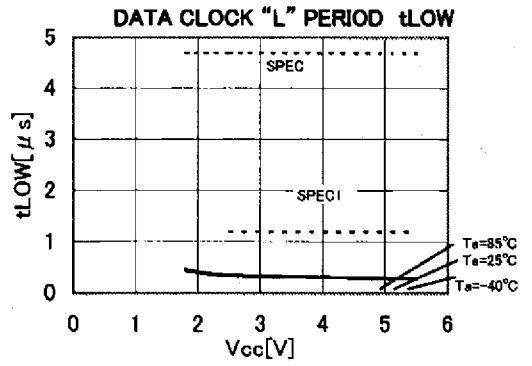


※SPEC1=FAST-MODE
※SPEC2=STANDARD-MODE

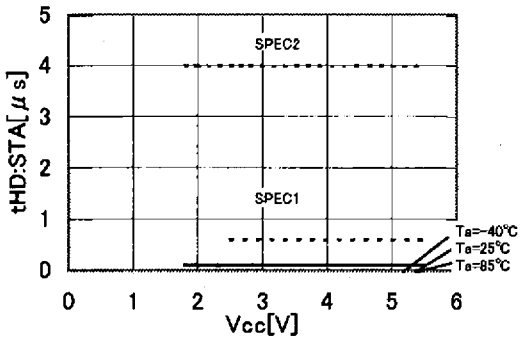
DATA CLOCK "H" PERIOD tHIGH



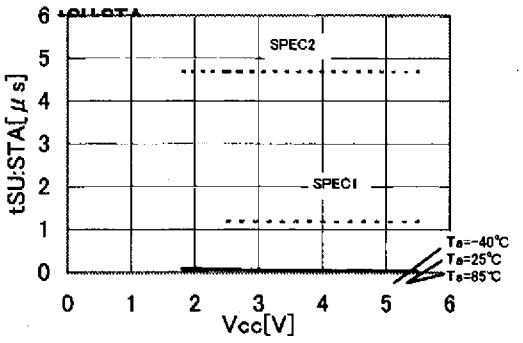
DATA CLOCK "L" PERIOD tLOW



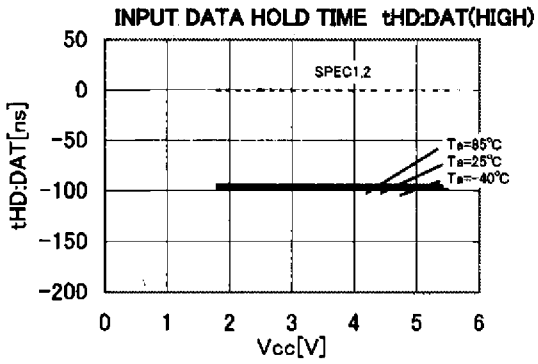
START CONDITION HOLD TIME tHD:STA



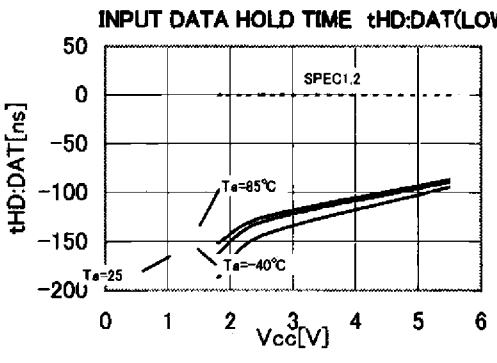
START CONDITION SETUP TIME



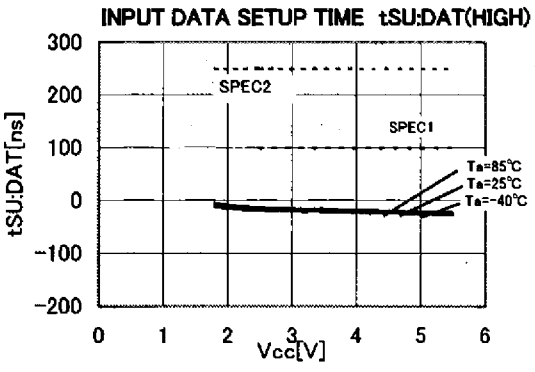
INPUT DATA HOLD TIME tHD:DAT(HIGH)



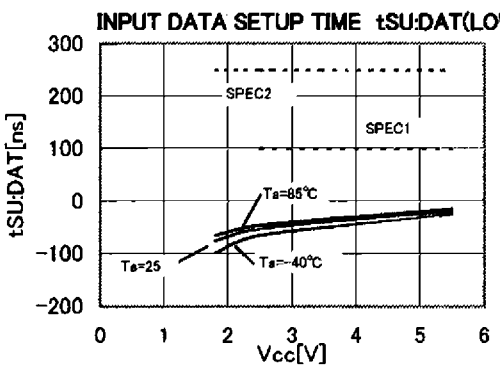
INPUT DATA HOLD TIME tHD:DAT(LOW)



INPUT DATA SETUP TIME tSU:DAT(HIGH)

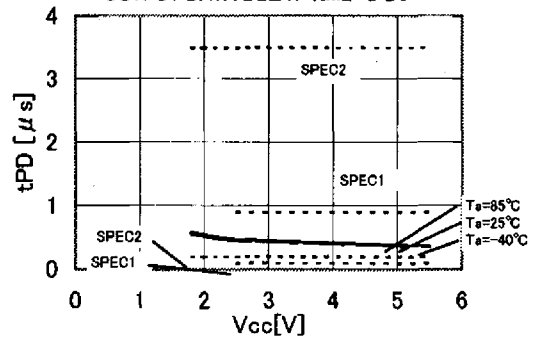


INPUT DATA SETUP TIME tSU:DAT(LOW)

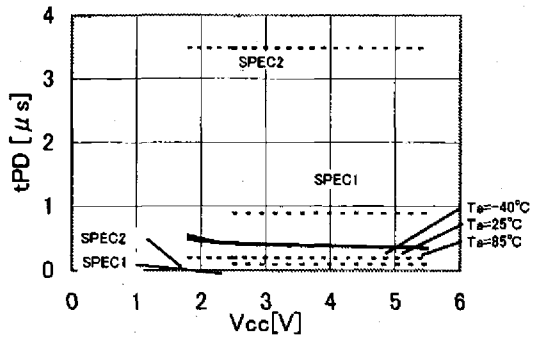


※SPEC1=FAST-MODE
※SPEC2=STANDARD-MODE

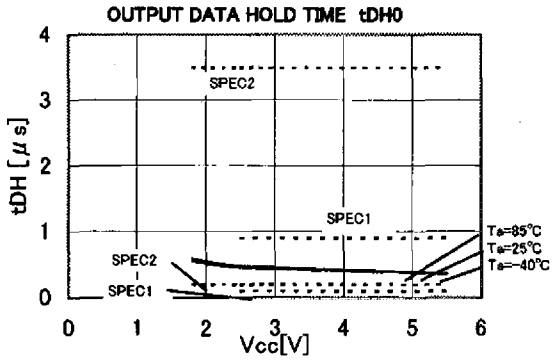
OUTPUT DATA DELAY TIME tPD0



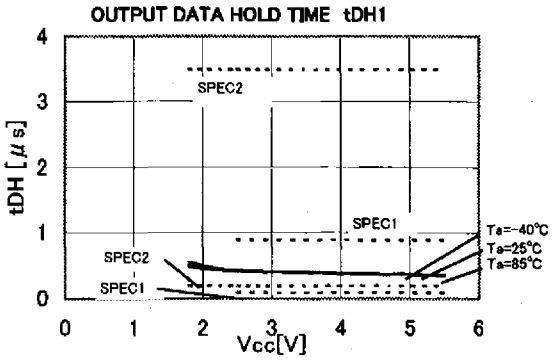
OUTPUT DATA DELAY TIME tPD1



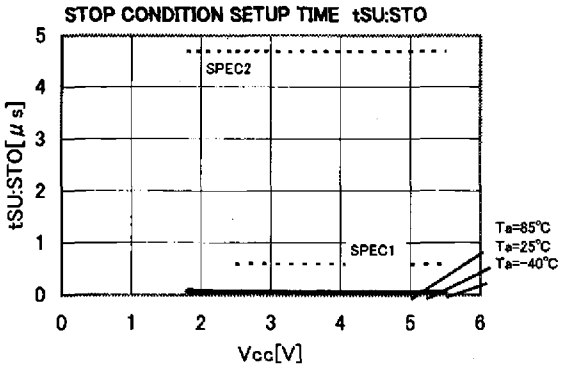
OUTPUT DATA HOLD TIME tDH0



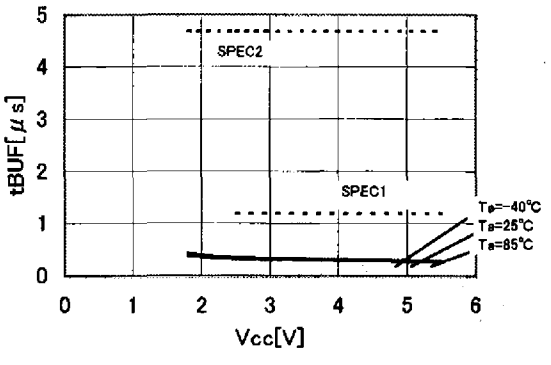
OUTPUT DATA HOLD TIME tDH1



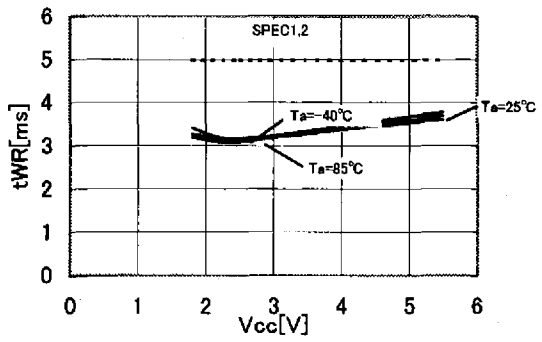
STOP CONDITION SETUP TIME tSU:STO



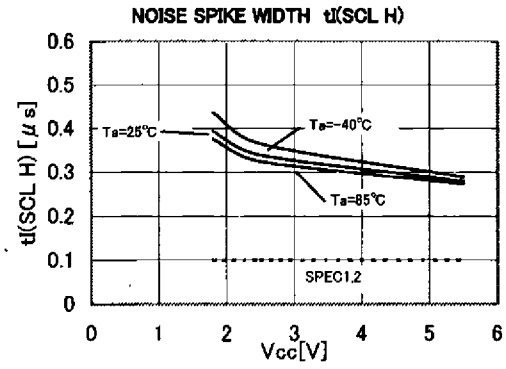
BUS FREE TIME tBUF

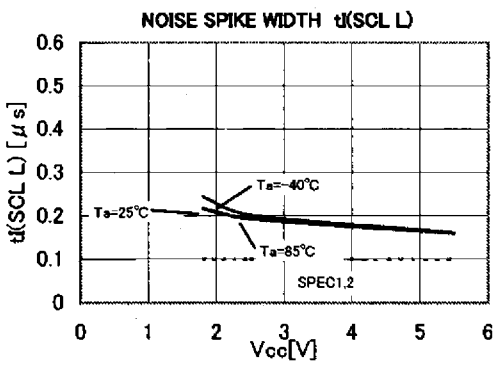


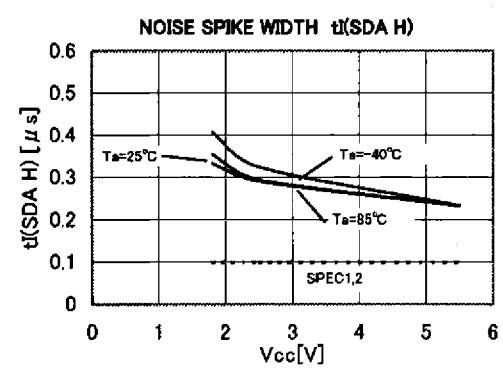
WRITE CYCLE TIME tWR

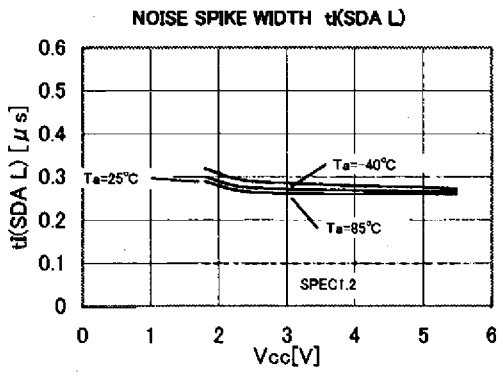


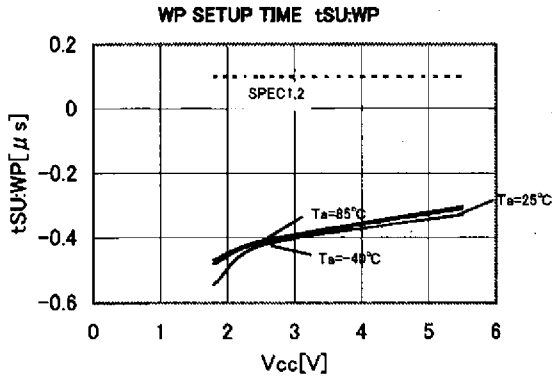
※SPEC1=FAST-MODE
※SPEC2=STANDARD-MODE

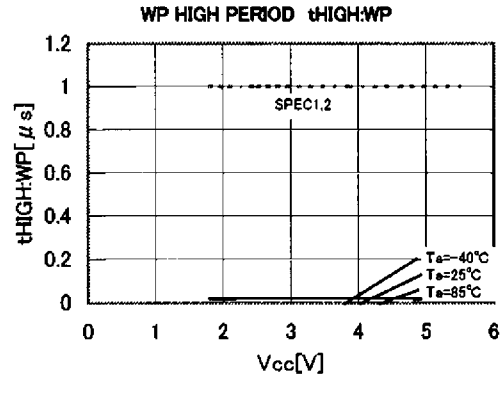












※SPEC1=FAST-MODE
※SPEC2=STANDARD-MODE