PLL frequency synthesizer for tuners
BU2621F

The BU2621F is a PLL frequency synthesizer designed for use in car stereos, high-fidelity audio systems, and CD radio cassettes. Featuring low power consumption, low superfluous radiation, and two separate frequency measurement counter systems, this chip is ideal for high-performance systems.

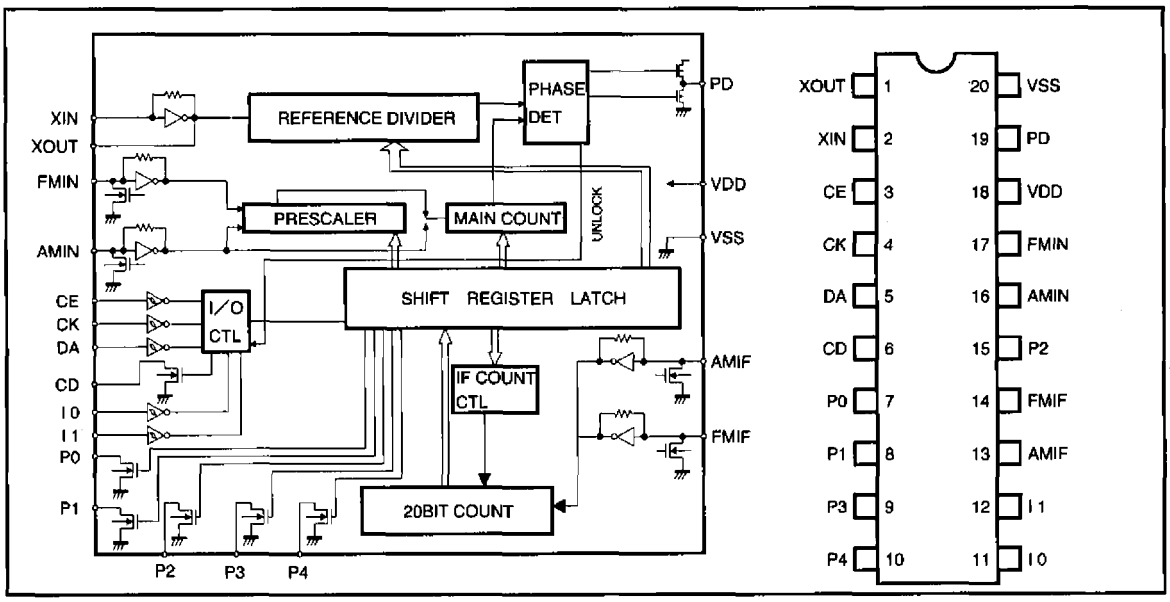
●Applications

Car stereos, mini components, radio cassettes, receivers, and other frequency generating devices

●Features

1) Built-in high-speed prescaler can divide 130MHz VCO.
2) Low power-consumption (during operation : 6mA PLL OFF 300 μA Typ.)
3) Seven standard frequencies : 50kHz, 25kHz, 12.5kHz, 10kHz, 9kHz, 5kHz, and 1kHz.
4) Two counter systems for intermediate frequency detection.
5) Unlock detection circuit.
6) Five output ports.
7) Two input ports.
8) Serial data input (CE.CK.DA)
9) Phase comparison output.

●Block diagram



●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit	Conditions
Supply voltage	V_{DD}	−0.3~7.0	V	VDD
Maximum input voltage 1	V_{IN1}	−0.3~7.0	V	CE, CK, DA, I_0, I_1
Maximum input voltage 2	V_{IN2}	−0.3~V_{DD}+0.3	V	XIN, FMIN, AMIN, FMIF, AMIF, I_0, I_1
Maximum output voltage 1	V_{OUT1}	−0.3~10.0	V	P_0,P_1,P_2,P_3,P_4,CD
Maximum output voltage 2	V_{OUT2}	−0.3~V_{DD}+0.3	V	PD,XOUT
Maximum output current	I_{OUT}	0~4.0	mA	P_0,P_1,P_2,P_3,P_4,CD
Power dissipation	Pd	＊450	mW	
Operating temperature	Topr	−40~85	℃	
Storage temperature	Tstg	−55~125	℃	

＊ Reduced by 4.5mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.0	—	6.0	V

●Pin description

Pin No.	Symbol	Pin name	Function	I/O
1	XOUT	Crystal oscillation terminal	For generation of standard frequency and internal clock.	OUT
2	XIN		Connected to 7.2 MHz crystal oscillator.	IN
3	CE	Chip enable	When CE is H, DA is synchronous with the rise of CK and read to the internal shift register. DA is then latched at the timing of the fall of CE. Also, output data is output from the CD terminal synchronous to the rise of CK.	IN
4	CK	Clock signal		
5	DA	Serial data		
6	CD	Count data	Frequency data and unlock data are output.	Nch open drain
7	PO	Output port	Controlled on the basis of input data.	
8	P1			
9	P3			
10	P4			
11	I0	Input port	Selected on the basis of control data, then output to the CD terminal.	IN
12	I1			Schmidt input
13	AMIF	AMIF input	Intermediate frequency input for AM	IN
14	FMIF	FMIF input	Intermediate frequency input for FM	IN
15	P2	Output port	Controlled on the basis of input data.	Nch open drain
16	AMIN	AM input	Local input for AM	IN
17	FMIN	FM input	Local input for FM	IN
18	VDD	Power supply	Power supply, with 4.0V to 6.0V applied voltage.	
19	PD	Phase comparison output	High level when value obtained by dividing local output is higher than standard frequency. Low level when value is lower. High impedance when value is same.	3-state
20	VSS	GROUND		

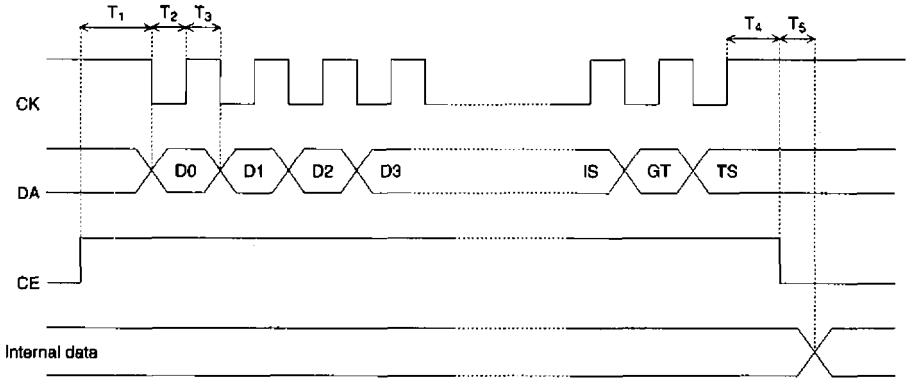
●Electrical characteristics (unless other specified, Ta = 25℃, V_{DD} = 5.0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
Supply current	I_{DD1}	—	6.0	10.0	mA	FM_{IN}=130MHz,100mVrms	
Quiescent circuit current	I_{DD2}	—	0.3	1.0	mA	No input, PLL=OFF	
"H" level input voltage	V_{IH}	0.8V_{DD}	—	—	V	CE,CK,DA,I_0,I_1	
"L" level input voltage	V_{IL}	—	—	0.2V_{DD}	V	CE,CK,DA,I_0,I_1	
"H" level input current 1	I_{IH1}	—	—	1.0	μA	CE,CK,DA,I_0,I_1	V_{IN}=V_{DD}
"H" level input current 2	I_{IH2}	—	0.3	—	μA	XIN	V_{IN}=V_{DD}
"H" level input current 3	I_{IH3}	—	6.0	—	μA	FMIN,AMIN,FMIF,AMIF	V_{IN}=V_{DD}
"L" level input current 1	I_{IL1}	−1.0	—	—	μA	CE,CK,DA,I_0,I_1	V_{IN}=V_{SS}
"L" level input current 2	I_{IL2}	—	−0.3	—	μA	XIN	V_{IN}=V_{SS}
"L" level input current 3	I_{IL3}	—	−6.0	—	μA	FMIN,AMIN,FMIF,AMIF	V_{IN}=V_{SS}
"L" level output voltage 1	V_{OL1}	—	0.2	0.5	V	P_0,P_1,P_2,P_3,P_4,CD	I_0=1.0mA
"OFF" level leak current 1	I_{OFF1}	—	—	1.0	μA	P_0,P_1,P_2,P_3,P_4,CD	V_O=10V
"L" level output voltage 2	V_{OL2}	—	—	0.3	V	FMIN,AMIN,FMIF,AMIF	I_{OUT}=0.1mA
"H" level output voltage	V_{OH}	V_{DD} −1.0	V_{DD} −0.25	—	V	PD	I_{OUT}=−1.0mA
"L" level output voltage	V_{OL4}	—	0.15	1.0	V	PD	I_{OUT}=1.0mA
"OFF" level leak current 2	I_{OFF2}	—	—	100	nA	PD	V_{OUT}=V_{DD}
"OFF" level leak current 3	I_{OFF3}	−100	—	—	nA	PD	V_{OUT}=V_{SS}
Internal feedback resistor 1	R_{F1}	—	10	—	MΩ	XIN	
Internal feedback resistor 2	R_{F2}	—	500	—	kΩ	FMIN,AMIN,FMIF,AMIF	
Input frequency 1	F_{IN1}	—	7.2	—	MHz	XIN,sine wave,C coupling	
Input frequency 2	F_{IN2}	10	—	130	MHz	FMIN,sine wave,C coupling	V_{IN}=50mVrms
Input frequency 3	F_{IN3}	0.5	—	30	MHz	AMIN,sine wave,C coupling	V_{IN}=70mVrms
Input frequency 4	F_{IN4}	0.4	—	16	MHz	FMIF,AMIF,sine wave,C coupling	V_{IN}=70mVrms
Input amplitude 1	V_{IN1}	50	—	1.5	Vrms	FMIN,sine wave,C coupling	
Input amplitude 2	V_{IN2}	70	—	1.5	Vrms	AMIN,FMIF,AMIF,sine wave,C coupling	
Minimum pulse width	TW	—	1.0	—	μs	CK,DA	
Input rise time	TR	—	—	500	ns	CE,CK,DA	
Input fall time	TF	—	—	500	ns	CE,CK,DA	

◎ Not designed for radiation resistance.

●Circuit operation

Input data format



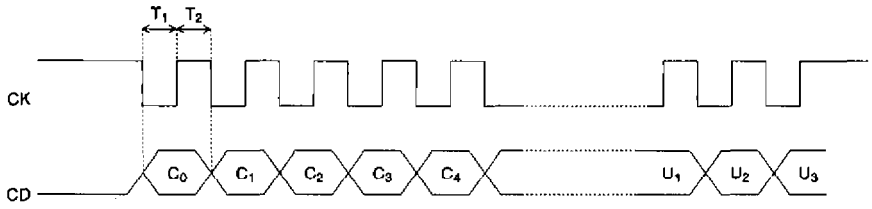
$T_1 \geqq 1.5\,\mu SEC$ $T_2,\ T_3 > 1\,\mu SEC$ $T_4 > 0\,\mu SEC$ $T_5 < 1.5\,\mu SEC$

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

← Input from Do.

P_0	P_1	P_2	P_3	P_4	PH	PL	CT	R_0	R_1	R_2	S	PS	IS	GT	TS

Output data format CE output is set to LO.



Figures for output assume the presence of pullup resistance. $T_1,\ T_2 > 1\,\mu SEC$

Output data format

C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}

← Input done from Co.

C_{16}	C_{17}	C_{18}	C_{19}	U_0	U_1	U_2	U_3

※ Data is output only when CT = 1 or GT = 1.

Explanation of the data

(1) Division data : For D_0 through D_{15} (When S = 1, use D_4 through D_{15}.)

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

Examples:

Divided frequency = 1106 (D)÷2=553 (D)=229(H) S=0

1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0

Divided frequency = 1107 (D) =453 (H) S=1, PS=1

1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0

Divided frequency = 926 (D) =39E (H) S=1, PS=0

×	×	×	×	0	1	1	1	1	0	0	1	1	1	0	0

(2) CT : Frequency measurement beginning data
1 : Begins measurement.
0 : Resets internal counter, FMIF and AMIF go to pulldown.

(3) Output port control data : P_0, P_1, P_2, P_3, P_4

(4) PL PH : Control of charge pump output
PH = 0, PL = 0 PLL operation
PH = 0, PL = 1 PD LO level
PH = 1, PL = 0 PD HI level
PH = 1, PL = 1 PD LO level

(5) R_0, R_1, R_2, standard frequency data

Data			
R_0	R_1	R_2	Standard frequency
0	0	0	25kHz
0	0	1	12.5kHz
0	1	0	50kHz
0	1	1	10kHz
1	0	0	5kHz
1	0	1	9kHz
1	1	0	1kHz
1	1	1	* PLL OFF

* FMIN = pulldown, AMIN = pulldown, PD = high impedance

(6) S : switch between FMIN and AMIN
0 : FMIN
1 : AMIN
When IF counter is in operation
0 : FMIF
1 : AMIF

(7) PS : If this bit is set to ON while AMIN is selected, swallow counter division is possible.

(8) IS : Input port selection
0 : I0 1 : I1

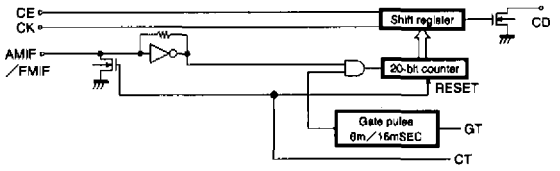
(9) GT : Frequency measurement time and unlock detection ON/OFF

CT	GT	Frequency measurement	Unlock detection	Data output
0	0	OFF	OFF	NG
0	1	OFF	ON	OK
1	0	ON Gate time = 8mSEC	ON	
1	1	ON Gate time = 16mSEC	ON	

(10) TS : Test data (0) is input

Frequency counter

(1) Structure



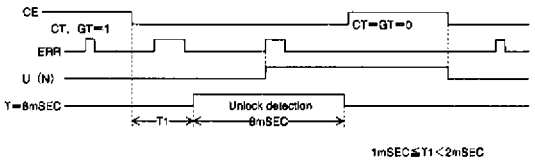
(2) How the frequency counter operates
When control data CT equals 1, the 20-bit counter and the amp go into operation. When CT equals 0, amp input goes to pulldown and the counter is reset. Measuring time (gate pulse) is selected (8mSEC/16mSEC) on the basis of control data GT. When control data CT equals 0, the counter is reset.

(3) Explanation of output data

D0 : LSB D_{19} : MSB

Unlock detection

When control data GT equals 1, or CT equals 1, the unlock detection circuit goes into operation for 8 mSEC. When CT equals 1, the unlock detection circuits stops operating before the frequency counter gate pulse is emitted. When CT equals 0, or GT equals 0, the unlock detection circuit is reset.

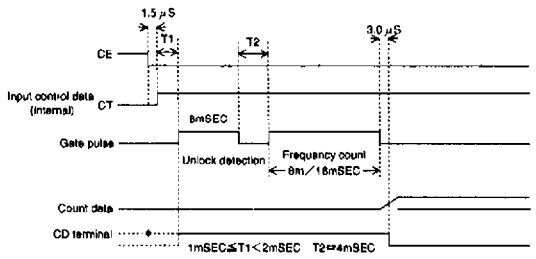


Explanation of the output data

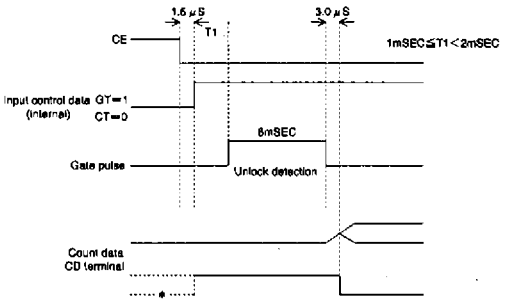
U0	U1	U2	U3					
0	0	0	0			ERR	<	1.1 μSEC
1	0	0	0	1.1 μSEC	<	ERR	<	2.2 μSEC
1	1	0	0	2.2 μSEC	<	ERR	<	3.3 μSEC
1	1	1	0	3.3 μSEC	<	ERR	<	4.4 μSEC
1	1	1	1	4.4 μSEC	<	ERR		

Frequency counter and unlock detection

(1) When CT = 1 : Frequency count and unlock detection are carried out.

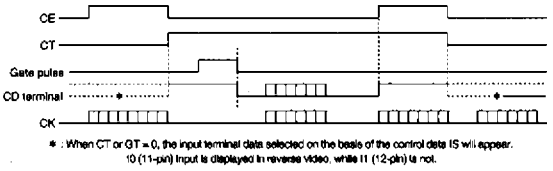


(2) When CT = 0 and GT = 1 : Only unlock detection is carried out.

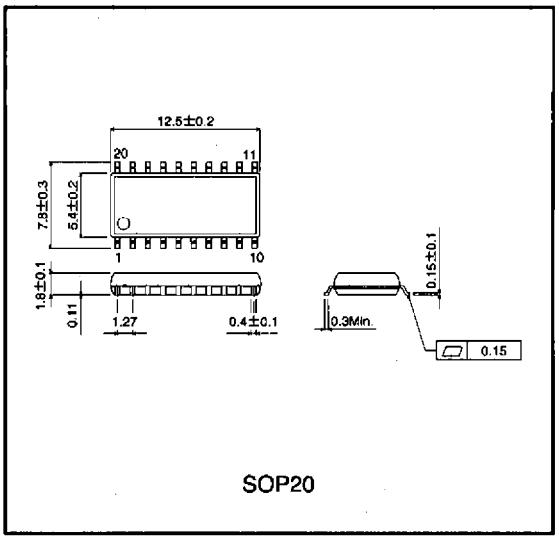


Explanation of CD terminal

When frequency measurement or unlock detection is finished, the CD terminal goes to LO to indicate that the count and unlock detection have finished. It also synchronizes with CK to output counter data. When the next data is input, it goes to HI.



●External dimensions (Unit: mm)



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