HARRIS SEMICONDUCTOR

CA3083

General Purpose High Current N-P-N Transistor Array

March 1993

Features

- **High I_C . . . . . 100mA Max**
- **Low $V_{CE\ sat}$ (at 50mA) . . . . . 0.7V Max**
- **Matched Pair (Q_1 and Q_2)**
  - **V_{IO} (V_{BE} Matched) . . . . . ±5mV Max**
  - **I_{IO} (at 1mA) . . . . . 2.5μA Max**
- **5 Independent Transistors Plus Separate Substrate Connection**

Applications

- **Signal Processing and Switching Systems Operating from DC to VHF**
- **Lamp and Relay Driver**
- **Differential Amplifier**
- **Temperature Compensated Amplifier**
- **Thyristor Firing**
- **See Application Note AN5296 "Applications of the CA3018 Circuit Transistor Array" for Suggested Applications**

Description

The CA3083 is a versatile array of five high current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q_1 and Q_2) are matched at low current (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design.

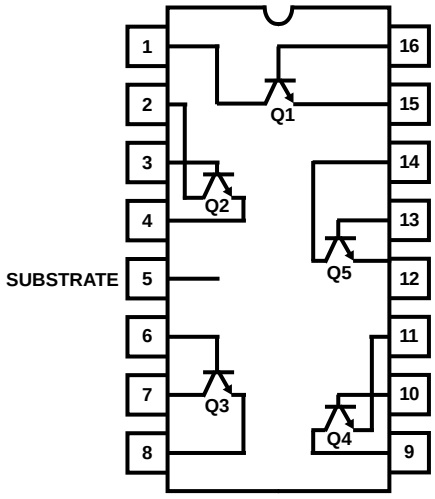
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3083	-55°C to +125°C	16 Lead Plastic DIP
CA3083F	-55°C to +125°C	16 Lead Ceramic DIP
CA3083M	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3083M96	-55°C to +125°C	16 Lead Narrow Body SOIC*

* Denotes Tape and Reel

Pinout

CA3083
(PDIP, CDIP 150mil SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **481.2**

Absolute Maximum Ratings (T_A = +25°C)

The following ratings apply for each transistor in the device:
Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current (I_C) 100mA
Base Current (I_B) 20mA
Power Dissipation
  Any One Transistor 500mW
  Total Package 750mW
  T_A > +55°C . . . . . Derate at 6.67mW/°C
Junction Temperature . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10 Sec.) . . . . . +300°C

Operating Conditions

Operating Temperature Range . . . . . -55°C ≤ T_A ≤ +125°C
Storage Temperature Range . . . . . -65°C ≤ T_A ≤ +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C. For Equipment Design

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
FOR EACH TRANSISTOR						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100µA, I_E = 0	20	60	-	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	15	24	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100µA, I_B = 0, I_E = 0	20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500µA, I_C = 0	5	6.9	-	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	-	-	10	µA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	-	-	1	µA
DC Forward-Current Transfer Ratio (Note 2) (Figure 1)	h_{FE}	V_{CE} = 3V, I_C = 10mA	40	76	-	
		V_{CE} = 3V, I_C = 50mA	40	75	-	
Base-to-Emitter Voltage (Figure 2)	V_{BE}	V_{CE} = 3V, I_C = 10mA	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage (Figures 3, 4)	$V_{CE\ SAT}$	I_C = 50mA, I_B = 5mA	-	0.40	0.70	V
Gain Bandwidth Product	f_T	V_{CE} = 3V, I_C = 10mA	-	450	-	MHz
FOR TRANSISTORS Q1 AND Q2 (As a Differential Amplifier)						
Absolute Input Offset Voltage (Figure 6)	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	-	1.2	5	mV
Absolute Input Offset Current (Figure 7)	$\lvert I_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	-	0.7	2.5	µA

NOTE:

1. The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.
2. Actual forcing current is via the emitter for this test.

Typical Performance Curves

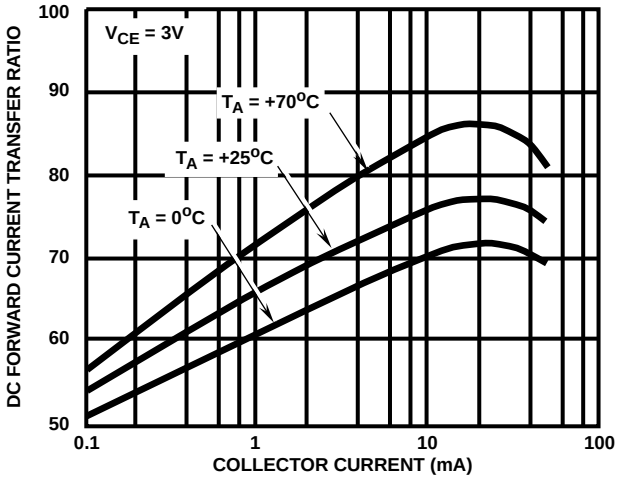


FIGURE 1. h_{FE} vs I_C

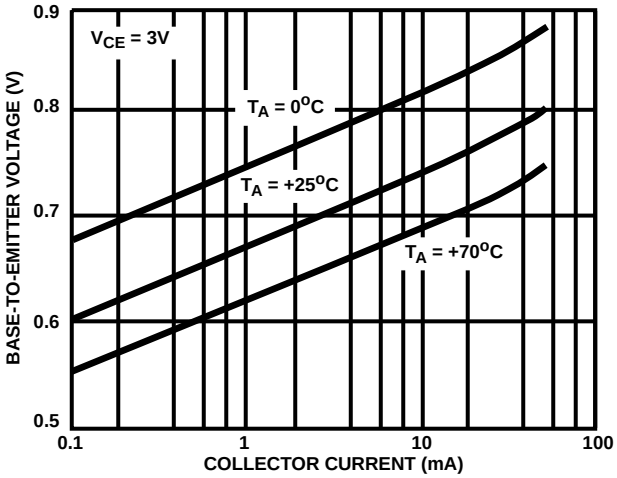


FIGURE 2. V_{BE} vs I_C

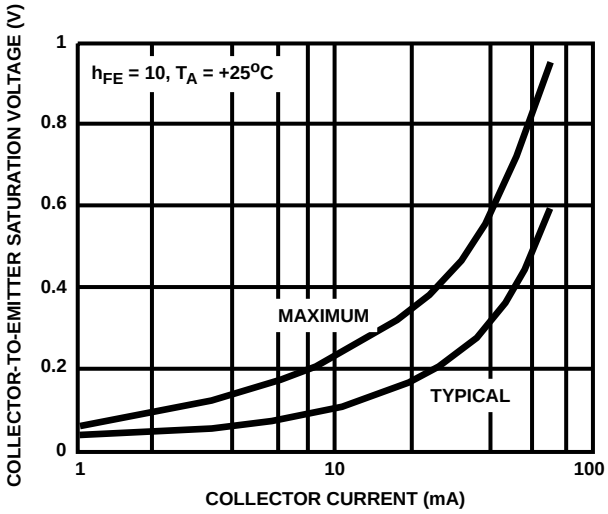


FIGURE 3. $V_{CE\ SAT}$ vs I_C AT +25°C

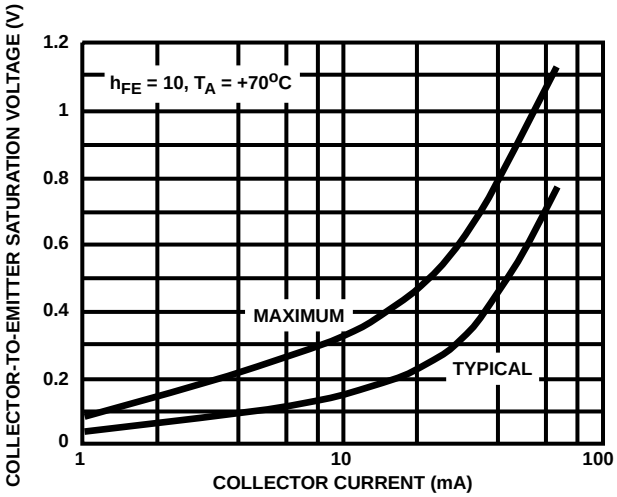


FIGURE 4. $V_{CE\ SAT}$ vs I_C AT +70°C

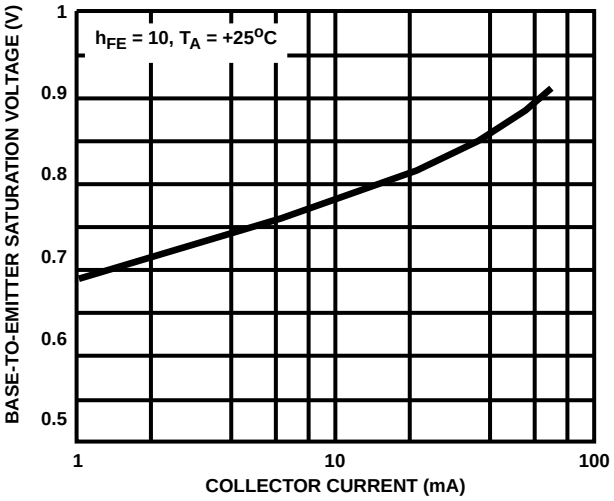


FIGURE 5. $V_{BE\ SAT}$ vs I_C

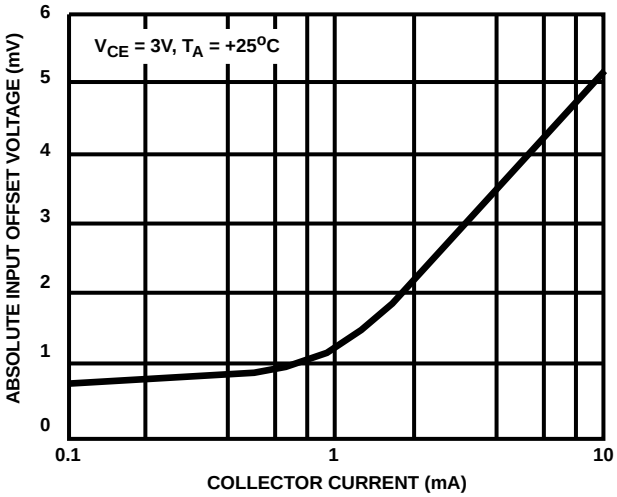


FIGURE 6. V_{IO} vs I_C (TRANSISTORS Q1 AND Q2 AS A DIFFERENTIAL AMPLIFIER)

Typical Performance Curves (Continued)

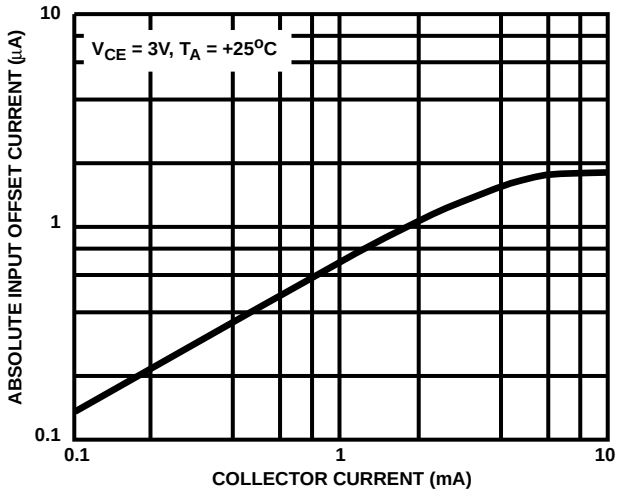


FIGURE 7. I_{IO} vs I_C (TRANSISTORS Q1 AND Q2 AS A DIFFERENTIAL AMPLIFIER)