# FM IF SYSTEM

### DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Figure 6 is a block diagram showing the CA3089 features, which include a three-state FM-IF amplifier/limiter configuration with level detectors for each stage, a doublybalanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of + 8 to + 18 volts.

The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF system is primarily a function of the phase linearity characteristic of the outboard detector coll.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40 °C to +85 °C.

#### **FEATURES**

- Exceptional limiting sensitivity: 10µV typ. at - 3dB point
- Low distortion: 0.1% typ. (with doubletuned coll)

#### **BLOCK DIAGRAM**

- Single-coil tuning capability
- High recovered audio: 400mV typ.
  Provides specific signal for control of
- interchannel muting (squeich) Provides specific signal for direct drive
- of a tuning meter • Provides delayed AGC voltage for RF
- amplifier • Provides a specific circuit for flexible
- AFC • Internal supply/voltage regulators
- internal supply/tertage regu

## **APPLICATIONS**

- · High-fidelity FM receivers
- Automotive FM receivers
- Communications FM receivers

## **ABSOLUTE MAXIMUM RATINGS**

#### PARAMETER RATING UNIT DC supply voltage: Between terminals 11 and 4 18 v Between terminals 11 and 14 18 v DC Current (out of terminal 15) 2 mΑ Device dissipation: 600 mW Up to $T_A = 60^{\circ}C$ Above $T_A = 60^{\circ}C$ derate linearly mW/°C 67 Ambient temperature range: Operating -40 to +85 °C °C Storage -65 to +150 Lead temperature (during soldering): °C At distance not less than 1/32" (0.79mm) +265 from case for 10 seconds max



ability PIN CONFIGURATION



CA3089

## EQUIVALENT SCHEMATIC



**Signetics** 

# CA3089

## DC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}C$ , V<sup>+</sup> = 12V unless otherwise specified.

			CA3089D2			
PARAMETER		TEST CONDITIONS	Min	Тур	Max	
STATIC ( I11 DC Volta	DC) CHARACTERISTICS Quiescent circuit current ges: <sup>4</sup>	No signal input, non-muted	16	23	30	mA
۷1	Terminal 1 (IF input)	No signal input, non-muted	1.2	1.9	2.4	V
V <sub>2</sub> V3	Terminal 2 (ac return to input) Terminal 3 (dc bias to input)	No signal input, non-muted No signal input, non-muted	1.2 1.2	1.9 1.9	2.4 2.4	v v
V <sub>6</sub> V <sub>7</sub> V <sub>10</sub>	Terminal 6 (audio output) Terminal 7 (A.F.C.) Terminal 10 (dc reference)	No signal input, non-muted No signal input, non-muted No signal input, non-muted	5.0 5.0 5.0	5.6 5.6 5.6	6.0 6.0 6.0	V V V
	C CHARACTERISTICS Input limiting voltage (-3dB point) <sup>3</sup>			10	25	μ٧
۷o	AMR AM Rejection (terminal 6) <sup>4</sup> Recovered audio voltage (terminal 6) <sup>3</sup>	$V_{IN} = 0.1V$ , $F_0 = 10.7MHz$ , $f_{mod} = 400Hz$ , AM Mod = 30%	45 400	55 500	600	dB mV
Total har THD THD	monic distortion: <sup>1</sup> Single tuned (terminal 6) <sup>3</sup> Double tuned (terminal 6) <sup>4</sup>	f <sub>mod</sub> = 400Hz, V <sub>IN</sub> = 0.1		0.5 0.1	1.0	%
S+N/N MUIN	Signal plus noise to noise ratio (terminal 6) <sup>3</sup> Mute input (terminal 5)	Deviation = $\pm 75$ kHz V <sub>IN</sub> = 0.1V V <sub>5</sub> = 2.5V	60 50	70 70		dB dB
MUOUT	Mute output (terminal 12)	$V_{IN} = 50\mu V$ $V_{IN} = 0V$	4.0		.5	v v
MTR	Meter output (terminal 13)	$V_{IN} = 0.1V$ $V_{IN} = 500\mu V$ $V_{IN} = 0V$	2.5 1.0	3.5 1.5	.7	
AGC	Delayed AGC (terminal 15)	$V_{IN} = .01V$ $V_{IN} = 10\mu V$	4.0	5.0	.5	v v
THD	Double tuned (terminal 6) <sup>4</sup>	f <sub>mod</sub> = 400Hz VIN = 0.1		0.1		%

NOTES

1. THD characteristics and Audio Level are essentially a function of the phase and Q

characteristics of the network connected between terminals 8.9, and 10

2. Test circuit Figure 1.

3. Test circuit Figure 2.

4. Test circuit Figures 1 and 2.

## **TEST CIRCUITS**



## SYSTEM DESIGN CONSIDERATONS

The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input by pass capacitors should be located close to the input terminals and the values should not be large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good by-pass capacitors would be ceramic disc with values in the range of .01 to .05 microfarad.

The input impedance of the CA3089 is approximately 10,000 ohms. It is not

recommended to match this impedance. The value of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50 and 100 ohms is recommended.

## **TYPICAL PERFORMANCE CHARACTERISTICS**



## **TEST CIRCUITS**

