HARRIS SEMICONDUCTOR

CA3096

March 1993

N-P-N/P-N-P Transistor Array

Applications

- **Five-Independent Transistors**
  - **Three N-P-N and**
  - **Two P-N-P**
- **Differential Amplifiers**
- **DC Amplifiers**
- **Sense Amplifiers**
- **Level Shifters**
- **Timers**
- **Lamp and Relay Drivers**
- **Thyristor Firing Circuits**
- **Temperature Compensated Amplifiers**
- **Operational Amplifiers**

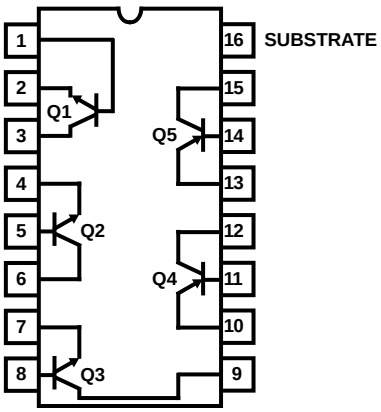
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3096AE	-55°C to +125°C	16 Lead Plastic DIP
CA3096AM	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3096AM96	-55°C to +125°C	16 Lead Narrow Body SOIC*
CA3096CE	-55°C to +125°C	16 Lead Plastic DIP
CA3096E	-55°C to +125°C	16 Lead Plastic DIP
CA3096M	-55°C to +125°C	16 Lead Narrow Body SOIC
CA3096M96	-55°C to +125°C	16 Lead Narrow Body SOIC*

* Denotes Tape and Reel

Pinout

CA3096, CA3096A, CA3096C
(PDIP, 150 mil SOIC)
TOP VIEW



Description

The CA3096C, CA3096, and CA3096A are general purpose high voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096A, CA3096, and CA3096C are identical, except that the CA3096A specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and V_{CE}(SAT). The CA3096C is a relaxed version of the CA3096.

CA3096A, CA3096, CA3096C Essential Differences

CHARACTERISTIC		CA3096A	CA3096	CA3096C
$V_{(BR)CEO}$ (V) Min				
	n-p-n	35	35	24
	p-n-p	-40	-40	-24
$V_{(BR)CBO}$ (V) Min.				
	n-p-n	45	45	30
	p-n-p	-40	-40	-24
h_{FE} at 1mA				
	n-p-n	150-500	150-500	100-670
	p-n-p	20-200	20-200	15-200
h_{FE} at 100µA				
	p-n-p	40-250	40-250	30-300
I_{CBO} (nA) Max.				
	n-p-n	40	100	100
	p-n-p	-40	-100	-100
I_{CEO} (nA) Max.				
	n-p-n	100	1000	1000
	p-n-p	-100	-1000	-1000
$V_{CE\ SAT}$ (V) Max.				
	n-p-n	0.5	0.7	0.7
$\|V_{IO}\|$ (mV)Max.				
	n-p-n	5	-	-
	p-n-p	5	-	-
$\|I_{IO}\|$ (µA) Max.				
	n-p-n	0.6	-	-
	p-n-p	0.25	-	-

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **595.2**

Absolute Maximum Ratings

	N-P-N	P-N-P
Collector-to-Emitter Voltage, V_{CEO}		
CA3096, CA3096A	35V	-40V
CA3096C	24V	-24V
Collector-to-Base Voltage, V_{CBO}		
CA3096, CA3096A	45V	-40V
CA3096C	30V	-24V
Collector-to-Substrate Voltage, V_{CIO} (Note 1)		
CA3096, CA3096A	45V	-
CA3096C	30V	-
Emitter-to-Substrate Voltage, V_{EIO}		
CA3096, CA3096A	-	-40V
CA3096C	-	-24V
Emitter-to-Base Voltage, V_{EBO}		
CA3096, CA3096A	6V	-40V
CA3096C	6V	-24V
Collector Current, I_C (All Types)	50mA	-10mA
Power Dissipation, P_D (Up to $T_A = +55^oC$)		
Device (Total)	750mW	
Each Transistor	200mW	
Above $T_A = +55^oC$	Derate Linearly at 6.67mW/^oC	
Junction Temperature (Plastic Packages)	+150^oC	
Lead Temperature (Soldering 10 Sec.)	+300^oC	

Operating Conditions

Operating Temperature Range . . . . . $-55^oC \le T_A \le +125^oC$
Storage Temperature Range . . . . . $-65^oC \le T_A \le +150^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static Electrical Specifications $T_A = +25^oC$

For Equipment Design

PARAMETERS	TEST CONDITIONS	LIMITS									UNITS
		CA3096A			CA3096			CA3096C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
FOR EACH N-P-N TRANSISTOR											
I_{CBO}	V_{CB} = 10V, I_E = 0	-	0.001	40	-	0.001	100	-	0.001	100	nA
I_{CEO}	V_{CE} =10V, I_B = 0	-	0.006	100	-	0.006	1000	-	0.006	1000	nA
$V_{(BR)CEO}$	I_C =1mA, I_B = 0	35	50	-	35	50	-	24	35	-	V
$V_{(BR)CBO}$	I_C =10µA, I_E = 0	45	100	-	45	100	-	30	80	-	V
$V_{(BR)CIO}$	I_{CI} = 10µA, $I_B = I_E = 0$	45	100	-	45	100	-	30	80	-	V
$V_{(BR)EBO}$	I_E = 10µA, I_C = 0	6	8	-	6	8	-	6	8	-	V
V_Z	I_Z = 10µA	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE\ SAT}$	I_C =10mA, I_B = 1mA	-	0.24	0.5	-	0.24	0.7	-	0.24	0.7	V
V_{BE} (Note 2)	I_C =1mA, V_{CE} = 5V	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE} (Note 2)		150	390	500	150	390	500	100	390	670	

Static Electrical Specifications $T_A = +25^oC$ (Continued)

For Equipment Design

PARAMETERS	TEST CONDITIONS	LIMITS									UNITS
		CA3096A			CA3096			CA3096C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\|\Delta V_{BE}/\Delta T\|$ (Note 2)	I_C = 1mA, V_{CE} = 5V	-	1.9	-	-	1.9	-	-	1.9	-	mV/^{o}C
FOR EACH P-N-P TRANSISTOR											
I_{CBO}	V_{CB} = -10V, I_E = 0	-	-0.006	-40	-	-0.06	-100	-	-0.06	-100	nA
I_{CEO}	V_{CE} = -10V, I_B = 0	-	-0.12	-100	-	-0.12	-1000	-	-0.12	-1000	nA
$V_{(BR)CEO}$	I_C = -100µA, I_B = 0	-40	-75	-	-40	-75	-	-24	-30	-	V
$V_{(BR)CBO}$	I_C = -10µA, I_E = 0	-40	-80	-	-40	-80	-	-24	-60	-	V
$V_{(BR)EBO}$	I_E = -10µA, I_C = 0	-40	-100	-	-40	-100	-	-24	-80	-	V
$V_{(BR)EIO}$	I_{EI} = 10µA, $I_B = I_C$ = 0	40	100	-	40	100	-	24	80	-	V
$V_{CE\ SAT}$	I_C = -1mA, I_B = -100µA	-	-0.16	-0.4	-	-0.16	-0.4	-	-0.16	-0.4	V
V_{BE} (Note 2)	I_C = -100µA, V_{CE} = -5V	-0.5	-0.6	-0.7	-0.5	-0.6	-0.7	-0.5	-0.6	-0.7	V
h_{FE} (Note 2)	I_C = -100µA, V_{CE} = -5V	40	85	250	40	85	250	30	85	300	
	I_C = -1mA, V_{CE} = -5V	20	47	200	20	47	200	15	47	200	
$\|\Delta V_{BE}/\Delta T\|$ (Note 2)	I_C = -100µA, V_{CE} = -5V	-	2.2	-	-	2.2	-	-	2.2	-	mV/^{o}C

I_{CBO}	Collector-Cutoff Current	V_Z	Emitter-to-Base Zener Voltage
I_{CEO}	Collector-Cutoff Current	$V_{CE\ SAT}$	Collector-to-Emitter Saturation Voltage
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage	V_{BE}	Base-to-Emitter Voltage
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage	h_{FE}	DC Forward-Current Transfer Ratio
$V_{(BR)CIO}$	Collector-to-Substrate Breakdown Voltage	$\|\Delta V_{BE}/\Delta T\|$	Magnitude of Temperature Coefficient: (for each transistor)
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage		

NOTE:

1. The collector of each transistor of the CA3096 is isolated from the substrate by an integral diode. The substrate (terminal 16) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. Actual forcing current is via the emitter for this test.

Static Electrical Specifications $T_A = +25^oC$ (CA3096A Only)

For Equipment Design

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS CA3096A MIN	LIMITS CA3096A TYP	LIMITS CA3096A MAX	UNITS
FOR TRANSISTORS Q1 AND Q2 (AS A DIFFERENTIAL AMPLIFIER)						
Absolute Input Offset Voltage	$\|V_{IO}\|$	V_{CE} = 5V, I_C = 1mA	-	0.3	5	mV
Absolute Input Offset Current	$\|I_{IO}\|$		-	0.07	0.6	µA
Absolute Input Offset Voltage Temperature Coefficient	$\frac{\|\Delta V_{IO}\|}{\Delta T}$		-	1.1	-	µV/°C
FOR TRANSISTORS Q4 AND Q5 (AS A DIFFERENTIAL AMPLIFIER)						
Absolute Input Offset Voltage	$\|V_{IO}\|$	V_{CE} = -5V, I_C = -100µA R_S = 0	-	0.15	5	mV
Absolute Input Offset Current	$\|I_{IO}\|$		-	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient	$\frac{\|\Delta V_{IO}\|}{\Delta T}$		-	0.54	-	µV/°C

Dynamic Electrical Specifications $T_A = +25^oC$

Typical Values Intended Only for Design Guidance

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
FOR EACH N-P-N TRANSISTOR				
Noise Figure (Low Frequency)	NF	f = 1kHz, V_{CE} = 5V, I_C = 1mA, R_S = 1kΩ	2.2	dB
Low-Frequency, Input Resistance	R_I	f = 1.0kHz, V_{CE} = 5V I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance	R_O	f = 1.0kHz, V_{CE} = 5V I_C = 1 mA	80	kΩ
Admittance Characteristics				
Forward Transfer Admittance	y_{FE} g_{FE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	7.5	mmho
	y_{FE} b_{FE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	-j13	mmho
Input Admittance	y_{IE} g_{IE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	2.2	mmho
	y_{IE} b_{IE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	j3.1	mmho
Output Admittance	y_{OE} g_{OE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	0.76	mmho
	y_{OE} b_{OE}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	j2.4	mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 1.0mA	280	MHz
		V_{CE} = 5V, I_C = 5mA	335	MHz
Emitter-To-Base Capacitance	C_{EB}	V_{EB} = 3V	0.75	pF
Collector-To-Base Capacitance	C_{CB}	V_{CB} = 3V	0.46	pF
Collector-To-Substrate Capacitance	C_{CI}	V_{CI} = 3V	3.2	pF

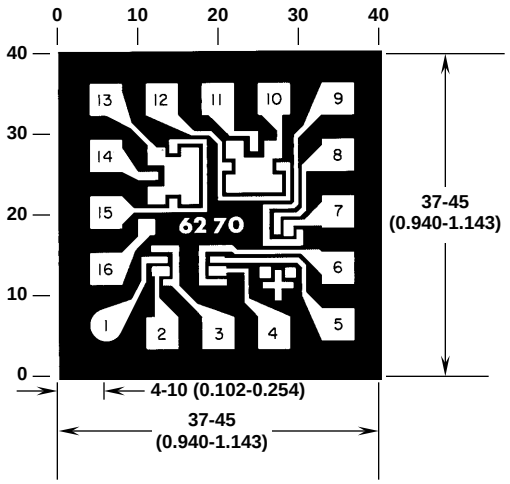
Dynamic Electrical Specifications $T_A = +25^oC$

Typical Values Intended Only for Design Guidance

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
FOR EACH P-N-P TRANSISTOR				
Noise Figure (Low Frequency)	NF	f = 1kHz, I_C = 100µA, R_S = 1kΩ	3	dB
Low-Frequency Input Resistance	R_I	f = 1kHz, V_{CE} = 5V, I_C = 100µA	27	kΩ
Low-Frequency Output Resistance	R_O	f = 1kHz, V_{CE} = 5V, I_C = 100µA	680	kΩ
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 100µA	6.8	MHz
Emitter-To-Base Capacitance	C_{EB}	V_{EB} = -3V	0.85	pF
Collector-To-Base Capacitance	C_{CB}	V_{CB} = -3V	2.25	pF
Base-To-Substrate Capacitance	C_{BI}	V_{BI} = 3V	3.05	pF

Metallization Mask Layout

CA3096H



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57^o instead of 90^o with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

Typical Performance Curves

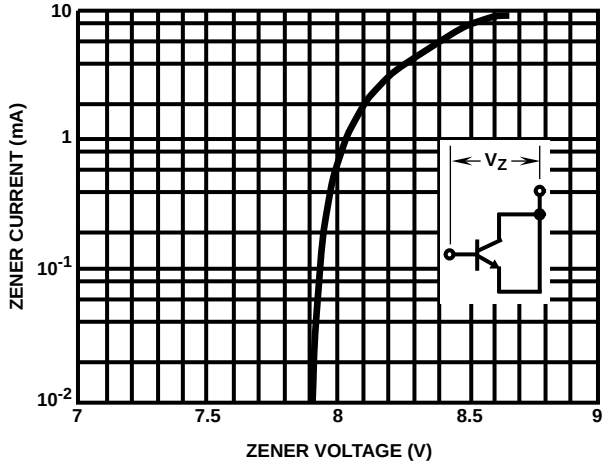


FIGURE 1. BASE-TO-EMITTER ZENER CHARACTERISTIC (N-P-N)

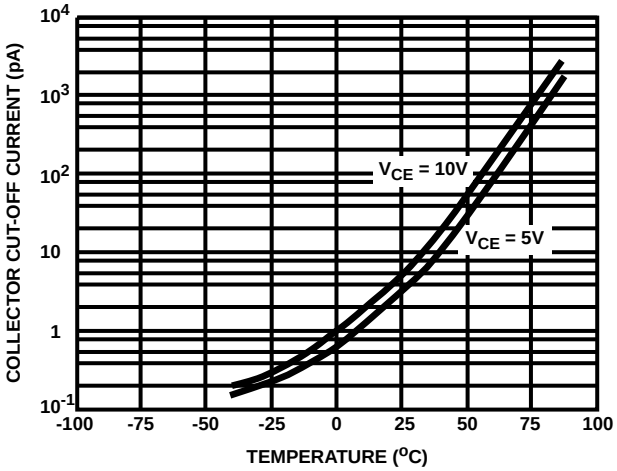


FIGURE 2. COLLECTOR CUT-OFF CURRENT (I_{CEO}) vs TEMPERATURE (N-P-N)

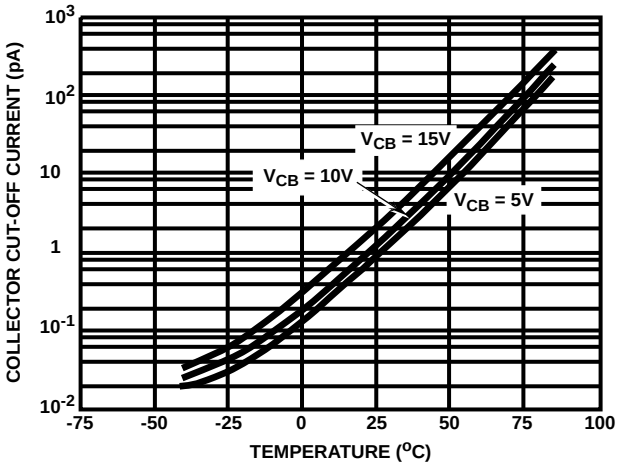


FIGURE 3. COLLECTOR CUT-OFF CURRENT (I_{CBO}) vs TEMPERATURE (N-P-N)

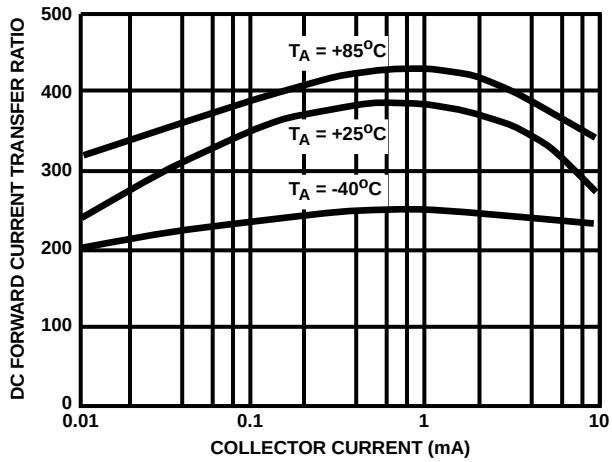


FIGURE 4. TRANSISTOR (N-P-N) h_{FE} vs COLLECTOR CURRENT

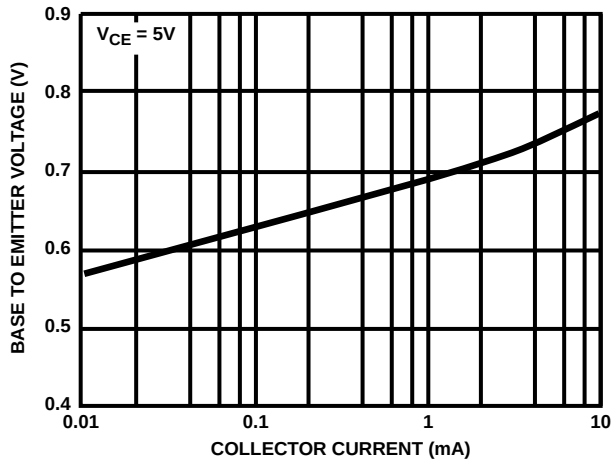


FIGURE 5. V_{BE} (N-P-N) vs COLLECTOR CURRENT

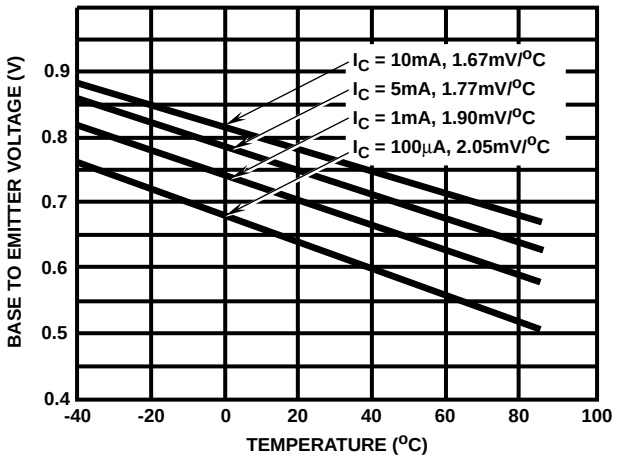


FIGURE 6. V_{BE} (N-P-N) vs TEMPERATURE

Typical Performance Curves (Continued)

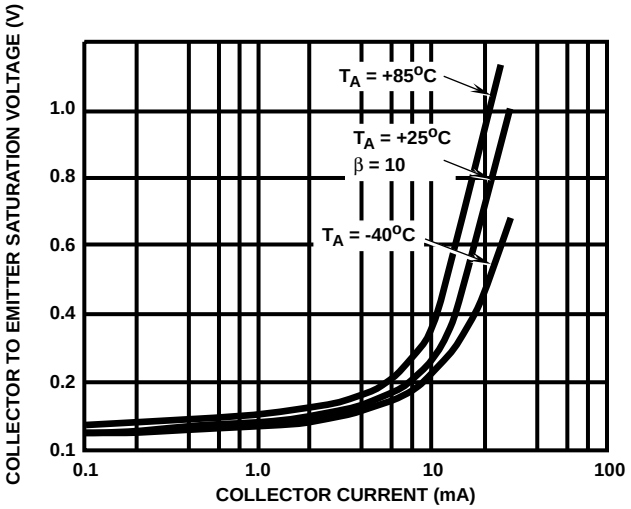


FIGURE 7. $V_{CE\ SAT}$ (N-P-N) vs COLLECTOR CURRENT

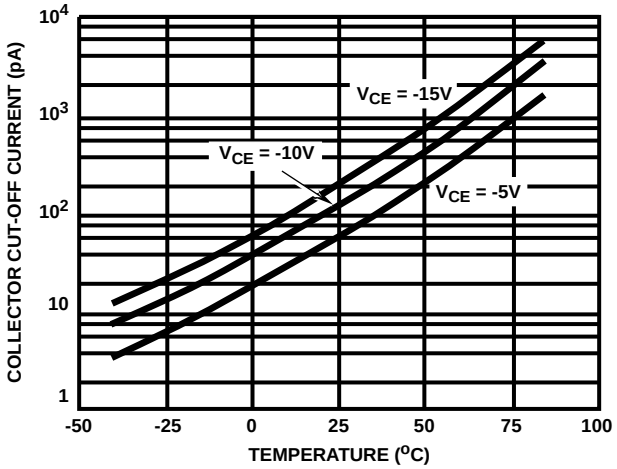


FIGURE 8. COLLECTOR CUT-OFF CURRENT (I_{CEO}) vs TEMPERATURE (P-N-P)

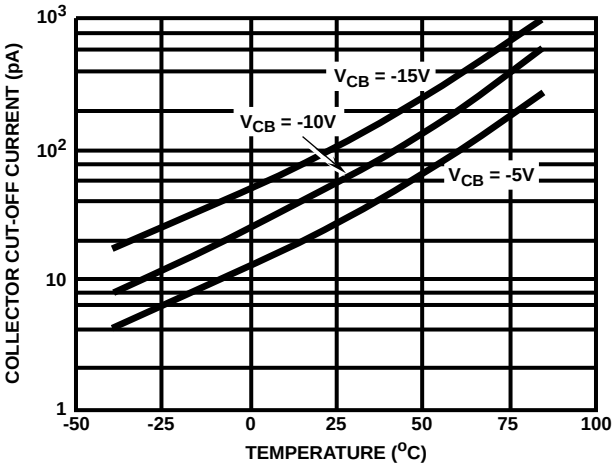


FIGURE 9. COLLECTOR CUT-OFF CURRENT (I_{CBO}) vs TEMPERATURE (P-N-P)

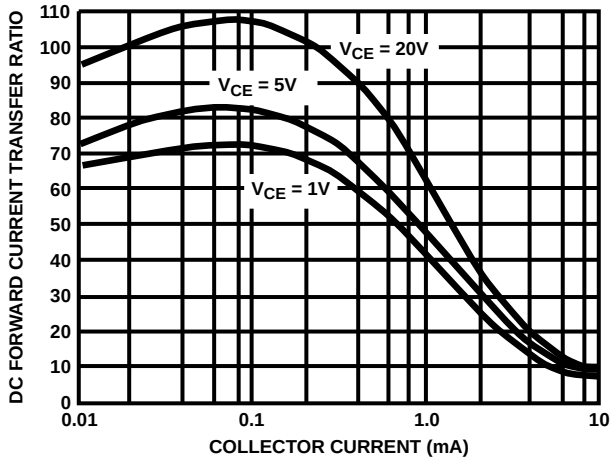


FIGURE 10. TRANSISTOR (P-N-P) h_{FE} vs COLLECTOR CURRENT

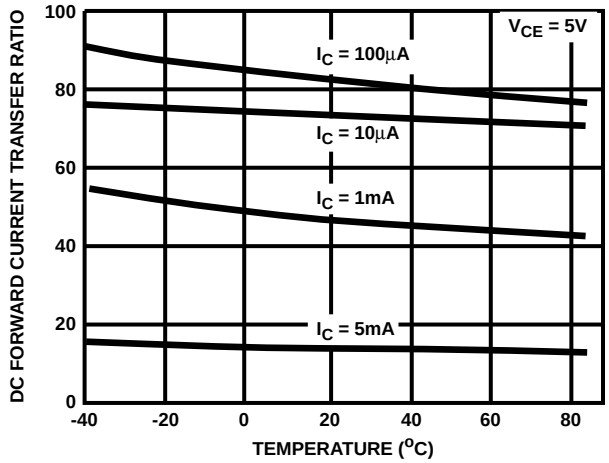


FIGURE 11. TRANSISTOR (P-N-P) h_{FE} vs TEMPERATURE

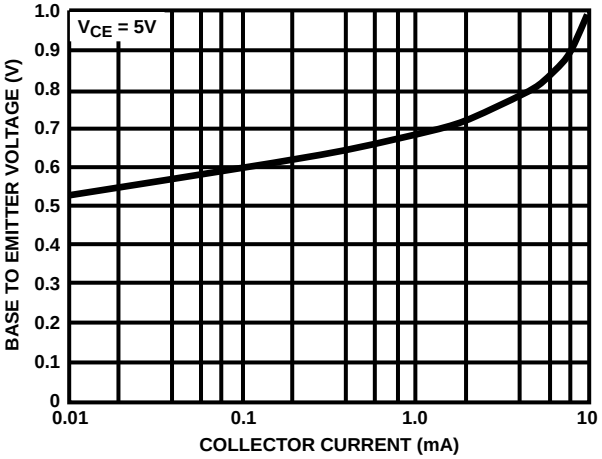


FIGURE 12. V_{BE} (P-N-P) vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

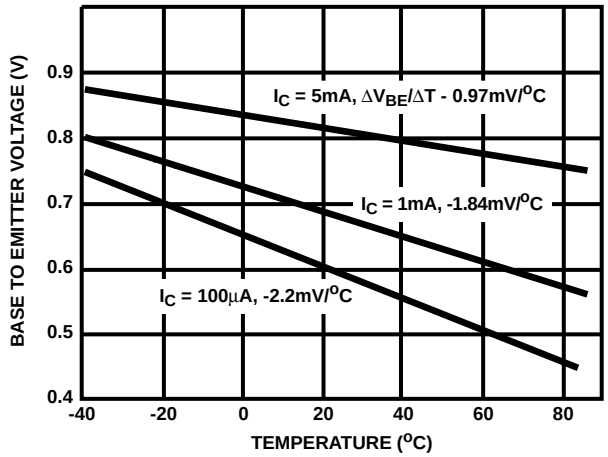


FIGURE 13. V_{BE} (P-N-P) vs TEMPERATURE

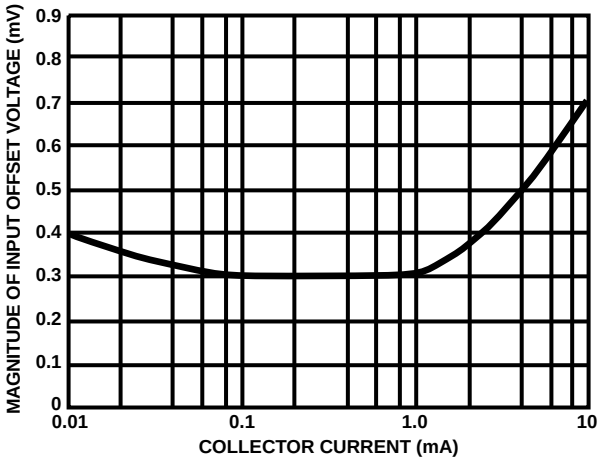


FIGURE 14. MAGNITUDE OF INPUT OFFSET VOLTAGE $|V_{IO}|$ vs COLLECTOR CURRENT FOR N-P-N TRANSISTOR Q1 - Q2

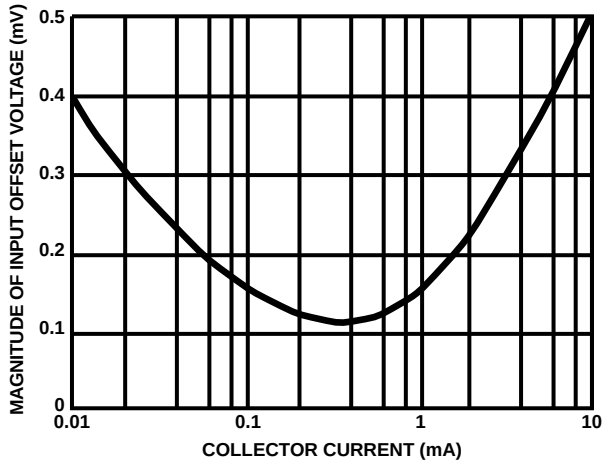


FIGURE 15. MAGNITUDE OF INPUT OFFSET VOLTAGE $|V_{IO}|$ vs COLLECTOR CURRENT FOR P-N-P TRANSISTOR Q4 - Q5

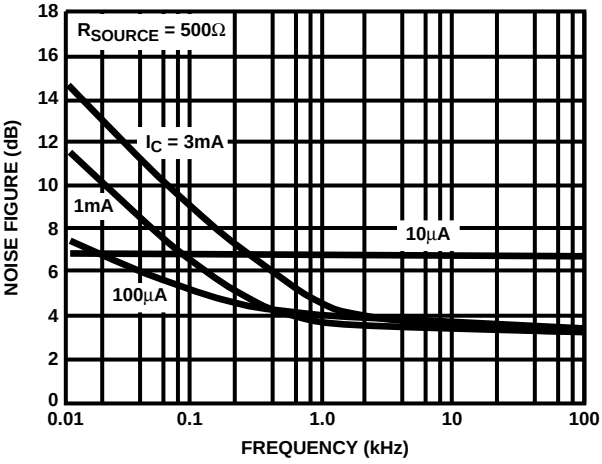


FIGURE 16. NOISE FIGURE vs FREQUENCY FOR N-P-N TRANSISTORS

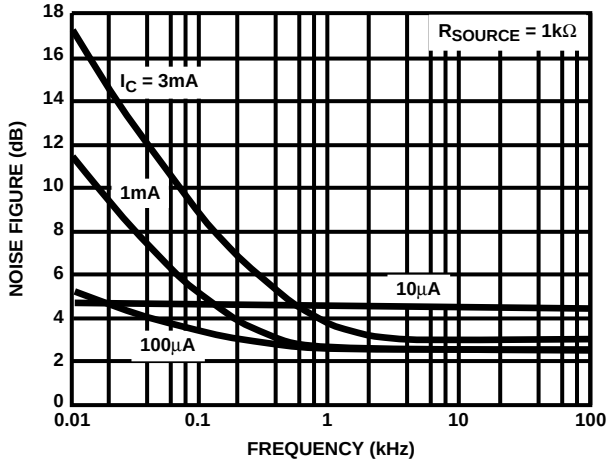


FIGURE 17. NOISE FIGURE vs FREQUENCY FOR N-P-N TRANSISTORS

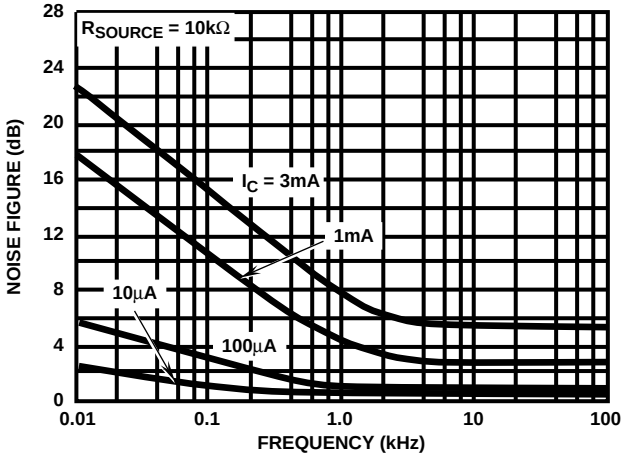


FIGURE 18. NOISE FIGURE vs FREQUENCY FOR N-P-N TRANSISTORS

Typical Performance Curves (Continued)

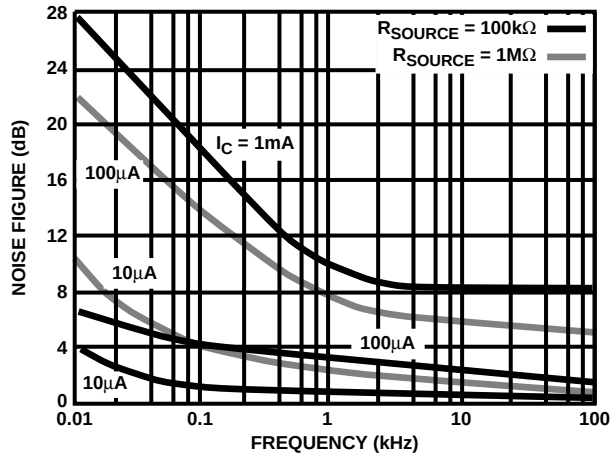


FIGURE 19. NOISE FIGURE vs FREQUENCY FOR N-P-N TRANSISTORS

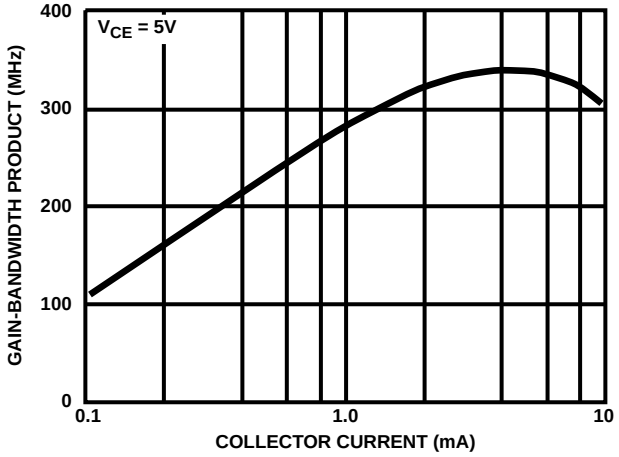


FIGURE 20. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT (N-P-N)

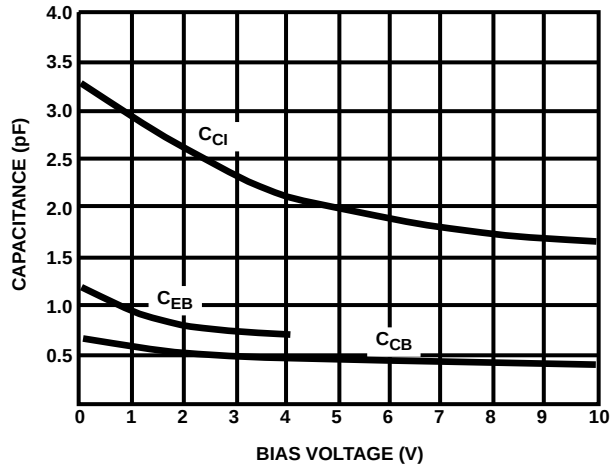


FIGURE 21. CAPACITANCE vs BIAS VOLTAGE (N-P-N)

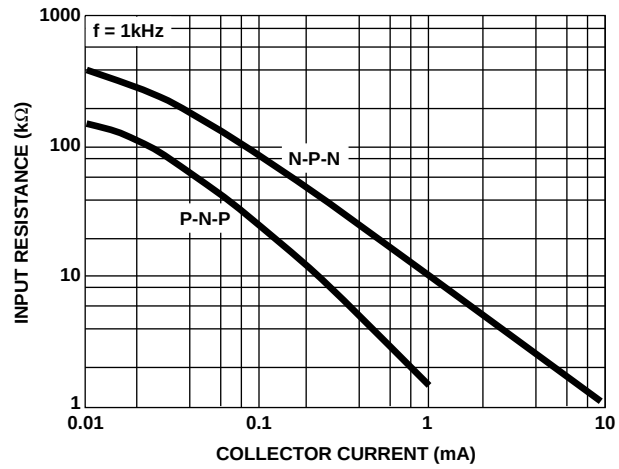


FIGURE 22. INPUT RESISTANCE vs COLLECTOR CURRENT

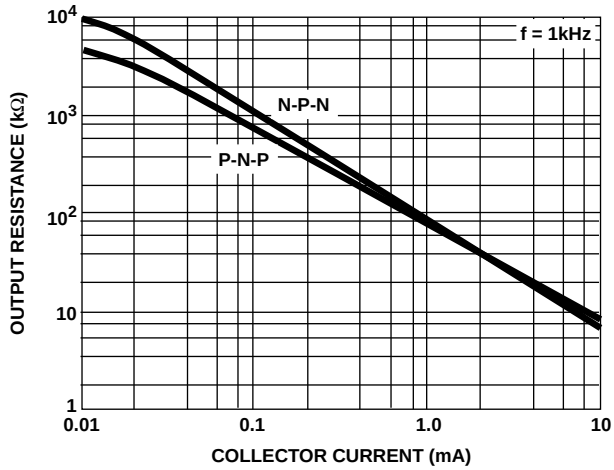


FIGURE 23. OUTPUT RESISTANCE vs COLLECTOR CURRENT

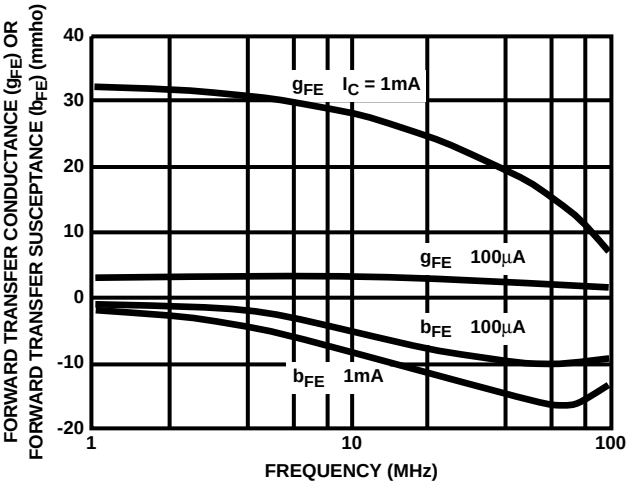


FIGURE 24. FORWARD TRANSCONDUCTANCE vs FREQUENCY

Typical Performance Curves (Continued)

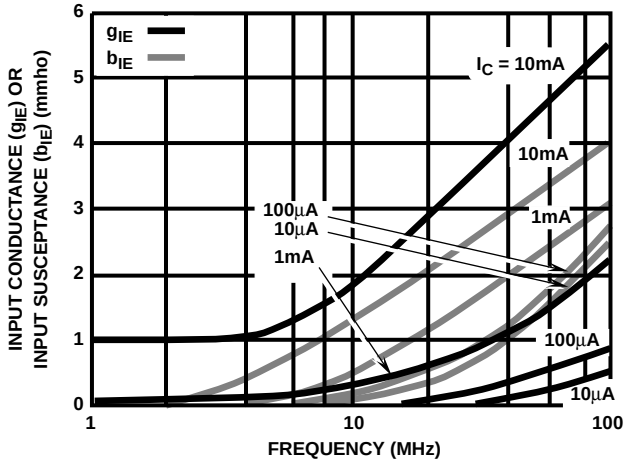


FIGURE 25. INPUT ADMITTANCE vs FREQUENCY

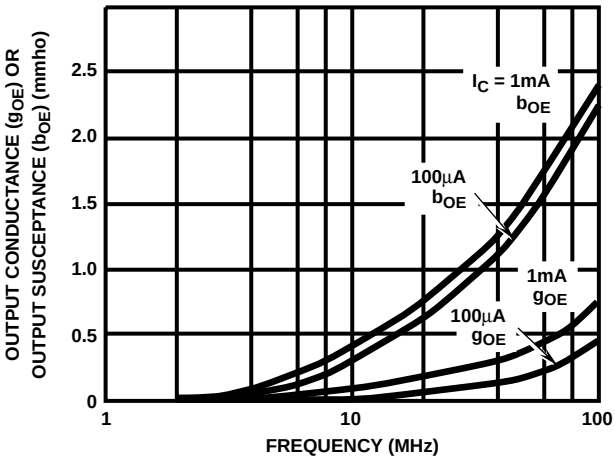


FIGURE 26. OUTPUT ADMITTANCE vs FREQUENCY

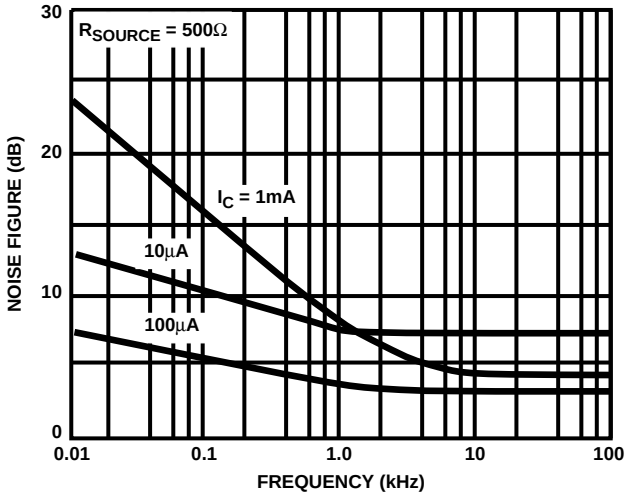


FIGURE 27. NOISE FIGURE vs FREQUENCY (P-N-P)

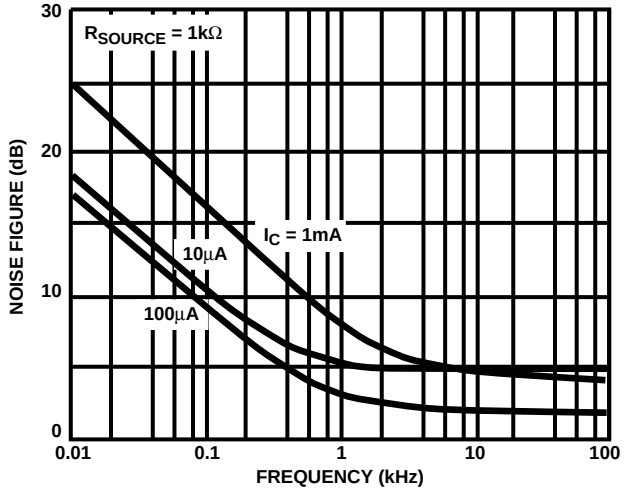


FIGURE 28. NOISE FIGURE vs FREQUENCY (P-N-P)

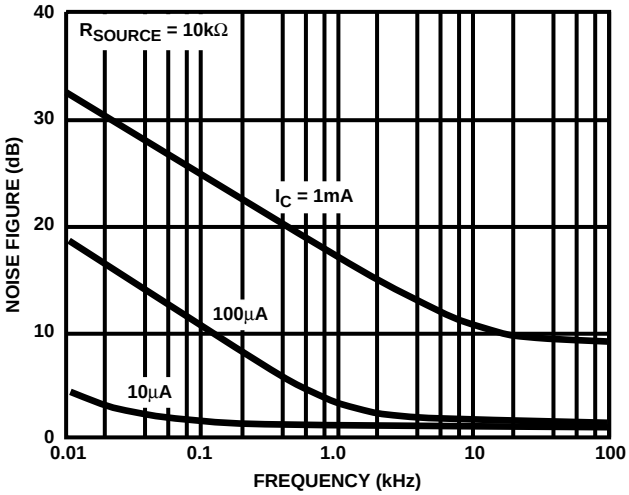


FIGURE 29. NOISE FIGURE vs FREQUENCY (P-N-P)

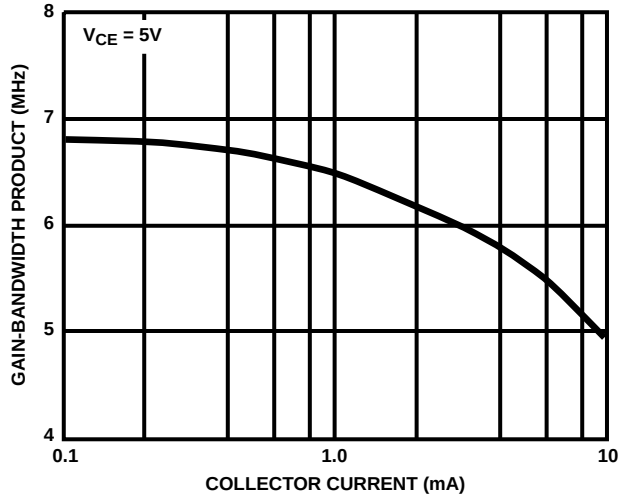


FIGURE 30. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT (P-N-P)

Typical Performance Curves (Continued)

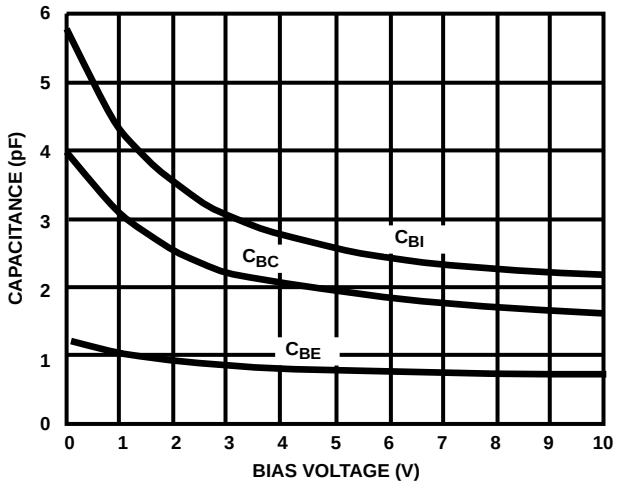


FIGURE 31. CAPACITANCE vs BIAS VOLTAGE (P-N-P)

Typical Applications

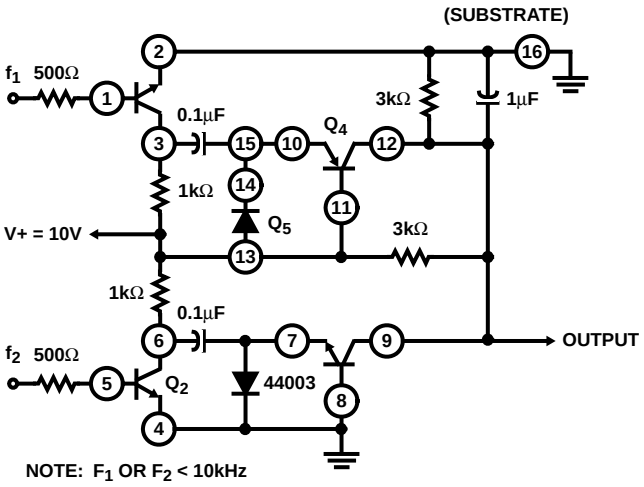


FIGURE 32. FREQUENCY COMPARATOR USING CA3096

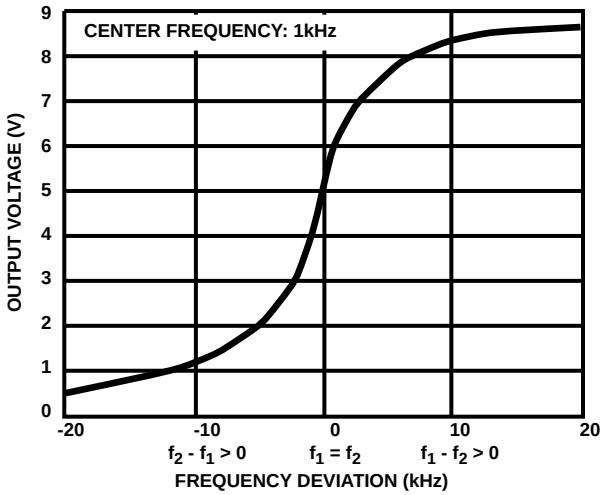


FIGURE 33. FREQUENCY COMPARATOR CHARACTERISTICS

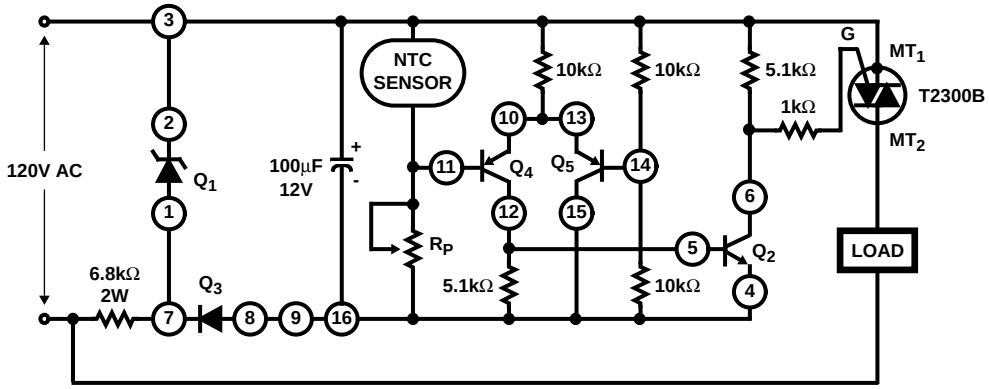


FIGURE 34. LINE-OPERATED LEVEL SWITCH USING CA3096A OR CA3096

Typical Applications (Continued)

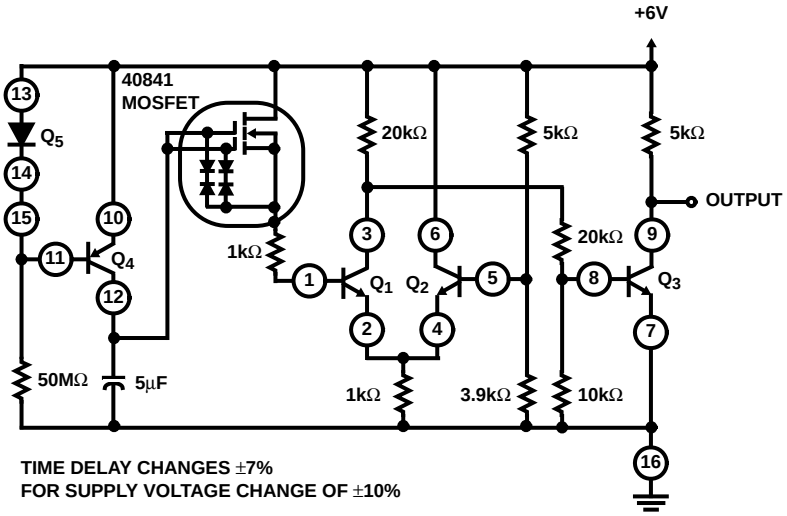
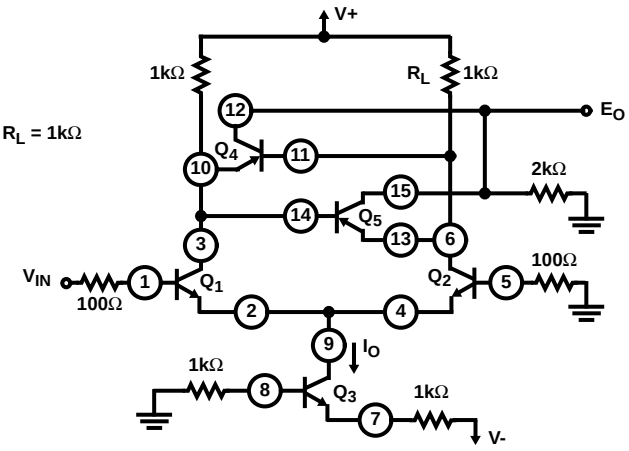


FIGURE 35. ONE-MINUTE TIMER USING CA3096A AND A MOSFET

$$V_T = \pm \frac{36}{I_O \ R_L}$$

IF I_O = 1mA AND R_L = 1kΩ

V_T = ± 36mV



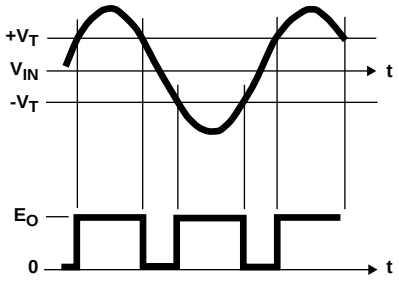


FIGURE 36. CA3096A SMALL-SIGNAL ZERO VOLTAGE DETECTOR HAVING NOISE IMMUNITY

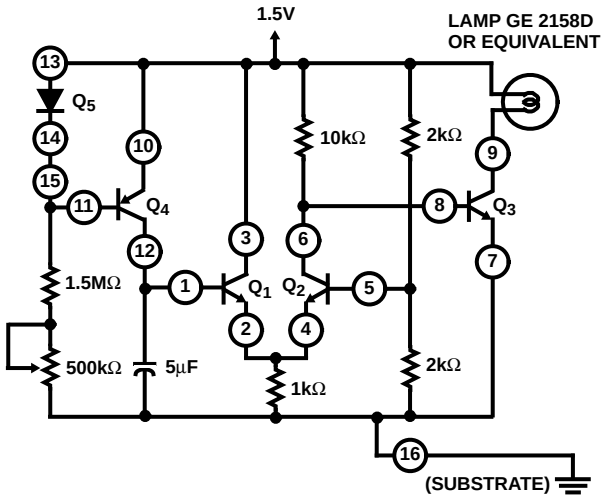
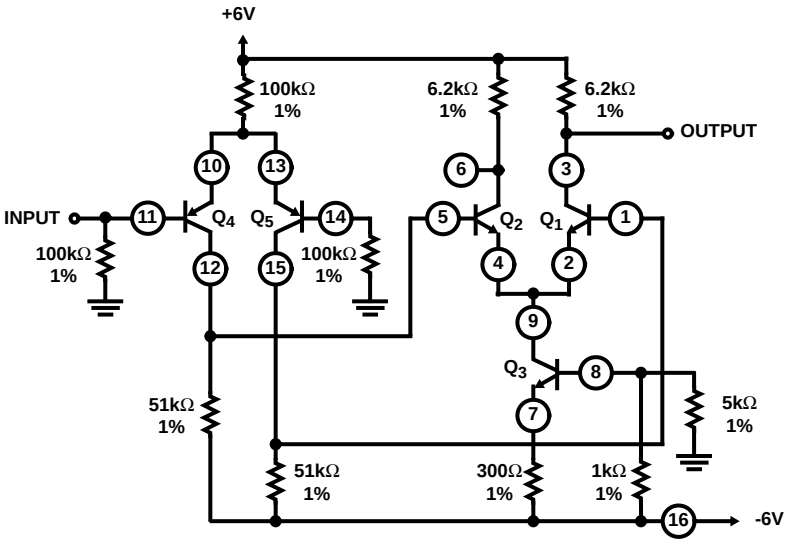


FIGURE 37. TEN-SECOND TIMER OPERATED FROM 1.5V SUPPLY USING CA3096

Typical Applications (Continued)



NOTES:

1. Can be operated with either dual supply or single supply.
2. Wide-input common mode range +5V to -5V.
3. Low bias current: <1μA.

FIGURE 38. CASCADE OF DIFFERENTIAL AMPLIFIERS USING CA3096A

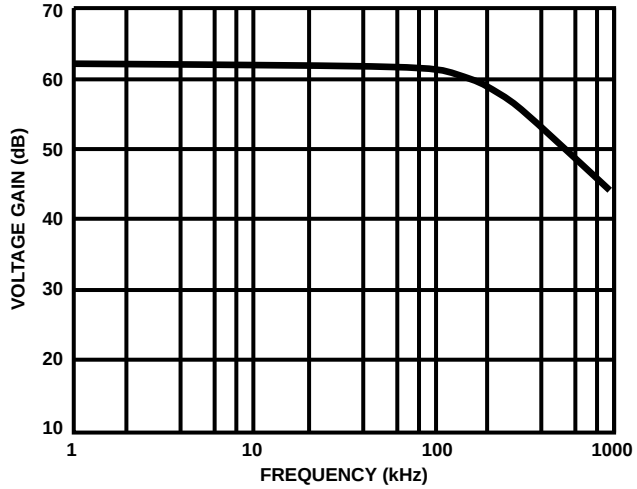


FIGURE 39. GAIN-FREQUENCY CHARACTERISTICS