

CD4000M/CD4000C Dual 3-Input NOR Gate Plus Inverter

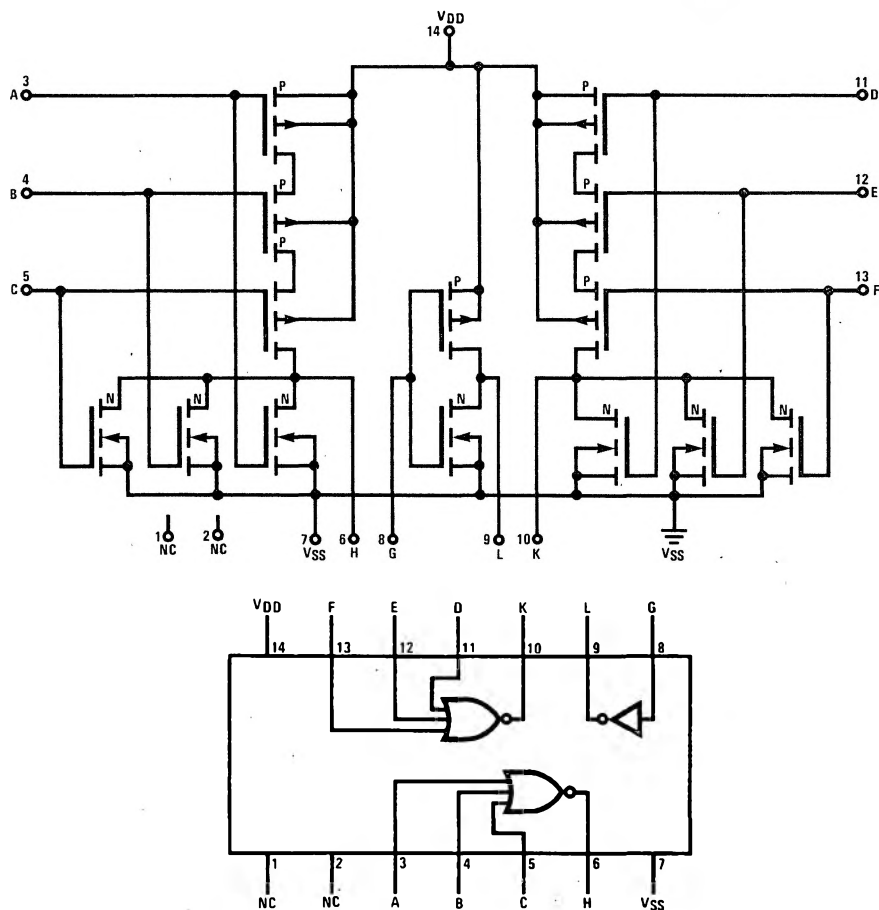
General Description

The CD4000M/CD4000C is a monolithic complementary MOS (CMOS) dual 2-input NOR gate plus an inverter. N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

- Wide supply voltage range 3.0 V to 15 V
- Low power 10 nW (typ.)
- High noise immunity 0.45 V_{DD} (typ.)

Schematic and Connection Diagram



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$V_{SS} - 0.3 \text{ V to } V_{DD} + 0.3 \text{ V}$
Operating Temperature Range	
CD4000M	$-55^{\circ}\text{C to } +125^{\circ}\text{C}$
CD4000C	$-40^{\circ}\text{C to } +85^{\circ}\text{C}$
Storage Temperature Range	$-65^{\circ}\text{C to } +150^{\circ}\text{C}$
Package Dissipation	500 mW
Operating V_{DD} Range	$V_{SS} + 3 \text{ V to } V_{SS} + 15 \text{ V}$
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics CD4000M (Note 2)

PARAMETER	CONDITIONS	-55°C		$+25^{\circ}\text{C}$			$+125^{\circ}\text{C}$		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5 \text{ V}$		0.05			0.05		3	μA
	$V_{DD} = 10 \text{ V}$		0.1			0.1		6	μA
V_{OL} Low Level Output Voltage	$V_{DD} = 5 \text{ V}$		0.05			0.05		0.05	V
	$V_{DD} = 10 \text{ V}$		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	$V_{DD} = 5 \text{ V}$	4.95		4.95			4.95		V
	$V_{DD} = 10 \text{ V}$	9.95		9.95			9.95		V
V_{NL} Noise Immunity (Note 3)	$V_{DD} = 5 \text{ V}, V_O = 1.4 \text{ V or } 3.6 \text{ V}$	1.5		1.5			1.4		V
	$V_{DD} = 10 \text{ V}, V_O = 2.8 \text{ V or } 7.2 \text{ V}$	3.0		3.0			2.9		V
V_{NH} Noise Immunity (Note 3)	$V_{DD} = 5 \text{ V}, V_O = 1.4 \text{ V or } 3.6 \text{ V}$	1.4		1.5			1.5		V
	$V_{DD} = 10 \text{ V}, V_O = 2.8 \text{ V or } 7.2 \text{ V}$	2.9		3.0			3.0		V
I_{DN} Low Level Output Current	$V_{DD} = 5 \text{ V}, V_O = 0.4 \text{ V}$	0.5		0.4			0.28		mA
	$V_{DD} = 10 \text{ V}, V_O = 0.5 \text{ V}$	1.1		0.9			0.65		mA
I_{DP} High Level Output Current	$V_{DD} = 5 \text{ V}, V_O = 2.5 \text{ V}$	-0.62		-0.5			-0.35		mA
	$V_{DD} = 10 \text{ V}, V_O = 9.5 \text{ V}$	-0.62		-0.5			-0.35		mA
I_{IN} Input Current	$V_{DD} = 15 \text{ V}, V_{IN} = 0 \text{ V}$	-1.0		-0.1	-10^{-5}		-1.0		μA
	$V_{DD} = 15 \text{ V}, V_{IN} = 15 \text{ V}$		1.0		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0 \text{ V}$ unless otherwise specified.

Note 3: For the NOR gates V_{NH} and V_{NL} are tested at each input while all other inputs are at V_{SS} .

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For explanation see 54C/74C Family Characteristics application note, AN-90.

AC Electrical Characteristics CD4000M $T_A = 25^{\circ}\text{C}$, $C_L = 50 \text{ pF}$, unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} Propagation Delay Time, High to Low Level	$V_{DD} = 5 \text{ V}$		40	50	ns
	$V_{DD} = 10 \text{ V}$		20	40	ns
t_{PLH} Propagation Delay Time, Low to High Level	$V_{DD} = 5 \text{ V}$		50	95	ns
	$V_{DD} = 10 \text{ V}$		25	45	ns
t_{THL} Transition Time, High to Low Level	$V_{DD} = 5 \text{ V}$		50	125	ns
	$V_{DD} = 10 \text{ V}$		20	70	ns
t_{TLH} Transition Time, Low to High Level	$V_{DD} = 5 \text{ V}$		70	175	ns
	$V_{DD} = 10 \text{ V}$		35	75	ns
C_I Input Capacitance	Any Input		5		pF
C_{PD} Power Dissipation Capacitance	(Note 4)		35		pF

DC Electrical Characteristics C4000C (Note 2)

PARAMETER	CONDITIONS	-40°C		+25°C			+85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current		0.5 5			0.5 5		15 30	μA μA
V_{OL}	Low Level Output Voltage		0.05 0.05			0.05 0.05		0.05 0.05	V V
V_{OH}	High Level Output Voltage	4.95 9.95		4.95 9.95			4.95 9.95		V V
V_{NL}	Noise Immunity (Note 3)								
	$V_{DD} = 5 V, V_O = 1.4 V \text{ or } 3.6 V$	1.5		1.5			1.4		V
	$V_{DD} = 10 V, V_O = 2.8 V \text{ or } 7.2 V$	3.0		3.0			2.9		V
V_{NH}	Noise Immunity (Note 3)								
	$V_{DD} = 5 V, V_O = 1.4 V \text{ or } 3.6 V$	1.4		1.5			1.5		V
	$V_{DD} = 10 V, V_O = 2.8 V \text{ or } 7.2 V$	2.9		3.0			3.0		V
I_{DN}	Low Level Output Current		0.35 0.72		0.3 0.6			0.24 0.48	mA mA
I_{DP}	High Level Output Current		-0.35 -0.3		-0.3 -0.25			-0.24 -0.2	mA mA
I_{IN}	Input Current		-0.3	-0.3	-10^{-5} -10^{-5}		-1.0		μA μA
	$V_{DD} = 15 V, V_{IN} = 0 V$								
	$V_{DD} = 15 V, V_{IN} = 15 V$		0.3			0.1		1.0	

AC Electrical Characteristics CD4000C $T_A = 25^\circ C$, $C_L = 50 \text{ pF}$, unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High to Low Level		40 20	80 55	ns ns
	$V_{DD} = 5 V$ $V_{DD} = 10 V$				
t_{PLH}	Propagation Delay Time, Low to High Level		50 25	120 65	ns ns
	$V_{DD} = 5 V$ $V_{DD} = 10 V$				
t_{THL}	Transition Time, High to Low Level		50 20	200 115	ns ns
	$V_{DD} = 5 V$ $V_{DD} = 10 V$				
t_{TLH}	Transition Time, Low to High Level		70 35	300 125	ns ns
	$V_{DD} = 5 V$ $V_{DD} = 10 V$				
C_I	Input Capacitance	Any Input	5		pF
C_{PD}	Power Dissipation Capacitance	(Note 4)	35		pF