National Semiconductor

February 1988

CD4009M/CD4009C Hex Buffers (Inverting)
CD4010M/CD4010C Hex Buffers (Non-Inverting)

General Description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface or as CMOS current drivers. Conversion ranges are from 3V to 15V providing $V_{CC} \leq V_{DD}$.

Features

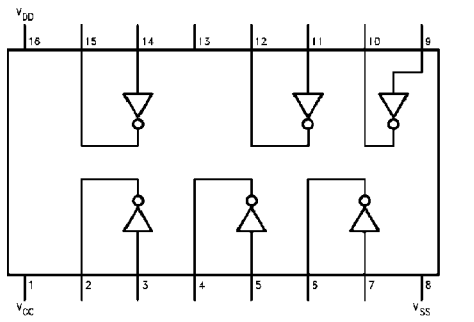
■ Wide supply voltage range	3.0V to 15V
■ Low power	100 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)
■ High current sinking capability	8 mA (min.) at V_O = 0.5V and V_{DD} = 10V

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Schematic and Connection Diagrams

Dual-In-Line Package



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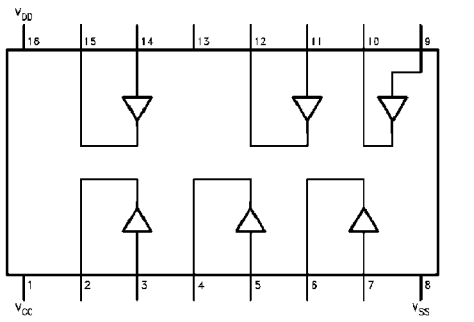
Top View

Dual-In-Line Package



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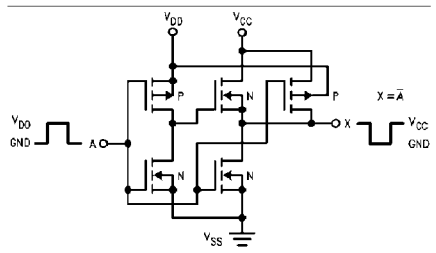
Top View

Order Number CD4009 or CD4010

CD4009M/CD4009C



Hex COS/MOS to DTL or TTL converter (non-inverting).

Connect V_{CC} to DTL or TTL supply.

Connect V_{DD} to COS/MOS supply.

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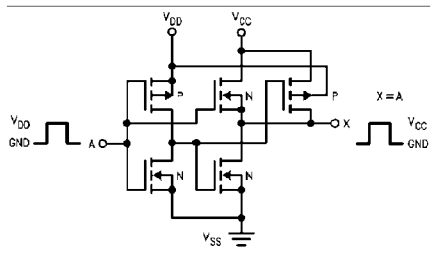
CD4010M/CD4010C



Hex COS/MOS to DTL or TTL converter (inverting).

Connect V_{CC} to DTL or TTL supply.

Connect V_{DD} to COS/MOS supply.

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  RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD40XXM	−55°C to +125°C
CD40XXC	−45°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
Operating Range (V_{DD})	V_{SS} + 3V to V_{SS} + 15V

DC Electrical Characteristics

Symbol	Characteristics	Test Conditions (Volts)		Limits														Units
				CD40XXM							CD40XXC							
				−55°C		+25°C			+125°C		−40°C		+25°C			+85°C		
		V_O	V_{DD}	Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
I_{CC}	Quiescent Device Current		5		0.3		0.01	0.3		20		3		0.03	3		42	μA
			10		0.5		0.01	0.5		30		5		0.05	5		70	μA
P_D	Quiescent Device Dissipation/Package		5		1.5		0.05	1.5		100		15		0.15	15		210	μW
			10		5		0.1	5		300		50		0.5	50		700	μW
V_{OL}	Output Voltage Low Level		5		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
			10		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
V_{OH}	High Level		5	4.99		4.99	5		4.95		4.99		4.99	5		4.95		V
			10	9.99		9.99	10		9.95		9.99		9.99	10		9.95		V
	Noise Immunity (All Inputs)																	
V_{NL}	CD4009M	$V_O \geq 4.0$	5	1		1	2.25		0.9		1		1	2.25		0.9		V
		$V_O \geq 8.0$	10	2		2	4.5		1.9		2		2	4.5		1.9		V
V_{NL}	CD4010M	$V_O \geq 1.5$	5	1.6		1.5	2.25		1.4		1.6		1.5	2.25		1.4		V
		$V_O \geq 3.0$	10	3.2		3	4.5		2.9		3.2		3	4.5		2.9		V
V_{NH}		$V_O \geq 3.5$	5	1.4		1.5	2.25		1.5		1.4		1.5	2.25		1.5		V
		$V_O \geq 7.0$	10	2.9		3	4.5		3		2.9		3	4.5		3		V
	Output Drive Current	0.4	5	3.75		3	4		2.1		3.6		3			2.4		mA
I_DN	N-Channel (Note 2)	0.5	10	10		8	10		5.6		9.6		8			6.4		mA
I_DP	P-Channel (Note 2)	2.5	5	−1.85		−1.25	−1.75		−0.9		−1.5		−1.25			−1		mA
		9.5	10	−0.9		−0.6	−0.8		−0.4		−0.72		−0.6			−0.48		mA
I_{IN}	Input Current						10							10				pA

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

Note 2: I_DN and I_DP are tested one output at a time.

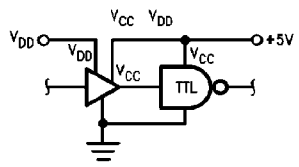
AC Electrical Characteristics*

T_A = 25°c, C_L = 15 pF, unless otherwise noted. Typical Temperature coefficient for all values of V_{DD} = 0.3%/°C

Characteristics	Test Conditions		Limits						Units
			CD40XXM			CD40XXC			
		V_{DD} (Volts)	Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time: High-to-Low Level (t_{PHL})	$V_{CC} = V_{DD}$	5	—	15	55	—	15	70	ns
		10	—	10	30	—	10	40	
	V_{DD} = 10V, V_{CC} = 5V		—	10	25	—	10	35	
Low-to-High Level (t_{PLH})	$V_{CC} = V_{DD}$	5	—	50	80	—	50	100	
		10	—	25	55	—	25	70	
	V_{DD} = 10V, V_{CC} = 5V		—	15	30	—	15	40	ns
Transition Time: High-to-Low Level (t_{THL})	$V_{CC} = V_{DD}$	5	—	20	45	—	20	60	ns
		10	—	16	40	—	16	50	
Low-to-High Level (t_{TLH})	$V_{CC} = V_{DD}$	5	—	80	125	—	80	160	ns
		10	—	50	100	—	50	120	
Input Capacitance (C_I)	Any Input		—	5	—	—	5	—	pF

*AC Parameters are guaranteed by DC correlated testing.

Typical Application



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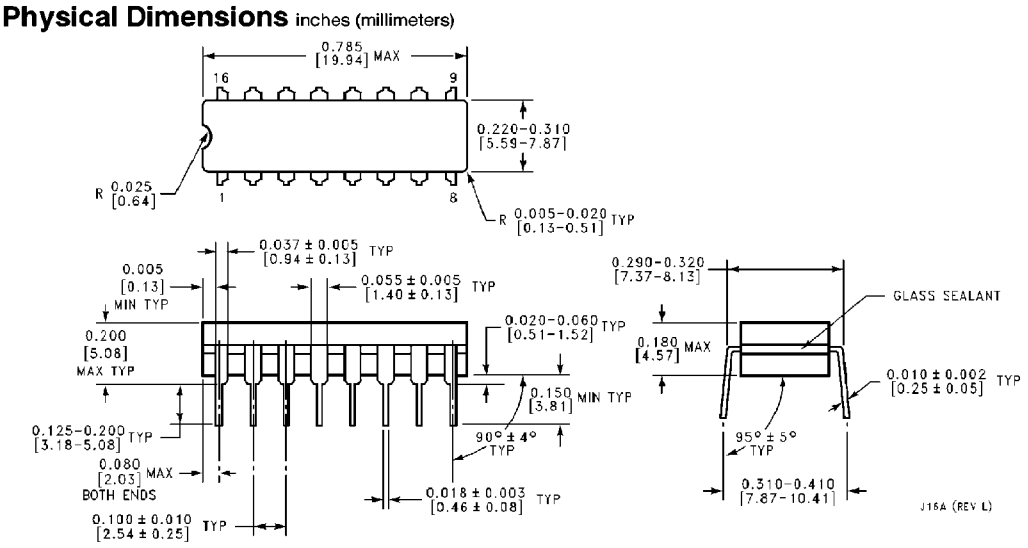
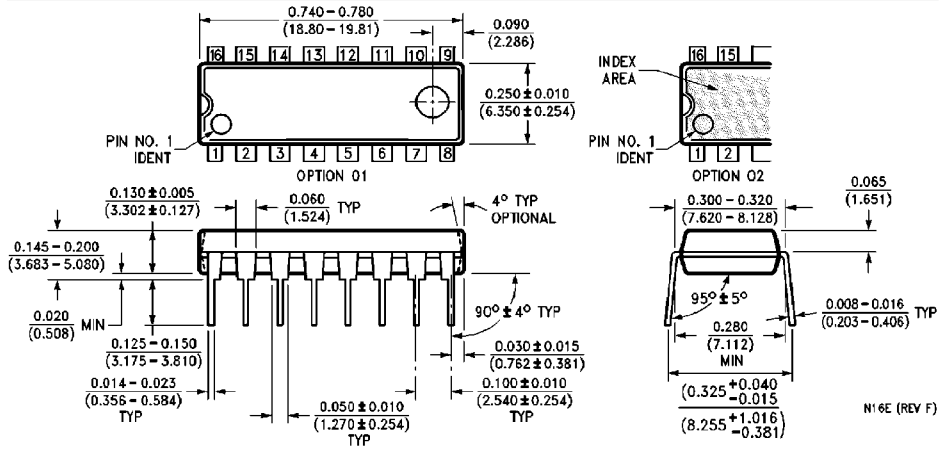
Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4009MJ, CD4009CJ, CD4010MJ or CD4010CJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD4009MN, CD4009CN, CD4010MN or CD4010CN
NS Package Number N16E

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