



CD40160BM/CD40160BC Decade Counter with Asynchronous Clear **CD40161BM/CD40161BC Binary Counter with Asynchronous Clear** **CD40162BM/CD40162BC Decade Counter with Synchronous Clear** **CD40163BM/CD40163BC Binary Counter with Synchronous Clear**

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the CD40162B and CD40163B is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the CD40160B and CD40161B is asynchronous and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

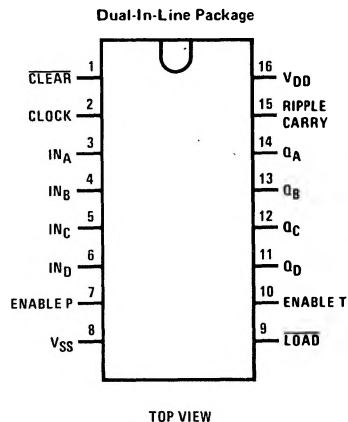
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can

be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity $0.45 V_{DD}$ (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Internal look-ahead for fast counting schemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable
- Equivalent to MC14160B, MC14161B, MC14162B, MC14163B
- Equivalent to MM74C160, MM74C161, MM74C162, MM74C163

Connection Diagram



CD40160BM/CD40160BC, CD40161BM/CD40161BC,
CD40162BM/CD40162BC, CD40163BM/CD40163BC

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	-0.5 to +18 VDC
V_{IN} Input Voltage	-0.5 to V_{DD} +0.5 VDC
T_S Storage Temperature Range	-65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 VDC
V_{IN} Input Voltage	0 to V_{DD} VDC
T_A Operating Temperature Range	-55°C to +125°C
CD40XXxBM	-40°C to +85°C
CD40XXxBBC	

DC Electrical Characteristics CD40160BC/CD40162BC/CD40163BC (Note 2)

PARAMETER	CONDITIONS	-55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		5			5		150	μA
	$V_{DD} = 10V$		10			10		300	μA
	$V_{DD} = 15V$		20			20		600	μA
V_{OL} Low Level Output Voltage	$ I_O < 1\mu A$								
	$V_{DD} = 5V$		0.05			0.05		0.05	V
	$V_{DD} = 10V$		0.05			0.05		0.05	V
	$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	$ I_O < 1\mu A$								
	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5			1.5		1.5	V
	$V_{DD} = 10V, V_O = 1V$ or 9V		3.0			3.0		3.0	V
	$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5			3.5		V
	$V_{DD} = 10V, V_O = 1V$ or 9V	7.0		7.0			7.0		V
	$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
	$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
	$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
	$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
	$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN} Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.10		-10^{-5}	-0.10		-1.0	μA
	$V_{DD} = 15V, V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD40160BM/CD40162BM/CD40163BM (Note 2)

PARAMETER	CONDITIONS	-40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		20			20		150	μA
	$V_{DD} = 10V$		40			40		300	μA
	$V_{DD} = 15V$		80			80		600	μA
V_{OL} Low Level Output Voltage	$ I_O < 1\mu A$								
	$V_{DD} = 5V$		0.05			0.05		0.05	V
	$V_{DD} = 10V$		0.05			0.05		0.05	V
	$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	$ I_O < 1\mu A$								
	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5			1.5		1.5	V
	$V_{DD} = 10V, V_O = 1V$ or 9V		3.0			3.0		3.0	V
	$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD40160BC/CD40161BC/CD40162BC/CD40163BC (Note 2)

PARAMETER	CONDITIONS	-40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V _{IH} High Level Input Voltage	V _{DD} = 5V, V _O = 0.5V or 4.5V	3.5		3.5			3.5		V
	V _{DD} = 10V, V _O = 1V or 9V	7.0		7.0			7.0		V
	V _{DD} = 15V, V _O = 1.5V or 13.5V	11.0		11.0			11.0		V
I _{OL} Low Level Output Current	V _{DD} = 5V, V _O = 0.4V	0.52		0.44	0.88		0.36		mA
	V _{DD} = 10V, V _O = 0.5V	1.3		1.1	2.25		0.9		mA
	V _{DD} = 15V, V _O = 1.5V	3.6		3.0	8.8		2.4		mA
I _{OH} High Level Output Current	V _{DD} = 5V, V _O = 4.6V	-0.52		-0.44	-0.88		-0.36		mA
	V _{DD} = 10V, V _O = 9.5V	-1.3		-1.1	-2.25		-0.9		mA
	V _{DD} = 15V, V _O = 13.5V	-3.6		-3.0	-8.8		-2.4		mA
I _{IN} Input Current	V _{DD} = 15V, V _{IN} = 0V		-0.30		-10 ⁻⁵	-0.30		-1.0	μA
	V _{DD} = 15V, V _{IN} = 15V		0.30		10 ⁻⁵	0.30		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

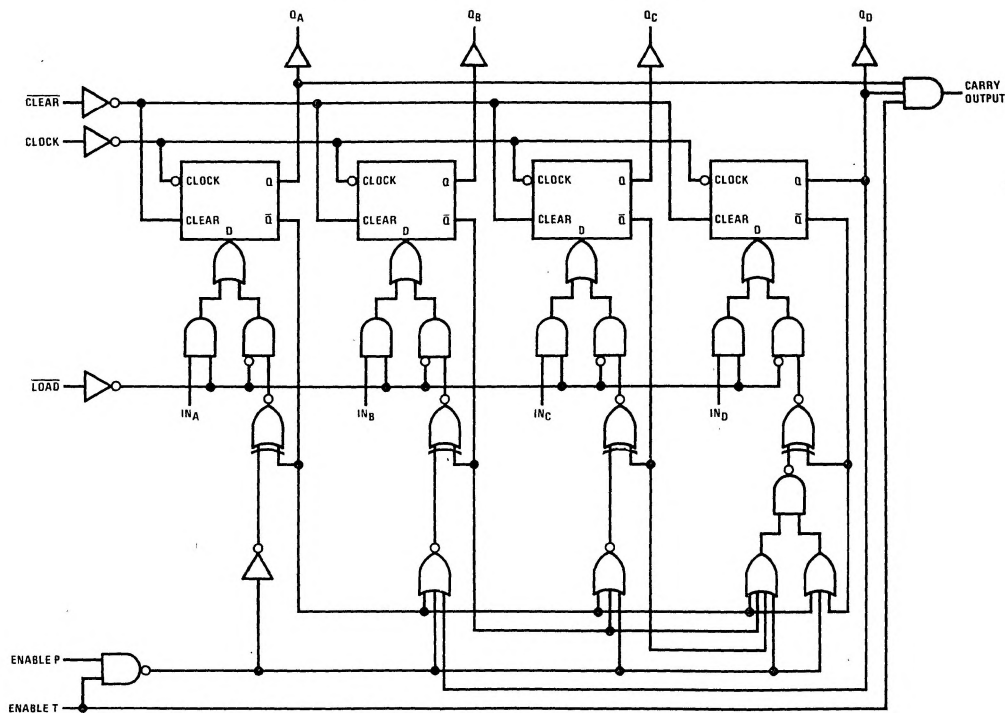
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-80.

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, unless otherwise specified.

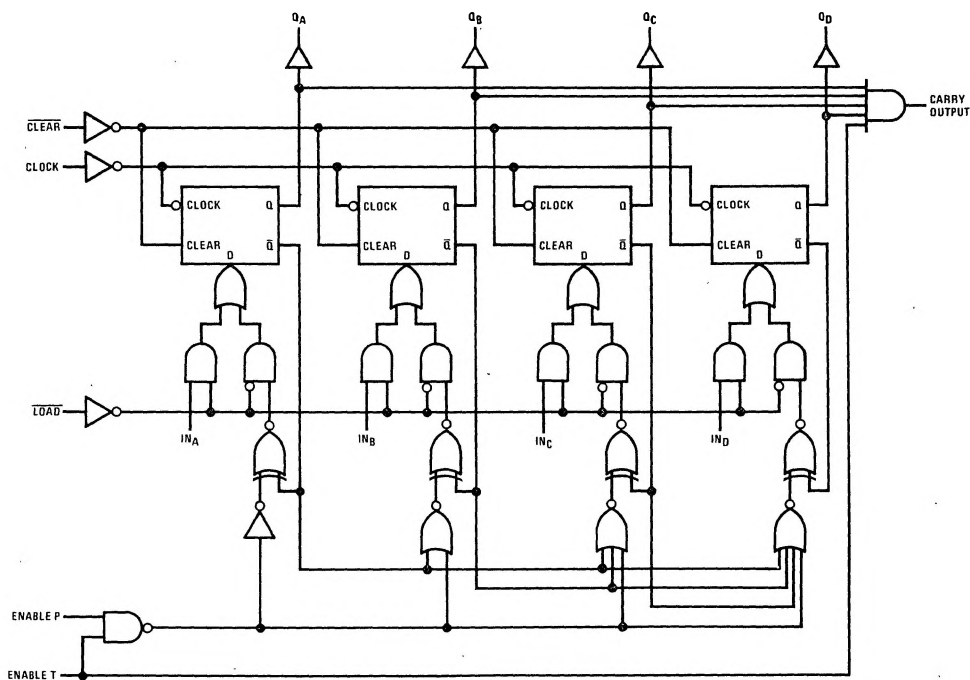
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t _{PHL} or t _{PLH} Propagation Delay Time From Clock to Q	V _{DD} = 5V		250	400	ns
	V _{DD} = 10V		100	160	ns
	V _{DD} = 15V		80	130	ns
t _{PHL} or t _{PLH} Propagation Delay Time From Clock to Carry Out	V _{DD} = 5V		290	450	ns
	V _{DD} = 10V		120	190	ns
	V _{DD} = 15V		100	160	ns
t _{PHL} or t _{PLH} Propagation Delay Time From T Enable to Carry Out	V _{DD} = 5V		180	290	ns
	V _{DD} = 10V		70	130	ns
	V _{DD} = 15V		60	110	ns
t _{PHL} Propagation Time From Clear to Q (CD40160B, CD40161B Only)	V _{DD} = 5V		190	300	ns
	V _{DD} = 10V		80	150	ns
	V _{DD} = 15V		70	120	ns
t _{SU} Minimum Time Prior to Clock that Data or Load must be Present	V _{DD} = 5V		120		ns
	V _{DD} = 10V		30		ns
	V _{DD} = 15V		25		ns
t _{SU} Minimum Time Prior to Clock that Enable P or T must be Present	V _{DD} = 5V		170	280	ns
	V _{DD} = 10V		70	120	ns
	V _{DD} = 15V		60	100	ns
t _{SU} Minimum Time Prior to Clock that Clear must be Present (CD40162B, CD40163B Only)	V _{DD} = 5V		120	190	ns
	V _{DD} = 10V		50	80	ns
	V _{DD} = 15V		40	70	ns
t _{WL} or t _{WH} Maximum Clock Pulse Width	V _{DD} = 5V		125	250	ns
	V _{DD} = 10V		45	90	ns
	V _{DD} = 15V		35	70	ns
t _{RCL} , t _{FCL} Maximum Clock Rise or Fall Time	V _{DD} = 5V			15	μs
	V _{DD} = 10V			5.0	μs
	V _{DD} = 15V			5.0	μs
f _{CL} Maximum Clock Frequency	V _{DD} = 5V	2	4		MHz
	V _{DD} = 10V	5.5	11		MHz
	V _{DD} = 15V	7	14		MHz
t _{THL} or t _{TLH} Transition Time	All Outputs				
	V _{DD} = 5V		100	200	ns
	V _{DD} = 10V		50	100	ns
	V _{DD} = 15V		40	80	ns
C _{IN} Average Input Capacitance	Any Input		5.0	7.5	pF
C _{PD} Power Dissipation Capacity	(Note 3)		95		pF

Logic Diagram

CD40160B, CD40162B Clear is Synchronous for the CD40162B

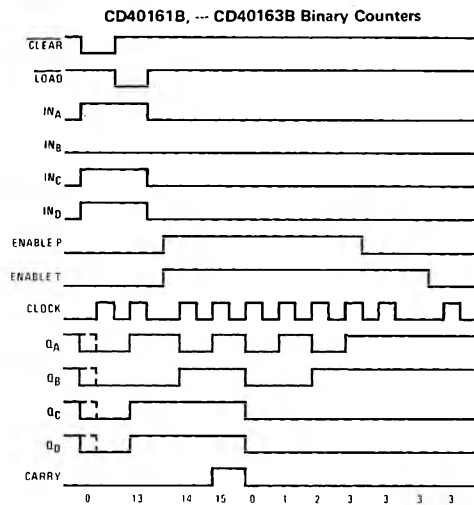
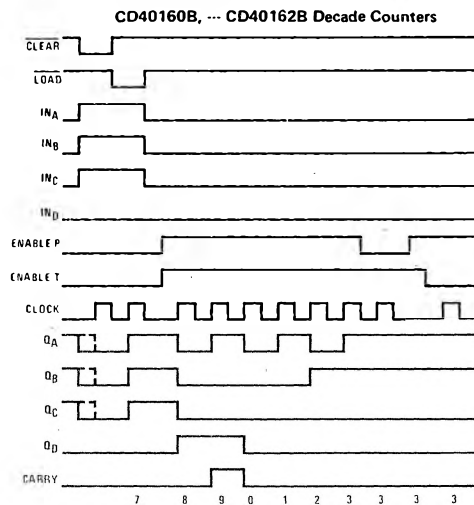


CD40161B, CD40163B Clear is Synchronous for the CD40163B

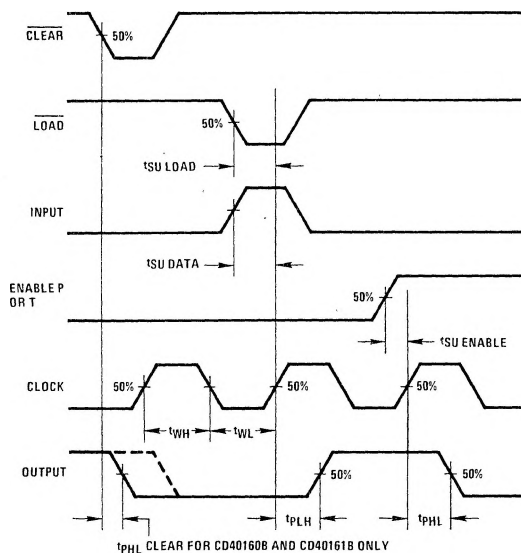


CD40160BM/CD40160BC, CD40161BM/CD40161BC,
CD40162BM/CD40162BC, CD40163BM/CD40163BC

Logic Waveforms



Switching Time Waveforms



Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f = 20 \text{ ns}$ $\text{PRR} \leq 1 \text{ MHz}$ duty cycle $\leq 50\%$, $Z_{\text{OUT}} \approx 60 \Omega$.

Note 2: All times are measured from 50% to 50%.

Cascading Packages

