CD40160BC,CD40160BM,CD40161BC,CD40161BM, CD40162BC,CD40162BM,CD40163BC,CD40163BM

CD40160BC CD40160BM Decade Counter with Asynchronous Clear CD40161BC CD40161BM Binary Counter with Asynchronous Clear CD40162BC CD40162BM Decade Counter with Synchronous Clear CD40163BC CD40163BM Binary Counter with Synchronous Clear

Literature Number: SNOS356A

National Semiconductor

March 1988

CD40160BM/CD40160BC Decade Counter with Asynchronous Clear
CD40161BM/CD40161BC Binary Counter with Asynchronous Clear
CD40162BM/CD40162BC Decade Counter with Synchronous Clear
CD40163BM/CD40163BC Binary Counter with Synchronous Clear

CD40160BM/BC Decade Counter with Asynchronous, CD40162BM/BC Synchronous Clear
CD40161BM/BC Binary Counter with Asynchronous, CD40163BM/BC Synchronous Clear

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the CD40162B and CD40163B is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the CD40160B and CD40161B is asynchronous and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

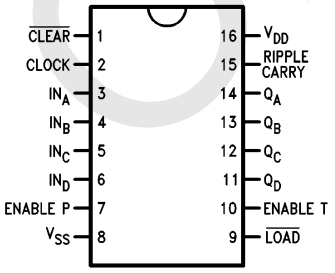
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Internal look-ahead for fast counting schemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable
- Equivalent to MC14160B, MC14161B, MC14162B, MC14163B
- Equivalent to MM74C160, MM74C161, MM74C162, MM74C163

Connection Diagram

Dual-In-Line Package



TL/F/5986–1

Top View

Order Number CD40160B, CD40161B, CD40162B or CD40163B

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to V_{DD} $+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD40XXXBM	$-55°C$ to $+125°C$
CD40XXXBC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD40160BM/CD40161BM/CD40162BM/CD40163BM (Note 2)

Symbol	Parameter	Conditions	Limits							Units
			$-55°C$		$+25°C$			$+125°C$		
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	-0.64		-0.51	-0.88		-0.36		mA
		V_{DD} = 10V, V_O = 9.5V	-1.6		-1.3	-2.25		-0.9		mA
		V_{DD} = 15V, V_O = 13.5V	-4.2		-3.4	-8.8		-2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		-0.10		-10^{-5}	-0.10		-1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD40160BC/CD40161BC/CD40162BC/CD40163BC (Note 2)

Symbol	Parameter	Conditions	Limits							Units
			$-40°C$		$+25°C$			$+85°C$		
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		0.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics CD40160BC/CD40161BC/CD40162BC/CD40163BC (Note 2) (Continued)

Symbol	Parameter	Conditions	Limits							Units
			−40°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V V_{DD} = 10V, V_O = 1V or 9V V_{DD} = 15V, V_O = 1.5V or 13.5V	3.5 7.0 11.0		3.5 7.0 11.0			3.5 7.0 11.0		V V V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V V_{DD} = 10V, V_O = 0.5V V_{DD} = 15V, V_O = 1.5V	0.52 1.3 3.6		0.44 1.1 3.0	0.88 2.25 8.8		0.36 0.9 2.4		mA mA mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V V_{DD} = 10V, V_O = 9.5V V_{DD} = 15V, V_O = 13.5V	−0.52 −1.3 −3.6		−0.44 −1.1 −3.0	−0.88 −2.25 −8.8		−0.36 −0.9 −2.4		mA mA mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V V_{DD} = 15V, V_{IN} = 15V		−0.30 0.30		-10^{-5} 10^{-5}	−0.30 0.30		−1.0 1.0	μA μA

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF, R_L = 200k, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Clock to Q	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		250 100 80	400 160 130	ns ns ns
t_{PHL} or t_{PLH}	Propagation Delay Time from Clock to Carry Out	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		290 120 100	450 190 160	ns ns ns
t_{PHL} or t_{PLH}	Propagation Delay Time from T Enable to Carry Out	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		180 70 60	290 130 110	ns ns ns
t_{PHL}	Propagation Time from Clear to Q (CD40160B, CD40161B Only)	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		190 80 70	300 150 120	ns ns ns
t_{SU}	Minimum Time Prior to Clock that Data or Load must be Present	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		120 30 25		ns ns ns
t_{SU}	Minimum Time Prior to Clock that Enable P or T must be Present	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		170 70 60	280 120 100	ns ns ns
t_{SU}	Minimum Time Prior to Clock that Clear must be Present (CD40162B, CD40163B Only)	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		120 50 40	190 80 70	ns ns ns
t_{WL} or t_{WH}	Maximum Clock Pulse Width	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		125 45 35	250 90 70	ns ns ns
t_{RCL} or t_{FCL}	Maximum Clock Rise or Fall Time	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V			15 5.0 5.0	μs μs μs
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V	2 5.5 7	4 11 14		MHz MHz MHz
t_{THL} or t_{TLH}	Transition Time	All Outputs V_{DD} = 5V V_{DD} = 10V V_{DD} = 15V		 100 50 40	 200 100 80	 ns ns ns
C_{IN}	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacity	(Note 4)		95		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

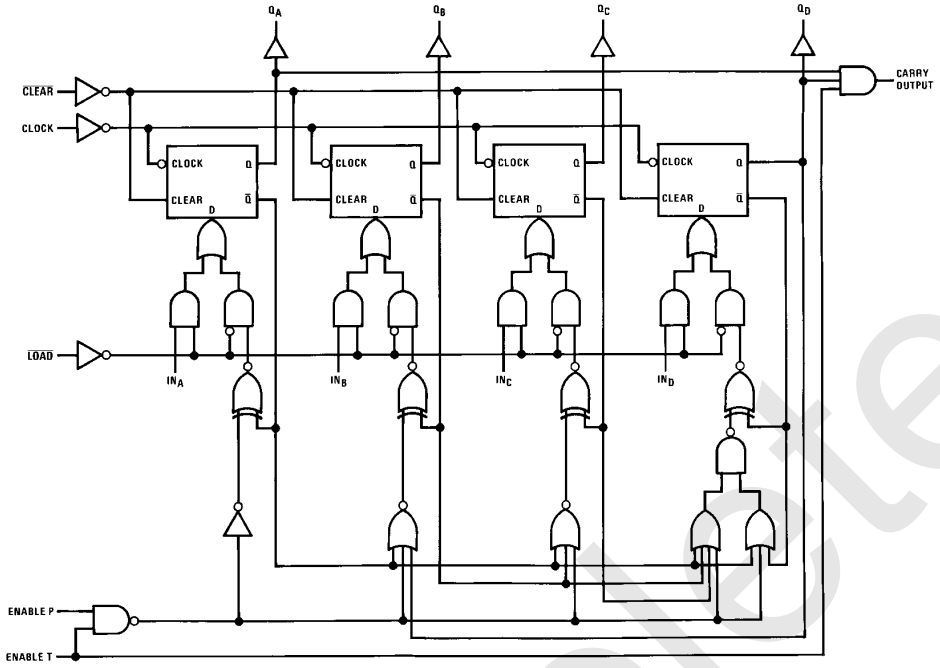
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

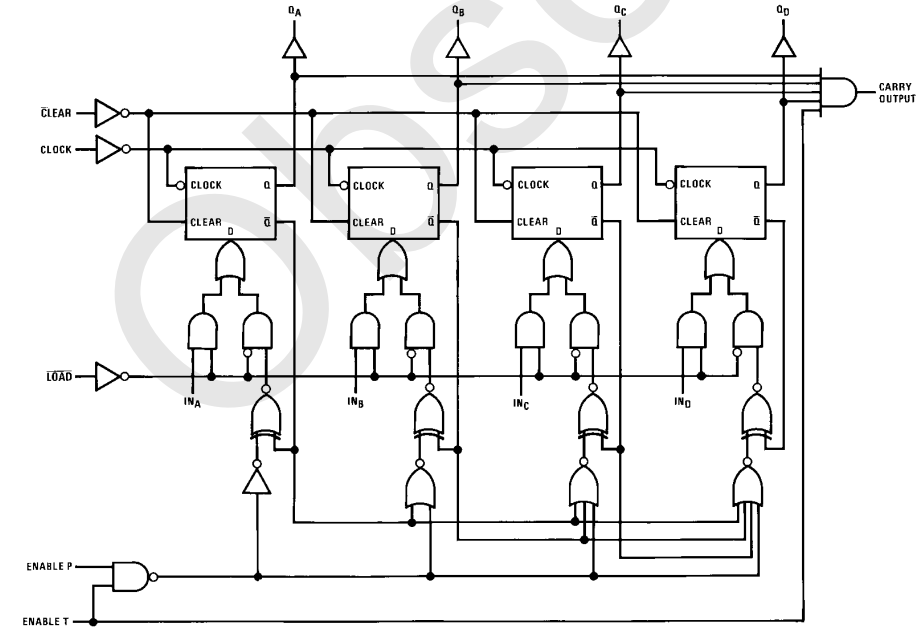
Logic Diagram

CD40160B, CD40162B Clear is Synchronous for the CD40162B



TL/F/5986–2

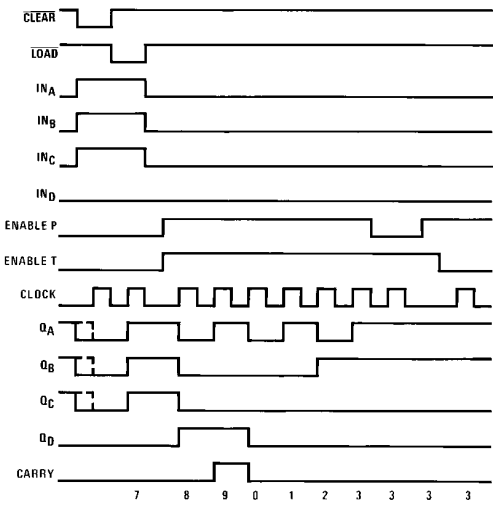
CD40161B, CD40163B Clear is Synchronous for the CD40163B



TL/F/5986–3

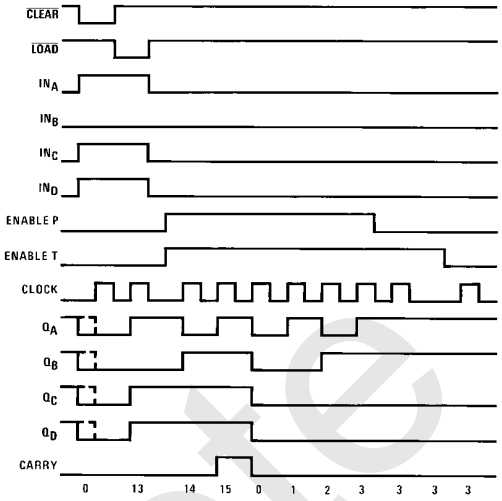
Logic Waveforms

CD40160B, . . . CD40162B Decade Counters



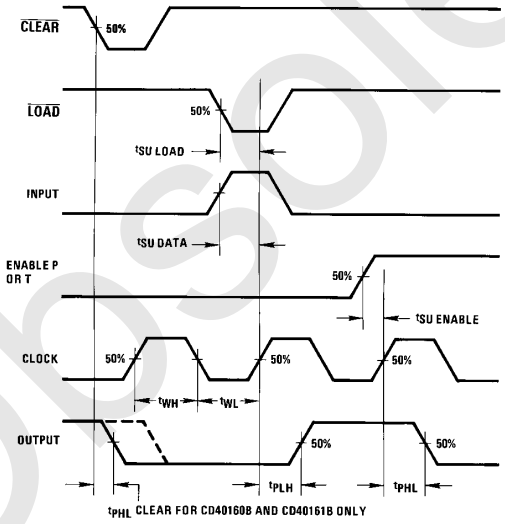
TL/F/5986–4

CD40161B, . . . CD40163B Binary Counters



TL/F/5986–5

Switching Time Waveforms

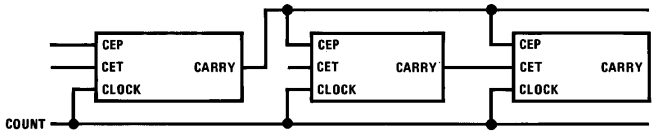


TL/F/5986–6

Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f = 20$ ns, PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

Cascading Packages



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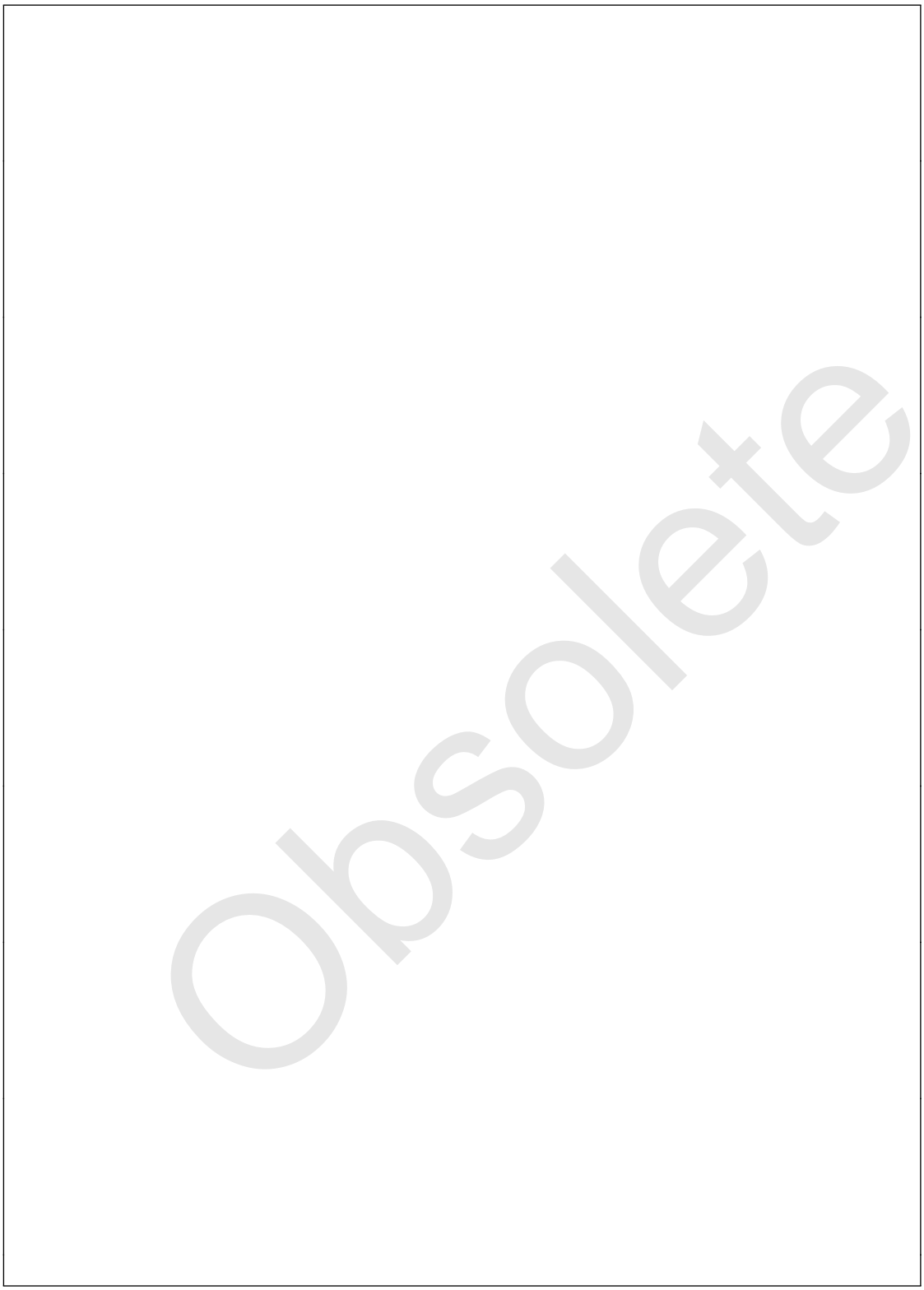
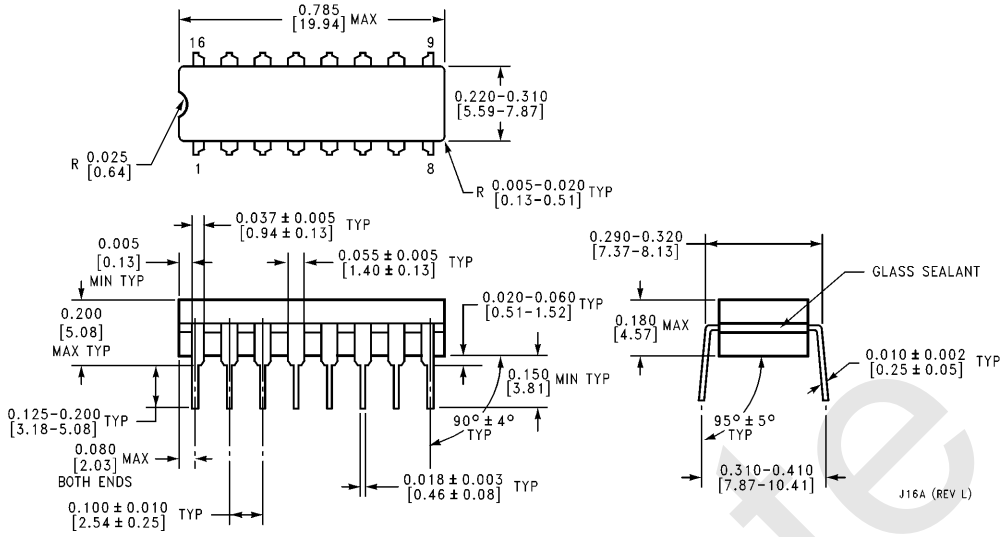
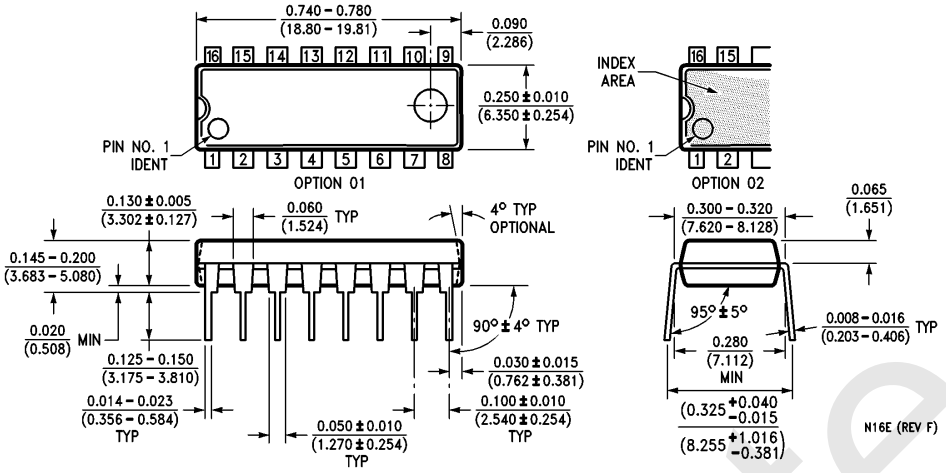

Obsolete

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD40160BMJ, CD40160BCJ, CD40161BMJ, CD40161BCJ, CD40162BMJ, CD40162BCJ, CD40163BMJ or CD40163BCJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number CD40160BMN, CD40160BCN, CD40161BMN, CD40161BCN, CD40162BMN, CD40162BCN, CD41063BMN or CD40163BCN
NS Package Number N16E

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