

CD40174BM/CD40174BC Hex D Flip-Flop CD40175BM/CD40175BC Quad D Flip-Flop

General Description

The CD40174B consists of six positive-edge triggered D-type flip-flops; the true output from each flip-flop are externally available. The CD40175B consists of four positive-edge triggered D-type flip-flops; both the true and complement outputs from each flip-flop are externally available.

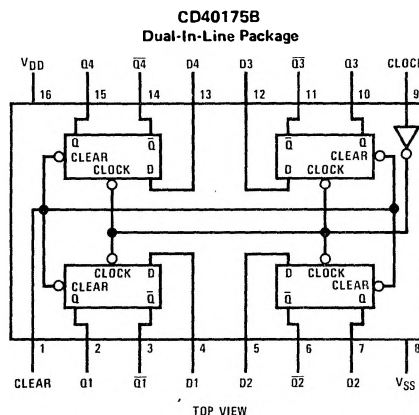
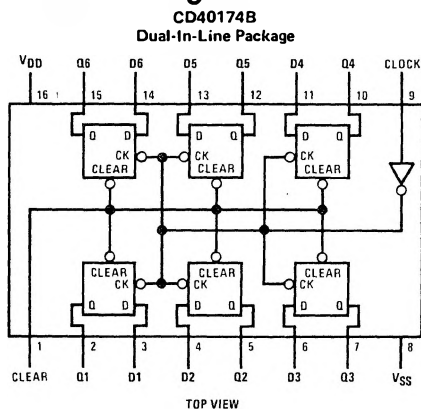
All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all Q outputs to logical "0" and $\bar{Q}$'s (CD40175B only) to logical "1."

All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS} .

Features

- Wide supply voltage range 3V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Equivalent to MC14174B, MC14175B
- Equivalent to MM74C174, MM74C175

Connection Diagrams



Truth Table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$ *
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level

L = Low level

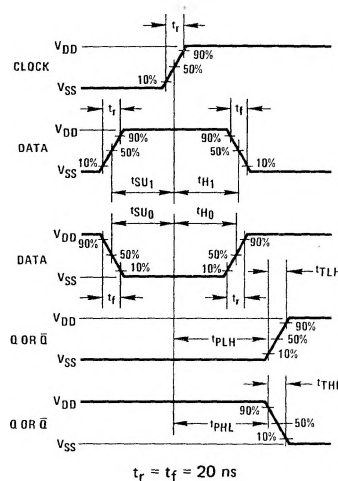
X = Irrelevant

↑ = Transition from low to high level

NC = No change

* = $\bar{Q}$ for CD40175B only

Switching Time Waveforms



Absolute Maximum Ratings

(Notes 1 and 2)

 V_{DD} dc Supply Voltage-0.5 to +18 V_{DC} V_{IN} Input Voltage-0.5 to $V_{DD} + 0.5 V_{DC}$ T_S Storage Temperature Range

-65°C to +150°C

 P_D Package Dissipation

500 mW

 T_L Lead Temperature, (Soldering, 10 seconds)

300°C

Recommended Operating Conditions

(Note 2)

 V_{DD} dc Supply Voltage3 to 15 V_{DC} V_{IN} Input Voltage0 to V_{DD} V_{DC} T_A Operating Temperature Range

-55°C to +125°C

CD40XXXBM

-40°C to +85°C

CD40XXXBC

DC Electrical Characteristics CD40174BM/CD40175BM (Note 2)

PARAMETER	CONDITIONS	-55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		1.0			1.0		30	μA
	$V_{DD} = 10V$		2.0			2.0		60	μA
	$V_{DD} = 15V$		4.0			4.0		120	μA
V_{OL} Low Level Output Voltage	$ I_{OL} < 1\mu A$								
	$V_{DD} = 5V$		0.05			0.05		0.05	V
	$V_{DD} = 10V$		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	$ I_{OL} < 1\mu A$								
	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$		1.5			1.5		1.5	V
	$V_{DD} = 10V, V_O = 1V \text{ or } 9V$		3.0			3.0		3.0	V
	$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$	3.5		3.5			3.5		V
	$V_{DD} = 10V, V_O = 1V \text{ or } 9V$	7.0		7.0			7.0		V
	$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
	$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
	$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5V, V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
	$V_{DD} = 10V, V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
	$V_{DD} = 15V, V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN} Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		-10^{-5}			-1.0	μA
	$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}			1.0	μA

DC Electrical Characteristics CD40174BC/CD40175BC/ (Note 2)

PARAMETER	CONDITIONS	-40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5V$		4			4		30	μA
	$V_{DD} = 10V$		8			8		60	μA
	$V_{DD} = 15V$		16			16		120	μA
V_{OL} Low Level Output Voltage	$V_{DD} = 5V$		0.05			0.05		0.05	V
	$V_{DD} = 10V$		0.05			0.05		0.05	V
	$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
	$V_{DD} = 10V$	9.95		9.95	10		9.95		V
	$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$		1.5			1.5		1.5	V
	$V_{DD} = 10V, V_O = 1V \text{ or } 9V$		3.0			3.0		3.0	V
	$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$	3.5		3.5			3.5		V
	$V_{DD} = 10V, V_O = 1V \text{ or } 9V$	7.0		7.0			7.0		V
	$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
	$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
	$V_{DD} = 15V, V_O = 1.5V$	3.6		8.0	8.8		2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5V, V_O = 4.6V$	-0.52		-0.41	-0.88		-0.36		mA
	$V_{DD} = 10V, V_O = 9.5V$	-1.3		-1.1	-2.25		-0.9		mA
	$V_{DD} = 15V, V_O = 13.5V$	-3.6		-8.0	-8.8		-2.4		mA
I_{IN} Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.30		-10^{-5}	-0.30		-1.0	μA
	$V_{DD} = 15V, V_{IN} = 15V$		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics

$T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}$, and $t_r = t_f = 20\text{ ns}$,
unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t _{PHL} or t _{PLH}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\bar{Q}$ (CD40175 Only)	V _{DD} = 5V		190	300	ns
		V _{DD} = 10V		75	110	ns
		V _{DD} = 15V		60	90	ns
t _{PHL}	Propagation Delay Time to a Logical "0" from Clear to Q	V _{DD} = 5V		180	300	ns
		V _{DD} = 10V		70	110	ns
		V _{DD} = 15V		60	90	ns
t _{PLH}	Propagation Delay Time to a Logical "1" from Clear to $\bar{Q}$ (CD40175 Only)	V _{DD} = 5V		230	400	ns
		V _{DD} = 10V		90	150	ns
		V _{DD} = 15V		75	120	ns
t _{SU}	Time Prior to Clock Pulse that Data must be Present	V _{DD} = 5V	100	45		ns
		V _{DD} = 10V	40	16		ns
		V _{DD} = 15V	35	13		ns
t _H	Time after Clock Pulse that Data must be Held	V _{DD} = 5V		-11	0	ns
		V _{DD} = 10V		-4	0	ns
		V _{DD} = 15V		-3	0	ns
t _{THL} or t _{TLH}	Transition Time	V _{DD} = 5V		100	200	ns
		V _{DD} = 10V		50	100	ns
		V _{DD} = 15V		40	80	ns
t _{WH} , t _{WL}	Minimum Clock Pulse Width	V _{DD} = 5V		130	250	ns
		V _{DD} = 10V		45	100	ns
		V _{DD} = 15V		40	80	ns
t _{WL}	Minimum Clear Pulse Width	V _{DD} = 5V		120	250	ns
		V _{DD} = 10V		45	100	ns
		V _{DD} = 15V		40	80	ns
t _{RCL}	Maximum Clock Rise Time	V _{DD} = 5V	15	450		μs
		V _{DD} = 10V	5.0	125		μs
		V _{DD} = 15V	5.0	125		μs
t _{fCL}	Maximum Clock Fall Time	V _{DD} = 5V	15	50		μs
		V _{DD} = 10V	5.0	50		μs
		V _{DD} = 15V	5	50		μs
f _{CL}	Maximum Clock Frequency	V _{DD} = 5V	2.0	3.5		MHz
		V _{DD} = 10V	5.0	10		MHz
		V _{DD} = 15V	6.0	12		MHz
C _{IN}	Input Capacitance	Clear Input,		10	15	pF
		Other Input		5.0	7.5	pF
C _{PD}	Power Dissipation	Per Package, (Note 3)		130		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.