National Semiconductor

CD4020BM/CD4020BC 14-Stage Ripple Carry Binary Counters
CD4040BM/CD4040BC 12-Stage Ripple Carry Binary Counters
CD4060BM/CD4060BC 14-Stage Ripple Carry Binary Counters

General Description

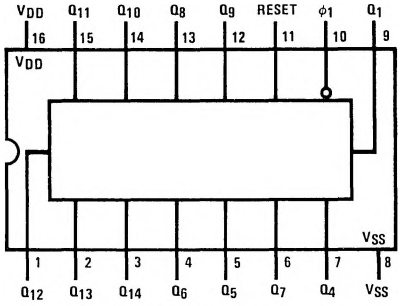
The CD4020BM/CD4020BC, CD4060BM/CD4060BC are 14-stage ripple carry binary counters, and the CD4040BM/CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

Features

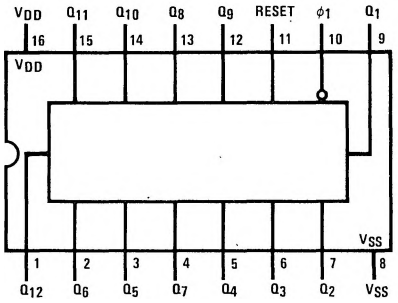
■ Wide supply voltage range	1.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	8 MHz typ. at V_{DD} = 10 V
■ Schmitt trigger clock input	

Connection Diagrams

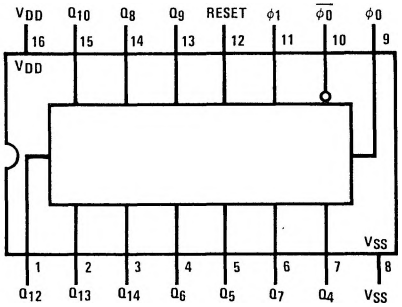
TOP VIEW



CD4020BM/CD4020BC



CD4040BM/CD4040BC



CD4060BM/CD4060BC

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5V to +18V
V_{IN}	Input Voltage	−0.5V to V_{DD} + 0.5V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

Recommended Operating Conditions

V_{DD}	Supply Voltage	+3V to +15V
V_{IN}	Input Voltage	0V to V_{DD}
T_A	Operating Temperature Range	
	CD40XXBM	−55°C to +125°C
	CD40XXBC	−40°C to +85°C

DC Electrical Characteristics CD40XXBM (Note 2)

PARAMETER		CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	(See Note 3)	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	(See Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		-0.10		-10^{-5}	-0.10		-1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Data does not apply to oscillator points ϕ_0 and $\overline{\phi_0}$ of CD4060BM/CD4060BC.

DC Electrical Characteristics 40XXBC (Note 2)

PARAMETER		CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.6	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics CD4020BM/CD4020BC, CD4040BM/CD4040BC

T_A = 25°C, C_L = 50pF, R_L = 200k, t_r = t_f = 20ns, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL1}, t_{PLH1}	Propagation Delay Time to Q_1	V_{DD} = 5V		250	550	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		75	150	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	V_{DD} = 5V		150	330	ns
		V_{DD} = 10V		60	125	ns
		V_{DD} = 15V		45	90	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{CD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	335	ns
		V_{DD} = 10V		50	125	ns
		V_{DD} = 15V		40	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V			no limit	ns
		V_{DD} = 10V			no limit	ns
		V_{DD} = 15V			no limit	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	4		MHz
		V_{DD} = 10V	4	10		MHz
		V_{DD} = 15V	5	12		MHz
$t_{PHL(R)}$	Reset Propagation Delay	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
C_{in}	Average Input Capacitance	Any Input (Note 1)		5	7.5	pF
C_{pd}	Power Dissipation Capacitance	(Note 2)		50		pF

Note 1: Capacitance guaranteed by periodic testing.

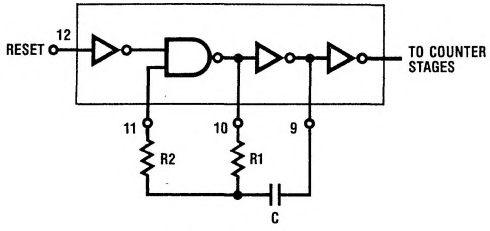
Note 2: Cpd determines the no-load etc.

AC Electrical Characteristics CD4060BM/CD4060BC $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, $t_r = t_f = 20\,ns$, unless otherwise noted

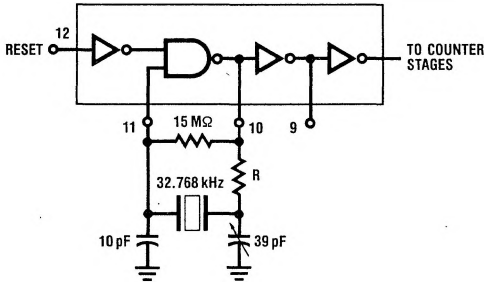
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL4}, t_{PLH4}	Propagation Delay Time to Q_4	$V_{DD} = 5V$		550	1300	ns
		$V_{DD} = 10V$		250	525	ns
		$V_{DD} = 15V$		200	400	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		170	500	ns
		$V_{DD} = 10V$		65	170	ns
		$V_{DD} = 15V$		50	125	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			no limit	ns
		$V_{DD} = 10V$			no limit	ns
		$V_{DD} = 15V$			no limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1	3		MHz
		$V_{DD} = 10V$	3	8		MHz
		$V_{DD} = 15V$	4	10		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
C_{in}	Average Input Capacitance	Any Input (Note 1)		5	7.5	pF
C_{pd}	Power Dissipation Capacitance	(Note 2)		50		pF

Note 1: Capacitance guaranteed by periodic testing.
Note 2: C_{pd} determines the no-load etc.

CD4060B Typical Oscillator Connections

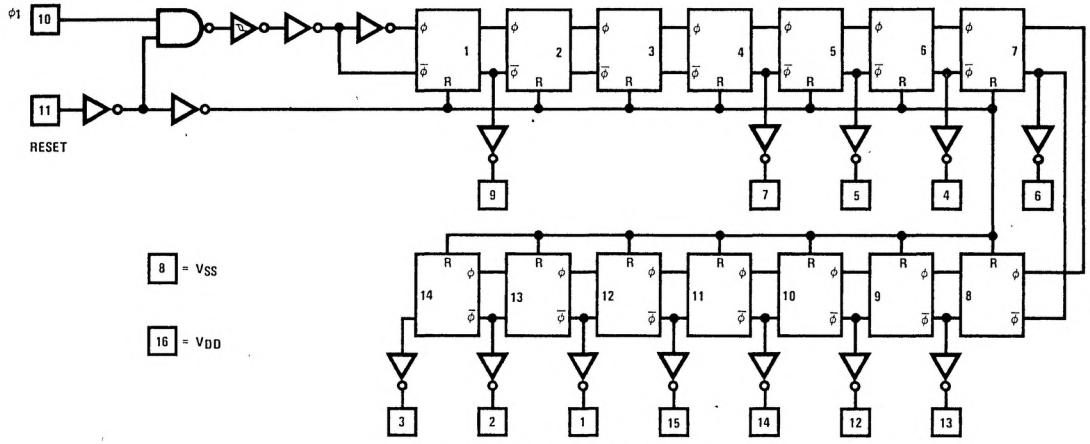


RC Oscillator

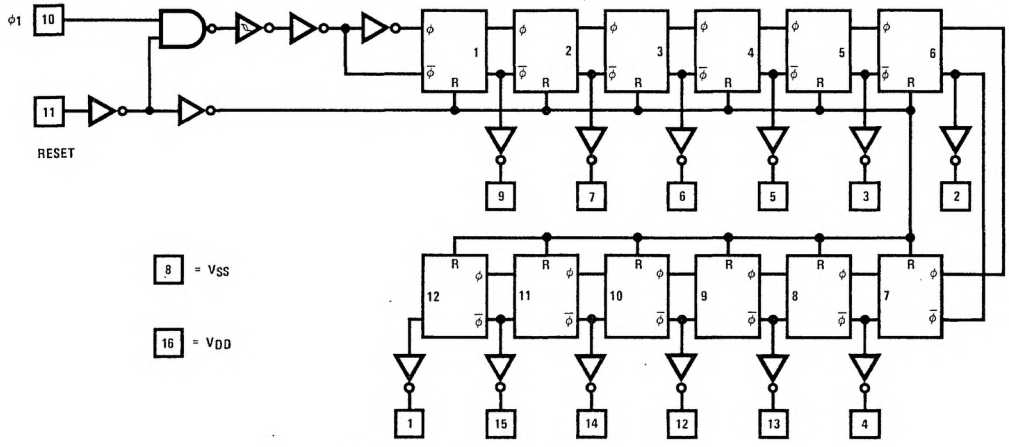


Crystal Oscillator

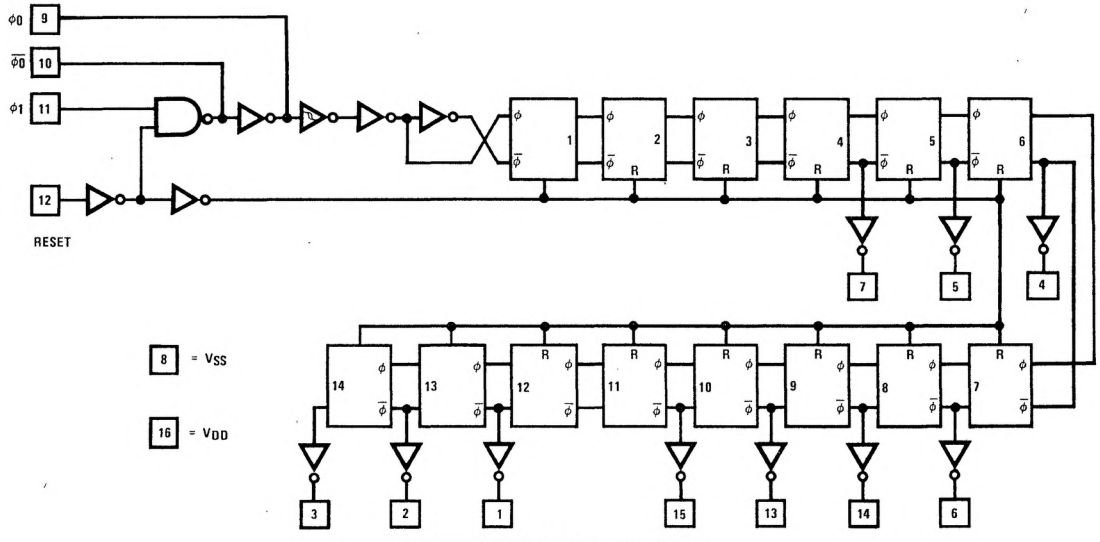
Schematic Diagrams



CD4020BM/CD4020BC Schematic Diagram



CD4040BM/CD4040BC Schematic Diagram



CD4060BM/CD4060BC Schematic Diagram