National Semiconductor

CD4031BM/CD4031BC 64-Stage Static Shift Register

General Description

The CD4031BM/CD4031BC is an integrated, complementary MOS (CMOS), 64-stage, fully static shift register. Two data inputs, DATA IN and RECIRCULATE IN, and a MODE CONTROL input are provided. Data at the DATA input (when MODE CONTROL is low) or data at the RECIRCULATE input (when MODE CONTROL is high), which meets the setup and hold time requirements, is entered into the first stage of the register and is shifted one stage at each positive transition of the CLOCK.

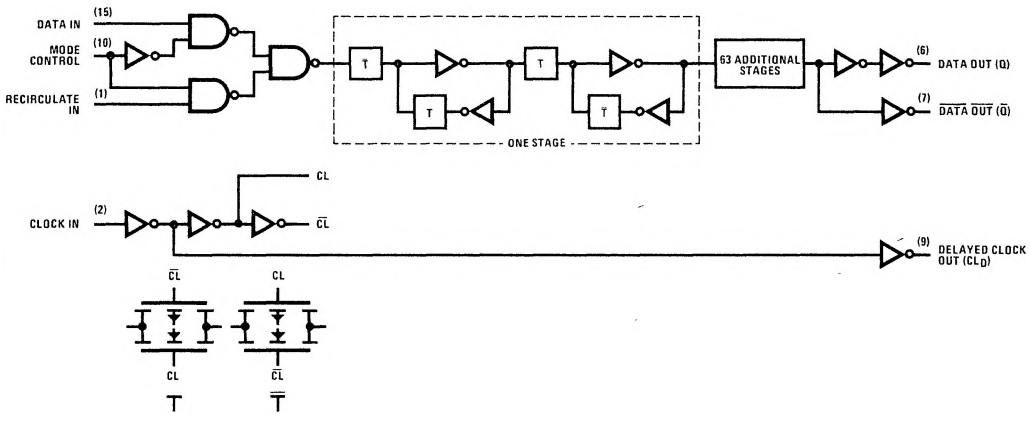
Data output is available in both true and complement forms from the 64th stage. Both the DATA OUT (Q) and $\overline{\text{DATA OUT}}$ ($\overline{Q}$) outputs are fully buffered.

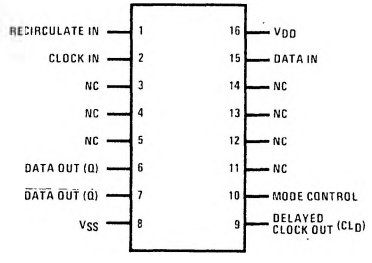
The CLOCK input of the CD4031BM/CD4031BC is fully buffered, and present only a standard input load capacitance. However, a DELAYED CLOCK OUTPUT (CL_D) has been provided to allow reduced clock drive fan-out and transition time requirements when cascading packages.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Fully static operation	DC to 8 MHz V_{DD} = 10 V (typ.)
■ Fully buffered clock input	5 pF (typ.) input capacitance
■ Single phase clocking requirements	
■ Delayed clock output for reduced clock drive requirements	
■ Fully buffered outputs	
■ High current sinking capability Q output	1.6 mA @ V_{DD} = 5 V and 25°C

Logic and Connection Diagrams





Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5 V to +18 V
V_{IN}	Input Voltage	−0.5 V to V_{DD} + 0.5 V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD}	Supply Voltage	+3 V to +15 V
V_{IN}	Input Voltage	0 V to V_{DD}
T_A	Operating Temperature Range	
	CD4031BM	−55°C to +125°C
	CD4031BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) CD4031BM

PARAMETER		CONDITIONS	−55°C MIN	−55°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+125°C MIN	+125°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		5		0.01	5		150	μA
		V_{DD} = 10 V		10		0.01	10		300	μA
		V_{DD} = 15 V		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V, $\lvert I_O \rvert < 1\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95	5		4.95		V
		V_{DD} = 10 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V, $\lvert I_O \rvert < 1\,\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V, $\lvert I_O \rvert < 1\,\mu A$		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\lvert I_O \rvert < 1\,\mu A$		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V, $\lvert I_O \rvert < 1\,\mu A$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V, $\lvert I_O \rvert < 1\,\mu A$	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\lvert I_O \rvert < 1\,\mu A$	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V, $\lvert I_O \rvert < 1\,\mu A$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current, Q Output	V_{DD} = 5 V, V_O = 0.4 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	2.3		1.9	3.8		1.3		mA
		V_{DD} = 10 V, V_O = 0.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	5.1		4.2	8.4		2.8		mA
		V_{DD} = 15 V, V_O = 1.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	10.5		8.8	17		6.1		mA
I_{OL}	Low Level Output Current, $\overline{Q}$ and CL_D Outputs	V_{DD} = 5 V, V_O = 0.4 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current, All Outputs	V_{DD} = 5 V, V_O = 4.6 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-5}	0.1		1.0	μA

Truth Tables

MODE CONTROL (data selection)

MODE CONTROL	DATA IN	RECIRCULATE IN	DATA INTO FIRST STAGE
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

EACH STAGE

D_n	CL	Q_n
0	⌐	0
1	⌐	1
X	¬	NC

X = irrelevant
NC = no change
⌐ = Low to High level transition
¬ = High to Low level transition

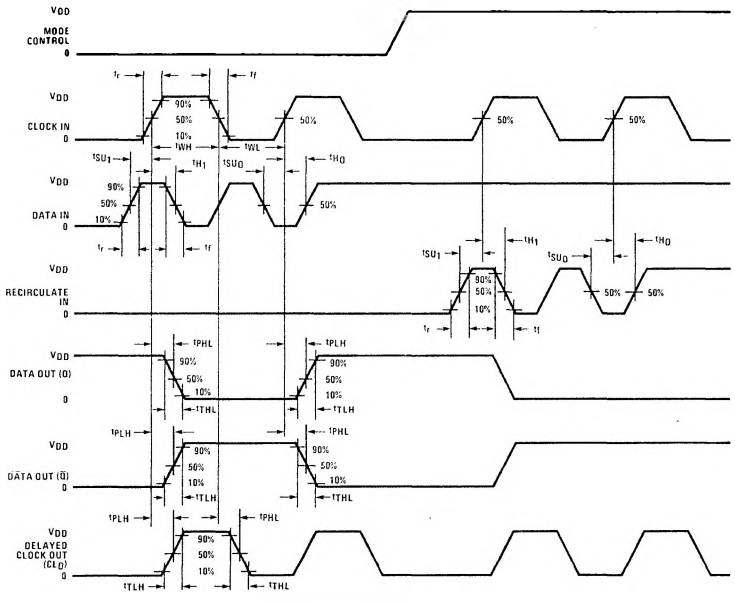
DC Electrical Characteristics (Note 2) CD4031BC

PARAMETER		CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		20		0.01	20		150	μA
		V_{DD} = 10 V		40		0.01	40		300	μA
		V_{DD} = 15 V		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95	5		4.95		V
		V_{DD} = 10 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V, $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\lvert I_O \rvert < 1\ \mu A$		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\lvert I_O \rvert < 1\ \mu A$	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current, Q Output	V_{DD} = 5 V, V_O = 0.4 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	1.8		1.6	3.8		1.3		mA
		V_{DD} = 10 V, V_O = 0.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	4.0		3.5	8.4		2.8		mA
		V_{DD} = 15 V, V_O = 1.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	8.7		7.5	17		6.1		mA
I_{OL}	Low Level Output Current, $\overline{Q}$ and CL_D Outputs	V_{DD} = 5 V, V_O = 0.4 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current, All Outputs	V_{DD} = 5 V, V_O = 4.6 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

Switching Time Waveforms



AC Electrical Characteristics

$T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock to Q and $\overline{Q}$	$V_{CC} = 5\,V$		300	600	ns
		$V_{CC} = 10\,V$		125	250	ns
		$V_{CC} = 15\,V$		100	200	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock to CL_D	$V_{CC} = 5\,V$		125	250	ns
		$V_{CC} = 10\,V$		60	125	ns
		$V_{CC} = 15\,V$		50	100	ns
t_{THL}, t_{TLH}	Output Transition Time, All Outputs	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{SU_0} t_{SU_1}	Minimum Data Setup Time, DATA IN or RECIRCULATE IN to Clock	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{H_0} t_{H_1}	Minimum Data Hold Time, Clock to DATA IN or RECIRCULATE IN	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{CC} = 5\,V$		150	300	ns
		$V_{CC} = 10\,V$		60	125	ns
		$V_{CC} = 15\,V$		50	100	ns
f_{CL}	Maximum Clock Frequency	$V_{CC} = 5\,V$	1.6	3.2		MHz
		$V_{CC} = 10\,V$	4.0	8.0		MHz
		$V_{CC} = 15\,V$	5.0	10		MHz
t_{RCL}, t_{FCL}	Maximum Clock Input Rise and Fall Times (Note 3)	$V_{CC} = 5\,V$	15			μs
		$V_{CC} = 10\,V$	10			μs
		$V_{CC} = 15\,V$	5			μs
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

Note 3: When clocking cascaded packages in parallel, one should insure that: $t_{r\,CL} \leq 2(t_{PD} - t_H)$ where: t_{PD} = the propagation delay of the driving stage and t_H = the hold time of the driven stage.

Block Diagram

cascading packages using DELAYED CLOCK (CL_D) output