National Semiconductor

CD4034BM/CD4034BC 8-State TRI-STATE® Bidirectional Parallel/Serial Input/Output Bus Register

General Description

The CD4034BM/CD4034BC is an 8-bit CMOS static shift register with two parallel bidirectional data ports (A and B) which, when combined with serial shifting operations, can be used to (1) bidirectionally transfer parallel data between two buses, (2) convert serial data to parallel form and direct them to either of two buses, (3) store (recirculate) parallel data, or (4) accept parallel data from either of two buses and convert them to serial form. These operations are controlled by five control inputs:

A ENABLE (AE): "A" data port is enabled only when AE is at logical "1". This allows the use of a common bus for multiple packages.

A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B): This input controls the direction of data flow. When at logical "1", data flows from port A to B (A is input, B is output). When at logical "0", the data flow direction is reversed.

ASYNCHRONOUS/SYNCHRONOUS (A/S): When A/S is at logical "0", data transfer occurs at positive transition of the CLOCK. When A/S is at logical "1", data transfer is independent of the CLOCK for parallel operation. In serial mode, A/S input is internally disabled such that operation is always synchronous. (Asynchronous serial operation is not possible.)

PARALLEL/SERIAL (P/S): A logical "1" P/S input allows data transfer into the registers via A or B port (synchronous if A/S = logical "0", asynchronous if A/S = logical "1"). A logical "0" P/S allows serial data to transfer into the register synchronously with the positive transition of the CLOCK, independent of the A/S input.

CLOCK: Single phase, enabled only in synchronous mode. (Either P/S = logical "1" and A/S = logical "0" or P/S = logical "0".

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

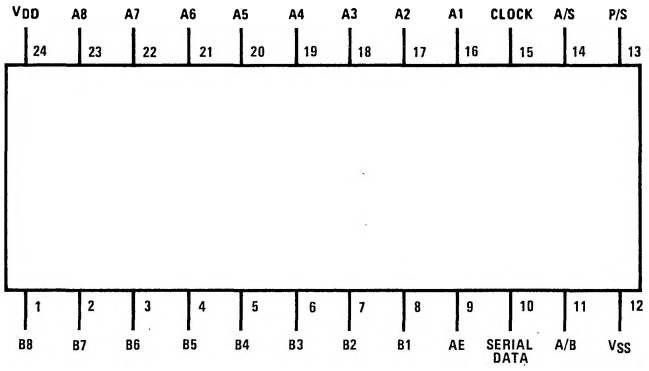
Features

- Wide supply voltage range — 3.0 to 18 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- RCA CD4034B second source

Applications

- Parallel Input/Parallel Output
  Parallel Input/Serial Output
  Serial Input/Parallel Output
  Serial Input/Serial Output register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storge, counting, display)
- Frequency and phase comparator

Connection Diagram



Absolute Maximum Ratings
(Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\,V_{DC}$ to $+18\,V_{DC}$
V_{IN}	Input Voltage	$-0.5\,V_{DC}$ to $V_{DD} + 0.5\,V_{DC}$
T_S	Storage Temperature Range	$-65°C$ to $+150°C$
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions
(Note 2)

V_{DD}	DC Supply Voltage	$+3\,V_{DC}$ to $+15\,V_{DC}$
V_{IN}	Input Voltage	$0\,V_{DC}$ to $V_{DD}\,V_{DC}$
T_A	Operating Temperature Range	
	CD4034BM	$-55°C$ to $+125°C$
	CD4034BC	$-40°C$ to $+85°C$

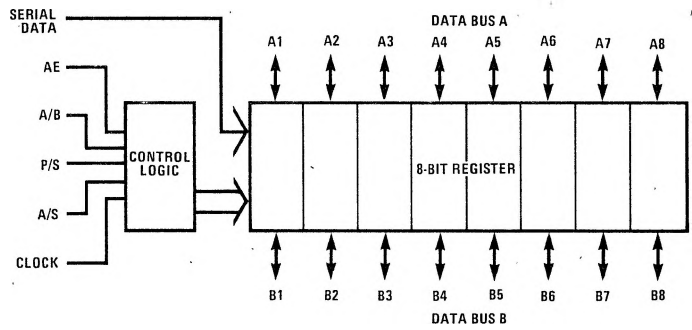
DC Electrical Characteristics CD4034BM (Note 2)

PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5\,V$		5			5		150	μA
	$V_{DD} = 10\,V$		10			10		300	μA
	$V_{DD} = 15\,V$		20			20		600	μA
V_{OL} Low Level Output Voltage	$V_{DD} = 5\,V$		0.05			0.05		0.05	V
	$V_{DD} = 10\,V$		0.05			0.05		0.05	V
	$V_{DD} = 15\,V$		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	$V_{DD} = 5\,V$	4.95		4.95			4.95		V
	$V_{DD} = 10\,V$	9.95		9.95			9.95		V
	$V_{DD} = 15\,V$	14.95		14.95			14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5\,V$, $V_O = 0.5\,V$ or $4.5\,V$		1.5			1.5		1.5	V
	$V_{DD} = 10\,V$, $V_O = 1.0\,V$ or $9.0\,V$		3.0			3.0		3.0	V
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$ or $13.5\,V$		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5\,V$, $V_O = 0.5\,V$ or $4.5\,V$	3.5		3.5			3.5		V
	$V_{DD} = 10\,V$, $V_O = 1.0\,V$ or $9.0\,V$	7.0		7.0			7.0		V
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$ or $13.5\,V$	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5\,V$, $V_O = 0.4\,V$	0.64		0.51			0.36		mA
	$V_{DD} = 10\,V$, $V_O = 0.5\,V$	1.6		1.3			0.9		mA
	$V_{DD} = 15\,V$, $V_O = 1.5\,V$	4.2		3.4			2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5\,V$, $V_O = 4.6\,V$	−0.64		−0.51			−0.36		mA
	$V_{DD} = 10\,V$, $V_O = 9.5\,V$	−1.6		−1.3			−0.9		mA
	$V_{DD} = 15\,V$, $V_O = 13.5\,V$	−4.2		−3.4			−2.4		mA
I_{IN} Input Current	$V_{DD} = 15\,V$, $V_{IN} = 0\,V$	−0.1		−0.1	-10^{-5}		−1.0		μA
	$V_{DD} = 15\,V$, $V_{IN} = 15\,V$		0.1		10^{-5}	0.1		1.0	μA
I_{OZ} Tri-State Leakage Current	$V_{DD} = 15\,V$, $V_O = 0\,V$	−0.1		−0.1	-10^{-5}		−1.0		μA
	$V_{DD} = 15\,V$, $V_O = 15\,V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0\,V$ unless otherwise specified.

Logic Diagram



DC Electrical Characteristics CD4034BC (Note 2)

PARAMETER	CONDITIONS	−40°C		+25°C			+85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	V_{DD} = 5 V		20			20		150	μA
	V_{DD} = 10 V		40			40		300	μA
	V_{DD} = 15 V		80			80		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
	V_{DD} = 10 V		0.05			0.05		0.05	V
	V_{DD} = 15 V		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
	V_{DD} = 10 V	9.95		9.95			9.95		V
	V_{DD} = 15 V	14.95		14.95			14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5 V, V_O = 0.4 V	0.52		0.44			0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1			0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0			2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5 V, V_O = 4.6 V	−0.52		−0.44			−0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	−1.3		−1.1			−0.9		mA
	V_{DD} = 15 V, V_O = 13.5 V	−3.6		−3.0			−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA
Tri-State Leakage Current	V_{DD} = 15 V, V_O = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
I_{OZ}	V_{DD} = 15 V, V_O = 15 V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

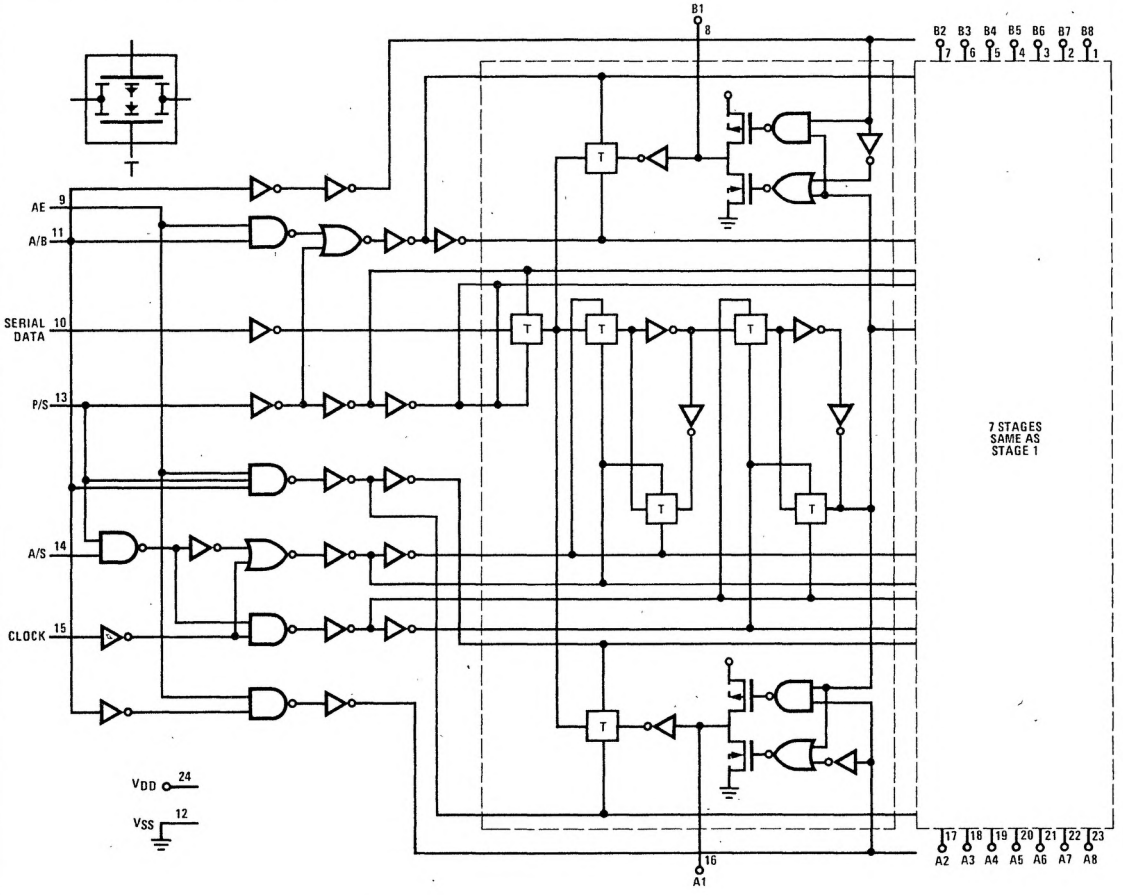
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, A(B) Synchronous Parallel Data or Serial Data Input, B(A) Parallel Data Output	V_{DD} = 5 V		280	700	ns
		V_{DD} = 10 V		120	270	ns
		V_{DD} = 15 V		85	190	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, A(B) A(B) Asynchronous Parallel Data Input, B(A) Parallel Data Output	V_{DD} = 5 V		280	700	ns
		V_{DD} = 10 V		120	270	ns
		V_{DD} = 15 V		85	190	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time from A/B or AE to High Impedance State at A Outputs or from A/B to High Impedance State at B Outputs	V_{DD} = 5 V, R_L = 1.0KΩ		95	220	ns
		V_{DD} = 10 V, R_L = 1.0KΩ		60	130	ns
		V_{DD} = 15 V, R_L = 1.0KΩ		45	100	ns
t_{PZH}, t_{PZL}	Propagation Delay Time from A/B or AE to Logical "1" or Logical "0" State at A Outputs or from A/B to Logical "1" or Logical "0" State at B Outputs	V_{DD} = 5 V, R_L = 1.0KΩ		180	480	ns
		V_{DD} = 10 V, R_L = 1.0KΩ		75	190	ns
		V_{DD} = 15 V, R_L = 1.0KΩ		55	140	ns
t_{THL}, t_{TLH}	Output Transition Time	V_{DD} = 5 V		100	200	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5 V	2	4		MHz
		V_{DD} = 10 V	5	10		MHz
		V_{DD} = 15 V	7	14		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5 V		125	250	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		35	70	ns

AC Electrical Characteristics (Cont'd.)

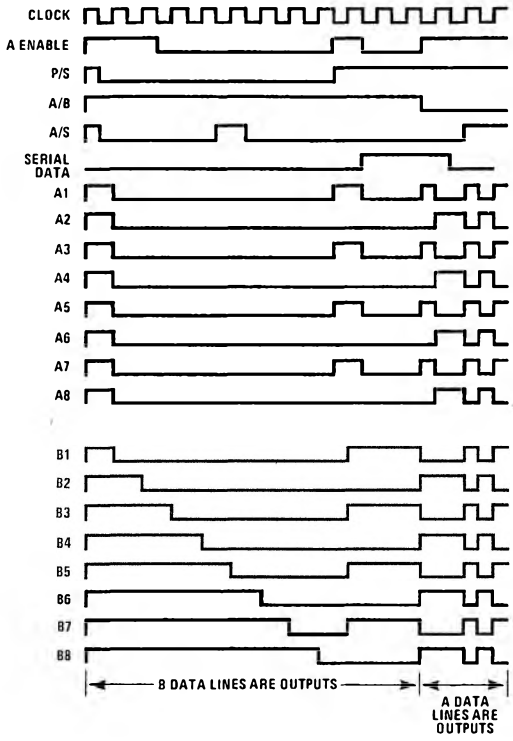
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{RCL}, t_{FCL}	Maximum Clock Rise & Fall Time	V_{DD} = 5 V	15			μs
		V_{DD} = 10 V	15			μs
		V_{DD} = 15 V	15			μs
t_{SU}	Parallel (A or B) and Serial Data Setup Time	V_{DD} = 5 V		25	70	ns
		V_{DD} = 10 V		10	30	ns
		V_{DD} = 15 V		7	20	ns
t_{SU}	Control Inputs AE, A/B, P/S, A/S Setup Time	V_{DD} = 5 V		110	280	ns
		V_{DD} = 10 V		35	100	ns
		V_{DD} = 15 V		20	60	ns
t_{WH}	Minimum High Level AE, A/B, P/S, A/S Pulse Width	V_{DD} = 5 V		160	400	ns
		V_{DD} = 10 V		70	160	ns
		V_{DD} = 15 V		40	90	ns
C_{IN}	Average Input Capacitance	A and B Data I/O and A/B Control Input		7	15	pF
		Any Other Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		155		pF

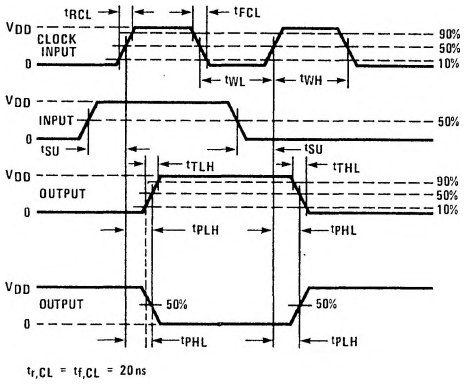
Note 3: C_{PD} determines the no-load power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Schematic Diagram

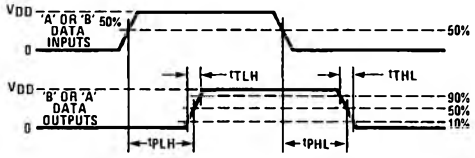


Switching Time Waveforms and Test Circuits

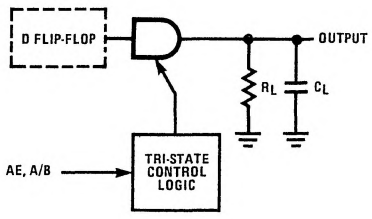


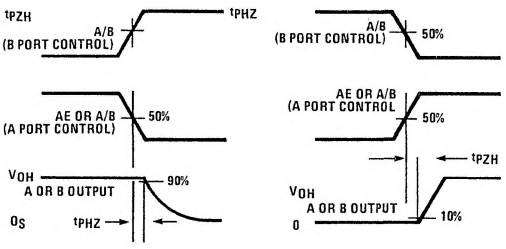


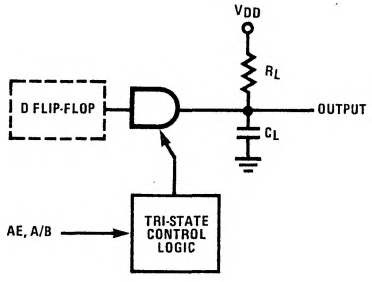
Synchronous Operation

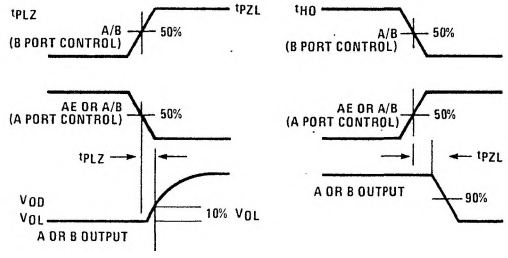


Asynchronous Operation

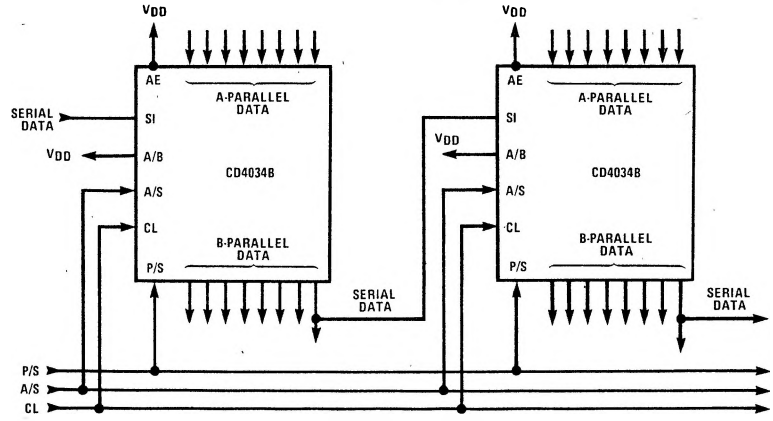




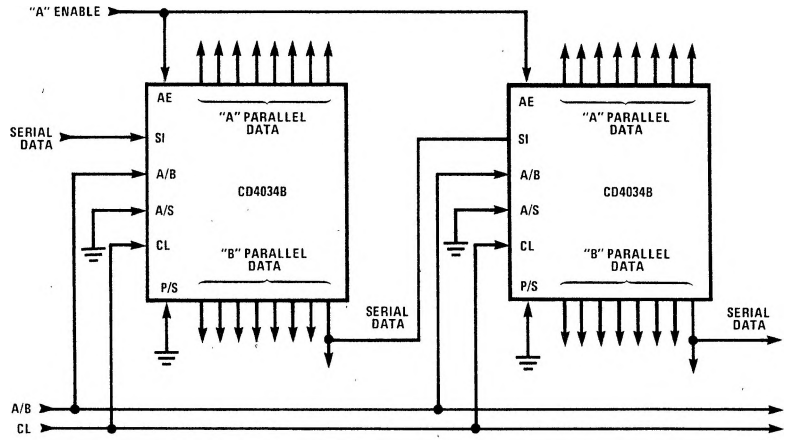




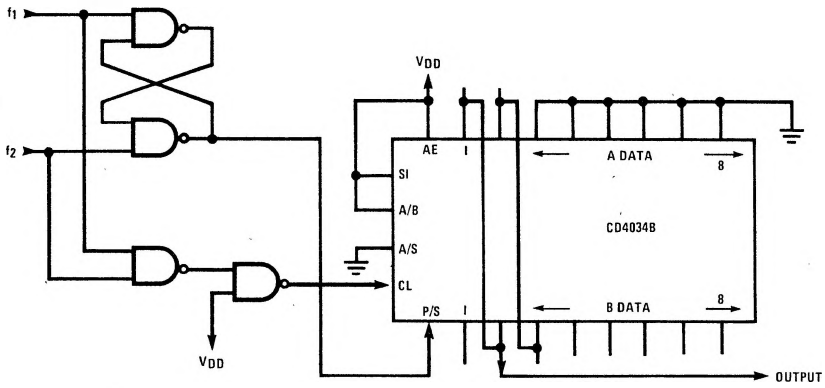
Applications



16-Bit parallel in/parallel out,parallel in/ serial out, serial in/parallel out, serial in/ serial out register.

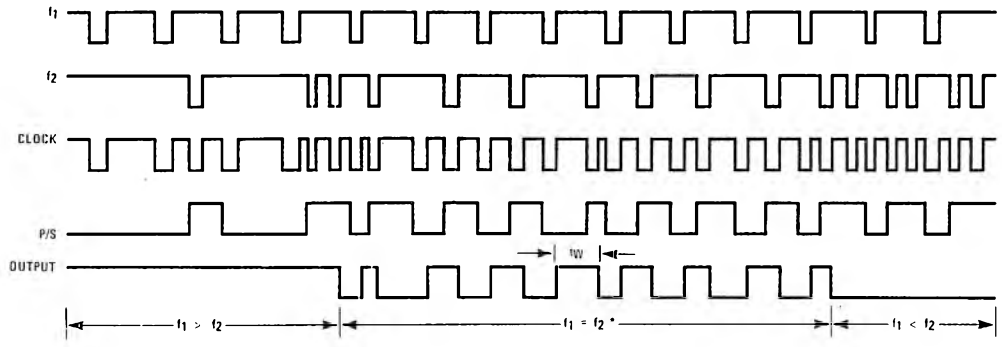


16-Bit serial in/gated parallel out register.

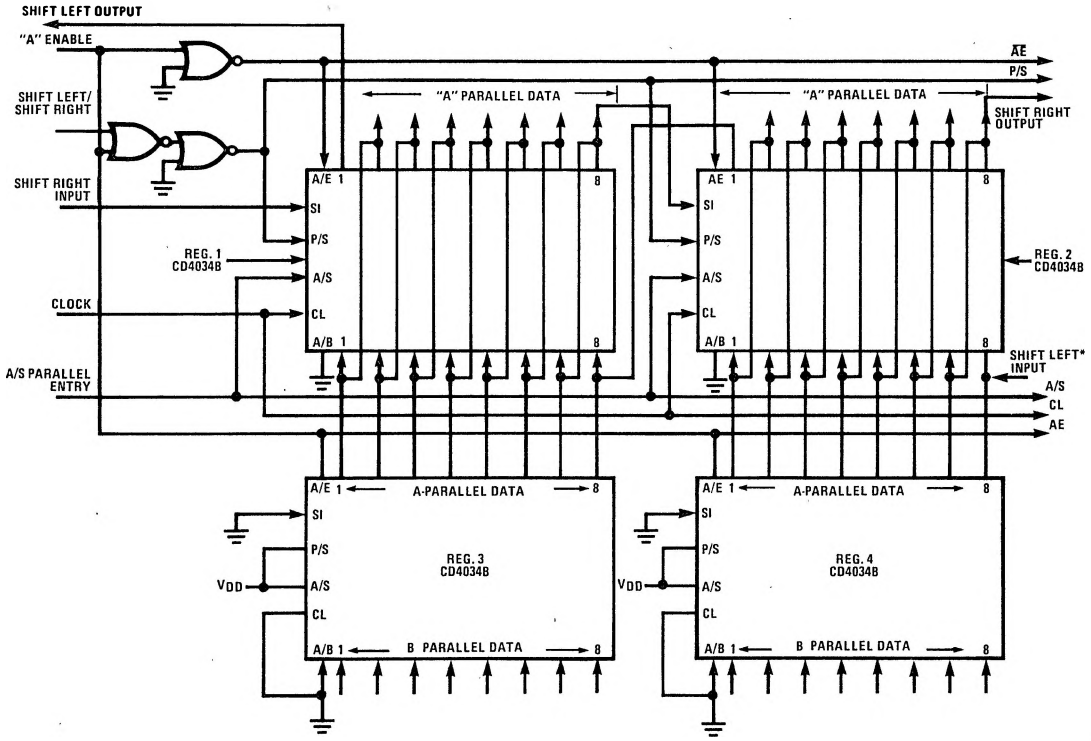


Frequency and Phase Comparator

Applications (Cont'd.)



*WHEN $f_1 = f_2$, t_W IS PROPORTIONAL TO THE PHASE OF f_1 WITH RESPECT TO f_2



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Registers 1 and 2 and enables the "A" data lines on Registers 3 and 4 and allows parallel data into Registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Registers 3 and 4 and associated logic are not required.

* Shift left input must be disabled during parallel entry.

Shift Right/Shift Left with Parallel Inputs

Truth Table

"A" ENABLE	P/S	A/B	A/S	MODE	OPERATION*
0	0	0	X	Serial	Synchronous Serial data input, A- and B-Parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous Serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
1	1	0	0	Parallel	B Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

*For synchronous operation (serial mode or when A/S = 0 in parallel mode), outputs change state at positive transition of the clock.