National Semiconductor

CD4035BM/CD4035BC 4-Bit Parallel-In/Parallel-Out Shift Register

General Description

The CD4035B 4-bit parallel-in/parallel-out shift register is a monlithic complementary MOS (CMOS) integrated circuit constructed with P- and N-channel enhancement mode transistors. This shift register is a 4-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via $J\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (parallel/serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the parallel/serial control is "high".

In the parallel or serial mode, information is transferred on positive clock transitions.

When the true/complement control is "high", the true contents of the register are available at the output terminals. When the true/complement control is "low", the outputs are the complements of the data in the register. The true/complement control functions asynchronously with respect to the clock signal.

$J\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With $J\overline{K}$ inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

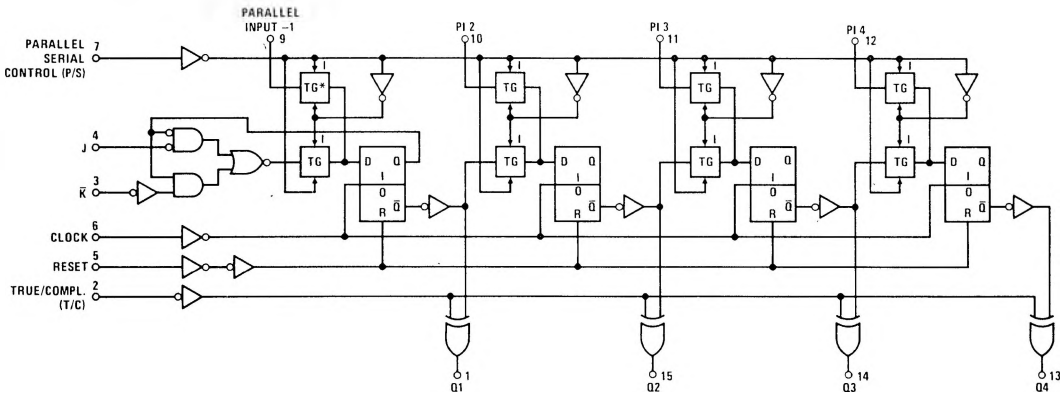
Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 4-stage clocked operation
- Synchronous parallel entry on all 4 stages
- $J\overline{K}$ inputs on first stage
- Asynchronous true/complement control on all outputs
- Reset Control
- Static flip-flop operation; master/slave configuration
- Buffered outputs
- Low power dissipation — 5 μW (typ.) (ceramic)
- High speed — to 5 MHz

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial controls
- Remote metering
- Computers

Logic Diagram



P/S = 0 = serial mode
T/C = 1 = true outputs
*TG = transmission gate

Input to output is:

a) A bidirectional low impedance when control input 1 is low and control input 2 is high.

b) An open circuit when control input 1 is high and control input 2 is low.

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 2)

V_{DD} dc Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD}V
T_A Operating Temperature Range	
CD4035BM	−55°C to +125°C
CD4035BC	−40°C to +85°C

DC Electrical Characteristics CD4035BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	0.36		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	0.9		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4035BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.5	20		150	μA
		V_{DD} = 10V		40		1.0	40		300	μA
		V_{DD} = 15V		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V

DC Electrical Characteristics (Cont'd.) CD4035BC (Note 2)

PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.36		−0.12		mA
	V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.9		−0.3		mA
	V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN} Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

AC Electrical Characteristics

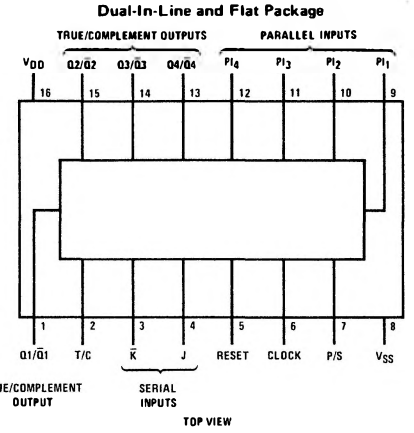
T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and t_f = 20 ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		75	150	ns
t_{THL}	Transition Time High Low to High	V_{DD} = 5V		90	175	ns
		V_{DD} = 10V		50	75	ns
		V_{DD} = 15V		40	60	ns
t_{TLH}	Transition Time Low to High	V_{DD} = 5V		135	270	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		60	120	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V	335	135		ns
		V_{DD} = 10V	165	50		ns
		V_{DD} = 15V	100	40		ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			10	μs
		V_{DD} = 15V			5	μs
t_S	Minimum Set-up Time J/$\overline{K}$ Lines	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_S	Parallel-In Lines	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_S	P/S Control	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		35	60	ns
f_{MAX}	Maximum Clock Frequency	V_{DD} = 5V	1.5	2.5		MHz
		V_{DD} = 10V	3	6		MHz
		V_{DD} = 15V	5	9		MHz
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
RESET OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		300	500	ns
		V_{DD} = 10V		150	200	ns
		V_{DD} = 15V		85	150	ns
t_{WH}	Minimum Reset Pulse Width	V_{DD} = 5V		75	250	ns
		V_{DD} = 10V		30	110	ns
		V_{DD} = 15V		25	80	ns

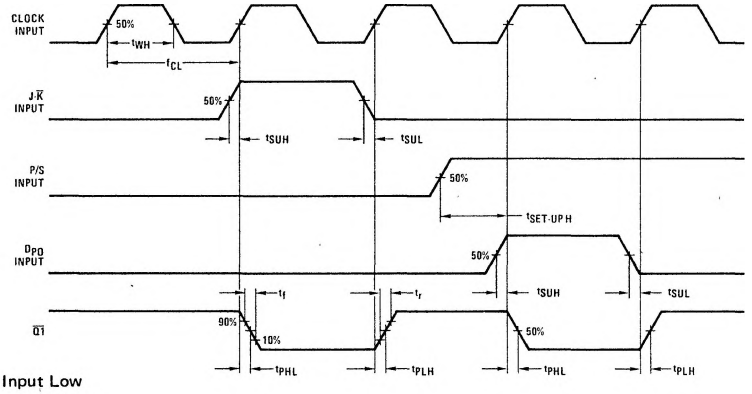
Truth Table

C_L	$t_n - 1$ (INPUTS)				t_n (OUTPUTS)
	J	$\overline{K}$	R	$Q_n - 1$	Q_n
⌐	0	X	0	0	0
⌐	1	X	0	0	1
⌐	X	0	0	1	0
⌐	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
⌐	X	1	0	1	1
⌙	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

Connection Diagram



Switching Time Waveforms



T/C Input Low
Reset Input Low